Development Board EPC9094 Quick Start Guide

200 V Half-bridge with Gate Drive, Using EPC2054

Revision 1.0

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC9094 is a half bridge development board with onboard gate driver, featuring the 200 V rated EPC2054 GaN field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2054 by including all the critical components on a single board that can be easily connected into the majority of existing converter topologies.

The EPC9094 evaluation board measures 2" x 2" and contains two EPC2054 GaN FETs in a half bridge configuration. The EPC9094 features the On-Semi NCP51820 gate driver. The board also contains all critical components and the layout supports optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A block diagram of the circuit is given in figure 1.

For more information on EPC2054 please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (T_A = 25°C) EPC9094

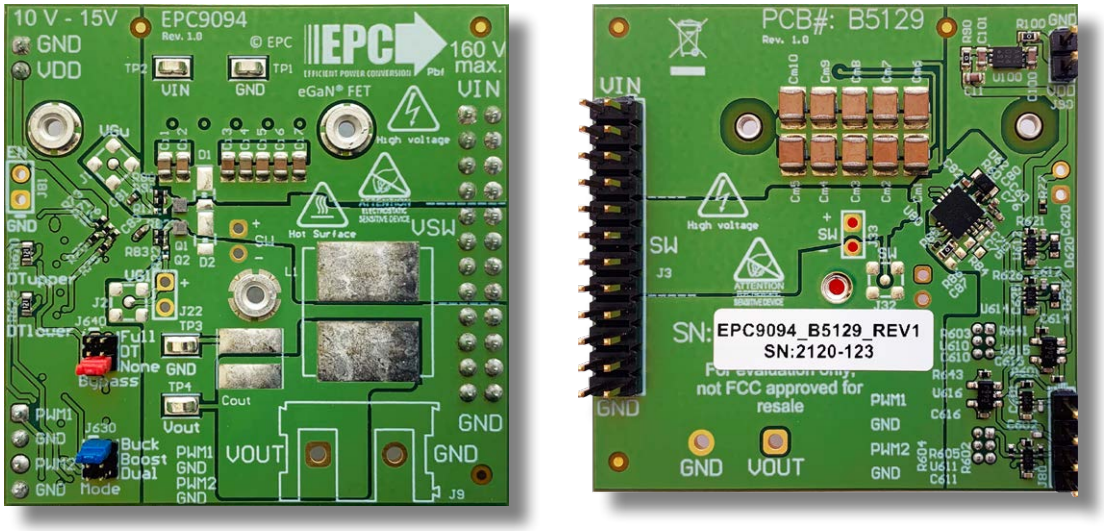
Symbol	Parameter	Conditions	Min	Nominal	Max	Units
V_{DD}	Gate Drive Input Supply Range		10		15	V
V_{IN}	Bus Input Voltage Range(1)				160	
I_{OUT}	Switch Node Output Current (2)				2	A
V_{PWM}	PWM Logic Input Voltage Threshold (3)	Input 'High'	3.5		5.5	V
		Input 'Low'	0		1.5	
V_{EN}	Enable Logic Input Voltage Threshold (3)	Input 'High'	3.5		5.5	V
		Input 'Low'	0		1.5	
	PWM 'High' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	50			ns
	PWM 'Low' State Input Pulse Width (4)	V_{PWM} rise and fall time < 10ns	200			

(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 200 V for EPC2054.

(2) Maximum current depends on die temperature – actual maximum current is affected by switching frequency, bus voltage and thermal cooling.

(3) When using the on board logic buffers, refer to the NCP51820 datasheet when bypassing the logic buffers.

(4) Limited by time needed to 'refresh' high side bootstrap supply voltage.



Front view

EPC9094 development board

Back view

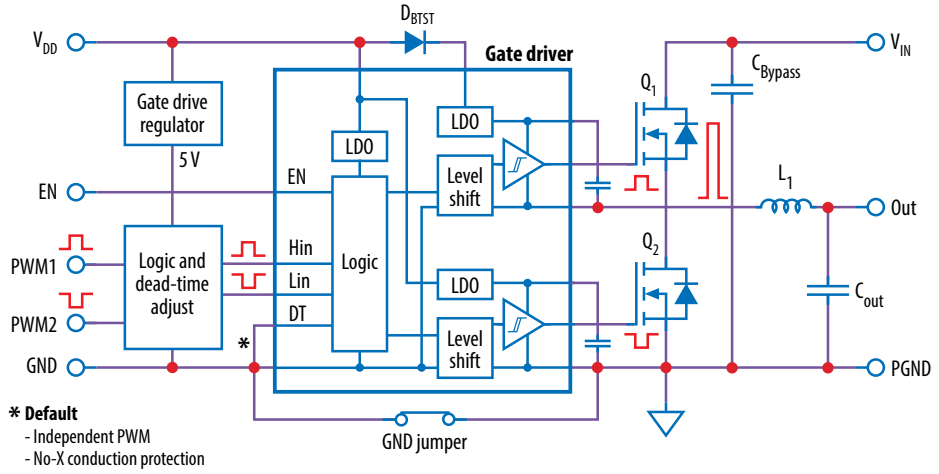


Figure 1: Block diagram of EPC9094 development board

QUICK START PROCEDURE

The EPC9094 development board is easy to set up as a buck or boost converter to evaluate the performance of two EPC2054 eGaN FETs. In addition to the deadtime features of the NCP51820 gate driver, this board includes a dead-time generating circuit that adds a delay from when the gate signal of one FET is commanded to turn off, to when the gate signal of the other FET is commanded to turn on. In the default configuration, the NCP51820 gate driver is set mode D (no-dead time, no-cross conduction protection - refer to datasheet for NCP51820) and the dead time circuit thus ensures that both the high and low side FETs will not be turned on at the same time thus preventing a shoot-through condition. The dead-time and/or polarity changing circuits can be utilized or bypassed for added versatility.

Single/dual PWM signal input settings

There are two PWM signal input ports on the board, PWM1 and PWM2. Both input ports are used as inputs in dual-input mode where PWM1 connects to the upper FET and PWM2 connects to the lower FET. The PWM1 input port is used as the input in single-input mode where the circuit will generate the required complementary PWM for the FETs. The input mode is set by choosing the appropriate jumper positions for J630 (mode selection) as shown in figure 2(a) for a **single-input buck converter** (**blue** jumper across pins 1 & 2 of J630), (b) for a **single-input boost converter** (**blue** jumpers across pins 3 & 4 of J630), and (c) for a **dual-input operation** (**blue** jumpers across pins 5 & 6 of J630).

Note: In dual mode there is no shoot-through protection as both gate signals can be set high at the same time. Refer to the NCP51820 datasheet for details on setting the dead time using R84 and R86.

Dead-time settings

Dead-time is defined as the time between when one FET turns off and the other FET turns on, and for this board is referenced to the input of the gate driver. The dead-time can be set to a specific value where resistor R620 delays the turn on of the upper FET and resistor R625 delays the turn on of the lower FET as illustrated in figure 3.

The required resistance for the desired dead-time setting can be read off the graph in figure 4. An example for 10 ns dead-time setting shows that a 120 Ω resistor is needed.

Note: This is the default deadtime and resistor value installed. A minimum dead-time of is 5 ns and maximum of 15 ns is recommended.

Bypass settings

Both the polarity changer and the deadtime circuits can be bypassed using the jumper settings on J640 (Bypass), for direct access to the gate driver input. There are three bypass options: 1) No bypass, 2) Dead-time bypass, 3) Full bypass. The jumper positions for J640 for all three bypass options are shown in figure 5.

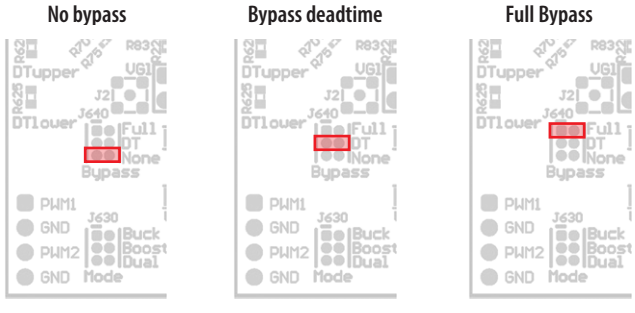


Figure 5: Bypass mode Jumper settings for J640

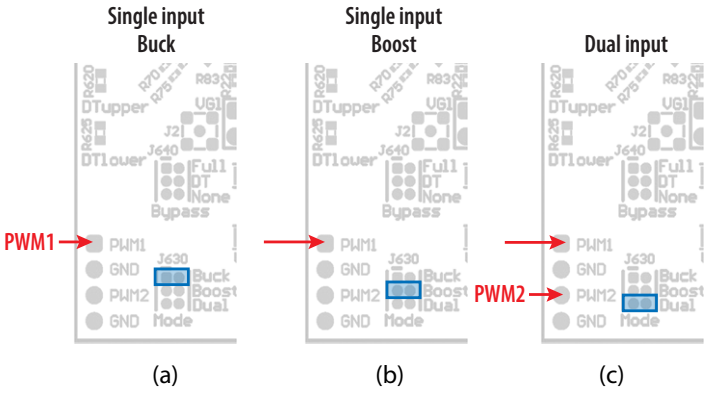


Figure 2: Input mode selection on J630

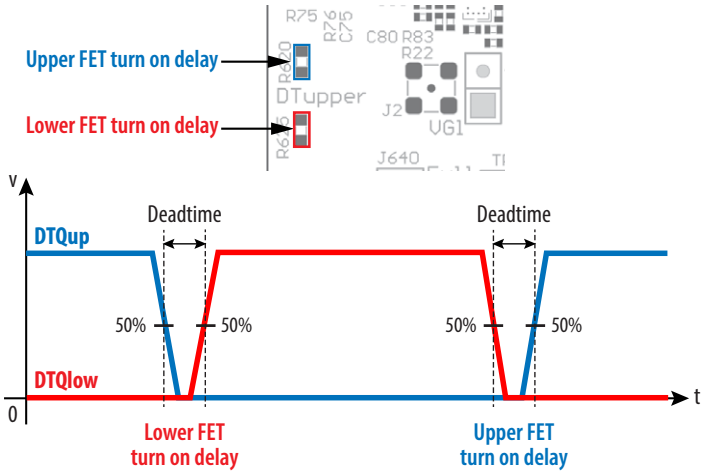


Figure 3: Definition of dead-time between the upper-FET gate signal (DTQup) and the lower-FET gate signal (DTQlow)

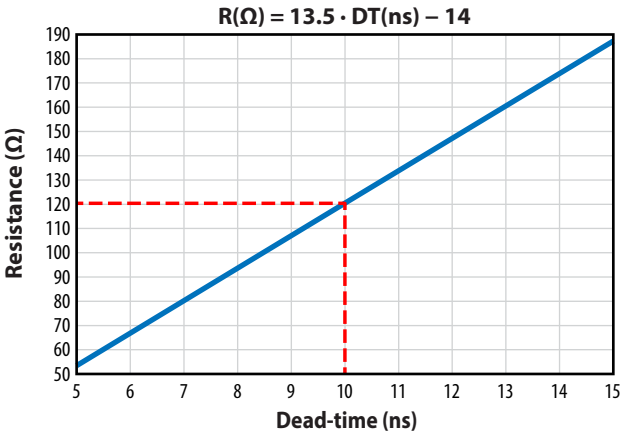


Figure 4: The required resistance values for R620 or R625 as a function of desired dead-time

In ***no-bypass mode***, figure 5(a) (**red** jumper across pins 5 & 6 of J640), both the on-board polarity and dead-time circuits are fully utilized.

In ***dead-time bypass mode***, figure 5(b) (**red** jumpers across pins 3 & 4 of J640), only the on-board polarity changer circuit is utilized, effectively bypassing the dead-time circuit.

In ***full bypass mode***, Figure 5(c) (**red** jumper across pins 1 & 2 of J640), the inputs to the gate driver are directly connected to the PWM1 and PWM2 pins and the on-board polarity and dead-time circuits are not utilized. Furthermore, the dead-time settings for the NCP51820 gate driver can now be utilized by placing the NCP51820 gate driver in either Mode B or C. This can be done by changing the values of or installing the following components: R84, R86 and C87. Refer to the NCP51820 datasheet for details.

Bypass mode warnings

- ***It is important to provide the correct PWM signals that includes dead-time and polarity for either buck or boost operation when making use of bypass modes.***
- When operating in ***full bypass mode***, the input signal specifications revert to that of the NCP51820 gate driver IC. Refer to the NCP51820 datasheet for details.
- It is not recommended to utilize both on board and gate driver dead-time settings simultaneously.datasheet for details.

Enable Function

An enable input is available, shown in figure 1, that can be used to turn off both FETs regardless of operating mode. Refer to the NCP51820 datasheet for additional details. If this function is not needed, then leave the connection (J81) empty and the gate driver will be enabled (default setting). Figure 6 shows three configurations that can be used for the enable function:

a) Using a shorting jumper or switch. When the enable terminals (J81) are shorted together, the gate driver will be disabled. When the enable terminals (J81) are open, then the gate driver will be enabled.

b) Using a transistor as a switch. This configuration is similar to (a) except that an open collector/drain transistor, such as a MOSFET or BJT, is used instead of a mechanical switch. The transistor must be rated to at least 10 V and be able to carry at least 20 mA. Note that pin 1 of the enable function (J81) is connected to the ground of the development board and hence the corresponding drive voltage/current needs to be referenced to the same ground.

c) Using a voltage source to drive the enable function. In this configuration a voltage source directly drives the enable/disable function. When the applied voltage exceeds 3.5 V then the gate driver will be enabled. When the drive voltage falls below 1.5 V then the gate driver will be disabled. The voltage source must be capable of sinking and sourcing at least 20 mA. Warning: In this configuration do not exceed the input voltage ratings of the gate driver. Refer to the NCP51820 datasheet for additional details.

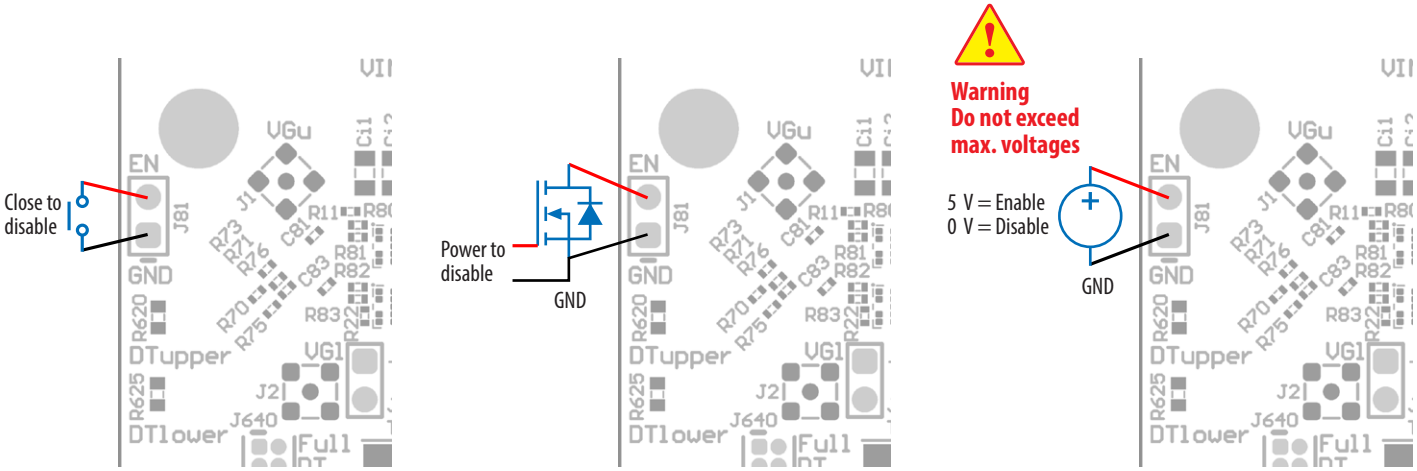


Figure 6: Enable function configurations

Buck converter configuration

To operate the board as a buck converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select ***Single Input Buck Mode***, the bypass jumper J640 ***must*** be set to the ***no-bypass mode***, the ***buck mode*** J630 ***must*** be selected as shown in figure 7(a).

To select ***Dual Input Buck Mode***, the bypass jumper J640 ***may*** be configured to any of the valid settings, the dual-input mode J630 ***must*** be selected as shown in figure 7(b).

Note: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in bypass mode.

Once the input source, dead-time settings and bypass config-urations have be chosen and set, then the boards can be operated.

1. With power off, connect the input power supply bus to VIN and ground / return to GND.
2. With power off, connect the switch node (SW) of the half bridge to your circuit as required (half bridge configuration). Or use the provided pads for inductor (L1) and output capacitors (Cout), as shown in figure 7.
3. With power off, connect the gate drive supply to VDD (J90, Pin-2) and ground return to GND (J90, Pin-1 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J80 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is set between 10 V and 15 V.
6. Turn on the controller / PWM input source.
7. Making sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the required value (***do not exceed the absolute maximum voltage***). Probe switch-node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters.
9. For shutdown, please follow steps in reverse.

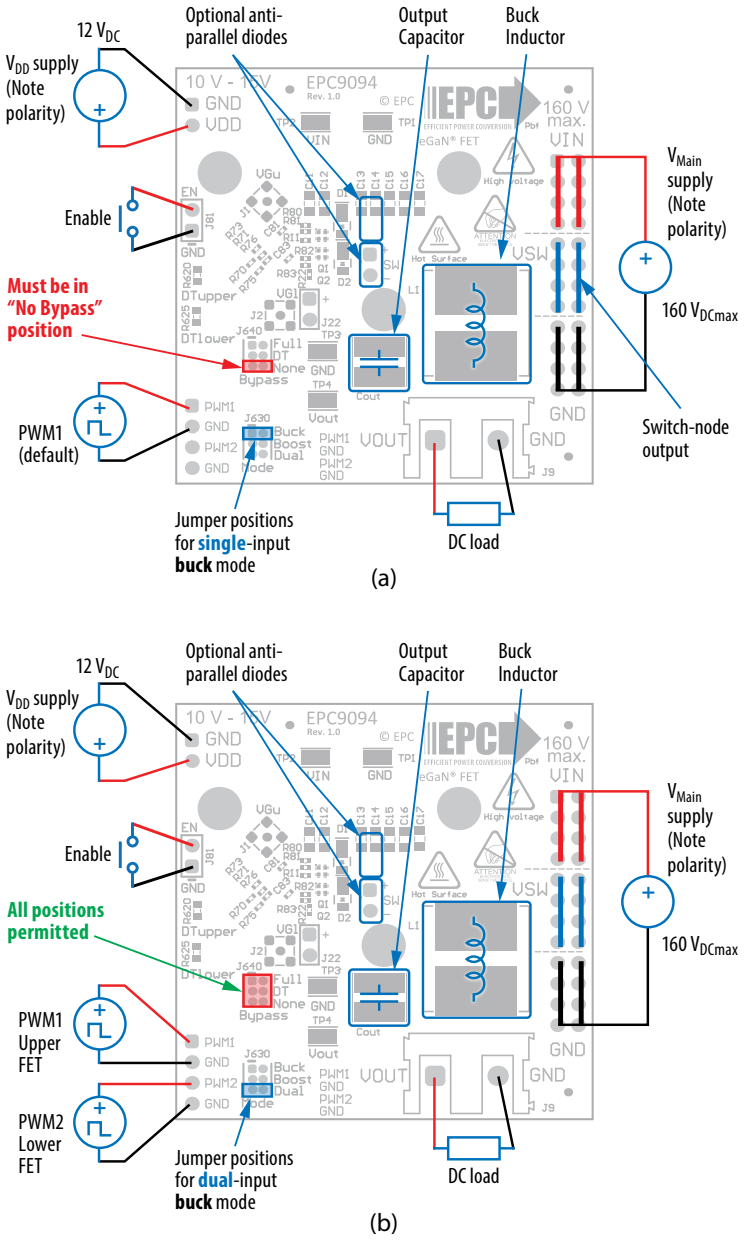


Figure 7: (a) Single-PWM input buck converter (b) Dual-PWM input buck converter configurations showing the supply, anti-parallel diodes, output capacitor, inductor, PWM, and load connections with corresponding jumper positions.

Boost Converter configuration

Warning: Never operate the boost converter mode without a load, as the output voltage can increase beyond the maximum ratings.

To operate the board as a boost converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select ***Single Input Boost Mode***, the bypass jumper J640 ***must*** be set to the ***no-bypass mode***, the boost mode J630 ***must*** be selected as shown in figure 8(a).

To select ***Dual Input Boost Mode***, the bypass jumper J640 ***may*** be configured to any of the valid settings, the ***dual-input mode*** J630 ***must*** be selected as shown in figure 8(b).

Note: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in bypass mode.

Once the input source, dead-time settings and bypass configurations have be chosen and set, then the boards can be operated.

1. The inductor (L1) and input capacitors (labeled as Cout) can either be soldered onto the board, as shown in figure 8, or provided off board. Anti-parallel diodes can also be installed using the additional pads on the right side of the FETs.
2. With power off, connect the input power supply bus to V_{OUT} and ground / return to GND, or externally across the capacitor if the inductor L1 and Cout are provided externally. Connect the output voltage (**labeled as VIN**) to your circuit as required, e.g., resistive load.
3. With power off, connect the gate drive supply to V_{DD} (J90, Pin-1) and ground return to GND (J90, Pin-2 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J2 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is between 10 V and 15 V.
6. Turn on the controller / PWM input source.
7. **Making sure the output is not open circuit**, and the input supply voltage is initially 0 V, turn on the power and slowly increase the voltage to the required value (***do not exceed the absolute maximum voltage***). Probe switch-node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters. Observe device temperature for operational limits.
9. For shutdown, please follow steps in reverse.

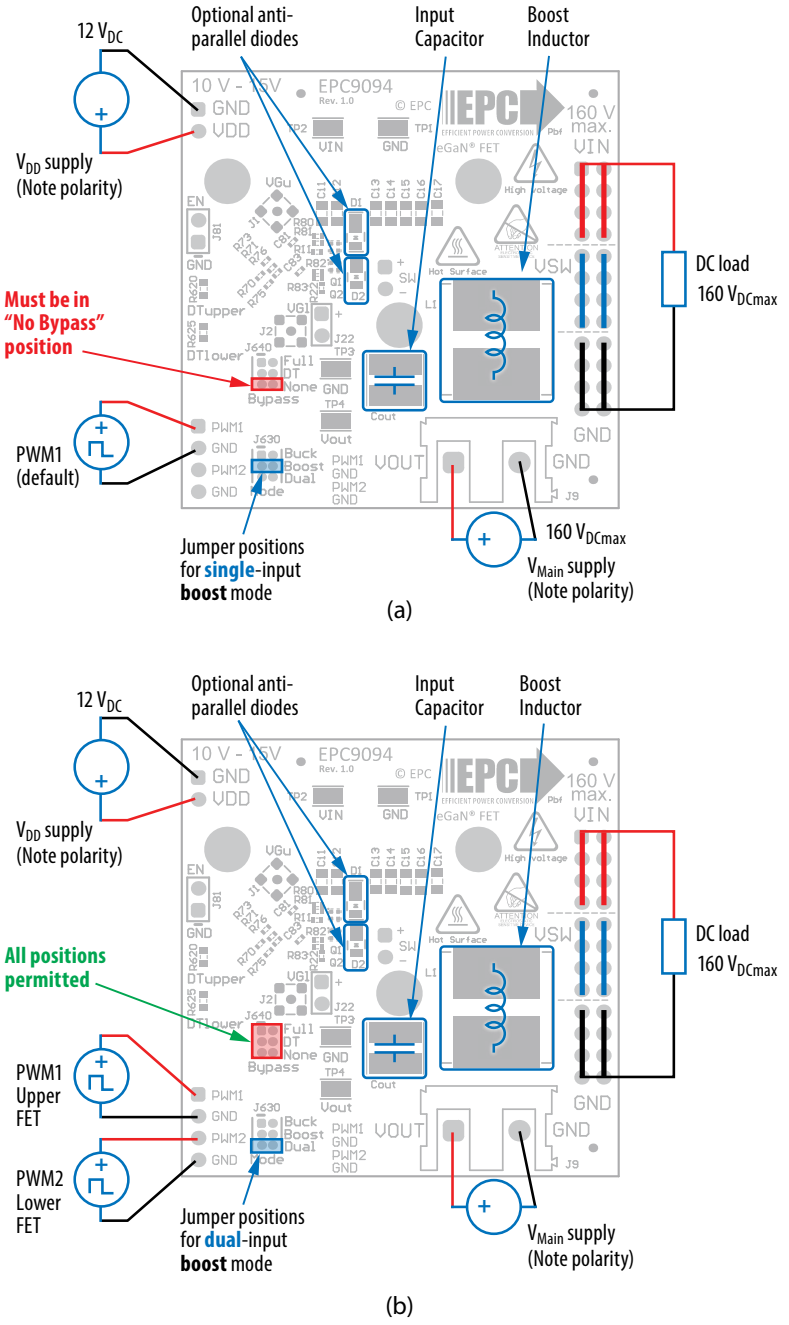


Figure 8: (a) Single-PWM input boost converter (b) Dual-PWM input boost converter configurations showing the supply, inductor, anti-parallel diodes, input capacitor, PWM, and load connections with corresponding jumper settings.

MEASUREMENT CONSIDERATIONS

Measurement connections are shown in figure 9. Figure 10 shows an actual switch-node voltage measurement when operating the board as a buck converter.

When measuring the switch node voltage containing high-frequency content, care must be taken to provide an accurate high-speed measurement. An optional two pin header (J33) and an MMCX connector (J32) are provided for switch-node measurement.

A differential probe is recommended for measuring the high-side bootstrap voltage. IsoVu probes from Tektronix has mating MMCX connector.

For regular passive voltage probes (e.g. TPP1000) measuring switch node using MMCX connector, probe adaptor is available. PN: 206-0663-xx.

Note:

For information about measurement techniques, the EPC website offers: "*AN023 Accurately Measuring High Speed GaN Transistors*" and the How to GaN educational video series, including: *HTG09-Measurement*

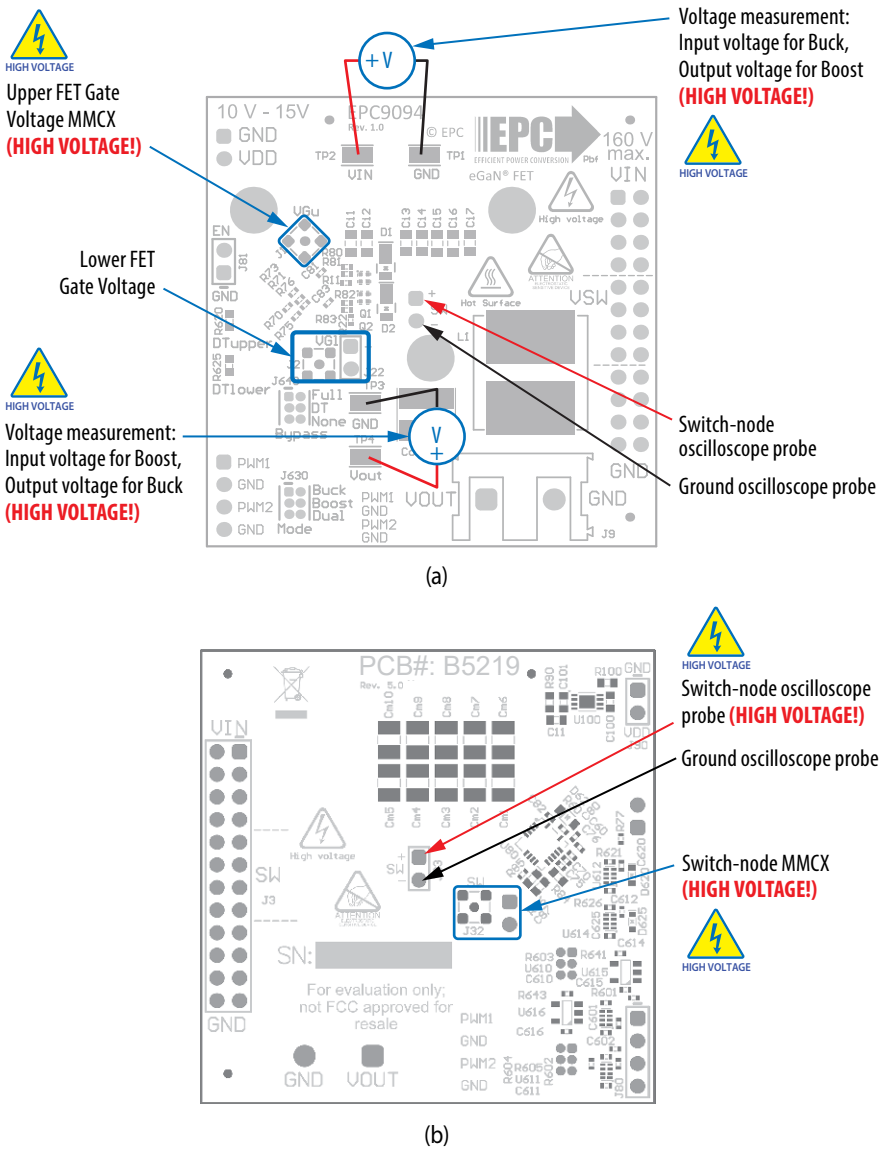
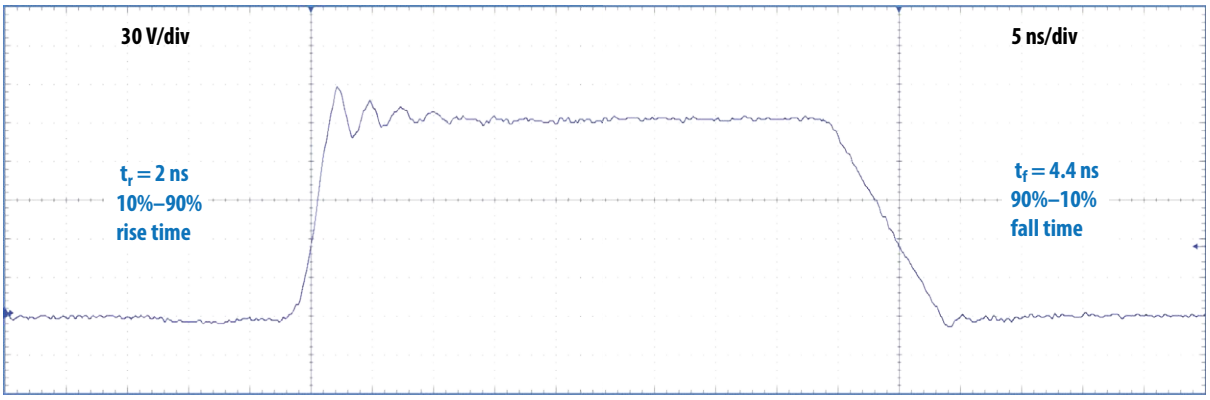


Figure 9: Measurement points (a) front side, (b) Back side



V_{IN} = 160 V, V_{OUT} = 12 V, I_{OUT} = 4 A, f_{sw} = 200 kHz, L = 30 µH

Figure 10: Typical switch-node waveform when operated as a buck converter

SPECIAL FEATURE: GND - PGND DISCONNECT

The EPC9094 board has been provided with the ability to disconnect the signal ground (GND) from the power ground (PGND) which is useful for applications where a shunt is used in the PGND path. The grounds can be disconnected by removing R85 as shown in figure 11. ***Note that the NCP51820 gate driver has a maximum ground difference voltage limit of ±3.5 V.***

THERMAL CONSIDERATIONS

The EPC9094 board is equipped with three mechanical spacers that can be used to easily attach a heat-spreader or heatsink as shown in figure 12 (a), and only requires a thermal interface material (TIM), a custom shape heat-spreader/ heatsink, and screws. Prior to attaching a heat-spreader, any component exceeding 1 mm in thickness under the heat-spreader area will need to be removed from the board as shown in figure 12 (b).

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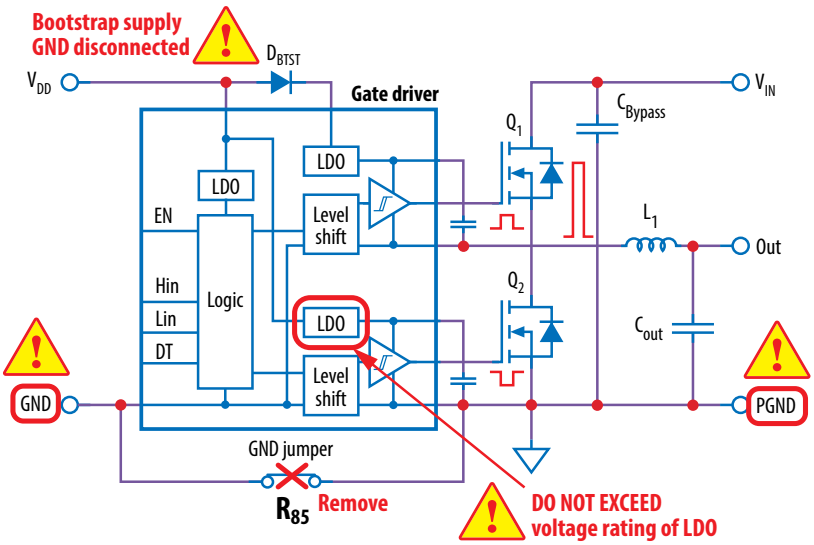
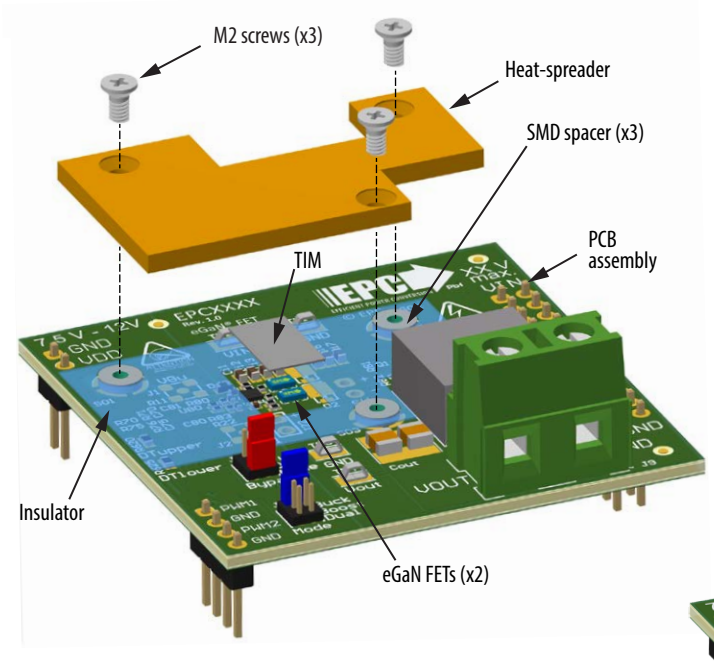
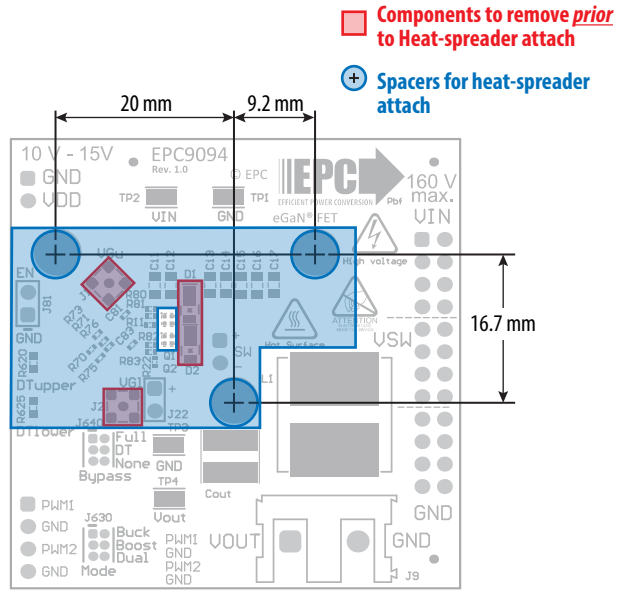
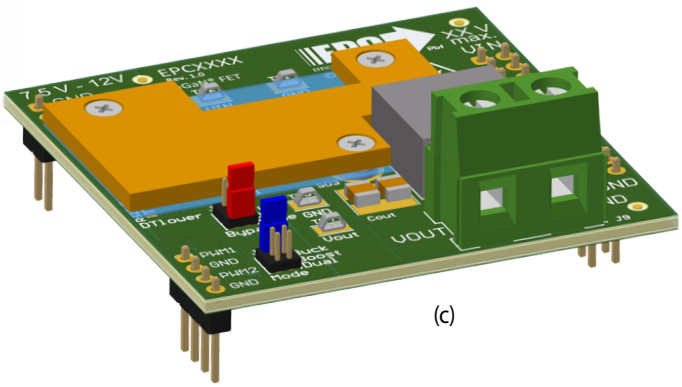


Figure 11: GND – PGND disconnect warnings





(b)



(c)

Figure 12: Details for attaching a heatsink to the development board. (a) 3D perspective, (b) top view details, (c) Assembled view with heat-spreader attached.

The design of the heat-spreader is shown in figure 13 and can be made using **aluminum** or **tellurium copper** for higher performance.

The heat-spreader is held in place using countersunk screws that fasten to the mechanical spacers which will accept M2 x 0.4 mm thread screws such as McMasterCarr 91294A002.

When assembling the heatsink, it may be necessary add a thin insulation layer to prevent the heat-spreader from short circuiting with components that have exposed conductors such as capacitors and resistors, as shown in figure 13. ***Note that the heat-spreader is ground connected by the lower most mounting post***. A rectangular opening in the insulator must be provided to allow the TIM to be placed over the FETs to be cooled with a minimum clearance of 3 mm on each side of the rectangle encompassing the FETs. The TIM will then be similar in size or slightly smaller than the opening in the insulator shown by the red dashed outline in figure 14.

EPC recommends Laird P/N: A14692-30, Tgard™ K52 with thickness of 0.051 mm the for the insulating material.

A TIM is added to improve the interface thermal conductance between the FETs and the attached heat exchanger. The choice of TIM needs to consider the following characteristics:

- **Mechanical compliance** – During the attachment of the heat spreader, the TIM underneath is compressed from its original thickness to the vertical gap distance between the spacers and the FETs. This volume compression exerts a force on the FETs. A maximum compression of 2:1 is recommended for maximum thermal performance and to constrain the mechanical force which maximizes thermal mechanical reliability.
- **Electrical insulation** – The backside of the eGaN FET is a silicon substrate that is connected to source and thus the upper FET in a half-bridge configuration is connected to the switch-node. To prevent short-circuiting the switch-node to the grounded thermal solution, the TIM must be of high dielectric strength to provide adequate electrical insulation in addition to its thermal properties.
- **Thermal performance** – The choice of thermal interface material will affect the thermal performance of the thermal solution. Higher thermal conductivity materials is preferred to provide higher thermal conductance at the interface.

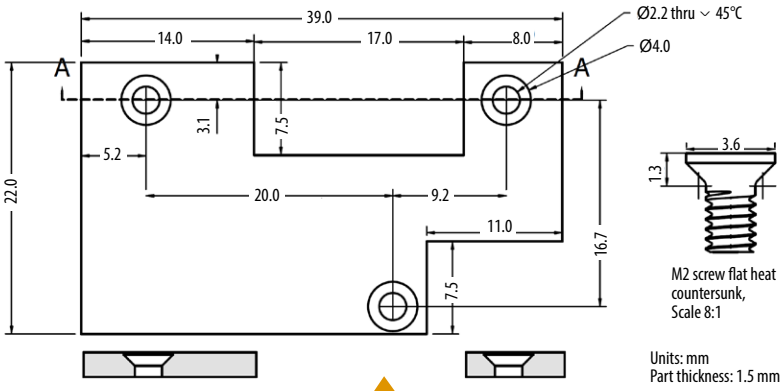
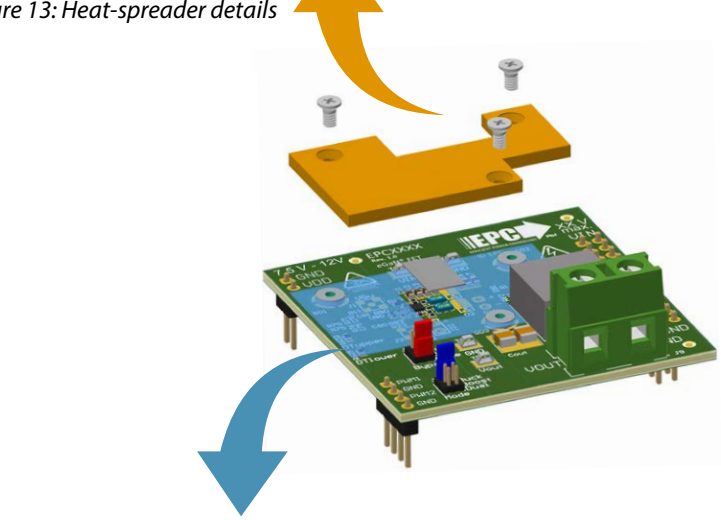


Figure 13: Heat-spreader details



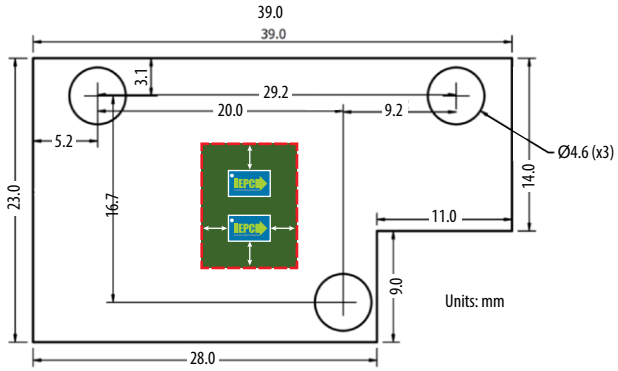


Figure 14: Insulator sheet details with opening for the TIM with location of the FETs

EPC recommends the following thermal interface materials:

- **t-Global** P/N: TG-A1780 X 0.5 mm (highest conductivity of 17.8 W/m.K)
- **t-Global** P/N: TG-A620 X 0.5 mm (moderate conductivity of 6.2 W/m.K)
- **Bergquist** P/N: GP5000-0.02 (~0.5 mm with conductivity of 5 W/m.K)
- **Bergquist** P/N: GPTGP7000ULM-0.020 (conductivity of 7 W/m.K)

NOTE. The EPC9094 development board does not have any current or thermal protection on board. For more information regarding the thermal performance of EPC eGaN FETs, please consult:
D. Reusch and J. Glaser, ***DC-DC Converter Handbook, a supplement to GaN Transistors for Efficient Power Conversion,*** First Edition, Power Conversion Publications, 2015.

Table 2: Bill of Materials

Item	Qty	Reference	Part Description	Manufacturer	Part Number
1	3	C11, C100, C101	CAP CER 1 µF 25 V X7R 0603	TDK	C1608X7R1E105K080AB
2	1	C60	CAP CER 0.1 µF 25 V X7R 0402	TDK	C1005X7R1E104K050BB
3	2	C70, C75	CAP CER 100 pF 50 V X7R 0402	Yageo	CC0402KRX7R9BB101
4	1	C76	CAP CER 15 pF 50 V C0G 0402	TDK	CGA2B2C0G1H150J050BA
5	3	C80, C81, C83	CAP CER 1 µF 25 V X5R 0402	TDK	C1005X5R1E105K050BC
6	1	C82	CAP CER 0.47 µF 25 V X5R 0402	TDK	C1005X5R1E474K050BB
7	2	C601, C602	CAP CER 47 pF 50 V C0G/NPO 0402	Yageo	CC0402JRNPO9BN470
8	6	C610, C611, C612, C614, C615, C616	CAP CER 0.1 µF 25 V X7R 0402	Yageo	CC0402KRX7R8BB104
9	2	C620, C625	CAP CER 100 pF 50 V X7R 0402	Yageo	CC0402KRX7R9BB101
10	7	Ci1, Ci2, Ci3, Ci4, Ci5, Ci6, Ci7	CAP CER 0.022 µF 500 V X7R 0805	KEMET	C0805W223KCRAC7800
11	10	Cm1, Cm2, Cm3, Cm4, Cm5, Cm6, Cm7, Cm8, Cm9, Cm10	CAP CER 0.15 µF 500 V X7R 1210	KEMET	C1210C154KCRAC7800
12	1	D62	DIODE GP 600 V 200 mA TUMD2SM	RΩ	RFU02VSM6STR
13	2	D620, D625	DIODE SCHOTTKY 30 V 30 mA SOD523	Diodes Inc.	SDM03U40-7
14	1	J3	Header Male 100 mil 2 row, 12 pos., Thru Vert.	Amphenol	67997-272HLF
15	1	J80	Header Male 100 mil 1 row, 4 pos., Thru Vert.	Tyco	4-103185-0-04
16	1	J90	Header Male 100 mil 1 row, 2 pos., Thru Vert.	Tyco	4-103185-0-02
17	2	J630, J640	Header Male 50 mil 2 row, 3 pos., Thru Vert.	Sullins	GRPB032VWVN-RC
18	1	JP630	50 mil Jumper **Blue** withHandle	Harwin Inc	M50-2030005
19	1	JP640	50 mil Jumper **Red** withHandle	Harwin Inc	M50-2020005
20	2	Q1, Q2	200 V 32 mΩ 2.4A	EPC	EPC2054
21	1	R60	RES 2 Ω 5% 1/16 W 0402	Stackpole	RMCF0402JT2R00
22	3	R70, R75, R77	RES SMD 2.2 Ω 5% 1/10 W 0402	Panasonic	ERJ-2GEJ2R2X
23	11	R71, R76, R601, R602, R603, R604, R605, R621, R626, R641, R643	RES SMD 10 K Ω 1% 1/16 W 0402	Yageo	RC0402FR-0710KL
24	1	R73	RES SMD 10 K Ω 1% 1/10 W 0402	Panasonic	ERJ-2RKF1002X
25	2	R80, R82	RES 4.7 Ω 1% 1/16 W 0402	Stackpole	RMCF0402FT4R70
26	2	R81, R83	RES SMD 1 Ω 1% 1/16 W 0402	Yageo	RC0402FR-071RL
27	1	R85	RES SMD 0 Ω JUMPER 1/16 W 0402	Stackpole	RMCF0402ZT0R00
28	3	R86, R90, R100	RES SMD 0 Ω JUMPER 1/10 W 0603	Panasonic	ERJ-3GEY0R00V
29	2	R620, R625	RES SMD 120 Ω 1% 1/10 W 0603	Yageo	RC0603FR-07120RL
30	3	SO1, SO2, SO3	Round Standoff Threaded M2x0.4 Steel 0.039" (1.00 mm)	Wurth	9774010243R
31	4	TP1, TP2, TP3, TP4	HookUP SMD	Keystone	5015
32	1	U80	650 V, Isolated high side, low side driver, UVLO, TTL Schmitt inputs	On Semiconductor	NCP51820AMNTWG
33	1	U100	5.0 V 250 mA DFN	MicroChip	MCP1703T-5002E/MC
34	4	U610, U611, U612, U614	Reconfig Logic	Nexperia	74LVC1G99GT,115
35	2	U615, U616	Bi directional SW 5E 5.5 V	Texas Instruments	SN74LVC1G66DBV

Table 3: Optional Components

Item	Qty	Reference	Part Description	Manufacturer	Part Number
1	1	C87	CAP CER 0.1 µF 25 V X7R 0603	TDK	C1608X7R1E104K080AA
2	1	Cout	TBD	TBD	TBD
3	2	D1, D2	DIODE SBR 400 V 1 A POWERDI123	Diodes Inc.	SBR1U400P1-7
4	3	J1, J2, J32	MMCX Jack SMD Vert.	Molex	734152063
5	1	J9	7.62 mm 2 pos. Euro Block	Wurth	691216410002
6	1	J81	Header Male 100 mil 1 row, 2 pos., Thru Vert.	Tyco	4-103185-0-02
7	1	L1	TBD	TBD	TBD
8	2	R11, R22	RES 0 Ω JUMPER 1/16 W 0402	Stackpole	RMCF0402ZT0R00
9	1	R84	RES SMD 10 K Ω 5% 1/10 W 0603	Yageo	RC0603JR-0710KL

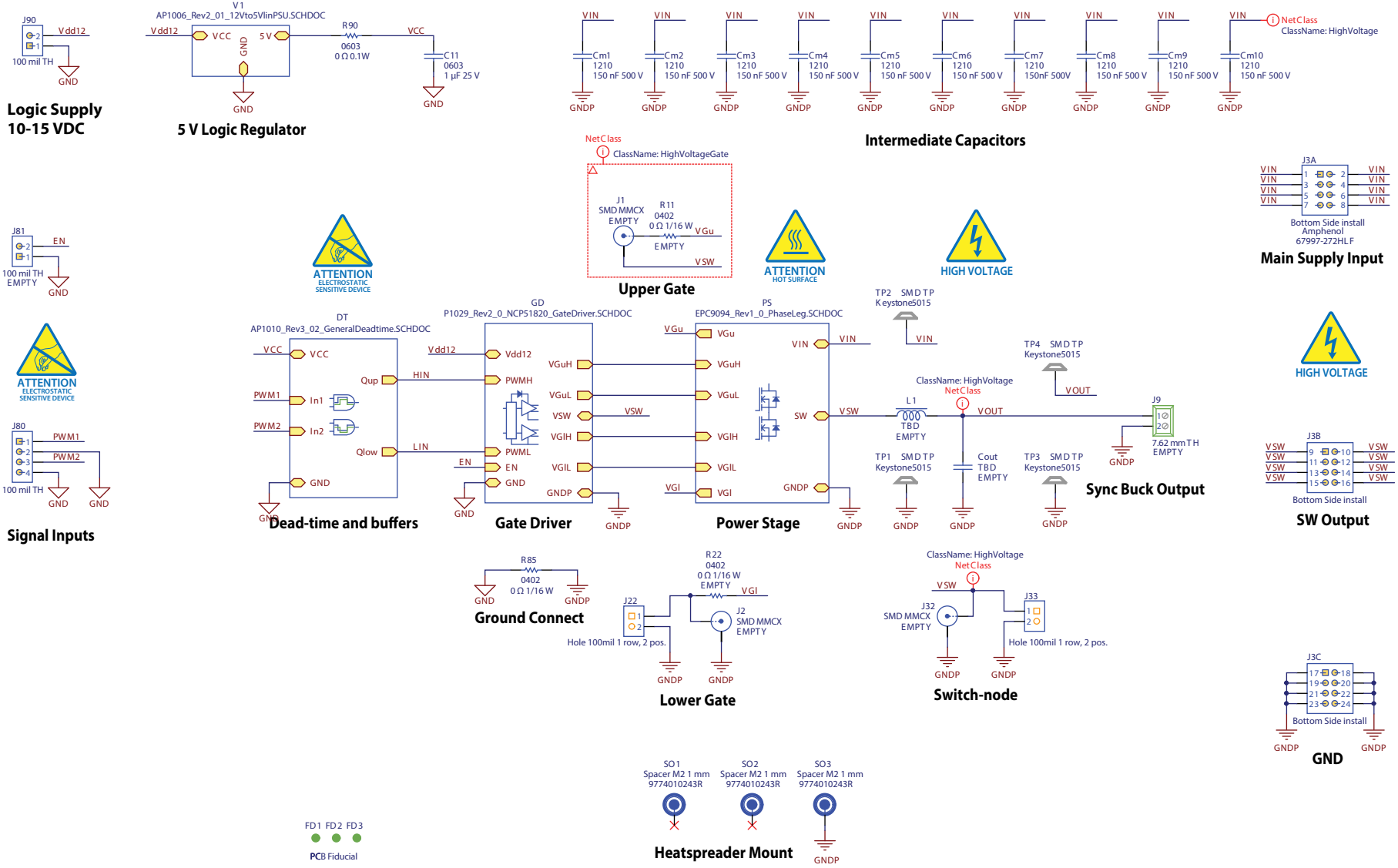


Figure 15: Main schematic

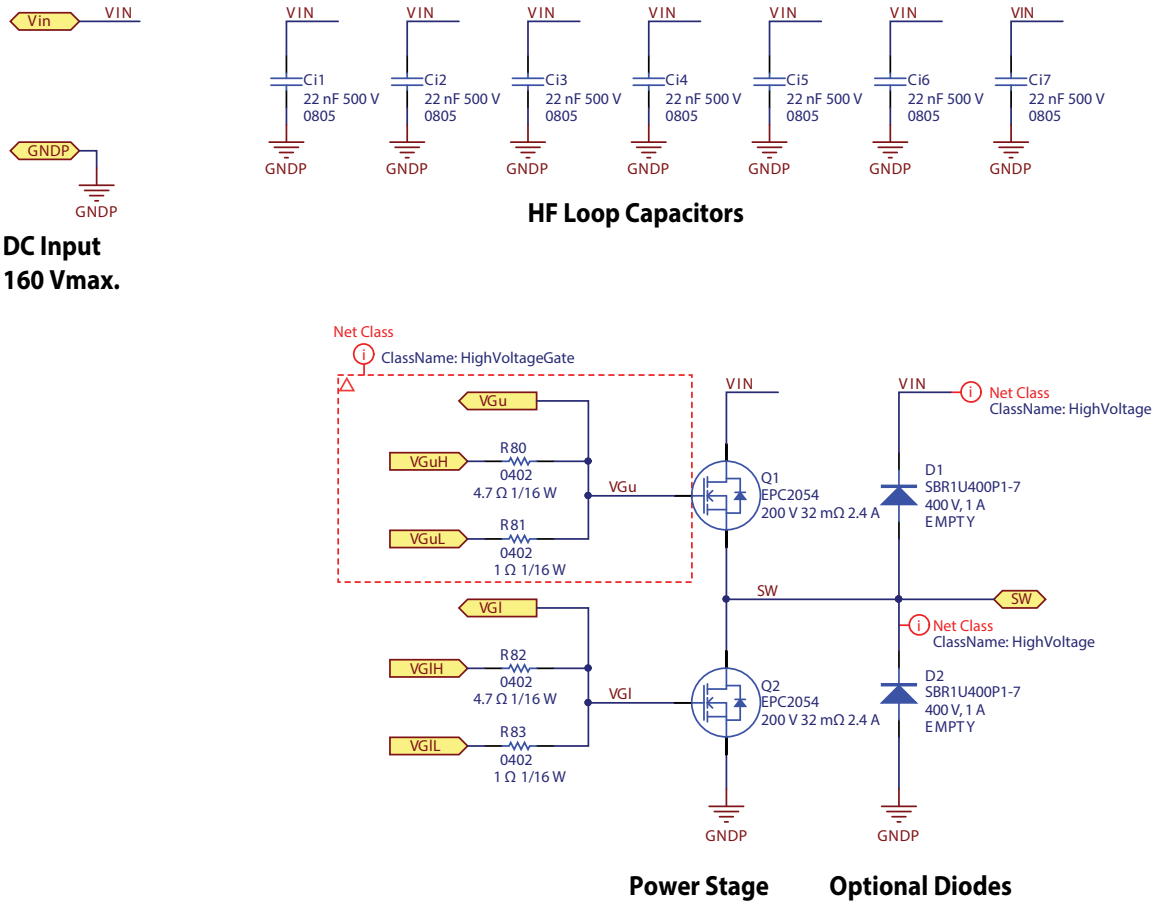


Figure 16: Power Stage schematic using EPC2054

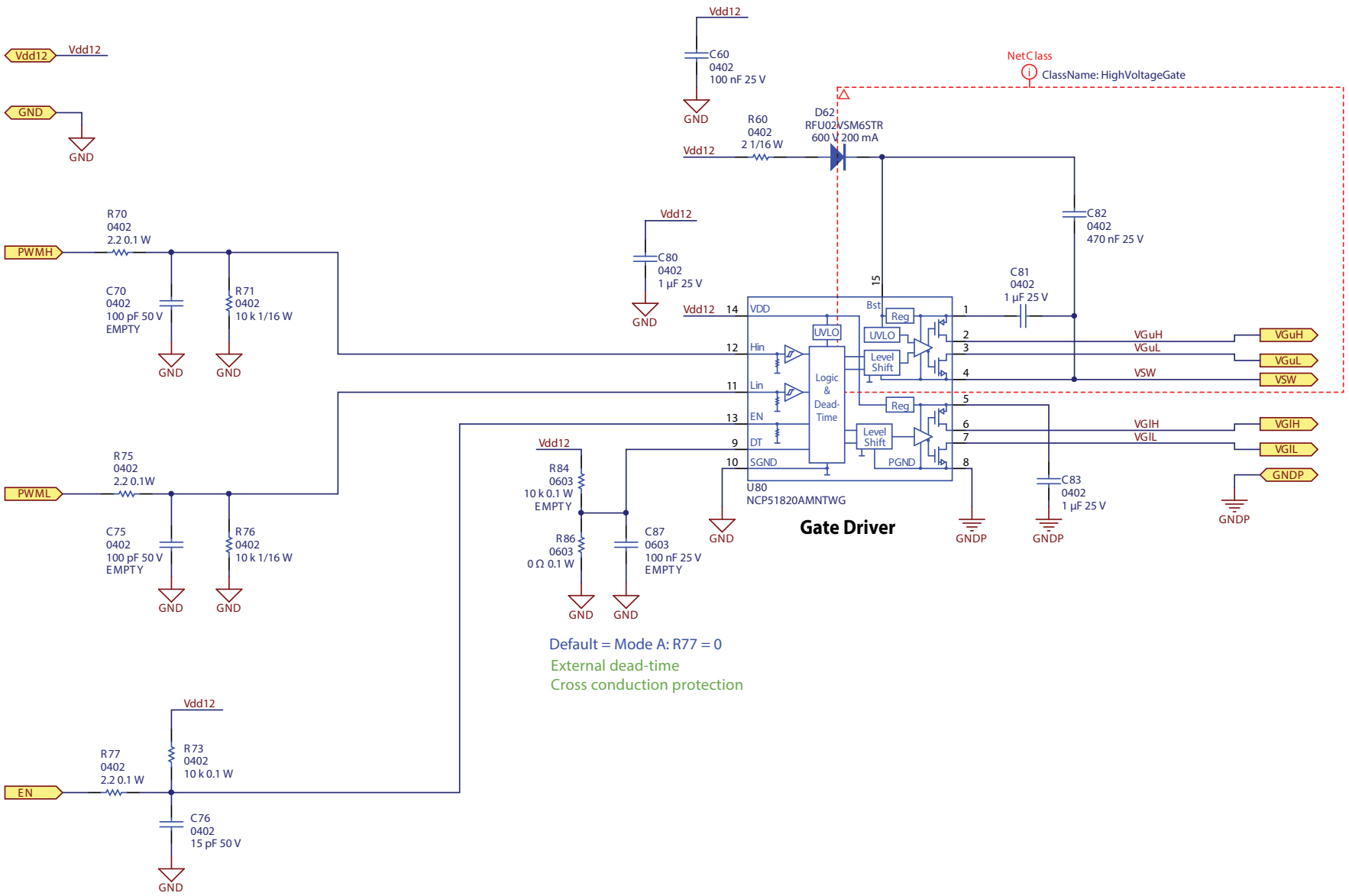


Figure 17: Gate Driver schematic

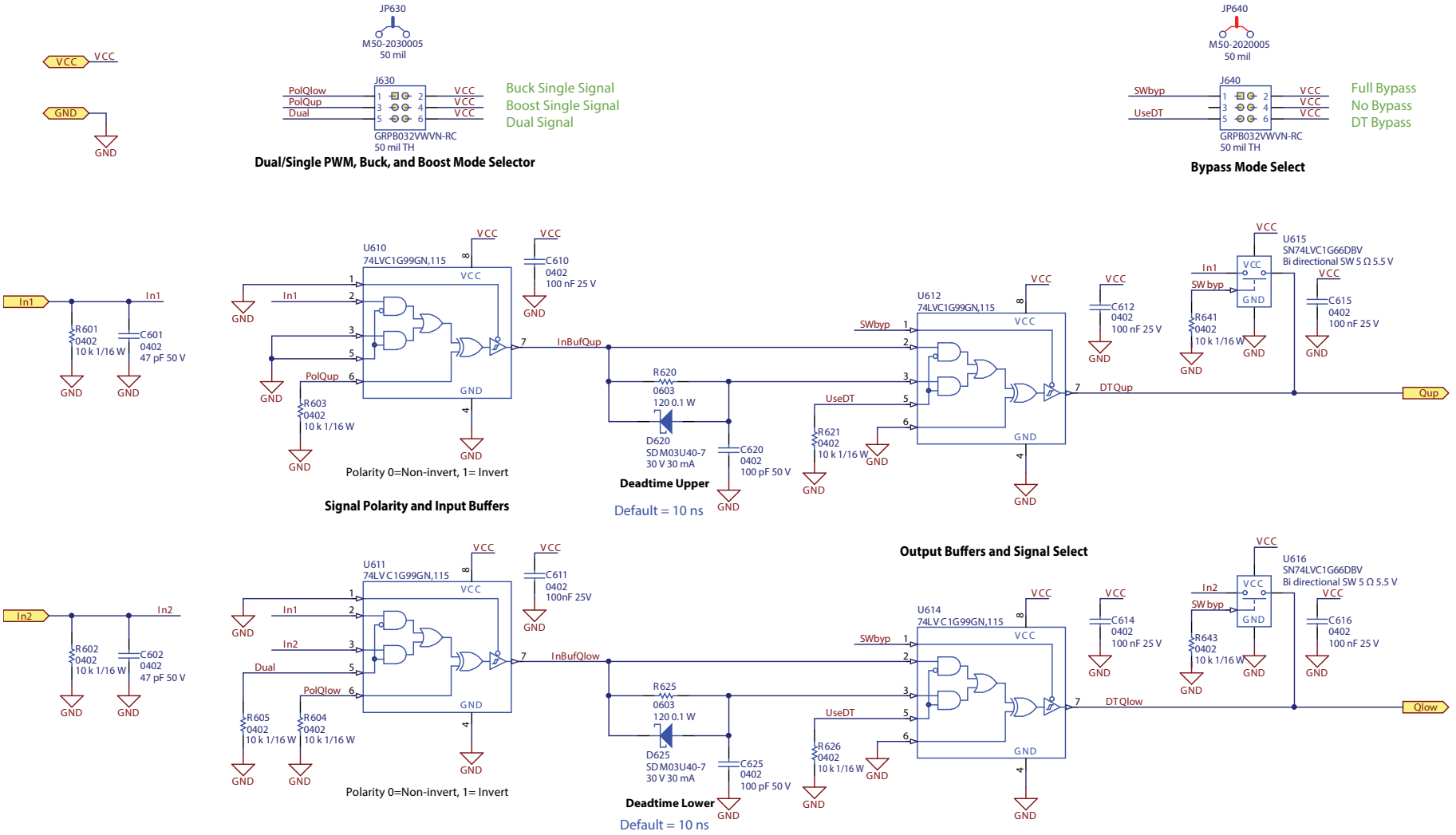


Figure 18: Dead-time and Bypass schematic

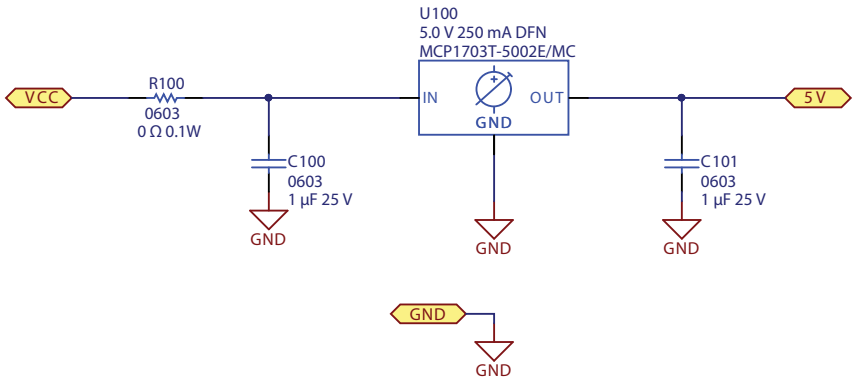


Figure 19: Logic Supply Regulator schematic

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