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A Programmable Microsystem Using System-on-Chip for Real-time Biotelemetry

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***Abstract*—A telemetry microsystem, including multiple sensors, integrated instrumentation and a wireless interface has been implemented. We have employed a methodology akin to that for System-on-Chip microelectronics to design an integrated circuit instrument containing several "intellectual property" blocks that will enable convenient reuse of modules in future projects. The present system was optimized for low-power and included mixed-signal sensor circuits, a programmable digital system, a feedback clock control loop and RF circuits integrated on a 5 mm × 5 mm silicon chip using a 0.6 μm, 3.3 V CMOS process. Undesirable signal coupling between circuit components has been investigated and current injection into sensitive instrumentation nodes was minimized by careful floor-planning. The chip, the sensors, a magnetic induction-based transmitter and two silver oxide cells were packaged into a 36 mm × 12 mm capsule format. A base station was built in order to retrieve the data from the microsystem in real-time. The base station was designed to be adaptive and timing tolerant since the microsystem design was simplified to reduce power consumption and size. The telemetry system was found to have a packet error rate of 10^{-3} using an asynchronous simplex link. Trials in animal carcasses were carried out to show that the transmitter was as effective as a conventional RF device whilst consuming less power.**

***Index Terms*—Biomedical telemetry, laboratory-in-a-pill, microsystems, system-on-chip, very-large-scale integration.**

I. Introduction

THERE is a growing need for microscale telemetry devices for a variety of medical applications. An important example is the development of wireless sensor systems that can be integrated into a noninvasive capsule format to perform endoscopic functions within the gastrointestinal (GI) tract. The first demonstration was described by Mackay more than four decades ago [1]. Since then several capsules have been prototyped, as listed in Table I [2]–[7]. In all cases, after oral administration, the ingestible capsule is naturally transported by peristalsis from the mouth to the anus, where it is egested. Different physiological parameters, including temperature, chemical concentrations and images, can be captured within the GI tract, and the data relayed wirelessly to a body-worn device (base station). The basic structure of such devices comprises contact (e.g., pH) or noncontact sensors (e.g., temperature), an instrumentation circuit, a transmitter, and a power source [8].

There are several key requirements for the ingestible telemetry systems. The capsule must be cheap to make since it will only be used once. Low-power consumption is a requirement to minimize battery, hence overall, size and increase operating time. Gastric emptying takes between 0.5–4 h to complete and semi-digested food (chyme) takes 2–3 h to pass through the small intestine. Once in the colon, gut content moves relatively slowly at approximately 5–10 cm/h. Peristaltic waves in the colon are known as mass movements and only occur 1–3 times per day. Overall the capsule might take a maximum of 8 h to traverse the upper alimentary tract and the small intestine, while a complete passage through the GI tract might take up to 32 h. Using silver oxide battery technology, an energy storage density of 500 mWh/mL can be achieved [9], thus we estimate that a suitable source, such as two SR48 cells (75 mAh each) could deliver enough energy to complete small intestinal measurements if the power consumption was less than 20 mW.

GI diagnostics, especially diagnostics of functional GI disorders, show a strong event-related character [10]. This indicates the importance for real-time monitoring, by which any symptom, e.g., heartburn or vomiting, can be simultaneously linked with intra-luminal physiological observations [11]. Unfortunately, existing telemetry devices do not provide multichannel real-time analysis. A further limitation of all the existing devices is the lack of on-capsule programmability that is important to achieve design flexibility and reconfigurability. In this paper, a programmable biotelemetry microsystem that can perform multiple analytical functions and work in real-time with a computer-based base station is presented. The results presented are the culmination of several prototyping stages.

II. Design Considerations

Early biotelemetry designs used a transmitter based on a single transistor oscillator circuit for which the sensor was an integral part [12], [13], and without digital technology. In the microsystem presented here a microcontroller with embedded software and RAM was implemented to provide greater control and flexibility. With the increasing complexity of instrumentation circuits, it was desirable to use a system-on-chip (SoC)

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TABLE I
TELEMETRIC DEVICES FOR GASTROINTESTINAL MONITORING

Device	Descriptions	Multiple sensing	Real-time analysis	RF (MHz)	Size (mm)	Comments
SMART pill	Intra-luminal pH measurement, tubeless gastric analysis, an alternative for pentagastrin tests.	Y	N	1.98	20.0 x 8.0	Upgraded Heidelberg-type pH pill [2]
M2A	Imaging within GI tract, positive for the inspection of IBDs and Crohn's disease.	N	N	434	26.0 x 11.0	GivenImaging ® [3]
NASA pill	Body temperature measurement; identify temperature changes within a potentially ulcerated area.	N	N	174 - 216	30.0 x 10.0	Implantable [4]
BRAVO	Catheter-free oesophageal pH monitoring, GERD diagnosis	N	N	433	25.0 x 6.0	Medtronic ® [5]
InteliSite	Drugs absorption assessment within a specific GI region	N	N	6.78	35.0 x 10.0	Proof-of-concept [6]
GI micro-robot	Bi-directional wireless endoscopes	N	Y	434	40.0 x 11.0	First-stage deliverables of its long-term goals [7]
Drug pill	The largest capsule for oral drug delivery		N / A		23.3 x 8.2	Size 00

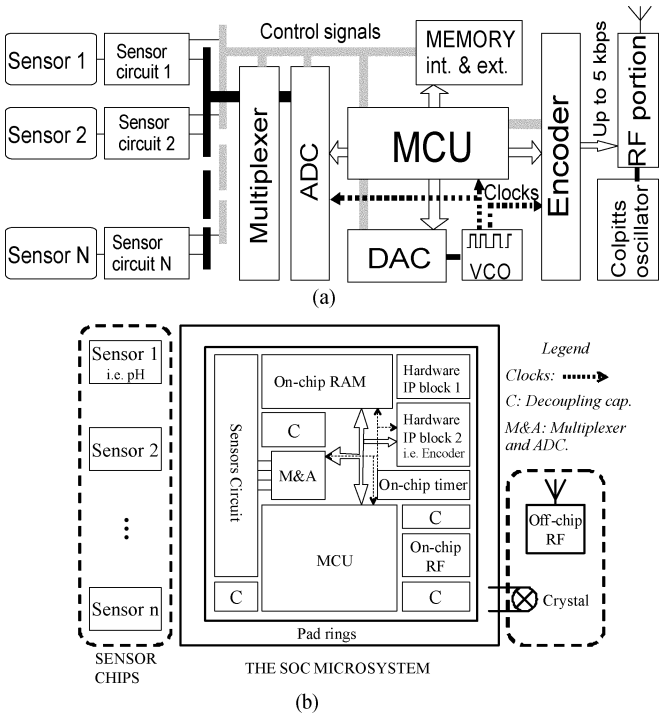

Fig. 1. (a) Block diagram of the microsystem instrument and (b) a block-by-block floorplan of the SoC.

design methodology, in which the whole circuit, including all digital and mixed-signal components, were integrated on to a single piece of silicon [14]. In such a heterogeneous design where hardware and embedded software co-exist, hardware intellectual property (IP) blocks can be implemented wherever the software cannot meet the timing constraints, e.g., in real-time data encoding and authentication. However, the use of dedicated hardware should be minimized in order to achieve greater flexibility via programmability [15]. With these constraints we specified the SoC micro-instrument design shown in Fig. 1.

Cadence EDA tools were used for analogue design, mixed-signal simulation, and back-end design tasks such as automatic place-and-route of structural net-lists. Synopsys tools were used for VHDL behavioral level simulation and register transfer level synthesis. Unlike an instrumentation circuit consisting of circuit boards, where component replacement and track modifications are relatively easy, post-fabrication changes to an integrated circuit (IC) is difficult. IC verification was therefore used, and the design was exhaustively simulated to ensure that it performed correctly. Field-programmable gate array verification was performed for complex digital components, prior to IC implementation. The chip was fabricated on a 0.6 μm, 3.3 V CMOS process from the Austriamicrosystems accessed through the Europractice small volume multiproject-wafer facility.

Although the use of a SoC-like architecture can enable the capsule to be functionally complex, the overall system configuration, including the base station, is highly asymmetric—i.e. the microsystem was made deliberately simple compared to the base station since the electrical power and computing resource available on the base station far exceed those that can be built into the microsystem. Since the microsystem was designed for relatively low data-rate acquisition and transmission [16], a 10 kbps transmission bandwidth was considered sufficient. This implies that a 320 bps "raw" data rate can be achieved using 16 sensors (if desired), a 10-bit ADC, 2 Hz sample rate and single-channel transmission with a 32-fold encoding and encryption overhead. The base station however, is required to decode the data, maintain a database, and present a user-friendly interface.

III. THE SOC IMPLEMENTATION

A photomicrograph of the fabricated SoC instrument is shown in Fig. 2. It includes multiple sensor circuits, an analogue-to-digital converter (ADC), a programmable microcontroller (MCU) and memory (SRAM) and hardware IP blocks. These include a serial peripheral interface (SPI), a direct-sequence spread-spectrum (DS-SS) digital encoder, a voltage-controlled oscillator (VCO) and a RF transmission circuit. The final size of the chip was 5 mm $\times$ 5 mm.

A. Sensor Circuit

The SoC has eight input channels. These comprise two temperature, two ISFET pH, two conductivity, and two dissolved oxygen sensors, providing channel redundancy. Two different bio-MEMS sensor chips were implemented [17]. One comprised a silicon diode temperature sensor, an ISFET pH sensor and a two-electrode conductivity sensor; the second chip had

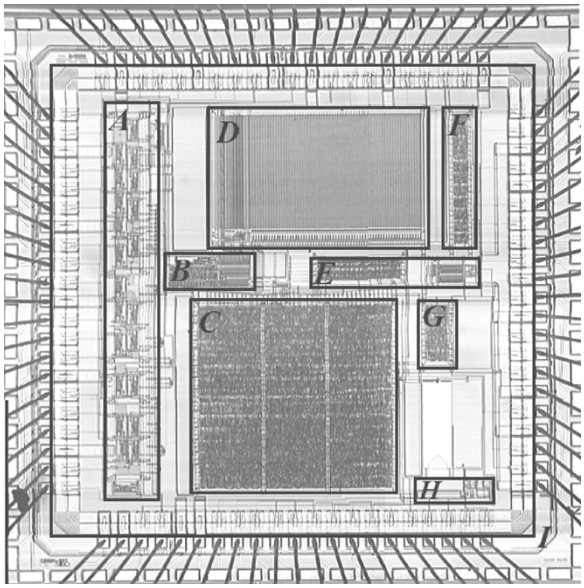

Fig. 2. Micrograph of the SoC instrument. (a) The multiple sensor circuits; (b) the ADC; (c) the MCU; (d) the SRAM; (e) the VCO and the clock feedback control circuit; (f) the DS-SS encoder; (g) the SPI; (h) the RF transmission circuit; and (i) the double pad-rings.

an oxygen sensor. Both sensor chips measured 5 mm × 5 mm. The analogue circuits on the SoC were designed to permit minimal physical dimension and power consumption, without reducing the sensitivity or dynamic range. All of the analogue outputs from the sensor circuits were fed into the ADC via a multiplexer (Table III). The bandwidth for individual analogue channel was limited by a sampling interval of 0.2 ms.

B. The Programmable Digital System

The 8-bit MCU, with its instruction code stored in the 2 kB SRAM, supervised the microsystem operation. When powered on, a bootstrapping program was activated, and the MCU waited for code to be downloaded from a host machine. The download procedure employed a three-wire unidirectional serial protocol, and the host machine set the download data rate. The bootstrapping program issued a soft reset when the required 2 kB had been sent, and passed control to the CPU for code execution. Once the program has been loaded the download connections can be removed. During the execution stage, the MCU regularly accesses the RAM to get instruction codes and data.

The optional SPI was implemented to allow the MCU to access up to 64 kB of external memory, which could be used for mass data storage when real-time data handling was not required. The SPI was a significantly reduced version of the standard specification using only one-fifth the number of transistors. The DS-SS encoder block was a serial-input serial-output digital block. Its core component was a pseudo-random (PN) noise code generator [18]. The PN code length was controlled by the MCU to provide an encrypted multiplication process for data transmission. The PN code could also be rearranged, making it possible for several telemetry microsystems to share one receiver, using code division multiple access. The SPI and the encoder were synchronized by the MCU.

C. On-Chip Oscillator Blocks and Transmission Circuit

A VCO was implemented to provide an on-chip clock as an alternative to an external clock source to eliminate the need for a bulky off-chip oscillator module [19]. The control voltage could be modified locally through an on-chip DAC, the inputs of which came from the MCU [Fig. 1(a)]. Using this technique, a feedback clock control loop was built, so that the clock rate could be dynamically adapted by the MCU. The problem with such a loop is that its initial state is unknown therefore the control voltage has to be externally derived during the code download stage. Once the execution stage has started, the MCU wrote the data into the DAC and set the control voltage close to the externally provided one. The external voltage source can then be disconnected so the clock control loop operates autonomously. In future implementations the initial control value may be determined from an on-chip reference. The oscillator signal was conditioned to a 50% duty cycle square-wave signal and used as the chip clock source. Previous experience revealed that, due to the fabrication tolerance of resistors and capacitors, there was an up to 30% variation between the designed oscillation frequency and the measured value [20]. By using such a control loop the on-chip timing could be adjusted to compensate for this variation.

The RF transmission circuit comprised a Colpitts oscillator, a frequency-shift-keying (FSK) modulator, and an output stage. A crystal device and two capacitors were externally connected to set the carrier frequency to 30 MHz. This frequency was chosen since the 300 kHz to 30 MHz range contains transmission frequency bands suitable for ingestible radio pills in animal and human medical applications [21], and experimental results have shown that the frequency spectrum below 25 MHz is crowded due to atmospheric channel noise, short-wave broadcasting (3–26 MHz) and high power generation [22]. In addition, the Colpitts oscillator provided an alternative crystal-stabilized oscillator signal for all of the digital system.

D. Back End Design and Embedded Software Design

In total, there were 84 input/output (I/O) and power pads in a primary pad-ring, approximately two-thirds of which were used for testing [23]. Eight separated power pad pairs were used, making it possible to measure the individual power consumption of each functional block. Due to reliability problems with wire-bonding to off-chip components, a second pad-ring comprising larger bond-pads (approximately $100\,\mu\text{m} \times 200\,\mu\text{m}$) was included. The floor plan separated the noise producing blocks from the sensitive analogue blocks, i.e., the VCO and the RF transmission circuits were placed apart from the sensor circuits.

In addition, guard-rings connected to the substrate enclosed all of the sensitive blocks. Power pads for the analogue circuits, digital systems and RF transmission circuit were isolated in order to minimize cross talk [24]. Approximately 100 pF of capacitance was distributed on-chip to aid power supply decoupling [25].

The embedded software occupied 25% of the total on-chip SRAM. It contained a main routine and a timer-interrupt routine. The sample interval was set at 2 seconds. The main routine did all the system scheduling, sampling control and coding operations. This routine was not timing critical and took approximately 100 ms to complete. Every 8 ms, the timer-interrupt was

TABLE II
DETAILED SPECIFICATIONS OF THE SoC MICRO-INSTRUMENTATION

Part	Functions	Key features	Size mm^2	Num. of transistor	IP * origin	IP ** status	Comments
Sensor Circuit	Analogue signal conditioning	8 channels, DC bias circuit and low-power consumption design	1.8	1,100	S	C	External sensor chips needed
ADC	Analogue-to-Digital conversion	8-bit rail-to-rail	0.4	2,100	F	C	Successive comparison
MCU	System scheduling	32 bytes internal RAM, 24 I/O ports, 16-bit free running timer, Interface circuit with the SRAM implemented, Motorola 6805 instruction-set compatible	2.7	51,000	S	C	Programmable, Bootstrapped, Maximum 4 MIPS
RAM	Codes and data storage	2048x8 bits	2.1	107,000	F	C	Dual port static RAM
VCO	Tuneable on-chip timing	Feedback controllable	0.5	4,200	S	O	Phase noise and jitter
DS-SS coder	Source coding and CDMA	PN length configurable	0.3	1,600	S	O	32x - 256x multiplication
SPI	EEPROM access	One-fifth of the origin specification	0.1	3,200	S	O	External EEPROM needed
RF Circuit	RF Transmission	FSK based on a Colpitts oscillator	0.2	50	S	O	External tuning devices needed
Pad-ring	I/O and power pads	Inner: 84 PLCC package Outer: manual bonding	10.0	0	S	C	Double rings
Total	-	-	25.0	170,000	-	-	-

* S- self-developed IP block or F- foundry IP block. ** C- core IP block or O- optional IP block.

invoked, and the content of a one-bit serial port was updated. Therefore, during each sample interval, the serial port output a 250-bit binary stream. The "raw" data rate was thus 125 bps. This output was directly fed into the DS-SS encoder. The binary stream comprised a 192-bit data packet followed by a 58-bit "zero-period." This "zero-period" was useful to ease the design effort for asynchronous real-time data acquisition, since it was an obvious landmark that could be used to confirm the location of every data packet, which contained two identical 64-bit codes and 64-bit authentication and parity redundancies. All the routines were fully simulated using a development tool before being downloaded into the SoC. Table II summarizes the individual blocks.

IV. SoC PERFORMANCE ANALYSIS

A. Function Evaluation

Evaluation of the SoC was performed using conventional laboratory test equipment. All digital blocks and the on-chip SRAM were analyzed. Desired waveforms from test pads were observed using a logic analyzer and a 4-channel oscilloscope. Execution codes were successfully downloaded from a standard PC parallel port. The SPI was found to be capable of accessing an external memory IC (AT25HP512 from ATMEL). The encoder generated the desired multiplication codes for all lengths from 32 bits to 256 bits. Several sensor chips were connected and tested to ensure correct functionality. Table III lists the test results. Each channel includes the external sensor and the sensor electronics for our design and one channel (T_E) is data from a commercial temperature sensor IC for comparison. The RF transmission circuit was tested with a standard crystal and two capacitances of 10 pF and 22 pF. Output from the Colpitts oscillator was measured to be 1.0 V p-p. Power consumption of the RF circuit was measured to be 5 mW at 30 MHz, with 3.3 V power supply.

TABLE III
SUMMARY OF THE SENSORS' CIRCUIT PERFORMANCE

Channel	Linear Dynamic Range	Sensitivity	Reso-lution	Output drift with supply voltage
T_I	10 °C - 50 °C	35 mV/°C (2.8 bit/°C)*	0.4 °C	Linear 600 mV / V @ 25 °C
ISFET pH	pH 1 - 10	50 mV/pH	0.1 pH	N/A
Conductivity	0.05 - 10 mS/cm	165 mV/ decade	0.02 mS/cm	N/A
Dissolved Oxygen	0 - 10 mg/mL	7.9 nA/mg	0.4 mg/L	N/A
T_E **	0 °C - 100 °C	28 mV/°C (2.2 bit/°C)*	0.5 °C	Linear 270 mV / V @ 25 °C

* At 12.5 mV per bit.
** Using an AD22103 temperature IC module.

The VCO was tested using a variable DC power supply and an oscilloscope. Three different tests were carried out to investigate the VCO performance under typical operating conditions: i) the clock control loop (Section III-C) was activated so the voltage for the VCO was changed by the MCU and the supply voltage was constant; ii) the control voltage was kept constant and supply voltage was changed; iii) the control voltage was set by the MCU to be one-fourth of the supply voltage (tracking) and the supply voltage was changed. For test i), the oscillation frequency was found to vary between 1 kHz and 10 MHz, when the supply voltage was fixed at 3.0 V and the control voltage was changed between 0.1 V and 1.0 V. The tuneable control voltage, V (V), and the oscillation frequency, f (kHz), show a logarithmic dependence ($V = A \log_{10} f + B$), where $A = 2.77$ for test i), 1.95 for test ii) and 2.35 test iii), respectively, and $R^2 > 0.95$. B was a constant that changes for each condition, but was not required for the compensation routine described in Section VI-A.

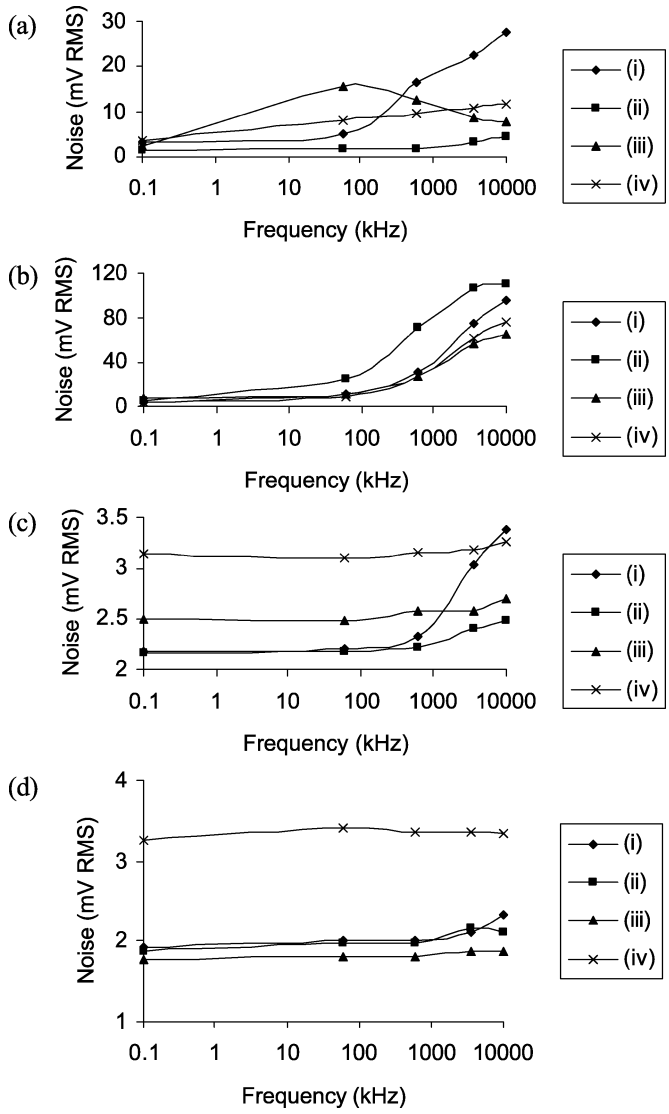

Fig. 3. On-chip noise distribution measured from (a) a positive power node, (b) a digital output node, (c) an analogue input node, and (d) an analogue output node. The VCO frequency was swept from 0.1 kHz to 10 MHz. For each figure the curves are i) the SoC with RF transmission circuit disabled; ii) the SoC with a 100 μF decoupling capacitor; iii) the SoC with the TX connected; and iv) the SoC with RF transmission circuit activated.

B. Noise Distribution Evaluation

On-chip noise distribution was measured when the SoC was powered with two SR48 cells. Four nodes: an analogue input node; an analogue output node; a digital output node; and a positive power node; were connected to the 4-channel oscilloscope so they could be measured simultaneously. The oscilloscope inputs had a bandwidth of 150 MHz and were AC coupled. The tests were carried out on the following configurations: the RF transmission circuit disabled; a 100 μF decoupling capacitor externally connected; a discrete transmitter (the TX, described in Section V) externally connected; the RF transmission circuit activated. In all the configurations, the VCO frequency was swept from 0.1 kHz to 10 MHz, and all other input nodes were grounded.

Fig. 3 shows the noise propagation within the SoC. Ambient noise (when the entire SoC was powered off) was measured to be less than 2 mV RMS. Frequency domain analysis clearly showed that $1/f$ noise made a very limited contribution to the overall noise at low frequency. Phase noise from the VCO was measured since it is the frequency accuracy and stability of the oscillators that is important, rather than the waveform itself. The VCO was tuned to around 10 MHz and the phase noise measured was -20 dBc/Hz at a 30-kHz offset.

TABLE IV
POWER CONSUMPTIONS FOR THE SOC MICROSYSTEM

Part	Static power dissipation (μW)	Dynamic power dissipation (μW/MHz)	Comments
MCU and the digital peripherals	N/A	1000	Including the SPI and the DS-SS encoder.
SRAM	100	560	Matched with the foundry specifications.
ADC	1000	20	Only active over 0.1 % of sample cycle.
VCO	2400	15	Constant for control voltage in range 0.1 V to 1.0 V.
Sensors and conditioning circuits	2500	0	Temperature sensors connected. Inputs to other channels were grounded.
On-chip RF circuit	5 mW		3.3 V power supply, 30 MHz oscillation.
Total	14 mW		3.3 V supply, 100 kHz clock rate, with temperature sensors, CPU 100% active.

C. Performance Summary

The SoC and each of its functional blocks worked successfully. During full-execution, the SoC power consumption (without the on-chip RF transmission circuit) was approximately 9 mW at 3.3 V and 6 mW at 2.7 V. Table IV details the dynamic and static power consumption. The SoC noise was almost entirely generated by the on-chip coupling between the VCO or the Colpitts oscillator and various IP blocks. The crystal-based Colpitts oscillator contributed approximately 50% more on-chip noise to the analogue I/O nodes than the VCO. Because of the physical block separation and the guard-rings, the couplings to the sensitive analogue I/O nodes were significantly reduced to the 2–3 mV RMS level. This was equivalent to 1/4 LSB of the ADC for 3.0 V power supply. The isolated power supplies however, had a limited effect on global noise reduction, since the power lines eventually joined at the batteries. The digital and power nodes suffered more noise in absolute terms, but this noise was of less significance to the overall system performance.

V. INTEGRATION TO A MICROSCALE DEVICE FORMAT AND IN SITU RF TRANSMISSION TESTS

The on-chip RF transmission circuit required discrete tuning components and an RF antenna, hence offered no real size improvement. As described in Section IV-C the Colpitts oscillator also injected excessive noise into the instrumentation circuits

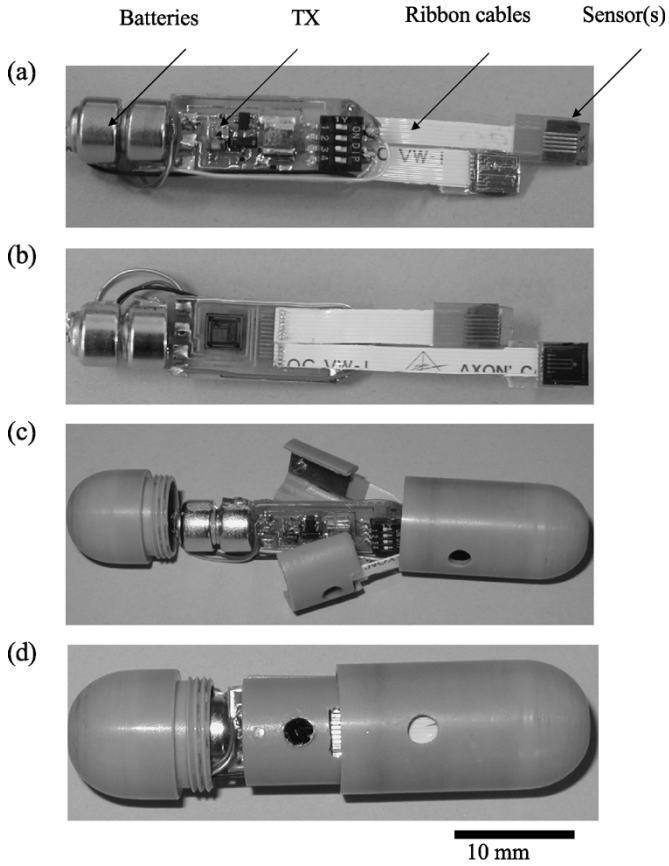

Fig. 4. The packaged capsule and its contents. (a) The inner structure—top side; (b) the inner structure—bottom side; (c) the fixing of sensor chips into the sensor holder clamps; and (d) alignment procedure with the outer case.

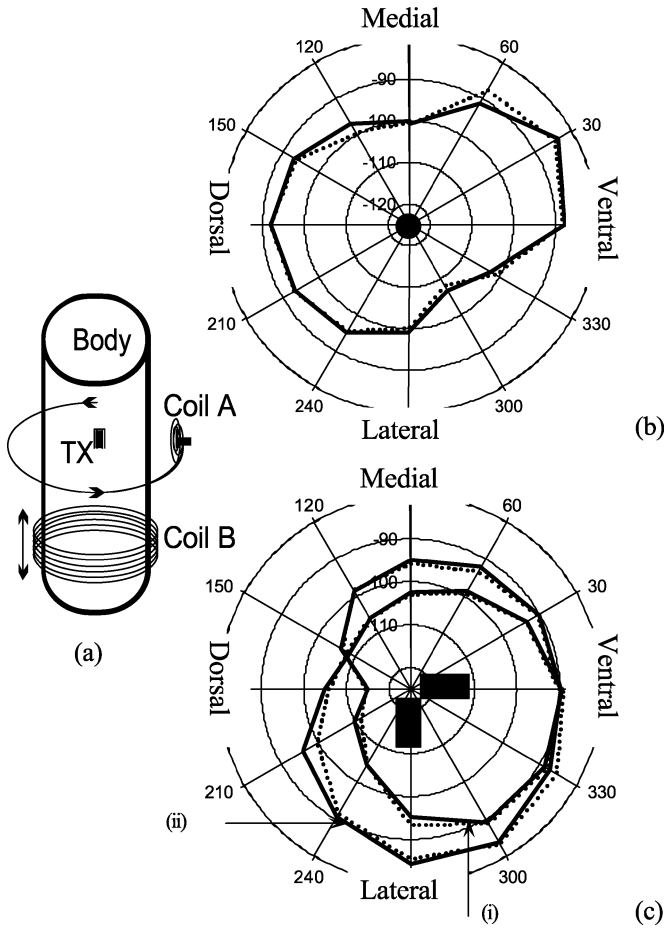

Fig. 5. (a) The *in situ* TX transmission test set-up showing how coils A and B were used. Coil A was 10 cm in diameter with its axis normal to a radial from the body axis. Coil B was 25 cm in diameter and 20 cm in width and enclosed the carcass such that it could be vertically moved. (b) RF field strength plot with the TX coil aligned on the cranial to caudal axis. (c) RF field strength plots with (i) the TX coil was placed in a dorsal to ventral orientation and (ii) the TX coil aligned on the medial to lateral axis. Solid lines show the measurement made by clockwise rotation of coil A and the dashed lines show the anticlockwise measurement, demonstrating an absence of hysteresis. Angular axis: degrees. Radial axis: dBm.

and was deactivated. Instead, a discrete transmitter (TX) with an identical circuit and tuning components was built [Fig. 4(a)]. The off-chip TX used a 1 μH surface mount coil inductor (ferrite core) in its output stage to act as a magnetic coupler, eliminating the need for an RF antenna [26], [27]. Tests indicated that the maximum data rate was 5 kbps and the FSK deviation was 10 kHz. Operating at a frequency of less than 50 MHz the device generated a quasi-static magnetic field and could communicate in the inductive near-field up to a range of 1 m in air [28]. As expected we found that there was no detectable signal at a range of 2 m due to the $1/r^3$ decay of the electromagnetic near-field strength thus we believe that, subject to testing in an appropriate standards laboratory, the TX was operating within the electromagnetic interference requirements for ingestible telemetry devices at a distance of 10 m [21].

Experimental measurements of RF transmission through animal tissue were carried out to verify the useful transmission range in a practical environment [29], [30]. Carcasses of three to four months old male pigs, with an average weight of 30 kg, were used in this experiment. The carcasses were not bled after slaughter, which was beneficial to this study due to the effect of blood and other body fluids on signal transmission [31]. An incision was made midline down the *linea alba* into the carcasses' abdomen. The TX was placed inside the carcasses' abdominal cavity in several known orientations. The incision was then sutured and the carcass hung (head up) from the ceiling of the pathology laboratory. The measurement setup is illustrated in Fig. 5(a).

Fig. 5(b), 5(c) show the detected RF field. Coil A was rotated around the carcass body in steps of 30° at a distance of 25 cm. A control run was performed for comparison prior to each *in situ* measurement. To estimate the overall signal strength for each set of measurements a single figure was derived using the arithmetic mean. Several runs with different TX orientations showed that the mean signal loss caused by carcass body absorption was approximately 1.5 dB hence the RF signal passed through the body relatively unimpeded. The noise floor was measured to be approximately -120 dBm.

Coil A was then removed. Coil B, similar to a wearable design [32], was "put on" the carcass abdomen and moved vertically at 10 cm increments. Results showed that the strongest RF signal was approximately -75 dBm and even with a further 5 dB signal attenuation due to variation in TX orientation and differences in carcass size, it was straightforward to retrieve in-gut information using coil B and a portable scanning receiver (WR-3150e from

WinRadio). The receiver could still detect a -105 dBm signal when the *in situ* TX was 0.5 m off the plane of coil B.

In addition to testing the TX, for the purpose of comparison, several commercially available transmitters (FM-RTFQ from RFsolutions) using conventionally propagating antennas operating at 315 MHz, 434 MHz and 868 MHz were tested in an identical manner [33], [34]. Each transmitter was built on to a small PCB with two size N batteries and sealed in a container. The antenna in each case was made using a square loop of 2 mm width copper track and a tuning capacitor, as required by the manufacturer's application notes. We found that the average carrier SNR detected by the coils was comparable for the TX and the RF transmitters. However, the TX was smaller $(8\ \text{mm} \times 5\ \text{mm} \times 3\ \text{mm})$ and consumed only 6 mW as opposed to 21 mW for each of the radio devices, representing a considerable power saving. By using the TX many of the drawbacks of the traditional RF systems such as scattering and security concerns can also be overcome.

The TX was therefore used to assemble a low-cost capsule package with the chip and the sensors. The packaging incorporated several discrete components connected using wire-bonding and chip-on-board technologies [35]. The overall size is 36 mm long and 12 mm in diameter. The complete capsule (including the SR48 cells) weighs 6.2 grams. The design included the use of the following components: an 8 mm wide double-sided PCB board to host the chip and the TX on each side; two flat flexible ribbon cables to connect the sensors; two sensor holder clamps attached to the sensor chips and to seal the sensing areas on each chip; miniature magnetic reed switches to enable external activation and deactivation of the microsystem; and a biocompatible polymer PEEK outer case, as illustrated in Fig. 4(b)–(d).

VI. Base Station Design and Overall Performance Analysis of the System

A. Base Station Architecture and Real-Time Data Retrieval

In order to operate the capsule over a simplex wireless communication link, the base station used the scanning receiver and a PCMCIA data acquisition card (DAQ) in a laptop PC to handle signal capture. Software routines were used for all fixed-point DSP tasks and graphical user interface (GUI) operations [36]. The scanning receiver was capable of outputting an analogue voltage proportional to the instantaneous transmission frequency within a preset channel bandwidth. This signal contained the transmitted data corrupted by electromagnetic interference. The DAQ device in turn digitised this analogue output by over-sampling at 1 kSps, which was 4 times higher than the *Nyquist* rate. The DAQ device was set to work in a continuous trigger model, in order not to lose any data samples between two sequential signal captures.

The DSP code was sophisticated to compensate for the relative simplicity of the microsystem design. A principal motivation for this was the timing inaccuracy of the low component count on-chip VCO [37]. The data processing flow for the base station is shown in Fig. 6. After pre-processing to generate a probability histogram for the analogue data values from the scanning receiver, the information was adaptively processed

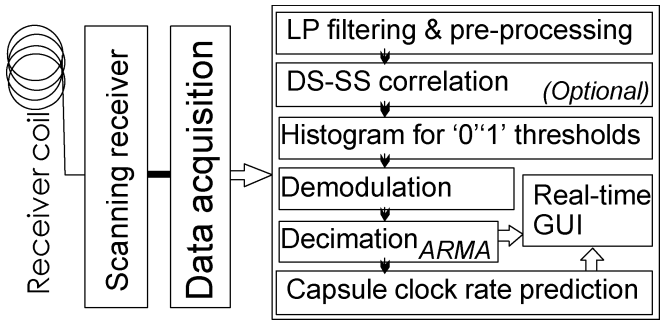

Fig. 6. Block diagram of the base station.

to generate a voltage threshold to distinguish between '0's and "1"s. Adequate discrimination between binary values was achieved for RF signal strength as low as -100 dBm. Signal demodulation was carried out on the captured data by an iterative routine that searched from both ends to find two 'zero-periods' and locate a data packet in-between. If a potential data packet was identified, further characters including bit integrity and bit length, were calculated to validate the data packet [38]. An auto-regression moving-average (ARMA) estimator and dynamically adjusted thresholds that were robust against timing variations were used for signal decimation. The output at this stage comprised the 192 information bits in memory that constituted a complete data packet. The odd parity and authenticity codes were checked to indicate whether the data had been corrupted. If all criteria were fulfilled, an indicator bit was set to '1', otherwise it issued a low-reliability warning "0." The final results, output in real-time via an interactive GUI, included data from the eight channels, the indicator bit, an estimated clock rate and an approximate time-stamp.

A routine that incorporates a means of predicting the possible change in supply voltage, based on an empirical logarithmic correlation between the VCO supply voltage and its oscillation frequency was implemented (Section IV-A). Frequency values were median-filtered prior to their predictions in order to be more robust. In addition, using the location information of the current data packet and the estimated clock rate, the start and termination locations of the following data packet were predicted to reduce the accumulated effect of timing deviation that could cause an outright loss of synchronization. The base station was thus able to match the expected data transmission rate to that of the microsystem.

Activating the on-chip multiplication process (through the DS-SS encoder) invoked an extra correlator routine in the base station. If the PN code length was set to be 32, the transmission data rate became $32\times$ the "raw" data rate (i.e., 4 kbps), and the over-sampling rate was modified to be 20 kbps. The decimated data packets could be directly recovered by thresholding the correlator output.

B. Real-Time Experimental Evaluation

For test purposes two temperature sensors ($\mathrm{T_I}$ and $\mathrm{T_E}$) were taped at a separation of 10 mm to the outside of a beaker. A laboratory thermometer (0.1 °C accuracy) probe was positioned halfway between the two sensors. The sensors and the probe were lightly insulated on the air-side. The beaker was filled with

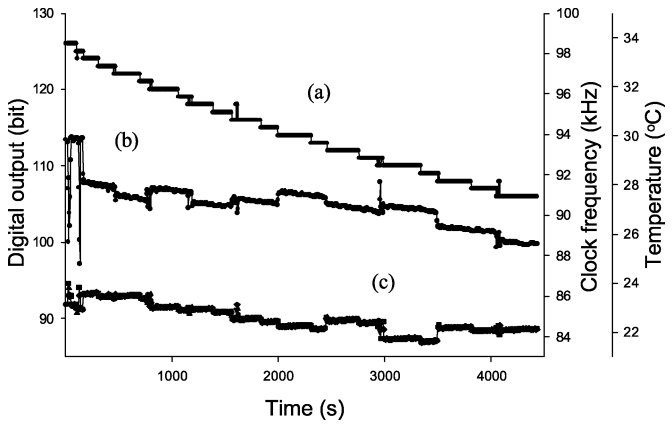

Fig. 7. Data retrieved in real-time over the first 1.2 h period when the timing drift is approximately 0.3 μs/h. (a) "Raw" binary value (left) from the temperature channel T_1; (b) clock frequency (right) estimated by the base station; and (c) linearly compensated temperature value (right offset) based on clock frequency falling as the supply (two SR48 cells) voltage drops over time.

water and placed on top of a hotplate so that its temperature could be controlled. The telemetry microsystem was placed on the central axis of coil B at a 0.2 m distance.

The telemetry microsystem was calibrated at different temperatures between 10 °C and 50 °C. The power supply was fixed at 3.0 V during calibration. Calibration results show a linear correlation between the environmental temperature and the digital output (y) such that $T_I = 0.33y_I - 15.5$ and $T_E = 0.51y_E - 10.7$, with $\boldsymbol{R}^2 > 0.98$ and 0.99, respectively.

The power supply was then replaced by two SR48 cells in order to assess performance as the terminal voltage degraded with time. It was found that the terminal voltage dropped from 3.3 V (fresh) to 2.0 V (end of life), and there was an 8–10 h operation period during which the terminal voltage was stable (drifting within 0.1 V). Fig. 7 shows a 1.2 h run. The temperature measured using the wireless microsystem was $22.6°\mathrm{C} \pm 0.5°\mathrm{C}$, which was in good agreement with the simultaneous thermometer readings of $22.5°\mathrm{C} \pm 0.1°\mathrm{C}$.

The concept of a packet error rate (PER) was introduced to quantify the data collection efficiency. It was calculated by dividing the number of low-reliability packets by the total number of data packets. Statistics from more than 100 runs show that the PER was approximately 10^{-3} when the RF signal strength was -90 dBm. This figure is approximately equivalent to a bit error rate of 10^{-5}, assuming each corrupt packet only has one corrupt bit. The PER could be less than 10^{-6} when the RF signal strength was stronger than -80 dBm. The noise floor was measured to be approximately -120 dBm, as before.

VII. Conclusion

We have developed a programmable telemetry microsystem for real-time biomedical monitoring. Operation and noise analysis have shown the System-on-Chip worked as designed. By using an on-chip VCO block, a clock feedback loop was realized, which eliminated the need for any external tuning devices. The magnetic induction-based transmitter was tested *in situ* and found to work well. The chip, the sensors, the TX and two SR48 cells were packaged into a capsule that was extensively tested. Using the concept of asymmetric system partitioning we were able to minimize the capsule complexity by using the greater resource of the base station to compensate for poor power quality and aggressive size constraints in the microsystem. The base station was capable of retrieving the sensor information from the microsystem in real-time and was robust against timing variations and RF interference. There were several noise sources that limited the overall system performance, such as the transient frequency changes caused by the VCO that was addressed by signal processing in the base station.

The operation of the system has been verified *in vitro* and in situ. We have been able to demonstrate the advantages of several new concepts in the context of a capsule-based telemetric device. Results from previous workers, as described in the introduction and in Table I, give us the confidence to believe that the techniques described in this paper can be readily translated to *in vivo* tests, and ultimately, human medical applications. Clearly there are several trade-offs to be made between this low-cost miniature microsystem and a more powerful solution. An in-capsule receiver would be useful in order to realize a synchronous wireless protocol and reduce the PER. However, this would have a negative impact upon size, weight, power consumption and cost. We therefore believe the asymmetric system presented in this paper could set a pattern for a wider range of wireless microsystem applications.

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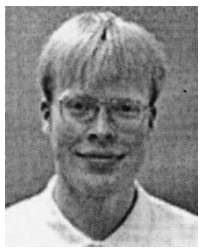

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