IEEE SOLID-STATE CIRCUITS SOCIETY™
IC Innovation

December 2020

UPCOMING VIRTUAL EVENTS

SSCS DECEMBER WEBINAR

Circuits and architectures for computation with ultra-wide power-performance adaptation - Well beyond voltage scaling

Presenter: Prof. Massimo Alioto
Wednesday, December 16, 2020
7:00 PM ET

Abstract: Wide power-performance adaptation is becoming crucial in always-on nearly real-time and energy-autonomous integrated systems that are subject to wide variability in the power availability and the performance target. Adaptation is indeed a prerequisite to assure continuous operation in spite of the widely fluctuating energy/power source (e.g., energy harvester), and to grant swift response upon the occurrence of events of interest (e.g., on-chip data analytics), while maintaining extremely low consumption in the common case. These requirements have led to the strong demand of a new breed of integrated systems having an extremely wide performance-power scalability and adaptation, beyond conventional voltage scaling or adaptive parallelism. In this talk, new techniques that drastically extend the performance-power scalability of digital circuits and architectures are presented. Silicon demonstrations of better-than-voltage-scaling adaptation to the workload are illustrated for both the data path (i.e., microarchitecture) and the clock path. Adaptation to a very wide range of energy/power availability is also discussed, presenting demonstrations of always-on systems (e.g., microcontrollers, power management units) with power down to sub-nW, and duty-cycled operation down to pW range. Several silicon demonstrations are illustrated to quantify the benefits offered by wide power-performance adaptation, and identify opportunities

and challenges for the decade ahead.

Bio: Massimo Alioto is a Professor at the ECE Department of the National University of Singapore, where he leads the Green IC group, and is the Director of the Integrated Circuits and Embedded Systems area and the FD-FAbrICS research center on intelligent&connected systems. He held positions at the University of Siena, Intel Labs CRL, University of Michigan Ann Arbor, University of California Berkeley, EPFL - Lausanne.

He is (co)author of 300 publications on journals and conference proceedings, and four books with Springer. His primary research interests include ultra-low power circuits and systems, self-powered integrated systems, near-threshold circuits for green computing, widely energy-scalable integrated systems, circuits for machine intelligence, hardware security, and emerging technologies.

He is the Editor in Chief of the IEEE Transactions on VLSI Systems, Distinguished Lecturer for the IEEE Solid-State Circuits Society, and was Deputy Editor in Chief of the IEEE Journal on Emerging and Selected Topics in Circuits and Systems. Previously, Prof. Alioto was the Chair of the "VLSI Systems and Applications" Technical Committee of the IEEE Circuits and Systems Society (2010-2012), as well as Distinguished Lecturer (2009-2010) and member of the Board of Governors (2015-2020). He served as Guest Editor of numerous journal special issues, Technical Program Chair of several IEEE conferences (ISCAS 2023, SOCC, PRIME, ICECS, VARI, NEWCAS, ICM), and TPC member (ISSCC, ASSCC). Prof. Alioto is an IEEE Fellow.

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Solid-State Circuits Directions Inaugural Workshop: Hardware Security

Monday, December 7th, 2020 at 7:00 AM PST / 10:00 AM EST
This event is free and open to all

EVENT DESCRIPTION

Solid-State Circuits Directions (SSCD) is a new technical committee within the IEEE Solid-State Circuits Society. Its charter is to promote forward-looking topics, improve our connection to developments at higher abstraction levels, and to stimulate interaction with other communities. One of SSCD's main activities will be member-driven technical workshops. The goal of this inaugural event is to introduce SSCD and its objectives in a two-hour online format. It will include two visionary talks on hardware security and its relevance to chip design.

AGENDA

7:00 AM PST: Welcome (Kenneth O, President, IEEE Solid-State Circuits Society)
7:10 AM PST: Introduction to Solid-State Circuits Directions (Boris Murmann, Stanford University)
7:20 AM PST: Call for Workshop Proposals (Vivienne Sze, MIT, and Payam Heydari, UC Irvine)
7:30 AM PST: Inaugural Workshop Presentations (Moderator: Chiraag Juvekar, Analog Devices)
Presentation 1: The Rise of the Insecure Processor (Chris Fletcher, University of Illinois)
Presentation 2: Post-quantum cryptography (Ingrid Verbauwhede, KU Leuven)
9:00 AM PST: Adjourn

PRESENTATIONS

The Rise of the Insecure Processor: What We Have Learned and Future Opportunities

Presenter: Chris Fletcher, University of Illinois

Abstract: The slowing of Moore's law has created a surge of innovation in the systems/hardware community, enabling once radical ideas such as "rethinking the computing stack" and "accelerators for everything" to enter the mainstream. With these new directions, however, comes potentially much greater system complexity, which in turn provides malicious actors ever more ways to exfiltrate and tamper with sensitive data.
My talk will describe this processor security landscape, present and future, in light of these technology trends. The main part of the talk will be to highlight several key, recurring techniques used by defenders and attackers, for both good and evil. I will discuss how these techniques apply in current threat models, hypothesize about how they will be used in the future and describe the cross-discipline opportunities that I see them enabling. The talk will conclude by highlighting several major open challenges.

Bio: Chris Fletcher is an Assistant Professor in Computer Science at the University of Illinois at Urbana-Champaign. He has broad interests ranging from Computer Architecture to Security to High-Performance Computing (ranging from theory to practice). These and related works have been awarded with election to the DARPA ISAT study group, the Intel CRC Outstanding Researcher Award, the NSF CAREER award, a Google Faculty Award, the George M. Sprowls Award for Outstanding Ph.D. Thesis in Computer Science at MIT, 13 paper awards, and were listed as one of ten "World Changing Ideas" designations by Scientific American. Among other projects at UIUC, he leads a center funded by Intel on Processor Security.

Post-Quantum Cryptography

Presenter: Dr. Ir. Ingrid Verbauwhede

Abstract: This presentation is not about quantum computing. Instead it will focus on novel cryptographic algorithms which are resistant to attacks from quantum computers. Indeed, the security of the most popular cryptographic algorithms relies on the computational complexity to break them, which

traditionally followed and still follows Moore's law. Yet, with the appearance of quantum computers, scaling key sizes following Moore's law is no longer valid: quantum algorithms can break existing cryptographic algorithms (so far only theoretically). Therefore, new computationally hard problems are being proposed: the so-called post-quantum secure cryptographic algorithms.
Besides resisting attacks from (future) quantum computers, these new algorithms should still run efficiently on existing processors, in hardware or software as dedicated ASIC's or instruction set extensions. Moreover, they should resist all current attacks, including side-channel and fault attacks. In this presentation we will show potential candidates, as the NIST post-quantum standardization is ongoing. We will also discuss the core hardware building blocks and implementation challenges.

Bio: Dr. Ir. Ingrid Verbauwhede is a Professor in the research group COSIC at the KU Leuven. She is a Member of IACR and a fellow of IEEE. She was elected as a member of the Royal Academy of Belgium in 2011. She is a recipient of an ERC Advanced Grant in 2016 and received the IEEE 2017 Computer Society Technical Achievement Award. She is a pioneer in the field of efficient and secure implementations of cryptographic algorithms on many different platforms: ASIC, FPGA, embedded, cloud. With her research she bridges the gaps between electronics, the mathematics of cryptography and the security of trusted computing, including Physically Unclonable Functions and True Random Number Generators. Her group owns and operates an advanced electronic security evaluation lab.

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NEWS

2021-2023 SSCS Members-at-Large

The 2021-2023 Members-at-Large on the IEEE Solid-State Circuits Society Administrative Committee are Ichiro Fujimori, Rikky Muller, Kazuko Nishimura, Esther Rodriguez-Villegas, and Hoi-Jun Yoo.

Please join us in congratulating the new Members-at-Large and thanking them and our other candidates -- Dina El-Damak, Don Draper, Ana Sonia Leon, Antonio Liscidini, Shanthi Pavan, Elkim Roa, and Farhana Sheikh -- for their participation and commitment to serving.

Congratulations IEEE Fellows 2021

Congratulations to the SSCS members elevated to IEEE Fellow in 2021.

The IEEE Grade of Fellow is conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest

Jun Ohta - *for contributions to CMOS image sensors and devices for biomedical applications*

Yogesh Chauhan - *for contributions to compact modeling of Si and GaN transistors*

Robert Henderson - *for contributions to solid-state single photon imaging*

Ahmed Ali - *for leadership in high-speed analog-to-digital converter design and calibration*

Benton Calhoun - *for contributions to sub-threshold integrated circuits and self-powered systems*

Inyup Kang - *for leadership in development of chip-set technologies for celluar communications*

Ali Keshavarzi - *for contributions to low-power circuits and devices in scaled CMOS technologies*

Dejan Markovic - *for contributions to low-power VLSI signal processing and neurotechnology*

A full list of SSCS members who are IEEE fellows are listed here.

Stay up-to-date with Learning with the SSCS Education Program

The **SSCS Education Program** provides Society members with free access to a wide range of quality educational content related to integrated circuits including tutorials, short courses, webinars, and eBooks.

- **Tutorials and Short Courses:** SSCS members have access to free tutorials and short courses from past years of ISSCC. Renowned experts in the field talk about new and ongoing developments in integrated circuits. **Click here to access.**
- **Webinars:** Monthly webinars are held for free for SSCS members on topics ranging from Analog/RF and future microprocessors to new biomedical applications. **Register for an upcoming webinar** or **view past webinars**
- **eBooks:** SSCS has two books available for download - **IC Design Insights** - a selection of tutorial and invited presentations given at CICC 2017 and **Low Power Circuit Design Using Advanced CMOS Technology** - part of the Tutorials in Circuits and Systems series.
- **CONFedu Series:** The CONFedu series features short 10-minute talks from SSCS sponsored conferences including ISSCC, CICC, ESSCIRC, and VLSI. **Click here to access.**
- **SSCSx Lecture Series:** The first series of lectures is five parts and is presented by Prof. Behzad Razavi on Noise. **Click here to access.**

Educational credits (PDH's and CEU's) are available at a low cost for select products.

SSCS Educational content can be accessed via the SSCS Resource Center and the SSCS YouTube Channel. The material is free for Society members.

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EDUCATION

Upcoming December 2020 Distinguished Lectures

SSCS Austria	**Deployment of EMC-Compliant IC Chip Techniques in Design for Hardware Security - Presented by Makoto Nagata**	**December 4th - VIRTUAL - Click here for more information**
SSCS Oregon State University Student Branch Chapter	**Talk Title TBD - Presented by Kaushik Sengupta**	**December 4th - VIRTUAL - Click here for more information**
SSCS IIT Guwahati Student Branch	**Multi-port mm-Wave Transceivers and Antenna Interfaces: Towards Programmable mm-Wave Front-ends - Presented by Kaushik Sengupta**	**December 8th - VIRTUAL - Click here for more information**
SSCS Oregon State University Student Branch Chapter	**Adaptive and Resilient Circuits for Processors - Presented by Keith Bowman**	**December 14th - VIRTUAL - Click here for more information**
SSCS Poland Chapter	**High Resolution Radar Imaging for Breast Cancer Detection: Trends and Challenges - Presented by Prof. Andrea Bevilacqua**	**December 16th - VIRTUAL- Click here for more information**
SSCS Poland Chapter	**Mixed-signal technologies for ultra-wide band signal processing systems - Presented by Gabriele Manganaro**	**December 16th - VIRTUAL- Click here for more information**

CONFERENCES

Upcoming 2021 SSCS-Sponsored Conferences

Below is the most up-to-date information as of press time on SSCS-sponsored conferences. However, things are changing daily due to the COVID-19 pandemic. For the most up-to-date information on these conferences, please visit each conferences website.

2021 IEEE International Solid-State Circuits	**Feb 13 - 22, 2021**

Conference (ISSCC) Virtual	
2021 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA) Hsinchu, Taiwan	**Apr 19 - 22, 2021**
2021 International Symposium on VLSI Design, Automation and Test (VLSI-DAT) Hsinchu, Taiwan	**Apr 19 - 22, 2021**
2021 IEEE Custom Integrated Circuits Conference (CICC) Virtual	**Apr 25 - 28, 2021**
2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Atlanta, GA USA & VIRTUAL	**Jun 6 - 8, 2021**
2021 Symposia on VLSI Technology and Circuits Kyoto, Japan	**Jun 14 - 17, 2021**

Call for Papers - 2021 Symposia on VLSI Technology and Circuits

June 14 - 17, 2021
Kyoto, Japan

Paper Submission Deadline: 23:59 JST Monday, February 8, 2021

The VLSI Technology symposium calls for papers in the following areas:

* Technologies for IOT including ultra-low power technologies; wearable devices/sensors, display, connectivity, power management; micro-controllers and application processors.

* Technologies for AI including CPU, GPU, in-memory computing, neuromorphic devices, and stochastic computing.

* Stand-Alone and Embedded Memories technology and reliability for SRAM, DRAM, 3D NAND and NOR Flash, MRAM, PCRAM, ReRAM, FeRAM and other new memories.

* CMOS Technology, Microprocessors and SoCs including scaling, VLSI manufacturing concepts, and yield optimization.

* RF / Analog / Digital Technologies and Sensors for mixed-signal SoC; RF front-end; analog, mixed-signal, I/O, high-voltage, MEMS, integrated sensors; power electronics.

* Process and Material Technologies including advanced transistor, modeling and reliability; high mobility channels; wide bandgap semiconductors and 2D devices; lithography; heterogeneous integration; interconnects scaling.

* Packaging Technologies and System-in-Package (SiP) including through-silicon-vias (TSVs) and 3D-system integration.

* Photonics Technology and Imaging Technology

* Beyond CMOS Devices, including Quantum Computing and Cryo-CMOS Technology

The Symposium on VLSI Circuits calls for papers in the following areas:

- Processors, SoCs, quantum computing, and machine learning
- Digital circuits, signal integrity, and IOs
- Hardware security
- Memory circuits, architectures, and interfaces
- Biomedical circuits and systems
- Sensors, imagers, and display circuits
- Power conversion circuits
- Analog building blocks
- Wireless receivers and transmitters
- Data converters
- Frequency generation and clock circuits
- Wireline and optical transceiver

Prospective authors must submit two-page papers and abstracts using the Symposia's website, www.vlsisymposium.org

SSCS-Sponsored Conferences: Proceedings

Click the links below to access the latest SSCS-Sponsored conference proceedings.

2019

[2019 IEEE International Solid-State Circuits Conference (ISSCC)]
[2019 IEEE Custom Integrated Circuits Conference (CICC)]
[2019 IEEE Symposium on VLSI Circuits]
[2019 IEEE 45th European Solid-State Circuits Conference (ESSCIRC)]
[2019 IEEE Asian Solid-State Circuits Conference (A-SSCC)]

2020

[2020 IEEE International Solid-State Circuits Conference (ISSCC)]
[2020 IEEE Custom Integrated Circuits Conference (CICC)]
[2020 IEEE Symposium on VLSI Circuits]

PUBLICATIONS

The latest in SSCS Flagship Publications...

IEEE Journal of Solid-State Circuits

Vol. 55, Issue 12, December 2020

[Special Issue on the 2020 IEEE International Solid-State Circuits Conference (ISSCC)]

A 4-GS/s 80-dB DR Current-Domain Analog Frontend for Phase-Coded Pulse-Compression Direct Time-of-Flight Automotive Lidar
Mahdi Kashmiri; Behnam Behroozpour; Vladimir P. Petkov; Kenneth E. Wojciechowski; Christoph Lang

A 28-W, −102.2-dB THD+N Class-D Amplifier Using a Hybrid ΔΣM-PWM Scheme
Shoubhik Karmakar; Huajun Zhang; Robert van Veldhoven; Lucien J. Breems; Marco Berkhout; Qinwen Fan; Kofi A. A. Makinwa

A Variable-Gain Low-Noise Transimpedance Amplifier for Miniature Ultrasound Probes
Eunchul Kang; Mingliang Tan; Jae-Sung An; Zu-Yao Chang; Philippe Vince; Nicolas Sénégond; Tony Mateo; Cyril Meynier; Michiel A. P. Pertijs

A Monolithic GaN-IC With Integrated Control Loop for 400-V Offline Buck Operation Achieving 95.6% Peak Efficiency
Maik Kaufmann; Bernhard Wicht

A Monolithic Resonant Switched-Capacitor Voltage Regulator With Dual-Phase Merged-LC Resonator
Prescott H. McLaughlin; Ziyu Xia; Jason T. Stauth

Highly Integrated ZVS Flyback Converter ICs With Pulse Transformer to Optimize USB Power Delivery for Fast-Charging Mobile Devices
Wei-Hsu Chang; Yen-Ming Chen; Ching-Jan Chen; Pin-Ying Wang; Kun-Yu Lin; Chun-Ching Lee; Li-Di Lo; Jenn-Yu G. Lin; Ta-Yung Yang

A Resonant Current-Mode Wireless Power and Data Receiver for Loosely Coupled Implantable Devices
Sung-Wan Hong

A 12-b 18-GS/s RF Sampling ADC With an Integrated Wideband Track-and-Hold Amplifier and Background Calibration
Ahmed M. A. Ali; Huseyin Dinc; Paritosh Bhoraskar; Scott Bardsley; Chris Dillon; Matthew McShea; Joel Prabhakar Periathambi; Scott Puckett

An 8-Bit 10-GS/s 16Ã- Interpolation-Based Time-Domain ADC With <1.5-ps Uncalibrated Quantization Steps
Minglei Zhang; Yan Zhu; Chi-Hang Chan; Rui P. Martins

A Cascaded Noise-Shaping SAR Architecture for Robust Order Extension
Lu Jie; Boyi Zheng; Hsiang-Wen Chen; Michael P. Flynn

A 13.5-ENOB, 107-Î¼W Noise-Shaping SAR ADC With PVT-Robust Closed-Loop Dynamic Amplifier
Xiyuan Tang; Xiangxing Yang; Wenda Zhao; Chen-Kai Hsu; Jiaxin Liu; Linxiao Shen; Abhishek Mukherjee; Wei Shi; Shaolan Li; David Z. Pan; Nan Sun

A 13-bit 0.005-mm2 40-MS/s SAR ADC With kT/C Noise Cancellation
Jiaxin Liu; Xiyuan Tang; Wenda Zhao; Linxiao Shen; Nan Sun

A Calibration-Free 14-b 0.7-mW 100-MS/s Pipelined-SAR ADC Using a Weighted-Averaging Correlated Level Shifting Technique
Jia-Ching Wang; Tsung-Chih Hung; Tai-Haur Kuo

A 64-Pixel 0.42-THz Source SoC With Spatial Modulation Diversity for Computational Imaging
Ritesh Jain; Philipp Hillger; Eamal Ashna; Janusz Grzyb; Ullrich R. Pfeiffer

A 12-mW 10-GHz FMCW PLL Based on an Integrating DAC With 28-kHz RMS-Frequency-Error for 23-MHz/Î¼s Slope and 1.2-GHz Chirp-Bandwidth
Pratap Tumkur Renukaswamy; Nereo Markulic; Piet Wambacq; Jan Craninckx

Multi-Watt, 1-GHz CMOS Circulator Based on Switched-Capacitor Clock Boosting
Aravind Nagulu; Tingjun Chen; Gil Zussman; Harish Krishnaswamy

A Multimode Multi-Efficiency-Peak Digital Power Amplifier
Si-Wook Yoo; Shih-Chang Hung; Sang-Min Yoo

A Reconfigurable Hybrid Series/Parallel Doherty Power Amplifier With Antenna VSWR Resilient Performance for MIMO Arrays
Naga Sasikanth Mannem; Min-Yu Huang; Tzu-Yuan Huang; Hua Wang

A 66-fs-rms Jitter 12.8-to-15.2-GHz Fractional-N Bang-Bang PLL With Digital Frequency-Error Recovery for Fast Locking
Alessio Santiccioli; Mario Mercandelli; Luca Bertulessi; Angelo Parisi; Dmytro Cherniak; Andrea L. Lacaita; Carlo Samori; Salvatore Levantino

Multi-Feed Antenna and Electronics Co-Design: An E-Band Antenna-LNA Front End With On-Antenna Noise-Canceling and Gm-Boosting
Sensen Li; Taiyun Chi; Hua Wang

A 0.5-V BLE Transceiver With a 1.9-mW RX Achieving -96.4-dBm Sensitivity and -27dBm Tolerance for Intermodulation From Interferers at 6- and 12-MHz Offsets
Masahisa Tamura; Hideyuki Takano; Hironori Nakahara; Hiroaki Fujita; Naoya Arisaka; Satoru Shinke; Norihito Suzuki; Yutaka Nakada; Yusuke Shinohe; Shinichirou Etou; Tetsuya Fujiwara; Fumitaka Kondo; Ken Yamamoto; Tomohiro Matsumoto; Yasushi Katayama

A Multiband FDD SAW-Less Transmitter for 5G-NR Featuring a BW-Extended N-Path Filter-Modulator, a Switched-BB Input, and a Wideband TIA-Based PA Driver
Gengzhen Qi; Haijun Shao; Pui-In Mak; Jun Yin; Rui P. Martins

NB-IoT and GNSS All-In-One System-On-Chip Integrating RF Transceiver, 23-dBm CMOS Power Amplifier, Power Management Unit, and Clock Management System for Low Cost Solution
Jongsoo Lee; Jaeyeol Han; Chi-Lun Lo; Jongmi Lee; Wan Kim; Seungjin Kim; Byoungjoong Kang; Juyoung Han; Sangdon Jung; Takahiro Nomiyama; Jongwoo Lee; Thomas Byunghak Cho; Inyup Kang

A Fully Integrated 27-dBm Dual-Band All-Digital Polar Transmitter Supporting 160 MHz for Wi-Fi 6 Applications
Assaf Ben-Bassat; Shahar Gross; Aaron Lane; Anna Nazimov; Bassam Khamaisi; Elad Solomon; Elan Banin; Eli Borokhovich; Nahum Kimiagorov; Nati Dinur; Phillip Skliar; Roi Cohen; Rotem Banin; Sarit Zur; Sebastian Reinhold; Smadar Breuer-Bruker; Tomer Abuhazira; Tom Livneh; Tzvi Maimon; Uri Parker; Ashoke Ravi; Ofir Degani

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IEEE Solid-State Circuits Letters

Early Access Articles

20-GS/s 8b Analog-to-Digital Converter and 5-GHz Phase Interpolator for Open-Source Synthesizable High-Speed Link Applications
Sung-Jin Kim; Zachary Myers; Steven Herbst; Byong Chan Lim; Mark Horowitz

A 3.2-to-3.8 GHz Harmonic-Mixer-Based Dual-Feedback Fractional-N PLL Achieving -65 dBc In-Band Fractional Spur
Masaru Osada; Zule Xu; Tetsuya Iizuka

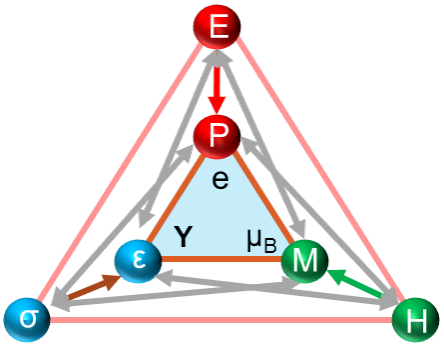
300-GHz 2nd-Order Sub-Harmonic Up-Conversion Mixer Using Symmetric MOS Varactors in 65-nm CMOS
Zhiyu Chen; Wooyeol Choi; K. O. Kenneth

Energy-Efficient Three-Stage Amplifier Achieving a High Unity-Gain Bandwidth for Large Capacitive Loads without Using a Compensation Zero
Hongseok Shin; Jinuk Kim; Doojin Jang; Donghee Cho; Yoontae Jung; Hyungjoo Cho; Unbong Lee; Chul Kim; Sohmyung Ha; Minkyu Je

A thermalized bias circuit for wider operating temperature range in bolometric infrared

imagers Patrick Robert; Christophe Curis; Vincent Gravot
A Fast Locking 5.8 -7.2 GHz Fractional-N Synthesizer with Sub-2 us Settling in 22 nm FDSOI Jeffrey Prinzie; Shuja Andrabi; Christophe Beghein; Changhua Cao; Hsin Hua Chen; Xiaochuan Guo; Jon Strange; Bernard Tenbroek
A Compact Fully Dynamic Capacitance-to-Digital Converter with Energy-Efficient Charge Reuse Haoming Xin; Kevin Pelzers; Peter Baltus; Eugenio Cantatore; Pieter Harpe
Synthesis and Design of Enhanced N-Path Filters with 60dB/decade RF Selectivity Sashank Krishnamurthy; Ali M. Niknejad
A Dual-Rail Hybrid Analog/Digital Low Dropout Regulator with Dynamic Current Steering for a Tunable High PSRR and High Efficiency Xiaosen Liu; Harish K. Krishnamurthy; Claudia Barrera; Jing Han; Rajasekhara M. Narayana Bhatla; Scott Chiu; Zakir K. Ahmed; Nachiket Desai; Krishnan Ravichandran; James W. Tschanz; Vivek De

IEEE Journal on Exploratory Solid-State Computational Devices and Circuits



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Hybrid-Phase-Transition FET Devices for Logic Computation Manuel Jiménez ; Juan Núñez ; María José Avedillo
Benchmarking and Optimization of Spintronic Memory Arrays Yu-Ching Liao ; Chenyun Pan ; Azad Naeemi

Early Access Articles

Implementation of Boolean Functions using Tunnel Field-Effect Transistors S. Garg; S. Saurabh
Digital Logic and Asynchronous Datapath with Heterogeneous TFET-MOSFET Structure for Ultralow-Energy Electronics Jo-Han Hung; Pei-Yu Wang; Yu-Chen Lo; Chih-Wen Yang; Bing-Yue Tsui; Chia-Hsiang Yang
Energy Efficient Ferroelectric Field Effect Transistor based Oscillators for Neuromorphic System Design Hossein Eslahi; Tara J. Hamilton; Sourabh Khandelwal
Experimental Demonstration of a Reconfigurable Coupled Oscillator Platform to Solve the Max-Cut Problem Mohammad Khairul Bashar; Antik Mallick; Daniel S Truesdell; Benton H. Calhoun; Siddharth Joshi; Nikhil Shukla
Minimum-Energy Digital Computing with Steep Subthreshold Swing Tunnel FETs Daniel S. Truesdell; Sheikh Z. Ahmed; Avik W. Ghosh; Benton H. Calhoun
Temporal Memory with Magnetic Racetracks Hamed Vakili; Mohammad Nazmus Sakib; Samiran Ganguly; Mircea Stan; Matthew W. Daniels; Advait Madhavan; Mark D. Stiles; Avik W. Ghosh

JxCDC papers listed in order of popularity can be found online HERE.

For paper submission details, click HERE.

For Society news and happenings, check out the Fall 2020 issue of the IEEE Solid-State Circuits Magazine.

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