PUBLIC

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of **RAMBUS INC.,** **a corporation.**	**Docket No. 9302**

RAMBUS INC.'S RESPONSES TO COMPLAINT COUNSEL'S PROPOSED FINDINGS OF FACT

VOLUME I

Introductory Statement

Respondent Rambus Inc. ("Rambus") will file stipulated witness and exhibit indices conforming to the requirements of Rules 3.46(b) and (c) concurrently with the filing of these Responses to Complaint Counsel's Proposed Findings of Fact.

Rambus's Responses to Complaint Counsel's Proposed Findings of Fact use the following forms of citation:

- Cross-references to particular responses in Respondent Rambus's Response to Complaint Counsel's Proposed Findings of Fact are designated by "RRFF" followed by the particular response number.
- Citations to Complaint Counsel's Proposed Findings of Fact are designated by "CCFF" followed by the particular finding number.
- Citations to Respondent Rambus's Proposed Findings of Fact (filed September 5, 2003) are designated "RPF" followed by the particular finding number.
- Citations to trial testimony, trial exhibits, deposition designations and *in camera* materials are in the form set forth by the Court's Order On Post Trial Briefs (July 10, 2003).

The parties have submitted certain designated deposition and trial testimony. (The Parties' Designated Deposition Testimony (Second Corrected Version) (filed August 25, 2003)). For some of these designations, the parties have submitted evidentiary objections. (*Id.*). As of the filing of these Responses, the Court has not yet ruled on the objections. Because Rambus believes that they are relevant and admissible, Rambus has cited to certain portions of the designated testimony in its Proposed Findings and in these Responses. In the event that these

portions of designated testimony are not admitted, Rambus requests that the citations be disregarded.

I. The DRAM Industry.

A. What is a DRAM?

10. DRAM stands for "Dynamic Random Access Memory." (Rhoden, Tr. 266-67). DRAM is a type of electronic memory. (Rhoden, Tr. 266). DRAM is "dynamic" because it needs to be refreshed every fraction of a second. (Rhoden, Tr.266-267 ("dynamic is something that is a temporary storage.")).

Rambus's Response to Finding No. 10:

Rambus has no specific response.

11. The primary use for DRAM is in computer systems. (Rhoden, Tr. 267 ("Probably the largest percentage of DRAM winds up in computer systems."); Gross, Tr. 2272-2273 (About 95% of Hewlett Packard purchases of memory are used in computers, including servers, the remaining 5% are used in printers, cameras and camera accessories).

Rambus's Response to Finding No. 11:

Rambus has no specific response.

12. DRAMs are also used in a wide range of other products. (Sussman, Tr. 1362 ("Q. What applications or end products would use these DRAMs? A. Basically everything that needed to temporarily store data, a very wide range of products. It could be from today's MP3 music to the supercomputer that NASA would have."). These products include servers (Kellogg, Tr. 4993; Tabrizi, Tr. 9126-9127;) , workstations (G. Kelley, Tr. 2376-2377; Krashinsky, Tr. 2770-2771; Farmwald, Tr. 8206-8207; Tabrizi, Tr. 9126-9127), printers (Kellogg, Tr. 4986-4987; Krashinsky, Tr. 2770-2771; Gross, Tr. 2272-2273), PDA's (Krashinsky, Tr. 2770-2771) and cameras (Gross, Tr. 2272-2273).

Rambus's Response to Finding No. 12:

The proposed finding is misleading to the extent that it suggests that servers and workstations are not parts of "computer systems." Rambus agrees that DRAMs are used in a wide range of products.

13. In a computer system, DRAM is the area where transactions and information is stored and processed, stored and retrieved while the computer is in operation. (Rhoden, Tr. 267-68).

Rambus's Response to Finding No. 13:

The proposed finding is misleading. After the testimony cited, Mr. Rhoden explained that processing of information actually takes place outside the DRAMs in the central processing unit (CPU), while the DRAM is used for temporary storage of information. (Rhoden, Tr. 271-72). Other processors can also be involved in information processing. (RRFF 15).

14. Typically, multiple DRAM chips are placed on a memory module, which is a small printed circuit board (Rhoden, Tr. 272-73; *see, e.g.,* DX0001). The module containing the DRAM chips connects to a motherboard. (Rhoden, Tr. 269, 273).

Rambus's Response to Finding No. 14:

The proposed finding is incomplete. In some applications, such as graphics cards, the DRAM chips are not put in memory modules. (Wagner, Tr. 3871-72).

15. The central processing unit ("CPU" or "microprocessor") is the "brains" of the computer. The CPU processes and makes decisions based on the information that it receives from memory devices, including the DRAM chips. (Rhoden, Tr. 271-72). The CPU is located on the motherboard. (Rhoden, Tr. 275-76; *see, e.g.,* DX0003).

Rambus's Response to Finding No. 15:

In order for this finding to be technologically accurate, the proposed finding should say the CPU is the "central brain" of the computer as Rhoden stated in the cited testimony. (Jacob, Tr. 5566 (graphics card can have a graphics coprocessor on it).

16. A chipset or controller is a group of computer chips that connect the various components of the motherboard, including the DRAMs and the central processing unit. (Rhoden, Tr. 275 (chipset "defines a grouping of chips that actually are the traffic cops for the motherboard. They connect . . . the memory, the CPU, all of the different I/O devices.")). The chipset communicates with the DRAM by sending signals for the clock, control, address, and data commands that travel along buses between the chipset and the DRAM. (Rhoden, Tr. 277-

79).

Rambus's Response to Finding No. 16:

The proposed finding is misleading to the extent that it suggests that all computers contain controllers. In some computers, the CPU communicates directly with the DRAMs. (Lee, Tr. 6727). Also, to be technologically accurate, the second sentence of the proposed finding should state that the signals travel along "one or more busses," since some systems can have the control, address, and data all travel along one bus. (Jacob, Tr. 5464).

17. A DRAM is made up of a number of cells. (Rhoden, Tr. 359). Information is stored in the cell capacitor as a either a high or low voltage. (Rhoden, Tr. 359). The cells of the DRAM are divided into an array via a series of rows and columns with the cells located at the intersections of those rows and columns. (Rhoden, Tr. 359-60). Access to the cell capacitor is made by activating a transistor, which transfers the voltage in the capacitor to a column or bit line. (Rhoden, Tr. 359-60).

Rambus's Response to Finding No. 17:

Rambus has no specific response.

18. In the early 1990s, the typical DRAM contained 16 million cells, or 16 "megabits". (Rhoden, Tr. 360-61).

Rambus's Response to Finding No. 18:

The proposed finding is overbroad and irrelevant. While there were DRAMs that contained 16 million cells in the early 1990s, the evidence does not support a finding that this was "*the* typical DRAM" for the whole period. For example, Rambus's first RDRAM in 1992 had 4 ½ million cells. (Horowitz, Tr. 8548-49; *see also* CX0027A at 2 (JEDEC meeting minutes showings work on 4M and 16M DRAMs)).

19. The row address strobe ("RAS") accompanies the row address information, which supplies the information necessary to identify the row within the DRAM that is required to respond to a particular request from the controller. (Rhoden, Tr. 365).

Rambus's Response to Finding No. 19:

The proposed finding is overbroad and not supported by the cited evidence. The RAS signal operates differently in asynchronous memory and synchronous memory. To be technologically accurate for asynchronous memory, the proposed finding should not state that RAS "accompanies" the row address; rather RAS instructs the memory device to capture the row address, which is typically driven earlier. (Rhoden, Tr. 368). In SDRAMs, there is a signal identified as "RAS," but it will serve to instruct the memory device to capture the row address only in conjunction with other control signals and the clock. (Rhoden, Tr. 374-75).

20. The column address strobe ("CAS") accompanies the column address information, which supplies the information necessary to identify the column within the DRAM that is required to respond to a particular request from the controller. (Rhoden, Tr. 368).

Rambus's Response to Finding No. 20:

The proposed finding is overbroad and not supported by the evidence. The CAS signal operates differently in asynchronous memory and synchronous memory. To be technologically accurate for asynchronous memory, the proposed finding should not state that CAS "accompanies" the column address; rather CAS instructs the memory device to capture the column address, which is typically driven earlier. (Rhoden, Tr. 368). In SDRAMs, there is a signal identified as "CAS," but it will serve to instruct the memory device to capture the column address only in conjunction with other control signals and the clock. (Rhoden, Tr. 374-75).

21. Information is sent to or from the DRAM cells in response to requests made by the chipset. The chipset provides row and column addresses that determine where the information can be found or should be stored. (Rhoden, Tr. 361-63). A sense amplifier senses whether the voltage in the cell capacitor is low or high. The sense amplifier, in turn, is connected to the data output "bus" lines. (Rhoden, Tr. 366).

Rambus's Response to Finding No. 21:

The proposed finding is incomplete, inaccurate and not supported by the cited testimony. The proposed finding assumes that the computer contains a chipset, which is not always the case. (RRFF 16). In addition, the testimony of Mr. Rhoden cited by Complaint Counsel does not suggest that the sense amplifier is connected to the data output lines, but rather that the "sense amplifier has been enabled to connect that sense amplifier to the data output lines of the device." (Rhoden, Tr. 366). In fact, as this testimony reflects, there is a great deal of circuitry between the sense amplifiers and any output driver.

22. There are different types of DRAM, including asynchronous and synchronous. The term "asynchronous" refers to a DRAM device that operates without reference to a free running clock. Instead, the controller sends instructions to the memory and waits for a response for a period of time that is not synchronized. (Rhoden, Tr. 368; Jacob, Tr. 5394)

Rambus's Response to Finding No. 22:

The proposed finding is inaccurate, not supported by the evidence and, indeed, conflicts with another of Complaint Counsel's proposed findings. An asynchronous DRAM is one in which control signals, including RAS and CAS, rather than a clock instruct the DRAM when to perform a read or write operation. (*See* CCFF 500 ("'Asynchronous DRAM' is a term that is used to describe DRAMs that are driven off the RAS and CAS signals where the RAS and CAS actually control the operation of the DRAM rather than a clock. (Jacob, Tr. 5394)"). Thus, a controller or CPU sends instructions to an "asynchronous DRAM" and waits for a response for an uncertain amount of time. (Horowitz, Tr. 8501). The characterization of the period of time in the proposed finding as "not synchronized" is vague.

23. The term "synchronous" refers to a DRAM device that is synchronous with a free running clock. (Rhoden, Tr. 370-372; Sussman, Tr. 1359).

Rambus's Response to Finding No. 23:

The proposed finding is incorrect and not supported by the cited evidence. The testimony cited by Complaint Counsel does not state that a synchronous DRAM device must be "*synchronous with* a free running clock." (Rhoden, Tr. 370-72 ("apply a continuous free running clock into a device"), Sussman, Tr. 1359 ("synchronous in that we're also making use of the system clock."). A "synchronous DRAM" is one that is not asynchronous; that is, one in which the DRAM receives control signals (often, but not always including signals designated as RAS and CAS) along with a system clock that instructs the DRAM when to perform a read or write operation. (RRFF 22; CCFF 500).

24. A free running clock operates continuously in contrast to other clock-type signals that only operate intermittently. (Rhoden, Tr. 368).

Rambus's Response to Finding No. 24:

The proposed finding is misleading and not supported by the weight of the evidence. The testimony of Mr. Rhoden cited by Complaint Counsel contrasts RAS and CAS signals, which are not "continuous and free running" clocks with clocks that are free running and operate in a "periodic fashion." (Rhoden, Tr. 368). RAS and CAS signals are not properly termed clocks, but rather strobe signals. (Fliesler, Tr. 8858, 8861; Macri, Tr. 4634 ("A clock is a free-running signal that forms kind of the watch of the system, whereas strobe can be loosely related to the clock, may or may not be free running . . . .")).

B. DRAMs Must be Compatible and Interoperable with Other Components.

25. DRAM chips are not sold individually to consumers. Instead, they are included in other products that are then sold to consumers. Examples of products that incorporate DRAM include personal computers, memory modules, graphics cards, printers, servers, and telecommunications switches. The customers for the DRAM manufacturers are those firms that

include DRAMs in their products. (Rhoden, Tr. 298; McAfee, Tr. 7183, *see also* DX0132). For example, SDRAM is used by HP in its printers, servers, and in some of its notebook computers. (Gross, Tr. 2275). DDR SDRAM is approximately 80% of the DRAM that HP buys, and it is used in desktop computers, notebook computers and servers. (Gross, Tr. 2274-76)

Rambus's Response to Finding No. 25:

The proposed finding is inaccurate and not supported by the evidence cited by Complaint Counsel. The cited testimony of Mr. Rhoden and Professor McAfee lists the customers as indicated, but not in a manner that excludes the existence of other customers – *i.e.* not in a manner that precludes the fact that DRAM chips are sold individually to consumers (which does occur).

26. A DRAM alone is not useful; it needs to communicate with many other components in the computer. (Macri, Tr. 4589 ("It needs to talk to other things, and there's a vast array of, you know, system types, from like a personal computer to a digital television, they all use the DRAM a bit differently."); Peisl, Tr. 4402-03 ("Memory is interfacing with a number of components on the motherboard . . . [including] the controller. . . modules . . . BIOS")).

Rambus's Response to Finding No. 26:

The proposed finding mischaracterizes the testimony. The cited testimony of Mr. Macri does not quantify the degree to which the DRAM must interoperate with other parts in the computer as Complaint Counsel's use of the word "many" would suggest. Mr. Macri stated: "DRAM alone doesn't really do anything. It needs to talk to other things…." (Macri, Tr. 4589). The proposed finding also references the testimony of Mr. Macri in a misleading way, suggesting that the "vast array" somehow describes the number of components in the computer with which the DRAM must communicate. Instead, the testimony "vast array of, you know, system types" is clearly not a reference to other components in the same computer, but to the fact that the vastly different types of computers use the DRAM differently, which is not relevant to this proposed

finding.

Likewise, the cited testimony of Mr. Peisl says only, without quantification, that the memory is "interfacing with a number of components on the motherboard." (Peisl, Tr. 4403). Peisl qualifies his use of the word "interfacing," such that some interfaces are "direct" – the kind that are the subject of this proposed finding – while other are indirect (Peisl, Tr. 4402-03), yet Complaint Counsel cite all of them.

27. In order for DRAM to have any value, it must be compatible with the other components in the products that include the DRAM. (Peisl, Tr. 4410 ("Interoperability between that the DRAM works flawlessly together with all the components in the system. It's not only one chip that the DRAM is interfacing with but all the other components on the motherboard, the position on the motherboard, the particular layout on the motherboard, other components on the modules, for instance, like registers. You have to make sure that your part is fully compliant with all the specifications of the other chips. This is why everybody is working towards the JEDEC specification. That's the common denominator."); CX1075 at 1 ("A phone or computer that is almost compatible is one that doesn't work. If people build parts 99% compatible, the systems companies won't buy them."); Heye, Tr. 3655-65, *see,* DX0030; Jacob, Tr. 5562-66, *see also* DX0105)).

Rambus's Response to Finding No. 27:

Respondent has no specific response except insofar as the proposed finding implies that there is some requirement of compatibility that extends beyond compatibility at an individual system level. The cited testimony supports the conclusion that a DRAM must be compatible with other parts in the same specific system, not that it must be compatible system to system (as, for example, a telephone or fax machine must be.) (Rapp, Tr. 9794).

28. It is important to DRAM customers such as PC-OEMs that the DRAM that they buy is interoperable with the other components of their systems. (Peisl, Tr. 4409 ("And the second issue is the interoperability. They of course wanted to make sure that our parts work together with all the other components in the system."); CCFF 27 and 114)

Rambus's Response to Finding No. 28:

The proposed finding is misleading and not supported by the cited testimony in that it changes the word "system" in Peisl's cited testimony to the word "systems"-- implying falsely that the interoperability requirements for DRAMs extend beyond the ability to interoperate with the other parts in the specific individual computer system into which that DRAM is installed. (*See* RRFF 27).

C. How DRAMs are Made.

1. Establishing a DRAM "Fab."

29. DRAMs are manufactured in plants commonly called "fabs." (Becker, Tr. 1101)

Rambus's Response to Finding No. 29:

Rambus has no specific response.

30. Billions of dollars are required to create factories and designs necessary to produce DRAMs (Rhoden, Tr. 297 ("there's a great deal of investment, billions of dollars, that go into the creation of factories and designs that are necessary to produce DRAM. . .") ; Shirley, Tr. 4161 ("when we bring a new production process to Micron, that's a very expensive process, the act of buying this new tooling for the production plant.")).

Rambus's Response to Finding No. 30:

The proposed finding is irrelevant and misleading. What is relevant is not the total dollar amount invested in buildings, machines and other capital equipment but rather the dollar amount of non-recoupable investments in plants, equipment and designs where such non-recoupable investments could only be used for manufacture of the specific DRAM types at issue here and where such investments were made before the DRAM manufacturers had actual or constructive notice of their potential infringement of actual or potential Rambus intellectual property. (Rapp, Tr. 10131-32, 9876-77).

The various proposed alternatives to Rambus's technology raised by Complaint Counsel, if they were to be implemented, could use the same fabs as current SDRAMs and DDR SDRAMs because they use the same process technology. The technology at issue here is not related to the memory array that makes up approximately 90% of a DRAM, but implicates only the "peripheral circuitry." (Geilhufe, Tr. 9559-60). The "vast majority" of development costs relate to the memory array. (Geilhufe, Tr. 9561). The costs of changes to the peripheral circuitry are much lower because they do not involve any changes to the manufacturing process. (*Id*.)

Moreover, as the 1992 Mitsubishi analysis of prospective patents that Rambus might obtain shows (along with significant other evidence of non-reliance outlined at RPF 466-702), the DRAM manufacturers were on notice of Rambus's intellectual property very early. The relevant amount of investment has not been established by Complaint Counsel but it is, in any event, either very small or zero.

31. The Infineon fab in Richmond, Virginia has so far cost approximately $1.5 billion. About $350 million of that amount was for the buildings and the building infrastructure, office furniture, computer systems and facilities systems. The balance, about $1.2 billion, was for the actual processing equipment used to manufacture the DRAM chips and modules. (Becker, Tr. 1108).

Rambus's Response to Finding No. 31:

The proposed finding is irrelevant and misleading. The cited investment amounts are relevant only to the extent that they could only be recouped by production of the specific types of DRAMs at issue in this case and where such investments were also made before the DRAM manufacturers had actual or constructive notice of their potential infringement of actual or potential Rambus intellectual property. (Rapp, Tr. 10131-32, 9876-77). The buildings and processing equipment cited can be used equally well to manufacture any of the proposed

alternatives to Rambus's technology raised by Complaint Counsel. (RRFF 30).

32. From groundbreaking to production of a qualified chip, it can take two years to build a new fab. (Becker, Tr. 1106-07).

Rambus's Response to Finding No. 32:

The factual assertion is irrelevant and misleading. What is relevant is not the time invested in building a fab but rather time invested where such investment can only be used for manufacture of the specific DRAM types at issue here and where such investment was also made before the DRAM manufacturers had actual or constructive notice of their potential infringement of actual or potential Rambus intellectual property. (Rapp, Tr. 10131-32, 9876-77). Here, the same fabs currently in use could also be used to manufacture any of the alternatives to Rambus's technology raised by Complaint Counsel. (RRFF 30).

33. Manufacturers generally require 20-25 identical mask sets to achieve full-ramp production of a DRAM. (Becker, Tr. 1123). A full mask set costs approximately $1 million. (Becker, Tr. 1122-23).

Rambus's Response to Finding No. 33:

The proposed finding is irrelevant misstates the cited evidence. The proposed finding would only be relevant to the extent that it separated out the cost of replacing only those masks that would be necessary to implement the alternatives raised by Complaint Counsel. For some of those alternatives, only a small number of masks would need to be replaced. Implementing the "fixed CAS latency" alternative, for example, would require changing only one mask. (Jacob, Tr. 5373-74; Geilhufe, Tr. 9576).

Moreover, the Becker testimony cited by Complaint Counsel addresses Infineon, not "manufacturers generally." Even as to Infineon, the proposed finding is a misstatement. The

cited testimony establishes that Infineon uses anywhere from 20 to 25 "masks in a mask set." It does not state that full production requires "20-25 identical mask sets."

34. Manufacturers frequently are forced to purchase multiple iterations of a mask set as defects are identified and redesigns occur. (Becker, Tr. 1150-51 ("Typically we'll do at least one all layer redesign, so we'll buy 22 layers, run those, we will find issues, and we will have to do a redesign of all 22 layers. We will order those 22 layers again with correction. And then typically we will have to. . . redesign maybe four or five of those layers two or three or four times after that to finetune the performance.")).

Rambus's Response to Finding No. 34:

The proposed finding is irrelevant because it is not related to costs of replacing only those particular masks necessary to implement the alternatives raised by Complaint Counsel. (RRFF 33). The proposed finding also misstates the cited evidence to the extent that it implies that more than two iterations of the entire mask set must be purchased. The quote indicates that only a few masks must be purchased more than twice.

2. The DRAM Manufacturing Process.

35. The starting point in the manufacturing process is a bare silicon wafer. (Becker, Tr. 1116-1117).

Rambus's Response to Finding No. 35:

Rambus has no specific response.

36. During the course of the manufacturing process, successive layers are built up on the silicon wafer. *(See generally* Becker, Tr. 1116-32 (describing the process on how a bare wafer becomes a processed layer containing hundreds of chips.)). DRAMs require as many as 22 distinct layers. (Becker, Tr. 1131). Each layer requires a series of manufacturing steps. (Becker, Tr. 1131-1132). Processing the wafer takes about 400 manufacturing steps. (Becker, Tr. 1131)

Rambus's Response to Finding No. 36:

Rambus has no specific response except to note that the cited Becker testimony is mischaracterized as stating that "a bare wafer becomes a processed layer containing hundreds of

chips." This is incorrect and not supported by the cited testimony. Instead, the cited Becker testimony states that the bare wafer becomes a processed wafer with many chips. There are many layers on a wafer. (Becker, Tr. 1131).

37. The manufacturing process is non-linear, meaning that a wafer will re-enter different processing area of the fab a number of times. (Becker, Tr. 1118).

Rambus's Response to Finding No. 37:

Rambus has no specific response.

38. A processed wafer contains hundreds of individual DRAM chips. (Becker, Tr. 1117).

Rambus's Response to Finding No. 38:

Rambus has no specific response.

39. The processed wafer is electrically tested in order to find the good chips. (Becker, Tr. 1132-1133)

Rambus's Response to Finding No. 39:

The proposed finding is misleading to the extent that it suggests that this electrical testing can accurately identify all of the die with disqualifying defects. Further, more stringent testing, is only possible after the die have been packaged. (Geilhufe, Tr.9570; CCFF 42).

40. After testing, the wafer is cut into individual DRAMs. (Becker, Tr. 1132-1134)

Rambus's Response to Finding No. 40:

Rambus has no specific response.

41. The individual chips are then bonded to a metal lattice like structure called a lead frame and are covered with a black hard plastic mold compound. (Becker, Tr. 1132-1134)

Rambus's Response to Finding No. 41:

Rambus has no specific response.

42. After packaging, the good chips are built into components and tested again. (Becker, Tr. 1132-1134).

Rambus's Response to Finding No. 42:

Rambus has no specific response.

43. The testing and packaging process takes approximately two weeks. (Becker, Tr. 1136).

Rambus's Response to Finding No. 43:

Rambus has no specific response.

44. The tested components may also be assembled onto circuit boards to create modules and are further tested. (Becker, Tr. 1135) This process takes approximately 1 ½ weeks. (Becker, Tr. 1136; *see generally* Becker, Tr. 1132-36 (describing the process on how the chips are built into components and connected to modules)).

Rambus's Response to Finding No. 44:

Rambus has no specific response.

45. The Infineon plant in Richmond produces approximately 3.5 million DRAM chips per week. (Becker, Tr. 1139).

Rambus's Response to Finding No. 45:

Rambus has no specific response.

3. Development of a New DRAM, From Specification to Full Production.

46. The development of the DRAM proceeds along a number of "phases" and milestones. Those are the design phase, the layout phase, the simulation phase, the verification phase, "tape out," initial silicon, the validation phase, internal qualification phase and the production phase. (Shirley, Tr. 4141-42; Reczek 4306-4341; *see* DX0044).

Rambus's Response to Finding No. 46:

Rambus has no specific response.

47. Concurrently with the development of the DRAM itself, industry participants dedicate substantial resources to ensuring that the future DRAM products will be available on the

same schedule as the other components that make up PCs, servers and workstations. (Gross, Tr. 2278 ("We frequently meet with the technical teams as well as the executive teams with each of our largest partners to exchange projections into the future of the types of technology that we're going to be needing in our computers, as well as the types of technologies and the mix in volumes that the suppliers plan to manufacture. And we endeavor to work toward a very close alignment of those technology roadmaps."); Peisl, Tr. 4447; Heye, Tr. 3636-3637; MacWilliams, Tr. 4799-4800).

Rambus's Response to Finding No. 47:

The proposed finding is not supported by the evidence insofar as none of the cited testimony attempts to quantify or qualify the resources ("substantial" or otherwise) dedicated to coordinating schedules.

48. In the design phase, the DRAM designers implement the DRAM specification as a set of circuit designs or schematics. (Shirley, Tr. 4142-43).

Rambus's Response to Finding No. 48:

Rambus has no specific response.

49. In the layout phase, the layout designers take the circuit designs created in the first step and create a representation of the circuit designs. (Shirley, Tr. 4143).

Rambus's Response to Finding No. 49:

Rambus has no specific response.

50. In the simulation phase, the design engineers simulate the designs in order to verify that the chips will perform as intended before they are first manufactured. (Shirley, Tr. 4144).

Rambus's Response to Finding No. 50:

Rambus has no specific response.

51. The verification phase involves ensuring that the schematics created in the design phase are in fact represented by the work done in the layout phase. (Shirley, Tr. 4144-45; Reczek, Tr. 4309).

Rambus's Response to Finding No. 51:

Rambus has no specific response.

52. Tape out involves the process of transferring the DRAM layout onto masks that will be used in the fabrication of the DRAM. (Shirley, Tr. 4145). The collection of individual masks necessary fabricate a DRAM design comprises a mask set. (Shirley, Tr. 4147).

Rambus's Response to Finding No. 52:

Rambus has no specific response.

53. A mask contains an image that is transferred to the wafer through a process of using light to expose the wafer to the image pattern in the mask and using gasses to etch the resulting pattern into the wafer. (Becker, Tr. 1122-24).

Rambus's Response to Finding No. 53:

Rambus has no specific response.

54. At some DRAM manufacturers, including Micron, the physical creation of masks is done by specialized firms that provide the service to the DRAM manufacturers. (Shirley, Tr. 4145-46). Other DRAM manufacturers, including Infineon, produce their own masks. (Reczek, Tr. 4312).

Rambus's Response to Finding No. 54:

Rambus has no specific response.

55. For a new design, it generally takes between 6 and 18 months from the beginning of the design phase for a DRAM to be taped out. (Shirley, Tr. 4149; Reczek, Tr. 4342-45; *see* DX0045).

Rambus's Response to Finding No. 55:

The proposed finding is not supported by the weight of the testimony. (*See* RRFF 59).

56. The mask set, once it is received, is used to create the first physical manifestation of the DRAM chips on wafers. Those wafers are referred to as "initial silicon." (Shirley, Tr. 4147).

Rambus's Response to Finding No. 56:

Respondent has no specific response except that (as the witness in the cited testimony

corrected Complaint Counsel), the term "initial silicon" does not refer to a specific part, but rather to a milestone – meaning a moment in time.

57. Initial silicon is then tested in the validation and internal qualification phases to ensure that the DRAM on the wafers operate the way they were intended (the validation phase) and that the DRAM on the wafers operate appropriately in the expected environments (the qualification phase). (Shirley, Tr. 4148-49).

Rambus's Response to Finding No. 57:

Respondent has no specific response beyond the clarification stated in RRFF 56.

58. It can take between 4 and 9 months for a DRAM design to proceed from tape-out through the internal qualification phase. The length of the period depends on the number and types of problems that are found during the test phases. (Shirley, Tr. 4149).

Rambus's Response to Finding No. 58:

The proposed finding is not supported by the cited testimony unless the phrase "internal qualification phase" (above) is the same as "product ready for production," and unless the phrase "test phases" (above) means "design and production processes."

59. Once internal qualification has been completed, it takes another 6 to 9 months to begin high volume production. (Shirley, Tr. 4150-51).

Rambus's Response to Finding No. 59:

The proposed finding is not supported by the weight of the testimony. Using the lower end of the ranges provided here and in CCFF 54 and 58 indicates that it will take at least 16 months to proceed from the beginning of the design phase of a DRAM to high volume production. However, where only changes to the peripheral circuitry, as opposed to the memory array, are involved, as would be the case with all of the alternatives raised by Complaint Counsel (*see* RRFF 30), much less time is required. For example, Dr. Oh of Hyundai testified that Hyundai was able to go from beginning of the design phase to mass manufacture of its first DDR

SDRAM in just eight months. (CX2108, Oh Depo., at 236-37).

60. Once the internal qualification is completed, "customer samples" of the new DRAM are sent to customers to allow them to test the DRAM. At the same time, additional mask sets are ordered to get ready for high volume production of the new DRAM. (Shirley, Tr. 4149-50).

Rambus's Response to Finding No. 60:

Rambus has no specific response.

61. Manufacturers must be in frequent contact with customers to provide technical support for the varied products of the customer in which the DRAMs will be installed. (Peisl, Tr. 4400-02). Manufacturers may send their own engineers to work in the facilities owned by the customers for the purpose of assisting in the validation of the customer samples. (Peisl, Tr. 4399).

Rambus's Response to Finding No. 61:

The proposed finding is not supported by the evidence. The Peisl testimony cited by Complaint Counsel does not suggest that manufacturers "must" be in frequent contact with customers to provide technical support." To the contrary, his testimony suggests the opposite, *i.e.* that "usually when [his company] send new parts to a customer . . . in most of the cases the parts didn't exhibit any failure. You just put them in . . . and start performing your tests . . . . [i]f there are failures for whatever reasons . . . then we were there to assist them to alleviate that failure or provide a work-around." (Peisl, Tr. 4400-02).

62. Manufacturers and customers must test the DRAM extensively. (Peisl, Tr. 4404 (test "all possible configurations, with all the controller chips that were available, all the major motherboard configurations . . . we couldn't predict where a weakness would occur, so we had to know all the different influences.")).

Rambus's Response to Finding No. 62:

The proposed finding is not supported by the evidence. The Peisl testimony cited by Complaint Counsel says nothing about customers testing the DRAM. It deals only with

manufacturer tests. (Peisl, Tr. 4404).

63. Once the DRAM is approved for purchase by the customer, DRAM manufacturers "ramp up" production of new DRAMs from low levels of production or no production. (Becker, Tr. 1144-45).

Rambus's Response to Finding No. 63:

The proposed finding is not supported by the cited evidence. To begin with the cited testimony refers only to the practices of Infineon, not the practices of "DRAM manufacturers." In addition, even as to Infineon the cited testimony is mischaracterized. The Becker testimony cited by Complaint Counsel states that a manufacturer would "ramp up" or ramp down "based on what the needs of the customer were." It does not state that such "ramp up" would follow an "approval for purchase" by a customer.

64. Ramping up a new DRAM at a DRAM fab requires a substantial amount of time. (Becker, Tr. 1158-60; Reczek, Tr. 4340-41 (it "takes somewhere in between four to six quarters, which is one to one and a half years, until you have fully converted all your production facilities to run the new -- the new part.")).

Rambus's Response to Finding No. 64:

The proposed finding is irrelevant because it relates to the time required to ramp up a new DRAM where new equipment and new processes are required. (Becker, Tr. 1158; Reczek, Tr. 4340). Implementing the alternatives to Rambus technology raised by Complaint Counsel would involve changes only to the peripheral circuitry, so new equipment or manufacturing processes would not be required. (RRFF 30).

65. From the time a manufacturer receives a completed specification, it can take more than two years to complete a new DRAM for production. (Peisl, Tr. 4373).

Rambus's Response to Finding No. 65:

The proposed finding is misleading. While it may be true that it "can" take that long, it

would not take nearly that long when only changes to the peripheral circuitry are involved. (*See* RRFF 59).

4. DRAM Design Modifications - Shrinks, Density Changes and Changes in Type.

66. There are three principal types of changes that are made by DRAM manufacturers: shrinks, changes in density, and changes in DRAM type. (Reczek, Tr. 4304; *see* DX0045).

Rambus's Response to Finding No. 66:

Respondent has no specific response other than to point out that the cited testimony deals only with the "types of changes" at Infineon and says nothing about "DRAM manufacturers."

67. A shrink involves taking an existing DRAM chip and re-designing it so that it can be used on a more advanced process that will allow the size of the chip to shrink. A shrink reduces costs by allowing more DRAMs to appear on each wafer, spreading the costs of producing that wafer over a larger number of chips. (Becker, Tr. 1155-57; *see,* DX0007 at 18 ("probably the biggest thing we do to influence or decrease our costs on a regular basis is we shrink the technology, and the reason that works so well is that we're able to produce the same part with the same function,... but we can produce it on a smaller chip.... So if you have a smaller chip, you can fit more of those chips on a wafer, your cost per chip is greatly reduced...")).

Rambus's Response to Finding No. 67:

Rambus has no specific response.

68. A shrink typically takes approximately 18 months. (Reczek, Tr. 4343; *see* DX0045).

Rambus's Response to Finding No. 68:

Respondent has no specific response other than to point out that the cited testimony deals only with the time requirements of a "shrink" at Infineon and says nothing about what is "typical" industry-wide.

69. Changes in density involve increasing the number of DRAM cells on a particular DRAM design, keeping the same interface elements. (Becker, Tr. 1141). DRAM manufacturers make different DRAM densities depending on the demand from DRAM customers. (*see,* Becker, Tr. 1153-54 ("[I]t was our belief or desire that the next density would be the 256-megabit

SDRAM, so we went from 64 – production of the 64 to developing the 256... but it turned out ... in reality, our customer base really wanted to purchase 128-megabit density. So, we then had to go back and do the work on the 128-megabit SDRAM density....")).

Rambus's Response to Finding No. 69:

The proposed finding is not supported by the cited evidence. The Becker testimony cited by Complaint Counsel does not suggest that density changes keep the same interface elements. Nor does the testimony suggest that changes in density involve increasing the number of DRAM cells on a particular DRAM design. The cited testimony states only "density describes how much memory capacity the – in this case the component has. So, the first one listed there is 128 megabit or it can store 128 million pieces or bits of memory." In addition, the cited testimony contradicts and does not support the proposed finding to the effect that manufacturers make different densities "depending on the customer demand." The cited evidence deals only with density choices by Infineon, not some standard industry-wide practice. It also establishes that, in one instance at least, Infineon followed its own "belief or desire" in deciding what density to make (256-megabit SDRAM) and then produced a different density (128-megabit SDRAM) after finding out what its customer base "really wanted."

70. A change in density can take two years or more, depending on the difficulty of the transition. (CX0415 at 5; Reczek, Tr. 4341-4346; *see also* DX0045).

Rambus's Response to Finding No. 70:

The proposed finding is not supported by the cited testimony, which deals only with Infineon. Even as to Infineon the proposed finding is incorrect. The Reczek testimony cited by Complaint Counsel states that it takes Infineon "up to 24 months, plus/minus little bit" (emphasis supplied). It does not state that "changes in density can take two years or more."

71. Changes to DRAM type involves making changes to the interface of the DRAM as well as making other changes required to accommodate changes in DRAM standards. (Reczek, Tr. 4304, 4310-11 ("So, for example, different types of DRAMs, the switch from an EDO part to a synchronous part or maybe from a synchronous part to a double data rate part, so this would refer to a change in type of the DRAM.")).

Rambus's Response to Finding No. 71:

The proposed finding is not supported by the cited evidence. The Reczek testimony cited by Complaint Counsel discusses neither "changes to the interface of the DRAM," nor "other changes required to accommodate changes in DRAM standards." Rambus also objects to this proposed finding because the term "Changes to DRAM type" is vague for the same reasons that the Court sustained Respondent's objection to the phrase " "changes in the type of DRAM" in the testimony cited by Complaint Counsel. *See* (Reczek, Tr. 4310).

72. A DRAM manufacturer's first step in manufacturing a new DRAM is to develop a DRAM specification. (Shirley, Tr. 4137; Peisl, Tr. 4373-4374). A DRAM specification is a set of functional and operational guidelines that describe what a DRAM should do under certain circumstances if it's given certain commands or if it's given certain parameters. (Shirley, Tr. 4137-38; Peisl, Tr. 4388-4389). These DRAM specifications are then used by the DRAM designers to design the DRAM. (Shirley, Tr. 4137).

Rambus's Response to Finding No. 72:

The proposed finding is not supported by the evidence. The cited evidence relates only to the practices of Micron and Infineon, not a generalized practice. Even as to Micron and Infineon the cited evidence does not support the proposed finding. The Shirley testimony cited by Complaint Counsel as support for the first sentence says nothing about the first step in the manufacturing process. The Peisl testimony discusses only redesigns of existing DRAMs -- not the design of a "new DRAM," let alone its manufacture.

73. Manufacturer's DRAM specifications are developed from JEDEC standards as well as from inputs from DRAM customers. (Shirley, Tr. 4138-40; Peisl, Tr. 4373-4374; Landgraf,

Tr. 1685; *see, e.g.*, CX2410 at 1 ("All inputs are compatible with the JEDEC Standard for SSTL_2")).

Rambus's Response to Finding No. 73:

The proposed finding is incomplete, misleading and irrelevant since it is written in the present tense. The Shirley testimony cited by Complaint Counsel merely states that Micron's marketing group develops "specifications based on several inputs, the foremost of which is … JEDEC…." (Shirley, Tr. 4138-40). The Peisl testimony cited by Complaint Counsel refers only to "redesigns" and states that "[t]he designers start with a specification, *usually* the JEDEC specification for a JEDEC-complaint part…." (Peisl, Tr. 4373-74 (emphasis added)). The Landgraf testimony cited by Complaint Counsel does not mention starting points in the development of DRAM specifications, but merely discuss labels placed on "lots of suppliers' data sheets…." Exhibit CX2410, an Infineon Preliminary Datasheet for 512 MBit DDR SDRAM, suggests only that the inputs to the auto refresh mode are compatible with JEDEC Standard for SSTL_2. It does not suggest that the outputs are JEDEC compatible, that anything other than the auto refresh mode is JEDEC compatible, and it does not suggest that Infineon started from the relevant JEDEC standard when it developed its own specification.

Additionally, the proposed finding – if it were to be read as applying to the past -- is contradicted by other evidence, which shows that companies began manufacturing SDRAM before JEDEC published its SDRAM standard in 1993. (*See, e.g.*, CX0688 at 1) (Tate email highlighting February 1993 EE Times Article: "Differences between Samsung, NEC and JEDEC standards." "NEC claims it is 'aligned' with JEDEC standards" "Comments that the JEDEC standard is an envelope and it will be like VRAMs where the concepts are the same but the

vendor's parts all differ in detail.")). Similarly, companies began manufacturing DDR SDRAMs before JEDEC published its first standard in August 1999. (CCFF 649-50; CX2108, Oh Depo. at 236-37 (Hyundai began manufacturing DDR SDRAMs in August 1998)). The evidence also suggests that companies began manufacturing DDRII before JEDEC published the standard sometime around May 2003. (Heye, Tr. 3865-66 ("I actually think there is a version of it that's been published now."); (Shirley, Tr. 4196) ("Q. And I believe you said [Micron] had a product that taped out – a DDR2 product that taped out in January 2002. Is that right? A. That is correct."); (Shirley, Tr. 4733-34) (Preliminary DDR2 specification, in which burst length was fixed at 4, was fixed in July 2001). Finally, the dominant types of memory devices for most of the late 1990s depended on the PC-66 SDRAM and PC-100 SDRAM standards as promulgated by Intel. (*See* RPF 1518-1522.)

74. The transition from one type of DRAM to another can take much longer than two years depending on how difficult the transition is. For example, when Infineon began its transition from SDRAM to DDR SDRAM, it had to go through three major redesigns before it was able to produce a device that showed acceptable customer performance. That required that Infineon had to repeat a number of steps to finally implement the design change. (Reczek, Tr. 4350-51; CX2107 (Oh, Dep.) at 55-56 (a change in DRAM type is a "very, very long procedure. It normally takes about three years."); Reczek, Tr. 4350-51 (transition from SDRAM to DDR SDRAM required three major redesigns).

Rambus's Response to Finding No. 74:

The proposed finding is vague, irrelevant and is not supported by the evidence. Dr. Oh testified that it can take three years from beginning a design to mass manufacture of a DRAM in a case where the process technology was changing. (CX2107, Oh Depo., at 147.) By contrast, if the same process technology was used then transitioning from one DRAM to another was "pretty simple." (*Id.*) Indeed, Hyundai was able to go quickly from beginning design work to mass

manufacture of its first DDR SDRAM part, because, like the various alternatives to Rambus technology raised by Complaint Counsel in this case, only the peripheral circuitry needed to be changed. (RRFF 30, 59).

The Reczek testimony cited by Complaint Counsel does not quantify the amount of time it takes Infineon to transition from one type of DRAM to another, nor does the testimony relate the length of time to the difficulty of the transition. Reczek did testify that it took "two years at least" to switch from fast page mode to EDO devices, and "this is valid for synchronous devices, and from my understanding and knowledge, also for other devices," (Reczek, Tr. 4336-37), which is not consistent with the language in the proposed finding "much longer than two years." Additionally, the evidence overwhelmingly demonstrates that the DRAM industry transitions between different versions of DRAM quite frequently. (*See* RPF 1267-1307).

The most revealing explanation of this issue can be found in the official "response script" that Micron prepared when Intel announced its decision to design its future generation of chipsets to accommodate Rambus DRAM devices, then called "nDRAM." As Micron explained, "switching from one product to another" is a relatively simple process where the same "core DRAM technology" is involved:

> "4. What would having to make 'nDRAM' or SyncLink mean to Micron?
>
> Keep in mind that ALL of these DRAM technologies use the same DRAM process, the same DRAM cell, and virtually the same DRAM array.
>
> . . .

> Switching from one product to another, while still using the same core technology, involves only changing priorities in design and product engineering and may mean some differences in our assembly and test equipment purchases. SDRAM, SLDRAM, nDRAM all use the same fab equipment and core DRAM technology. *In short, while the flavors might change, it's still a DRAM*."

(RX 836 at 3) (emphasis added).

75. A DRAM manufacturer normally does not attempt to do two different types of changes at the same time. (Reczek, Tr. 4305-4306). For example, when a DRAM manufacturer does a shrink, it does a shrink on a product that already exists so that there are fewer changes to track. (Becker, Tr. 1157-58 ("[F]or instance, when we went from .24 [micron] to .20 [micron], we did that with the same 64-meg SDRAM. So, we did all of our product learning at 0.24 [micron], we had to do all of our process and technology learning at 0.2 [micron], but we did it with a product we already knew."); CX2108 (Oh, Dep.) at 254 (when doing a shrink, "You don't change anything" on the inside of the DRAM, "It has nothing to do with the circuit. No circuit change at all."), 257 (Hyundai's practice was not to modify its design at the time it did a shrink)).

Rambus's Response to Finding No. 75:

The proposed finding is incomplete, vague in its use of the term "different types of changes" and misleading. It also is not supported by the cited testimony, which in any event, deals only with the practices of Hyundai and Infineon and not with what "a DRAM manufacturer" would "normally" do. Even as to Infineon and Hyundai the proposed finding is incorrect. The Becker testimony cited by Complaint Counsel does not discuss "fewer changes to track" as a reason for performing the shrink on products it is already producing, but states only that the reason is so that "you don't change too many things at once." The testimony of Dr. Oh relates to "shrinks" only and does not support the broader assertion that Hyundai – much less

DRAM manufacturers as a whole – would not attempt multiple changes at the same time. Moreover, Dr. Oh testified that a shrink may result in certain problems that *would* require other changes to the DRAM. (CX2108, Oh Depo. at 254 ("after you shrink it . . . then we check whether that dumb shrink cause any problems processing and, you know, the lines are too narrow, then there's a bridging and so on, those things we just change.").)

76. A DRAM manufacturer would not attempt to make a change to a DRAM type at the same time it was doing a shrink or a change in density because multiple changes makes it difficult to determine what is going wrong if the DRAM has a defect. (Reczek 4304-4305 ("So, in the case you take two steps at one time, so this might lead to very big problems, and for example, if something is not working, you don't know whether the technology is not working or the design is not working. So, its very difficult to figure out what's really going on, what's really going wrong there.")).

Rambus's Response to Finding No. 76:

The proposed finding is incomplete and misleading. The Reczek testimony cited by Complaint Counsel has no basis other than the practices of Infineon and, in any event, is misstated. The cited testimony was qualified by the witness as "[n]o, probably not," which is not the same as "A DRAM manufacturer would not attempt" to make multiple changes as indicated. (Reczek, Tr. 4305). Rambus also objects to this proposed finding because the term "DRAM type" is vague for the same reasons that the Court sustained Respondent's objection to the phrase "changes in the type of DRAM" in the testimony cited by Complaint Counsel in Proposed Finding No.71. (Reczek, Tr. 4310).

77. On occasion, manufacturers undertake a so-called "revision" design at the time of a shrink or a change in density. A revision design involves taking an existing design and changing certain circuitry in that design. A revision design usually occurs only when a DRAM manufacturer has found something fundamentally wrong with a DRAM design project that has already made it to silicon. (Shirley, Tr. 4168; CX2108 (Oh, Dep.) at 257 ("We normally don't [redesign some of the internal circuitry at the time of a shrink] unless . . . [the part] has a big

problem, if it does not work, then we do, but normally we don't do that.")).

Rambus's Response to Finding No. 77:

The proposed finding is not supported by the evidence. The Shirley testimony cited by Complaint Counsel does not in any way correlate in time the undertaking of a "revision design" with either a shrink or a change in density.

D. DRAM Industry Market Structure.

78. The DRAM industry is cyclical, and is characterized by sharp fluctuations in price. (Appleton, Tr. 6277-78 ("It's probably one of the most volatile businesses that exists today . . . the selling price of the product dramatically changing over time. You can have as much as an 80 or 90 percent drop in selling price in as short a period of time as 18 to 24 months.") and 6281 ("Q. Do you regard the DRAM business as a cyclical business in any way? A. Yes, well, it's very cyclical. When you consider that Micron's revenues can go up 3X and then drop by 80 percent from one year to the next, and when you talk about the supply that comes online in relatively large chunks, if you will, then it creates a very cyclical business"); Heye, Tr. 3641 ("The DRAM industry is very cyclical")).

Rambus's Response to Finding No. 78:

The proposed finding is in the present tense and is therefore irrelevant. Respondent also objects to the proposed finding to the extent it is meant to imply that the cyclical nature of normal market forces has been responsible for past price fluctuations in the DRAM industry. Such a conclusion ignores the evidence collected in connection with the pending Department of Justice criminal grand jury investigation of DRAM manufacturers and the evidence of market manipulation contained in RPF 1555-1599. *See also* RRFF 81.

79. The DRAM industry has been marked by consolidation. (Appleton, Tr. 6259) In the early to mid 1980's, there were approximately 20-25 DRAM manufacturers. (Appleton, Tr. 6259) Today, there are only 5-6 major DRAM manufacturers left, along with 2-3 much smaller manufacturers in Taiwan. (Appleton, Tr. 6276-6277)

Rambus's Response to Finding No. 79:

The proposed finding is not supported by the evidence. The Appleton testimony cited by Complaint Counsel does not speak to the number of manufacturers in the "mid 1980's." Additionally, the cited testimony does not state, as Complaint Counsel suggest, that "there are only 5-6 major DRAM manufacturers left, along with 2-3 much smaller manufacturers in Taiwan." Instead the cited evidence says only that "the majority of the business have now been reduced to five or six."

80. Approximate shares of sales of DRAMs in 2001 were: Samsung: 27%; Micron:19%; Hynix: 14.5%; Infineon: 9.7%; Elpida:8.5%; Toshiba: 6.4%. (CX2464 at 1)

Rambus's Response to Finding No. 80:

Respondent has no specific response other than to note that the cited evidence does not necessarily offer support for it. The cited evidence deals with "revenue ranking", which it appears to assume equates to "share of sales" without making any attempt, for example, to adjust for differing average selling prices or product mixes among different manufacturers.

81. The consolidation is due to uncompetitive manufacturers leaving the industry. (Appleton, Tr. 6277 ("[I]t's – it's been a very competitive business over time. Those companies that weren't able to focus on cost and reduction of cost simply weren't able to remain competitive, and the more competitive companies are the ones that have been able to remain, and the other ones have exited the business.")

Rambus's Response to Finding No. 81:

The proposed finding is vague, incomplete and misleading, is not supported by the cited evidence and leaves out relevant information to the extent it appears to suggest that a lack of competitiveness is the only reason some competitors left the DRAM business. For example, Micron's CEO Steve Appleton testified on cross-examination that it purchased the only other

DRAM manufacturer in the United States which, as part of the purchase agreement but before the closing, shut down its DRAM production. (Appleton, Tr. 6502; *see also* Appleton, Tr. 6277 stating that now, other than Micron, there are no other DRAM manufacturers in the United States).

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These are not natural market forces at work, as the proposed finding suggests. This is naked market manipulation, accomplished through an anti-competitive covenant not to compete, with the intent to restrict the marketplace availability of RDRAM. The proposed finding is thus contradicted by the evidence in the record.

82. In 1994, Micron was coming out of what had been a downturn in 1991 and 1992. (Appleton, Tr. 6288)

Rambus's Response to Finding No. 82:

Rambus has no specific response.

83. From 1998 through 2002, Micron made losses in each year except 2000. (Appleton, Tr. 6282-6284 and 6286-6287; *see* DX114). By mid way through 2003, Micron had made losses of approximately $1 billion. (Appleton, Tr. 6284)

Rambus's Response to Finding No. 83:

The proposed finding is misleading and incomplete. {

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84. Typically, only one type of DRAM tends to dominate the market at any one time. As each generation of DRAM is succeeded by a new one, the volume of sales of the older generation slowly drops off, and is replaced by sales of the new generation. (See McAfee, Tr. 11216-11217).

Rambus's Response to Finding No. 84:

The proposed finding is misleading and not supported by the evidence to the extent it suggests that there is no co-existence of different incompatible standards in the market at any one time. For example, Dr. Rapp testified that "[i]n 1995, fast page mode has an 87.2 share. In the following year, it's down to 40 percent, 39 – sorry – 39.4 percent, and EDO has taken the lead with 52.7. But there's a difference between them of 12 percentage points. The market in that year is divided between two different standards and it teaches just the opposite. . . . The following year just one year later, SDRAM is in the market and has captured, if I'm reading this right, a 33.5 percent share and FPM isn't gone with either. So what we've got in any given year is the market being divided amoung incompatible standards. . . . I don't know whether that's true of FPM and EDO, but it seems to me that it teaches exactly the opposite thing, that there is no technological requirement that only one standard has to dominate." (Rapp, Tr. 10103-04). The McAfee testimony cited by Complaint Counsel merely speaks of the DRAM industry "generally" and does not speak to the volume of sales in succeeding or older generations, as the proposed finding requests.

85. Thus, in the mid 1990's, the dominant form of DRAM was asynchronous. In 1995, fast page mode (FPM) accounted for 87.2% and extended data out (EDO) 9.9% of DRAM revenue share. (Rapp, Tr. 10248)

Rambus's Response to Finding No. 85:

Rambus has no specific response.

86. By the late 1990's, however, synchronous DRAMs (SDRAMs) had supplanted asynchronous as the dominant form of memory sold in the market. In 1998, SDRAMs accounted for approximately 60.8% of DRAM revenue share; EDO accounted for about 27.6%, FPM accounted for about 8.8%, RDRAM accounted for 1.6% and others accounted for about 1.3%. (Rapp, Tr. 10249).

Rambus's Response to Finding No. 86:

Rambus has no specific response.

87. In 2001, SDRAMs accounted for about 69.7%, RDRAM accounted for 12.5%; EDO accounted for 7.7%, DDR SDRAM accounted for 5.3%, FPM accounted for 4% and others accounted for 0.8%. (Rapp, Tr. 10249).

Rambus's Response to Finding No. 87:

The proposed finding is incomplete as it does not identify what the percentages are calculated in reference to, namely revenue share.

88. In January 2001, according to Rambus CEO Tate, DDR SDRAM accounted for 10 percent of the market, SDRAM accounted for 80 percent of the market, and RDRAM accounted for between 5 and 10 percent of the market. (CX2061 at 45-46 (Tate, Dep.)).

Rambus's Response to Finding No. 88:

The proposed finding misstates the evidence. Mr. Tate testified that based on market research he had seen, DDR SDRAM accounted for *less than* 10 percent of the market, and SDRAM "probably 80 percent, perhaps higher." (CX2061, Tate Infineon Depo., at 45-46).

89. In January 2001, according to Rambus CEO Tate, all systems shipping in the PC desktop and lap top market are using one of: Rambus DRAM, SDRAM, or DDR SDRAM for main memory. (CX2061 at 51-52 (Tate, Dep.)).

Rambus's Response to Finding No. 89:

Rambus has no specific response.

90. Over time, the bus speeds with which DRAMs have been able to operate has increased. In 1988 DRAM bus speeds were around 10 MHz. (Horowitz, Tr. 8081) The 2002 Infineon product information guide, in comparison, lists DDR SDRAMs running as high as 333 Mhz and SDRAMs running as high as 166 Mhz. (CX2466 at 5-7; *see* Becker, Tr. 1142)

Rambus's Response to Finding No. 90:

Rambus has no specific response.

91. Over time, the capacity of memory has increased substantially. (CX2853 at 37-41; CX2225 at 251-252) For example, from the mid-1990's to 2001 Infineon went from producing 64 Mb SDRAMs to 512 Mb DRAMs. (Peisl, Tr. 4384-4385; Becker, Tr. 1168-1173; Reczek, Tr. 4298-4300) Currently, companies are in the process of designing 1 Gb DRAMs. (Soderman, Tr. 9426)

Rambus's Response to Finding No. 91:

Rambus has no specific response.

92. Over time, the process technology, or size of the circuits and traces on each DRAM, has decreased. For example, Micron has decreased its process technology from .20 to .11 microns. (Appleton, Tr. 6294).

Rambus's Response to Finding No. 92:

Rambus has no specific response.

E. DRAMs are Commodities.

93. DRAMs are regarded in the industry as commodity products. (Appleton, Tr. 6280 ("Q. Have you ever heard the DRAM business referred to as a commodity business? A. Sure. Q. And do you agree with that characterization? A. Ah, I do in many ways"); Bechtelsheim, Tr. 5756 ("the nature of the memory market is that there's a number of suppliers which are fiercely competing for the memory business and the cost or prices for memories in the market behave very much like a commodity-type market."); Gross, Tr. 2307 ("among the components that we purchase for computers, it is the most commodity-like, it is the most influenced by the global supply and demand variables."); Heye, Tr. 3636 ("every memory in itself is a commodity.") and 3641); CX2107 at 30, Oh, Dep. Tr. 136 ("DRAM is – is a commodity in – in this electronic market, and they are – the DRAM manufacturers are producing standard products, so anybody who – can come and make the standard products."); Becker, Tr. 1138 ("[T]he DRAMs that we build in the manufacturing factory or the Richmond facility are considered commodity parts."); Polzin, Tr. 3960 ("We needed to make sure that whatever memory we chose in our systems for our microprocessors was a commodity and met the performance requirements at the lowest possible cost.").

Rambus's Response to Finding No. 93:

Respondent has no specific response except to the extent that the use of the phrase "commodity products" is meant to imply that price changes in DRAM markets are only the product of supply and demand, a conclusion undercut by the DRAM collusion evidence set forth

in RPF 1555-1599, and that may be challenged shortly by developments in the Department of Justice's ongoing criminal grand jury investigation of the DRAM industry. For example, in late 2001 and early 2002, immediately after a key Intel chipset that was to support RDRAM was dropped from the Intel roadmap, there was an apparent "consensus" that if Micron raised prices, the other DRAM manufacturers "will do the same and make it stick" (RX1922 at 1. after which the prices of DDR increased 400% over a four month period. (RX 1991 at 1. {

} (*in camera*)).

94. Business decisions of the DRAM manufacturers are driven by the fact that DRAMs are commodity products. (Becker, Tr. 1138-39 and 1154-55; CX2107 (Oh, Dep.) at 136, 159 (importance of cost); Horowitz, Tr. 8516-17 (choice of design)).

Rambus's Response to Finding No. 94:

The proposed finding is not supported by the evidence. While, the Becker and Horowitz testimony cited by Complaint Counsel discuss the commodity nature of the DRAM business, they do not speak to how or whether the business decisions of DRAM manufacturers are based on DRAMs being commodity products. The evidence shows that other factors, in any event, appear to drive the decisions and conduct of the DRAM manufacturers. (*See* RRFF 81, 93; *see also* RPF 1555-1599).

F. DRAM Manufacturers are Driven to Reduce Costs.

95. Cost in the DRAM industry is measured on a cost-per-bit basis. (Appleton, Tr. 6278-79 ("And so the cost to produce that individual bit is the way that we measure through time ... either cost reductions or how competitive we are.")).

Rambus's Response to Finding No. 95:

Rambus has no specific response.

96. On a per-bit basis, DRAM prices have dropped by about 30 percent per year for at least the last 25 years. (Becker, Tr. 1160 ("That's the -- that's the historical ASP or average selling price curve that we get for our memory, and that's been for the last 25, almost 30 years.").

Rambus's Response to Finding No. 96:

The proposed finding is not supported by the evidence. The Becker testimony cited by Complaint Counsel suggests that the average selling price of Infineon memory on a cost-per-bit basis has dropped about 30 percent over the last 25 to 30 years, not that industry prices have dropped at this rate. In addition, the proposed finding ignores relevant evidence, including evidence that there are sharp variations from this claimed downward trend. For example, in late 2001 and early 2002, immediately after a key Intel chipset that was to support RDRAM was dropped from the Intel roadmap, there was an apparent "consensus" that if Micron raised prices, the other DRAM manufacturers "will do the same and make it stick" (RX1922 at 1), after which the prices of DDR increased 400% over a four month period. (RX 1991 at 1. {

} (*in camera*).).

97. As a result of the fact that DRAM prices have dropped by 30 percent per year, DRAM manufacturers have historically reduced costs per bit by about 30 percent per year as well. (Becker, Tr. 1155 ("within our industry, over the last 25 years or so. . . our industry has had to reduce its cost per bit or cost per piece of memory by about 30 percent per year just to remain competitive."); Appleton, Tr. 6279 ("Micron's been able to average over the last 20 years reducing our costs every year, compounded, approximately 25 to 30 percent annually.")).

Rambus's Response to Finding No. 97:

The proposed finding is not supported by the evidence and is misleading in discussing a "result." As noted in response to Proposed Finding No. 96, Complaint Counsel have not presented evidence that DRAM prices have dropped by 30 percent per year. Also, the cited

Appleton testimony does not attribute a reason to why DRAM manufacturers have historically reduced such costs, as the proposed finding of fact suggests.

98. DRAM manufacturers must strive to reduce costs by about 30 percent per year in order to remain competitive. (Appleton, Tr. 6279 ("the most predominant factor in being successful in the DRAM business has been a company's ability to continue to lower its cost per bit, and that's why we focus so much on it."); Becker, Tr. 1155 ("fact that we can't control the selling price but can only control the cost, that means we have to do a very good job of controlling those costs. We have to be very aggressive to keep those costs down.") and 1160-1161 (If Infineon does not reduce costs by 30 percent per year, "[m]y costs are significantly higher than my competitors, and I slowly go out of business."); Bechtelsheim, Tr. 5761 ("It was well understood that the memory market was a very cost-competitive market") and 5975 ("I would claim that memory prices are very competitive and there is in fact fierce competition in the market where virtually no manufacturer is returning a reasonable profit on their fab investment."); Heye, Tr. 3636 ("they're constantly cost reducing memory technology."); McAfee, Tr. 7200-02, 7206-07).

Rambus's Response to Finding No. 98:

The proposed finding is incomplete and ignores important evidence that collusion on price – a factor other than cost and the workings of the open market – appears also from time to time to play a role in making DRAM manufacturers stay competitive. (*See* RPF 1555-99).

99. DRAM manufacturers are extremely concerned about reducing their costs because their customers demand low cost products. (CX1708 at 2 (Richard Crisp writing "Compaq (Dave Wooten) like the others, stressed that price was the major concern for all of their systems. They didn't particularly seem to care if the SDRAMs had 1 or two banks so long as they didn't cost any more than conventional DRAMs. . . . Sun echoed the concerns about low cost. They really hammered on that point."); CX1030 at 2 ("Mr. Choi said that when he met with Compaq, Compaq (server group) said that they will not use Rambus because of the royalty for the chip set."); CX2383 ("[S]ince we are very cost conscious we are willing to drop features that add too much cost or complexity"); CX0711 at 34 (Richard Crisp writing "[T]hey want cheap, cheap, cheap"); JX0027 at 13 ("The Committee noted they wanted highest performance and lowest price SDRAM."); CX2777 ("[T]he age old rule for DRAMs still apply. Customers will take as much performance as we can give them for absolutely no added cost over the previous technology. They will not pay extra for increased DRAM performance.")).

Rambus's Response to Finding No. 99:

The proposed finding is not supported by the evidence and ignores important evidence on

the ability of the DRAM manufactures to force price increases on customers by acting together. None of the cited exhibits or testimony suggest that the concern of DRAM manufacturers was "extreme[]" or that their customers "demand[ed]" low cost products. The documents cited in the cross-reference reflect a few hearsay comments from some customers and others standing for the unremarkable proposition that they prefer low costs, but this does not mean that all DRAM customers are "price sensitive" in that they would curtail purchasing or forgo performance due to small increases in price. The evidence shows a great concern among DRAM customers that DRAM performance was limiting computer system performance. (*See* RPF 35-40; RX 285A ("the DRAM interface has become more and more a problem for system developers")).

100. DRAM manufacturers also are extremely concerned about reducing cost because producing at low cost is a critical factor to a DRAM manufacturer's success in the marketplace. (Appleton, Tr. at 6277 ("Those companies that weren't able to focus on cost and reduction of cost simply weren't able to remain competitive, and the more competitive companies are the ones that have been able to remain, and the other ones have exited the business.") and 6279 ("the most predominant factor in being successful in the DRAM business has been a company's ability to continue to lower its cost per bit"); CX2107 at 136 (Oh, Dep.) (" . . . the competition is very severe, and, as a result, the margin, the profit margin, is very, very small, so we have to be really concerned on the cost.")).

Rambus's Response to Finding No. 100:

The proposed finding ignores important evidence. As noted in RPF 1555-1599, collusion among the DRAM manufacturers and the boycotting of competing products also appear to factors that contribute to success in the marketplace. Also, as noted in Response to CCFF 99, the cited evidence again does not support a finding of "extreme" concern by all the DRAM manufacturers.

101. The pressure to reduce costs creates incentives for DRAM manufacturers run their fabs continuously. (Becker, Tr. 1136 ("We try to operate our factory seven days a week, 24 hours a day, 365 days a year"), 1139 ("What we can control and what we can influence is what it

costs us to manufacture those chips, and the lower our manufacturing costs, especially compared to our competitors, the better off we are, and one of the ways we do that is we leverage that $1 and a half billion investment is by running it constantly. If it's sitting there not producing anything, then it's costing me money, and I'm getting no return on it."); Appleton, Tr. 6254 ("we ran 24 hours, seven days a week beginning in 1983 shortly after I started with the company.")).

Rambus's Response to Finding No. 101:

Rambus has no specific response.

102. Because of the complexity of shutting down and restarting a fab, shutting down for a single day can cause a loss of productivity equal to 2.5 days. (Becker, Tr. 1137-38).

Rambus's Response to Finding No. 102:

The proposed finding misstates the evidence, which, in any event, applies only to a single fab operated by Infineon in Virginia. Even as to that single Infineon fab, the Becker testimony cited by Complaint Counsel says that idling the factory for one day lost productivity on the order of "two to two and a half days," not "equal to 2.5 days" as Complaint Counsel suggests. (Becker, Tr. 1138).

103. One of the major ways that DRAM manufacturers are able to reduce cost is by performing shrinks on DRAMs already in production. (Becker, Tr. 1156 ("probably the biggest thing we do to influence or to decrease our costs on a regular basis is we shrink the technology, and the reason that that works so well is we're able to produce the same part with the same function . . . but we can produce it on a smaller chip, because we're using a smaller technology, and the wafer size doesn't change for us.")).

Rambus's Response to Finding No. 103:

Rambus has no specific response.

104. Shrinks reduce costs by allowing manufacturers to achieve economies of scale by producing a higher volume of DRAMs pe silicon wafer. (Williams, Tr. 872 ("Q. And it's been your experience that there are economies of scale which are realized in the manufacture of integrated circuits, correct? A. Correct. Q. The higher the volume, generally the cheaper the cost of manufacture? A. Correct."); Peisl, Tr. 1156 ("So, if you have a smaller chip, you can fit more of those chips on a wafer, and if you get more of those chips on a wafer, your cost per chip is greatly reduced.")).

Rambus's Response to Finding No. 104:

Respondent has not specific response other than to note that the "Peisl" testimony cited by Complaint Counsel was actually offered by Mr. Becker. (Becker, Tr. 1156).

105. The current high volume DRAM product are the first to experience cost reduction efforts by the DRAM manufacturers. (CX2544 at 1 ("Toggle happen[s] when volume hits... the memory vendors migrate the highest volume memory to the new processes first, therefore giving cost advantage."); MacWilliams, Tr. 4837-4838 ("What it means is the transition of volume from one standard to the next. So what we're referring to is the fact that the DRAM vendors, for operating reasons, typically will shrink their highest-volume parts first, and therefore those parts have an advantage because they get the process technologies, the best cost structures first, its in their economic interest to do so.")).

Rambus's Response to Finding No. 105:

The proposed finding is not supported. The proposed finding regarding the application of die shrinks rests on evidence from a non-manufacturer. (*See* RRFF 105). The evidence shows that DRAM manufacturers are constantly redesigning different types of DRAM. (*See* RPF 1278-86). For example, Micron taped out from { } new DRAM designs in each year between 1998 to 2002, and is { } (Shirley, Tr. 4218-29, 4282 (*in camera*)).

106. Because current-generation commodity DRAMs are generally the highest volume DRAMs in production, current-generation DRAMs often have the lowest prices to DRAM customers. (Gross, Tr. 2306 ("[I]ndustry standard products are most often produced in the highest volume in the industry, and those efficiencies in manufacturing and the level of competition in that production enables the best cost per bit.")).

Rambus's Response to Finding No. 106:

The proposed finding misstates the cited testimony, and is not supported by the evidence. The Gross testimony cited by Complaint Counsel does not support the notion that "current-generation DRAMS are *generally* the highest volume DRAMs in production." Gross testifies that

"often" (not "generally") industry standard products are produced in the highest volume. The cited testimony also does not quantify in any way the relationship between "current-generation DRAMs" and price. Nor does it support a necessary relationship between high volume and low price. Ms. Gross simply testified that high volume "*enables* the best cost per bit," not that such volumes actually result or "often" actually result in the lowest price to customers.

107. The pressure to reduce costs also drives the DRAM industry to avoid paying royalties whenever possible. CX0711 at 13 ("Terry Walther of Micron . . . Said they are very nervous about doing a deal. Don't like license type business he says."), 35 ("Our proposition should be attractive there if we do not scare them away with extremely high license/royalty terms."), 61 ("Farhad . . . says their #1 issue with the Rambus business proposal is the royalty rate. They do not want to be straddled [sic] with 3% royalties."); CX0913 at 1 ("[IBM] asked lots of suspicious questions on our IP, patent pooling, and biz model. . . . He assured me that they are seriously considering Rambus. But the IP thing is a real dilemma."); CX1030 at 2 ("Mr. Choi said that when he met with Compaq, Compaq (server group) said that they will not use Rambus because of the royalty for the chip set."); CX0838 at 1 ("I think that Samsung is on a path to do anything they can to get out of paying us royalties"); Heye, Tr. 3731 ("The second concern [about Rambus's patent claims] was a possible cost disadvantage we might incur in the infrastructure due to the incremental royalty fees"); Appleton, Tr. 6299 ("when I became CEO in 1994, we were paying approximately 10 percent of our revenues in royalties, and we knew that going forward that that just wasn't going to work for the DRAM business model, it just wasn't possible to do that, and as a result, we focused on developing our own know-how, if you will, developing our own intellectual property, and we already talked about capturing that intellectual property so that we could reduce those royalty rates."); CX2107 at 158 (Oh, Dep.) ("[A royalty] will add additional cost to the manufacturing cost, so we are very much concerned.")).

Rambus's Response to Finding No. 107:

The proposed finding is incomplete and misleading and ignores relevant testimony. The evidence shows that the DRAM industry routinely agrees to pay royalties for licensed technology and that JEDEC routinely adopts patented technologies knowing that royalties will need to be paid. DRAM industry members pay royalties for licensed technologies and have not rejected proposals for technologies that would require the payment of royalties. Hyundai agreed to pay Texas Instruments 8% to license technology used in DRAMs. *Texas Instruments, Inc. v.*

Hyundai Electronics Indus., 42 F. Supp. 2d 660, 663-64, 671, 676-77 & n.39 (E.D. Tex. 1999); *Texas Instruments, Inc. v. Hyundai Electronics Indus.*, 49 F. Supp. 893, 897 (E.D. Tex. 1999). Samsung licensed technology from Texas Instruments and agreed to pay 9% on the sales of DRAMs in the United States and 3% on the sales of DRAMs in Japan. *Texas Instruments, Inc.*, 49 F. Supp. at 902. Andreas Bechtelscheim testified that Sun expected memory module manufacturers to pay for the use of Sun's patented technology when they made products for Sun's SPARC workstations. (Bechtelscheim, Tr. 5899-901).

Similarly, JEDEC has repeatedly standardized technologies that have patent implications. For instance, in May 1990, JC 42.3 sent a ballot to Council to standardize the 256K x4 MPDRAM technology knowing that Digital Equipment Corporation had a patent on the technology and demanded a royalty rate of 1%. (JX 1 at 6, 24). In July 1992, JC 42.3 passed ballots to standardize 2M x8/x9 Sync DRAM in TSOP II knowing that Motorola had an issued patent on the technology and would demand royalties. (JX 13 at 9-10, 136). Similarly, JEDEC members voted to rescind a hold on TI's Quad CAS technology knowing that TI would require the payment of royalties. (RX 562 at 13; JX 25 at 5).

DRAM industry members also agreed to pay Rambus royalties for its RDRAM technologies, which ranged from 2% to 5%. In July 1991, long before Intel became interested in RDRAM, NEC signed an RDRAM license agreement that specified a 2% royalty rate for Rambus Microprocessors and Microcontrollers, 1% for Rambus Memory Devices, 3% for Rambus Peripherals, and 3% for Customer Specific Rambus Products. (RX 538 at 22). In November 1994, again well before Intel selected RDRAM for the next generation DRAM, Samsung agreed to an RDRAM license that specifies a 2% royalty rate, which declines at certain

volume marks. (RX 518 at 23). Hyundai agreed, in December 1995, to an RDRAM license agreement that specifies a 2.5% royalty rate for Rambus DRAMs (which declines to 2% then 1.5% in 2000 and 2002 respectively), 3% for Rambus processors, and 5% for Rambus ASICs and Peripherals. (CX 1600 at 12). Micron agreed to an RDRAM license in March 1997 that specifies a 2% royalty rate. (CX 1646 at 11). Also in 1997, Siemens entered into an RDRAM license that specified a royalty rate of 2.5% for Rambus DRAMs (which reduced to 2% if RDRAMs exceeded 25% of Siemens total DRAM sales) and 5% for Rambus Peripherals. (CX 1617 at 12). Mitsubishi entered into a February 1998 RDRAM license that specifies a 2.5% royalty rate on Rambus DRAMs, 3% for Rambus processors, and 5% for Rambus ASICs and Peripherals. (CX 1609 at 11). AMD {

} (Heye, Tr. 3919-20 (*in camera*); CX 1420 at 8 (*in camera*)).

The evidence also shows that industry royalty rates, including those paid by DRAM manufacturers, average approximately 4.5%. (See RPF 1378-1393). IBM's policies, which were shown to JEDEC, set forth royalty rates for its technologies from 1-5% of selling price. (JX 9 at p.24; Kellogg, Tr. 5232, 5238-39; Kelley, Tr. 2618-20; see also RX 653 at IBM/2 128124 ("The normal royalty rate for a license to IBM patents ranges from 1% to 5% of the selling price for the apparatus that practices the patents"). Further, royalty rates applied uniformly across the industry are not shown by the cited testimony to be the kind of "cost disadvantage" referenced by the cited testimony that would make any one manufacturer less competitive.

108. DRAM manufacturers were particularly concerned to avoid royalties on high-volume, commodity DRAMs. (CX2107 at 159 (Oh, Dep.) ([C]ost is"very, very important" on high volume commodity parts); CX2250 at 2 ("License is ok for niche, but not for main

memory."); Lee, Tr. 7047 ("He had made a statement on the order that having a license fee for some small-volume product would be reasonable, but it didn't make sense for a very high-volume product of that magnitude for main memory."); *id*. at 7047-48 ("the 2 percent [royalty demand] was larger than anything we'd ever heard of for an interface technology and certainly the largest thing we ever heard of for some sort of fee we'd have to pay to produce main memory."); CX0676 ("[Samsung] will think that 2% is high for a commodity (memories).")

Rambus's Response to Finding No. 108:

The proposed finding is incomplete and misleading and ignores relevant testimony. (*See* RRFF 107).

109. Concerns about royalties on high-volume commodity DRAMs have caused the industry to prefer royalty-free open standards whenever possible. (CX2107 at 137 (Oh, Dep.) (open architecture was important to Hyundai "[b]ecause it means that it is adopted by JEDEC, and thus it requires no royalty or no fees at all."); CX2294 at 15 ("Strong Points . . . Open architecture without royalties or fees"); CX0676 ("[Samsung] will think that 2% is high for a commodity (memories)"); CX2726 at 7 "Why DDR Is Cost Effective No Royalties")

Rambus's Response to Finding No. 109:

The proposed finding is incomplete, misleading and ignores relevant testimony for the reasons stated above. (*See* RRFF 107). In addition, the evidence cited does not support the proposed finding for other reasons as well. Dr. Oh's testimony is entitled to no weight because it was clearly based on a false premise. Dr. Oh testified, in the testimony cited in the proposed finding, that he believed a standard was royalty-free *because* it was a JEDEC standard. This statement is clearly contrary to the RAND policy of JEDEC and is contradicted by the many patents and cross-licenses covering JEDEC standards.

The proposed finding is also contradicted by the clear evidence showing that JEDEC's policies, even under Complaint Counsel's construction of those policies, left significant intellectual property undisclosed. For example, even under that construction, only patents "known" to the actual JEDEC participant had to be disclosed. (Kelly, Tr. 1870). It follows that

other patents held by a participating company would be a basis for future royalty demands.

As another example, IBM informed JEDEC in December 1991 that: "The normal royalty rate for a license to IBM patents ranges from 1 percent to 5 percent of the selling price for the apparatus that practices the patents. This is a very reasonable rate in our industry and generally meets the requirements of standards organizations that licenses be made available on reasonable and nondiscriminatory terms and conditions." (Kelley, Tr. 2617). Although this statement presented at JEDEC and included in the JEDEC meeting minutes (JX9 at 24), Complaint Counsel has presented no evidence that JEDEC members *preferred* not to pay IBM's licensing rates, that anyone was *concerned* that these licensing rates might apply to high-volume commodity DRAMs, or even that anyone ever thought the rates were unreasonable.

110. Even with respect to DRAM architectures that were not regarded as high-volume commodity products (including RDRAM before it received Intel's endorsement), DRAM manufacturers sought to negotiate royalties down as far as possible. (CX0733 (Tate e-mail: "Big stumbling block is royalties – they [Samsung] want numbers in 1% or less range."); CX0711 at 61-62 (Crisp e-mail: Hyundai "didn't care that much about the first xxx million units: their worry was what if the product was wildly successful: how can they minimize the upside risk? SO he liked the idea of a pre-set schedule of declining royalties."; "So my suggestion is a . . . 2.5% DRAM royalty declining to 1.25% after 50 million cum units ship.")).

Rambus's Response to Finding No. 110:

The proposed finding is misleading and incomplete. While DRAM manufacturers naturally sought better terms in their negotiations with Rambus for RDRAM licenses, DRAM manufacturer agreed to pay royalties of ranging from 2% to 5% for Rambus technologies in various types of products, both before and after Intel endorsed RDRAM. (*See* RRFF 107, 109.) In addition, to the extent that the actions or preferences of any memory manufacturers can be understood from Exhibit CX0711, cited by Complaint Counsel, that document suggests that at

least one memory manufacturer, Hyundai, did not seek to negotiate down royalties for lower volume products as far as possible: Hyundai "didn't care that much about the first xxx million units …." (CX0711 at 61-62).

111. When the DRAM industry is unable to avoid royalties completely, they have sought to negotiate royalties down as far as possible. CX0961 at 1 ("I had requested a 1:1 with pat g[elsinger of Intel] as a result of his request . . . to lower our rdram royalties to <0.5%"); CX0974 at 1 ("On royalty reduction we tried several trial discussion with major dram partners and NONE were willing to trade royalty reductions for CHANGES IN BEHAVIOR: all said give me lower royalty and I'll be more motivated."); Appleton, Tr. 6300 (Micron has "gone through negotiations, future negotiations as we developed our own property, and as a result of that, our royalties today are very insignificant. Essentially they have gone from 10 percent of the company to an insignificant percentage of the company.")).

Rambus's Response to Finding No. 111:

The proposed finding is not supported by the evidence and is contradicted by other evidence. (*See* RRFF 110). Moreover, in the Micron example cited by Complaint Counsel, it is not clear whether it was the negotiations that signicantly reduced royalties or – as seems to be the case – the purchase by Micron of Texas Instrument's DRAM manufacturing facilities, the expiration of some of Texas Instrument's relevant patents, and Micron's own aggressive filing of patents. (*See* Appleton, Tr. 6507).

G. Strong Forces Drive Standardization in the DRAM Industry.

112. Standards are essential in the DRAM industry. (CX2634 at 3 (article by former Rambus expert states: "Deviation from the herd is not tolerated by the marketplace. Not since the 1970s have individual DRAM vendors had the power to innovate architecturally.") CX1284 at 28 (Rambus's co-founder Mike Farmwald once stated, "There is real value in having a world DRAM standard.")).

Rambus's Response to Finding No. 112:

The proposed finding is vague as to whether "standards" is intended to refer to "*de jure* standards" or "*de facto* standards" or both. In any event, the cited evidence does not support any

construction of this proposed finding. The purported market intolerance of "deviation from the herd" and the purported "lack of DRAM manufacturer power to innovate architecturally" – even if established by the cited evidence – say nothing about standards. Nor do these purported facts speak to standards (of any kind) being "essential." Dr. Farmwald's recognition of "real value" in a "world standard" likewise does not speak to standards being "essential." Moreover, Dr. Farmwald was not addressing the kind of formal standards that are adopted by JEDEC and are primarily at issue here.

113. Standardization benefits the DRAM industry generally by ensuring quality and reliability. (J. Kelly, Tr. 1791 ("to the extent that companies are following JEDEC standards, there is a consistency in terms of quality and reliability"); Prince, Tr. 9016-17 ("when something comes for formal standardization, it has the review of peers throughout the industry. Everyone gets a chance to review it and make comment, and if there are good and bad features, they can be modified. And what ultimately comes out for the users in the industry is the most adequate device that the industry collectively can prepare.")).

Rambus's Response to Finding No. 113:

The proposed finding is incomplete, misleading, unsupported by the cited evidence and contradicted by more reliable evidence. The testimony of Mr. Kelly cited by Complaint Counsel states that "companies following JEDEC standards" produce "consistency" in the areas of "quality and reliability." This statement about "consistency" does not speak to the ensuring of either *high* quality or a *high* level of reliability, as the proposed finding implies. Moreover, if (as Complaint Counsel allege) JEDEC was indeed trying to follow a standardization process that avoided patents and patent royalties then, it was foregoing certain technological improvements and, necessarily, sacrificing quality. The Prince testimony cited by Complaint Counsel supports and certainly does not contradict this conclusion. It speaks only to achieving the "most *adequate*" device, which implies quality trade-offs.

Finally, the cited testimony from JEDEC's president, general counsel and long term employee John Kelly is not as reliable as testimony solicited from Complaint Counsel's witness Pete MacWilliams of Intel, a distinguished engineer who explained that SDRAMs being produced in 1995 – two years after JEDEC "standardized" SDRAM it in 1993 – were based on data sheets that "didn't all match", which meant "they were going to build incompatible parts." Mr. MacWilliams further explained:

> "[Vendors] could all say they were compliant because they followed the JEDEC ballots, but the fact there was always an ongoing stream of ballots made it somewhat problematic. And most of the differences were very subtle. The basic devices were all the same, but there were a few timing differences. There were basically two functions in the devices that were a little bit different between vendors, and so it wasn't an issue of being able to make the devices work, but if you're trying to do the device in high-volume manufacturing, you want all vendors to supply a compatible device. We thought there would be problems."

(MacWilliams, Tr. 4908-10). Mr. MacWilliams' testimony is more reliable because Intel generally as a consumer of standardized DRAMs, and Mr. MacWilliams (a design engineer and Director of Platform Architecture at Intel), is in a better position than Mr. Kelly (a lawyer) to determine whether JEDEC standardization "ensured quality and reliability."

114. Standards in the DRAM industry ensure that the DRAM devices are compatible with other components. (Peisl, Tr. at 4410 ("Interoperability… [means] the DRAM works flawlessly together with all the components in the system. It's not only one chip that the DRAM is interfacing with but all the other components on the motherboard, the position on the motherboard, the particular layout on the motherboard, other components on the modules, for instance, like registers. You have to make sure your part is fully compliant with all the specifications of the other chips. That is why everybody is working towards the JEDEC

specification.") and 4382 (Standards are "of utmost importance…not only for…a DRAM designer on one side, but it's very important…for the chip designers at Intel, AMD and other companies who design the chips that communicate with our DRAMs as well, and it enables essentially the whole industry to develop products that work together in more or less a predefined manner."); Heye, Tr. 3715 ("AMD spends a lot of time -- AMD works collaboratively with the memory vendors through JEDEC to ensure that the memory standards going forward can be implemented both by the chipset vendors and the memory vendors.")).

Rambus's Response to Finding No. 114:

The proposed finding is not supported by the evidence, is contradicted by other, more reliable evidence (if it is meant to apply to the past) and is irrelevant (if, as written, it is meant to apply only in to the present tense). (*See* RRFF 113). Moreover, the Peisl testimony cited by Complaint Counsel (Peisl, Tr. 4410) does not suggest that standards in the DRAM industry ensure interoperability; rather, the testimony was merely offered by Mr. Peisl as an explanation of what he meant by "interoperability" when he indicated that it was a concern of Infineon's customers in the testimony on the previous page (Peisl, Tr. 4409). The same is true for the Peisl testimony (Peisl, Tr. 4382), which states only that standards "enable[]" the collaboration, not that they "ensure" compatibility. The Heye testimony cited by Complaint Counsel similarly only describes what AMD "works" to achieve with respect to standards. It does not purport to establish —and does not establish — that the standards themselves "ensure" anything. Mr. Heye's testified only that AMD "works" to achieve a result such that that standards can be "implemented" by both chipset and memory vendors. Mr. Heye did not testify as to whether this "work" by AMD (or his acknowledged work as leader of "team DDR," for that matter) actually results in such implementations being successful – in terms of compatibility or in any other terms. As explained by Mr. MacWilliams (RRFF 113; MacWilliams, Tr. 4908-10), such JEDEC's SDRAM standardization efforts did not result in DRAM device compatibility with

other components.

115. Standards in the DRAM industry ensure that the entire industry, including manufacturers of systems and compatible components, settles on one solution, thus allowing firms to make long-term investments the success of which depend on long-term investments made by others. (Macri, Tr. 4620-21 (Discussing CX1315, he states "[U]sually in the DRAM world, there is only one choice. You know, it's not a matter of what; it's a matter of when. So, users, they can plan their transition based on their own -- you know, their own internal decision-making process, plan their transition to meet their own business needs. The suppliers, they know making the investment up front is going to be realized, because they know the users will eventually move over. It may not all be at once, but over a period of time, they can count on the market slowly building up. In this particular case [when both DDR SDRAM and RDRAM could have become the dominant standard], there were two choices, and it was very unclear which way the world would go."); Heye, Tr. 3678 ("from the time you start thinking about a chipset to implementing it, especially when it's brand new like the one for AMD, it's about two years prior to shipping."); Bechtelsheim, Tr. 5796-5797 ("[O]ur design cycle was typically one to two years for a new product, so we would need to know at the beginning of that design cycle which exact memory technology we could use at the time the product would be manufactured.")).

Rambus's Response to Finding No. 115:

The proposed finding is not supported by the evidence, ignores more reliable evidence (if it is meant to apply to the past) and is irrelevant (if, as written, it is meant to apply only in to the present tense). The Macri, Heye and Bechtelsheim testimony cited by Complaint Counsel express the desire of the witnesses (and their companies) to know what memory technology their products would be using several years before their own products are manufactured. The testimony does not in any way suggest the standards in the DRAM industry "ensure" that the industry settled on one solution and the evidence at trial shows that, at any one time, multiple solutions co-exist in the marketplace. (Rapp, Tr. 9791-9798). As Mr. MacWilliams explained (RRFF 113; MacWilliams, Tr. 4908-10), JEDEC's SDRAM standardization effort did not "ensure" one solution that could be used consistently or reliably by others in the industry. It was for this reason that Intel issued its own PC-100 standard in 1995 (*id.*) and Intel's modifications

were adopted back into a subsequent SDRAM standard at JEDEC. (Peisl, Tr. 4411 ("and it was later on added into the JEDEC specification.")).

1. Benefits to DRAM Purchasers.

116. Customers require standardized DRAM because standards ensure that parts purchased from various manufacturers are perfect substitutes, thereby ensuring customers of multiple sources of supply. (CX1075 ("everyone wants multiple-sourced DRAMs, so to make DELL happy, you need multiple suppliers of DRAMs, modules, connectors, and clock chips"); CX1354 at 5 ("DRAM Industry: commodity business, Customers want multiple sourced, compatible DRAMs."); Peisl, Tr. 4408-10 ("JEDEC essentially ensured that it had multiple sources because everybody in the industry, every major DRAM company or every DRAM company and every controller company designed towards the agreed-upon JEDEC standard."); Polzin, Tr. 3973 ("JEDEC allows manufacturers to all design to a common standard and basically enables the commodity marketplace. Everybody is designing compatible parts at the lowest possible cost competing on manufacturing cost."); Sussman, Tr. 1324 ("we have no choice, we must standardize the part so it will fit within the consumer's application") and 1327-28 ("if the part is standardized, [customers] can buy it from multiple sources, they have options, and in that there are multiple sources . . . So, often the customers will be very hesitant to design a part into their system that is not standardized. They want more than one vendor to be able to provide it to them."); G. Kelley, Tr. 2387-88 (DRAM "must be available for many suppliers, and it must be interchangeable from those suppliers"); Becker, Tr. at 1152-1153 ("Our customers, customers like Dell, IBM, Compaq, they're interested in buying DRAM models or components from…[Infineon's] parts or Samsung's parts or Micron's part and use them interchangeably, and through the standards process, they get that benefit."); Rhoden, Tr. 296 ("Essentially what they're asking for is they want interchangeability where they can get it from multiple places, get the same thing from multiple places. It gives them a great deal of advantage in the market.") and 298-299 ("Q. Why do the customers want standardization? A. Well, they -- frankly, they like to have a broad customer supply base so they can pit one supplier against the other and get the lowest possible price"); Williams, Tr. 763 ("Their customers are mainly computer customers who require that they are able to buy products from multiple sources and that these products interoperate, and JEDEC is the body that sets those standards by which there are interoperability and everybody has, in essence, the same part based upon the JEDEC standard") and 823 ("customers were very concerned, like they always are, to ensure that you've got multiple sources and that they're not locked into a proprietary product where then you can charge whatever you want. They want to make sure that there's a plentiful supply and that . . . they can get it from everybody."); Williams, Tr. 763 ("for Micron, they make memory products that are used in the industry. Their customers are mainly computer customers who require that they are able to buy products from multiple sources"); Gross, Tr. 2305 ("[G]enerally industry standard material is made in the highest volumes, which enables the most competitive costs and price.") and 2306-2307 ("all of the DRAM manufacturers would strive to meet those standards and produce product that aligned with those standards."), 2307 (HP procures DRAM from all of the largest

DRAM manufacturers in the world.); Lee, Tr. 6859 ("[I]n our business, we have to have perfectly substitutable products from other suppliers, so there needs to be multiple sources of the same part."); Polzin, Tr. 3943-44 ("It was crucial that we had a common standard that would allow interoperability"); Bechtelsheim, Tr. 5789 ("the primary concern was that JEDEC was in fact able to develop a standard that was suitable for manufacturing of identical parts by all the memory manufacturers"), 5863-64; Farmwald, Tr. 8296 ("[Interchangeability is] very important to the DRAM customers"); Heye, Tr. 3641 ("because the volume of memory is so great, Apple thought it was very, very important to have multiple suppliers"); Goodman, Tr. 6013 ("we try and avoid a single-source scenario")).

Rambus's Response to Finding No. 116:

The proposed finding is vague with respect to the term "standardized." To the extent that this is intended to refer to standardization at JEDEC, the proposed finding is not supported by the evidence, ignores more reliable evidence (if it is meant to apply to the past) and is irrelevant (if, as written, it is meant to apply only to the present). The bulk of the testimony cited by Complaint Counsel merely suggests that customers desire or require parts that are interchangeable, and they suggest this is so for various reasons including to get multiple sources and enable price competition. The evidence does not support a finding that standardization at JEDEC was necessary to achieve this result. Nor is JEDEC standardization sufficient to achieve this result, as shown by the testimony from Mr. MacWilliams regarding JEDEC's 1993 SDRAM standard, which was not sufficient to ensure interchangeability or multiple sources. (RRFF 113; MacWilliams, Tr. 4908-10).

117. Customers benefit from the presence of multiple DRAM suppliers because competition between the suppliers ensures customers will receive lower prices for DRAM. (Bechtelsheim, Tr. 5762 ("it was well-understood that in a competitive market where multiple manufacturers make essentially the same type of component that the cost to us as a customer would be significantly superior and there would be a lot more cost pressure on the manufacturers themselves to optimize the manufacturing of their components."); Polzin, Tr. 3973 ("JEDEC allows manufacturers to all design to a common standard and basically enables the commodity marketplace. Everybody is designing compatible parts at the lowest possible cost competing on manufacturing cost."); Peisl, Tr. 4409 (A very simple economic law says: The more suppliers

you have, the lower you can drive the cost."); Gross, Tr. 2307-2308 ("When you have several sources, they, of course, will compete for business, which generally produces a lower price."); Rhoden, Tr. 298-99 (customers "like to have a broad customer supply base so they can pit one supplier against the other and get the lowest possible price."); G. Kelley, Tr. 2388); J. Kelly, Tr. 1791 ("any company wishing to comply can and can develop product to the standards, and that tends to mean more sources of supply"; this means "more competition in the manufacture of product," which "tends over time to drive the price down")).

Rambus's Response to Finding No. 117:

The proposed finding is not supported by the evidence, ignores more reliable evidence (if it is meant to apply to the past) and is irrelevant (if, as written, it is meant to apply only in to the present tense). The cited evidence is a recitation of traditional laws of supply and demand in markets assumed to be free of supplier price collusion. It does not purport to – and does not – establish what has actually happened in the real world DRAM market. In fact, the existence of multiple vendors in the past for DDR has not "ensured" lower prices for DRAM, as witnessed by the 400% increase in DDR DRAM prices that followed the "consensus " reached among DRAM manufacturers in the four months following the internal Micron email dated November 26, 2001, RX-1922A ("The consensus from all suppliers is that if Micron makes the move [to raise prices on DDR], all of them will do the same and make it stick."). *See also* RX 1991 at 1 (*in camera*).

118. Customers benefit from the presence of multiple DRAM suppliers because having multiple sources reduces the risk of losing supply. (Gross, Tr. 2308 ("[A]ny change to our business or the DRAM supplier's manufacturing would impact directly the other partner, and that's,... a fairly unacceptable risk, since its not a necessary risk to take."); Landgraf, Tr. 1692-93 ("We also had assurance of supply going forward. . .many of HP's products are supported for a five to seven, maybe ten-year product life cycle, and in some cases that exceeds the manufacturing cycle for some suppliers . . .by having a standard, we would have a greater chance of having continuity of supply for any time in production or even in support life."); Rhoden, Tr. 298-99 ("they also have the capability that if one supplier disappears or whatever, they still have a continuous supply. So, standardization is something that they. . . basically demand."); Heye, Tr.3641 ("availability is very, very important and when you have a commodity like memory, you know if you don't get the memory, you can't chip your Mac…you're out of business. And because the volume of memory is so great, Apple thought it was very, very important to have

multiple suppliers.")).

Rambus's Response to Finding No. 118:

Rambus has no specific response.

2. Benefits to DRAM Suppliers.

119. Standardization in the DRAM industry benefits suppliers by providing a high degree of assurance that there will be a demand for product and by allowing suppliers to leverage their design costs over a number of designs. (Rhoden, Tr. 296-298 ("there's a great deal of investment, billions of dollars, that go into the creation of factories and designs that are necessary to produce DRAM, and the supplier gets a large demand, because working with the customer inside an area like JEDEC, because you're working together with your customers and with the supply base, and when everyone agrees, then they have essentially an automatic market . . . they have basically a presold customer base just by complying and working with the standard."); Appleton, Tr. 6275 (" . . . when the whole world can design to a standard, then it has a benefit . . . to those of us that manufacture, because we all then cumulatively put resources towards bringing that product to market and it's more cost-effective because we're able to know what's going to be consumed in the marketplace in aggregate"); Macri Tr. 4596 (Discussing CX0378 at 1 he states "[O]ur goal was to create a broad enough standard to be used by as many people as possible in the world, so it made sense that if that was our goal, we would have as many people attend the meeting from as many different, you know, applications of DRAMs as well as builders of DRAMs, everything surrounding DRAM, so that the final standard would have, you know, the consensus of the world, so that it would become widely adopted and used throughout the world.") and 4620-21 (Discussing CX2315, he states "[U]sually in the DRAM world, there is only one choice. You know, it's not a matter of what; it's a matter of when. So, users, they can plan their transition based on their own -- you know, their own internal decision-making process, plan their transition to meet their own business needs. The suppliers, they know making the investment up front is going to be realized, because they know the users will eventually move over. It may not all be at once, but over a period of time, they can count on the market slowly building up. In this particular case, there were two choices, and it was very unclear which way the world would go."); Rhoden, Tr. 298).

Rambus's Response to Finding No. 119:

The proposed finding is vague, incomplete, is not supported by the cited evidence and is contradicted by more specific evidence. It is also irrelevant if (as it is written) it is meant to apply only in the present tense. As an initial matter, the cited evidence does not support the second half of the proposed finding — the notion that standardization allows "suppliers to

leverage their design costs over a number of designs." To the contrary, there is significant evidence in the record that suppliers must incur significant design costs and other costs for each of the large number of design variations that they regularly produce. (Becker, Tr. 1150-51).

As to the first half of the proposed finding, it is supported by the cited testimony only in the present tense, and, even then, remains vague and incomplete. The proposed finding is vague as to whether JEDEC standards or *de facto* standards benefit suppliers, and if the latter, what degree of *de facto* standardization is necessary to accrue the benefit.

JEDEC standardization, on the other hand, is neither necessary nor sufficient to assure demand for a product. Standardization of SDRAM by JEDEC in 1993 did not assure that there would be demand for SDRAM devices (RRFF 113; MacWilliams, Tr. 4908-10), and Complaint Counsel present no evidence that SDRAM would ever have enjoyed demand from the market absent Intel's development of the PC100. Other products, such as Micron's Burst EDO, were standardized by JEDEC but were never in demand. (RRFF 507). Moreover, there are various standards that have received market demand absent JEDEC standardization, such as RLDRAM (Bechtolsheim, Tr. 5962) and Samsung's video RAM product (Prince, Tr. 9021).

In addition, the proposed finding is incomplete and inaccurate for other reasons insofar as it implies that standardization by itself assures demand. The record, for example shows that Intel's choices, not standardization, was a critical factor in demand. (*See* RPF 1543-1546, 1548). The record further shows that considerable marketing efforts and apparently illegal collusion and price fixing among the DRAM manufacturers were necessary to create demand for DDR among computer manufacturers like Dell and Compaq who had committed to support RDRAM instead. (RPF 1595-1599).

120. One way that standardization in the DRAM industry helps to assure a demand for new DRAM standards is by having an open standard setting process that involves all interested firms. (Macri Tr. 4596 (Discussing CX0378 at 1 he states "[O]ur goal was to create a broad enough standard to be used by as many people as possible in the world, so it made sense that if that was our goal, we would have as many people attend the meeting from as many different, you know, applications of DRAMs as well as builders of DRAMs, everything surrounding DRAM, so that the final standard would have, you know, the consensus of the world, so that it would become widely adopted and used throughout the world.")).

Rambus's Response to Finding No. 120:

The proposed finding is not supported by the evidence, is irrelevant if (as it is written) it applies only in the present tense, and is vague in its use of the phrase "open standard setting process" if that phrase is meant to mean anything other than a process that involves all interested firms. The Macri testimony cited by Complaint Counsel does not speak to "assur[ing] demand for new DRAM standards," but rather speaks only to the "goal" of the specific standard setting he directed with respect to one type of DRAM: DDR2. Macri's reference to the goal of having DDR2 "widely adopted and used throughout the world," is not evidence that standardization helped to "assure" anything and, in any event, refers to adoption and use by OEMs, not necessarily to demand among end users. Complaint Counsel has not offered evidence that having "an open standard setting process that involves all interested parties" changes in any way the demand for DRAM standards. In fact, as noted above, standardization at JEDEC does not assure demand. (RRFF 119).

121. Standardization benefits suppliers by allowing them to save resources on development. (Appleton, Tr. 6304 (standardized products benefit manufacturers because "we can look at all of that in a cumulation and save on resources . . . that would otherwise be required to come up with a device")).

Rambus's Response to Finding No. 121:

Rambus has no specific response.

H. A Variety of Factors Affect the Selection of Technology to be Included in DRAM Industry Standards.

1. Timeliness.

122. Standard setting at JEDEC is time-consuming. (Peisl, Tr. 4453 ("JEDEC is traditionally a very slowly moving consortium, and there's a reason for that, because there's so many companies involved, it's basically the whole industry that produces parts for the PC and the laptop and the server business, so to try to reach consensus at JEDEC, based on my experience, have been incredibly hard and tough."); Macri, Tr. 4607-608 ("The design process is long.")).

Rambus's Response to Finding No. 122:

Rambus has no specific response.

123. Industry participants consider time to market an important factor in developing standards. (Bechtelsheim, Tr. 5797 ("for example, if the synchronous DRAM did not have a completed spec, we would chose the previous memory technology. . . we would not be able to take advantage of the performance characteristics of the next-generation synchronous DRAM") and 5803 ("Sun itself did not have a strong view of what exact features the part should have as long as it would meet the cost, complexity and timely completion of the standard."); Rhoden, Tr. 299-300 ("You can't really wait until after you develop something and then decide to standardize it. You have to move in real time at the time that technology is being developed to create the standards. . . there is an urgency in the development of standards, because if you delay and if you wait too long, then sooner or later someone else will replace and do the job for you."); Heye Tr. 3747 ("anything that impacts time to market . . . would put us at a competitive disadvantage"); Macri, Tr. 4600 ("Time to market is extremely critical in this world"); CX0302 at 3 ("Delay is NOT a viable market option."); JX0027 at 12 ("Concern about JEDEC taking too long to produce a standard was mentioned as a reason not to pursue a standard within it.")).

Rambus's Response to Finding No. 123:

The proposed finding is vague, misleading and not supported by the evidence. First, it is unclear whether the proposed finding refers to the time that it takes to develop a standard or the time that it takes to bring a technology to market. The Bechtolsheim and Rhoden testimony as well as JX0027 (at 12), cited by Complaint Counsel, seem to support the former concept, while the Macri testimony seems to support the latter. The Heye testimony is taken completely out of its context; Mr. Heye was testifying regarding the effect Rambus's assertions of patent rights

against DDR and SDRAM had on "AMD's competitive position compared to Intel" (Heye, Tr. 3747), and had nothing to do with the time to develop a JEDEC standard or the time to develop a technology.

Moreover, the proposed finding is not supported by the cited evidence if it is meant to imply that the timeliness of a standard setting process would adversely impact business – as opposed to adversely impacting the success of the standard itself. Both the testimony of Bechtolsheim and Rhoden suggest that delay in the specification of a standard has little effect on business because of either older or different specifications that can be used. (Bechtolsheim, Tr. 5797) ("Q. And would delay in the specification of the memory design have the potential to impact adversely Sun's business in terms of its sales and its delivering to its customers? A. I wouldn't say it would impact Sun's business, but it would impact the decision which memory, specific memory component to use."); (Rhoden, Tr. 300) (if the standards setting organization delays for "too long, then sooner or later someone else will replace and do the job for you."). Complaint Counsel's cited exhibit, JX0027, fully supports this same conclusion. It is a set of slides entitled "Are Standards Worth the Effort" by Desi Rhoden, and suggests that standards must be made quickly to be useful, and that a standards organization must try to standardize ahead of technology, otherwise there would be other technology options waiting in the wings; "Look behind you If no one is following you are not leading." (CX302 at 15, slide labeled "Time to Market for Standards"). As even Complaint Counsel noted in citing this exhibit, JEDEC risked becoming inconsequential in the DRAM industry because its standardization process took too long (citing JX0027 at 12).

124. The potential impact on time to market is a factor that influences the decisions of

JEDEC members regarding what technologies to include in a standard. (CX2383 ("We are willing to make compromises if necessary to reach a quick resolution on a standard"); Bechtelsheim, Tr. 5794-95; Lee, Tr. 6635 (Although it preferred the SDRAM-Lite device, Micron "agreed in the interests of schedule to just go ahead and accept the full-feature proposal.") and 6683 ("Our preference was still not to have [strobes], but our action was to -- to go along with the committee in general with this compromise, because there was -- because of these differences of opinion, it was causing some delay in the standardization process.")).

Rambus's Response to Finding No. 124:

The proposed finding is vague and incomplete and unsupported by the cited testimony if it is intended to refer to a group deliberative process as opposed to the compromises or concessions made by individual members. The exhibits and testimony cited by Complaint Counsel suggest, at best, individual decisions by a handful of JEDEC participants based on timing concerns. None of the cited evidence purports to or does speak to the decision making of JEDEC as a whole.

2. Cost.

125. The potential cost of manufacturing and implementing a prospective technology is a factor that influences the decisions of whether a particular technology is included in a standard. Industry participants often are willing to forego performance advantages in exchange for lower cost products. (CX1708 at 2 (Richard Crisp writing "[Compaq] didn't particularly seem to care if the SDRAMs had 1 or two banks so long as they didn't cost any more than conventional DRAMs."); CX2383 ("Since we are very cost conscious we are willing to drop features that add too much cost or complexity"); CX0711 at 34 (Richard Crisp writing "They want cheap, cheap, cheap"); JX0027 at 13 ("The Committee noted they wanted highest performance and lowest price SDRAM."); CX2777 ("[T]he age old rule for DRAMs still apply. Customers will take as much performance as we can give them for absolutely no added cost over the previous technology. They will not pay extra for increased DRAM performance.")).

Rambus's Response to Finding No. 125:

The proposed finding, that industry participants "often" as opposed to "sometimes" forgo performance advantages in exchange for lower cost products, is not supported by the cited evidence. The evidence shows a great concern among DRAM customers that DRAM

performance was limiting computer system performance. (*See* RPF 35-40; RX 285A ("the DRAM interface has become more and more a problem for system developers")).

126. In order for a new memory technology to achieve high volume, it must be price competitive with the previous technology already in high volume. (MacWilliams, Tr. 4805 ("[W]e were concerned that with any new memory technology, for it to achieve high volume we need to be price competitive with the previous technology that was already in high volume."); CX2370 at 2 ("Must be within 5%"); CX0034 at 4 ("Dallas Task Group Conclusions Mr. Kelley summarized the presentations of 7.2 and 7.3 and presented some of the consensus views of the Dallas meeting: 1) To be cost effective sync DRAM must cost no more than 5% over conventional DRAMs for many applications"); CX0711 at 1 (Richard Crisp writes: "Desi added that if the SDRAM doesn't cost less than 5% more than standard DRAM they will not be used."); Tabrizi, Tr. 9082 - 83 ("For any product, if it doesn't become a low cost to manufacture, it never becomes reality. The issue is cost, cost, cost.")).

Rambus's Response to Finding No. 126:

The proposed finding is vague, incomplete and misleading, irrelevant to the extent (as it is written) it is meant to apply only to the present tense, and is not supported by the cited evidence if it is meant to apply to the past. It is unclear from the proposed finding what "price competitive" means in this context (*e.g.* what degree of increase is acceptable and whether the measure of comparison applies to just the cost of the DRAM or to the overall system level cost of achieving comparable performance levels using a new memory technology). The proposed finding is also unclear as to what is meant by "to achieve high volume.'' The proposed finding is incomplete because it fails to take into account the scale of potential performance advantages in new technology or to reflect potential system-wide savings that may offset any increase in DRAM cost.

In any event, the cited evidence does not support the proposed finding. The MacWilliams testimony is about Intel's "concerns," not about what it actually takes for memory technology to "achieve high volume." Mr. Rhoden's testimony and Mr. Crisp's hearsay recollection of

Mr. Rhoden's statement are directed only to the transition from "conventional" DRAMs to "sync DRAMs," not to all new memory technologies. The other cited evidence consists of simply generalized statements about cost concerns.

127. Changes in the DRAM industry tend to be incremental or evolutionary in nature, with only a handful of changes from standard to standard. (Rhoden, Tr. 408 ("[W]ithin JEDEC, we follow the process of evolutionary progress. So, there's some thousand things that go into the making of a particular DRAM, and we tend to change just a few, maybe a handful, maybe -- sometimes two or three, sometimes four or five, but that's the typical process, is we just evolve one to the next, to the next, with as little changes as possible, because it's much easier to bring the whole industry along when you make minor changes."); Sussman, Tr., 1362 ("The customer base does not really want to jump ahead to something new and different.").

Rambus's Response to Finding No. 127:

The proposed finding is incomplete, relies on an oversimplification, is irrelevant if (as it is written) it applies only in the present tense, is not supported by the cited evidence and ignores important information. As testimony from Complaint Counsel's economic expert points out, evolutionary and revolutionary are two points on a continuum, which requires comparison of the technologies and not just the terms themselves:

> "Q. Let me ask you about the final point, evolutionary versus revolutionary. As you use that term, have you formed a view as to whether the switch or transition from EDO to SDRAM would be described as evolutionary or revolutionary? A. I think evolutionary/revolutionary is a continuum. The switch from EDO to SDRAM was more revolutionary than it – than a switch from EDO to burst EDO would have been, but less revolutionary than a switch from EDO to RDRAM. So, was it revolutionary or evolutionary? Well, it was more revolutionary than going to the burst EDO, but not as revolutionary as other alternatives available at the

time."

(McAfee, Tr. 7691-92). Micron proposed this less revolutionary asynchronous burst EDO technology in early 1995 as a cheaper alternative to SDRAM (Appleton, Tr. 6315) and JEDEC standardized it (Williams, Tr. 873), yet it was not adopted by the DRAM industry. (RRFF 507). It follows that the DRAM industry does not necessarily favor the more incremental or evolutionary changes.

One reason that the DRAM industry does not necessarily favor more evolutionary changes is that, at times, customers and system architects require the more revolutionary change. For example, in explaining why Intel endorsed RDRAM instead of higher speed versions of SDRAM in 1996, MacWilliams testified: "We felt that we needed something revolutionary in the sense that to try to meet the performance goals we had was going to be hard, to try to meet the performance goals and get scalability beyond that was even harder, and the real chance that we had to do that was to pick a revolutionary technology." (MacWilliams, Tr. 4823). The same thing was true in the 1991-1993 timeframe when JEDEC decided to move away from asynchronous technology to SDRAM. (McAfee, Tr. 7387 ("There were quite a bit of debate at the time that JEDEC standardized SDRAM about whether to move to synchronous or stay with asynchronous designs. Asynchronous designs had evolutionary advantages over synchronous designs, but at that time JEDEC made the determination to move to asynchronous – to synchronous – move away from asynchronous to synchronous designs."); Rapp, Tr. 10103-04).

Mr. Rhoden's testimony, cited by Complaint Counsel, does not support the proposed finding, because it speaks only of the standard setting process of JEDEC, not of the broader issue of "changes in the DRAM industry." Mr. Sussman's testimony relates to purported customer

desires but not about how those desires do or do not influence "changes in the DRAM industry."

128. Evolutionary, as opposed to revolutionary, changes serve to minimize cost, and to ease the introduction of new DRAM standards. Bechtelsheim Tr., 5835 ("Because if it's not broken, we don't fix it. In other words, unless there's an overarching reason to make a change, people tend to do the same as they did previously....Well, it takes time to verify, validate, prove new memory components at the system level, which is quite extensive. So yes, there's a significant cost in qualifying new types of memories."); Appleton Tr., 6297 ("Sure, Micron's preference, of course, is to go evolutionary, because it's more stable for us, it's less costly for us, and we can more easily plan for it.... Well, customers in general would prefer to have an evolutionary process as well. It -- the changes don't just affect us, they affect the people we are selling the product to, and when you start talking about reliability of the device, reliability of the technology platform, reliability of the supply, it's also a much easier transition for them."); Peisl, Tr. 4378 ("JEDEC wanted to do an evolutionary step going from SDR to DDR, evolutionary in order to keep the costs down in the industry because it affected much more than the DRAM design, . . .")).

Rambus's Response to Finding No. 128:

The proposed finding is misleading, overly simplistic and not supported by the evidence. The proposed finding is misleading and overly simplistic because the terms evolutionary and revolutionary have indefinite meanings, as discussed by Complaint Counsel's expert. (*See* RRFF 127). The testimony cited by Complaint Counsel speaks to a general preference for keeping costs down. In some cases, however, more significant changes may be necessary to meet the computing needs of the computer industry and those changes may minimize the total system-wide cost-per-bit and ease the introduction of new standards in the long run. Complaint Counsel have offered no evidence that what they call the evolutionary transition to SDRAM and from SDRAM to DDR resulted in lower costs or easier transitions than had the DRAM industry adopted a more revolutionary one, such as RDRAM, from the start. Complaint Counsel have made no effort to reconcile this proposed finding with the facts that the JEDEC chose to transition from asynchronous to synchronous DRAM in 1991-1993 and that the DRAM industry

chose to shift from Fast Page Mode (FPM) to SDRAM in 1995-1996, despite the existence of more "evolutionary" alternatives.

3. Need.

129. A technology might not be standardized if the technology's performance improvements are ahead of their time from the standpoint of what customers demand. For example, JEDEC began considering a form of dual-edged clocking in the early 1990s but did not adopt it until the DDR standard because the industry did not require the additional performance that dual-edged clocking could provide. (Rhoden, Tr. 462-63 ("[W]e talked about dual edge clocking, and at the time . . . we actually decided to postpone implementation of that until a later date. . . Many of those wound up in DDR ultimately. . .We said, well, since we don't need it at this time, perhaps we don't need to expend the effort."); Kelley, Tr. 2515 ("[W]e decided as a group that we could meet the requirements of the high-performance systems for the next-generation DRAM without needing a double-edged clock for that doubling of the performance and that we would reconsider the double-edged feature in the next generation."); CX0742 at 4 ("The implication here is that customers are willing to leave performance on the table in exchange for having lower cost systems.")).

Rambus's Response to Finding No. 129:

The proposed finding is overbroad, incomplete, vague, and contrary to the evidence. As to the first sentence, "ahead of their time" and "what customers demand" are vague – it is unclear, for example, whether this is intended to include Intel's demands and whether "ahead of its time" accounts for the need of memory technologies to have "headroom" permitting further system-wide improvements. (*See, e.g.*, Polzin, Tr. 4033-34). The second sentence is misleading and not supported by the weight of the evidence in suggesting that dual edge clocking, as incorporated in the DDR SDRAM standard, was discussed in the early 1990s. (*See* RRFF 578).

4. Uncertainty.

130. At the time that the technologies are selected for incorporation into a standard, not all of the facts are known. Industry participants must make decisions on what technologies to include in the standard based on predictions with respect to the likely future performance, implementation difficulties and manufacturing costs. (Wagner, Tr. 3841 ("The decision was made to support both SDR SDRAM and DDR SDRAM so that if DDR didn't show up, we still

had a fallback plan and could still ship our product on the market"); MacWilliams, Tr. 4884 ("Because server design cycles are longer than desktop, [OEM's] were going to make some decisions in terms of what they were going to build for a much longer time frame."); Gross, Tr. 2296 (chose DDR because it "appeared to us to be the next mainstream high volume memory technology.")).

Rambus's Response to Finding No. 130:

The proposed finding is misleading, incomplete and not supported by the cited evidence. The Wagner, MacWilliams and Gross testimony all speak to the choice of which type of DRAM to use in their products (graphics chips, servers and computers respectively), and not to any purported uncertainty regarding facts relating to technologies to be incorporated into a JEDEC standard. Ms. Gross does not speak to uncertainties at all in the quoted passage. The Wagner and MacWilliams testimony suggest that the decisions of their companies were each based on the perceived supply and price (cost to purchase) of RDRAM, and nowhere suggest these decisions were based on likely future performance, implementation difficulties or costs of DRAM manufacturers to manufacture. Indeed, Wagner and MacWilliams each suggest that the choice of nVidia and server OEMs to go with DDR SDRAM over RDRAM was based on perceived supply problems. (Wagner, Tr. 3841-42; MacWilliams 4883).

131. The predictions of industry participants are not always correct. For example, when Intel first evaluated DDR SDRAM in 1996 it did not appear to Intel employees that it would work. (MacWilliams, Tr. 4881 ("so when we looked at it back in the 1996 time frame, it didn't look like it would work ...")). Even in 1999, when Intel began to consider using DDR for use in servers, it was believed at Intel that DDR could not be used in main memory for personal computer systems. (MacWilliams, Tr. 4881-82). However, by September of 2001, Intel was working to deliver robust DDR platforms for all Intel architecture CPUs. (RX-1761 at 16).

Rambus's Response to Finding No. 131:

Rambus agrees that companies are not always correct in their predictions. The remainder of the proposed finding is misleading and not supported by the evidence. Complaint Counsel

have selectively quoted from the MacWilliams testimony to suggest that Intel's decisions not to adopt DDR SDRAM in 1996 (for computers) and in 1999 (for servers) were incorrect and were later corrected in 2001. With this proposed finding, Complaint Counsel ask this Court to remove those decisions from their historical context and judge them by the DDR SDRAM standard as it existed years later. On the same page twice cited by Complaint Counsel, MacWilliams testified: "you know, you can make most anything work if you spend enough energy and time on it. So if we fast-forward in time to more of the 1998-1999 time frame, the industry had done a lot of work on DDR addressing the issues we saw back in 1996."

132. Paragraphs 132 - 199 are unused.

II. JEDEC Is An Industry Organization for Developing Consensus-Based Standards.

A. The Founding and History of JEDEC.

200. The formal name of JEDEC is the "JEDEC Solid State Technology Association." (J. Kelly, Tr. 1750-51).

Rambus's Response to Finding No. 200:

This finding is incomplete and potentially misleading because it does not reflect the changes in JEDEC's status over time. The cited testimony by EIA General Counsel John Kelly appears to refer to the present. According to the EIA's 1990 Annual Report, however, "JEDEC" at that time stood for "Joint Electron Devices Engineering Council," which was then a "subdivision" of the EIA's Solid State Products Division, which was itself a division of the EIA's Components Group. (CX 3092 at 14, 27). According to a May 1, 2000 letter by Mr. Kelly, JEDEC did not become an independent "association" until the year 2000. (CX 419 at 1). Proposed Findings that reflect these changes over time can be found at RPF 108, 114-115.

201. JEDEC was founded in 1958 and originally named the "Joint Electron Device Engineering Council." (CX0302 at 10; *see also* J. Kelly, Tr. 1773-74 ("JEDEC has been active within an EIA organization under the name JEDEC since approximately 1958, and under other names with slightly different functions for a number of years prior to that, probably dating back to the 1940s.")).

Rambus's Response to Finding No. 201:

Rambus has no specific response.

202. Between 1991 and 1996, JEDEC was an entity within the Electronic Industries Association Engineering Department. (J. Kelly, Tr. 2075). EIA is alliance of organizations engaged in the electronics industry in the United States. (J. Kelly, Tr. 1750 ("EIA is a broad-based association that represents the electronics industry in the United States, and it engages in a variety of different activities in support of that industry."); CX0302 at 28).

Rambus's Response to Finding No. 202:

The word "entity" in the first sentence of this proposed finding misstates the cited testimony and is misleading if it is intended to suggest that JEDEC was an independent organization or "entity" in the early or mid-1990's. The cited testimony by EIA General Counsel John Kelly uses the word "activity" rather than "entity:"

> "Q. And of course between '91 and '96, at least, focusing on that time period, JEDEC was an activity within the EIA engineering department?
>
> A. Yes.
>
> Q. And it didn't enter into its own contracts on its own; right, during that time period?
>
> A. No, it did not."

(Kelly, Tr. 2075). (*See also* Rhoden, Tr. 289: Prior to 1998, "JEDEC was a subpart" of the EIA that "existed inside the engineering department" of the EIA). *See* RPF 108, 114-115.

203. In 1998, EIA changed its name to the Electronic Industries Alliance. (CX0302 at 11). In 1998, JEDEC became a separate division of EIA. (CX0302 at 11).

Rambus's Response to Finding No. 203:

Rambus has no specific response.

204. In 1999, JEDEC became independently incorporated. (CX0302 at 11). Both EIA and JEDEC are headquartered in Arlington, Virginia. (J. Kelly, Tr. 1751).

Rambus's Response to Finding No. 204:

Rambus has no specific response.

B. The Purpose of JEDEC.

205. JEDEC develops standards for semiconductors and solid state products. (J. Kelly, Tr. 1751 ("JEDEC is focused on standard-setting in support of the industry sector that it represents, which is semiconductors and solid state products.")).

Rambus's Response to Finding No. 205:

The cited testimony is irrelevant because it refers to the *current* focus of JEDEC. (J. Kelly, Tr. 1751). Rambus attended its last JEDEC meeting in December 1995, almost eight years ago. According to a contemporaneous document (JEDEC Manual of Organization and Procedure 21-H), JEDEC was in the late 1980's and early 1990's an "engineering standardization body for solid state products in the United States." (RX 1211 at 4).

206. The purpose of JEDEC is to create consensus-based standards. (CX2767 at 1 ("JEDEC exists because of an industry need for standardization."); CX0035 at 14-15 ("The work we do on the JC-42.3 DRAM committee continues to approach a design by committee."); Becker, Tr. 1152 (JEDEC "tries to build a consensus across the industry to produce a specification or an industry standard [to which] everybody manufactures and conforms their products."); J. Kelly, Tr. 1784 ("In every instance, our standards have to be based upon a consensus of the formulating committee and a consensus of the board . . . formerly the JEDEC Council, indicating that they agree with the content of the. . . standard"); Landgraf, Tr. 1685 ("JEDEC is a standardization body that . . . brings together memory -- or electronic component manufacturers as well as customers using those devices to formulate common standards that can be used by manufacturers and be understood by the users."); Polzin, Tr. 3946-47 ("JEDEC was the natural forum and process for resolving the numerous differences."); Lee, Tr. 6682-84 (discussing differing views on using DLL in DDR SDRAM)).

Rambus's Response to Finding No. 206:

This finding is irrelevant because it refers to JEDEC's current purpose, instead of JEDEC's purpose in the early 1990's when Rambus was a member. As an example, the first-cited exhibit, CX 2767, is a July 2000 e-mail by Desi Rhoden that was created in connection with a debate over the relative merits of RDRAM and DDR SDRAM devices. At the time, Mr. Rhoden was employed by AMI2, a consortium of DRAM manufacturers devoted to the promotion of DDR SDRAM devices. (Rhoden, Tr. 697-704). The e-mail thus has no relevance,

is suspect given the bias of its author, and should be given no weight.

This proposed finding is also misleading if it is intended to suggest that the "consensus" it refers to extends beyond DRAM manufacturers. The evidence demonstrates that DRAM manufacturers believed by the late 1990's, if not earlier, that JEDEC had become "OUR organization and will approve whatever we decide to approve." (RX 1424 at 1) (capitalization in original). Even the e-mail by Mr. Rhoden that Complaint Counsel cite (CX 2767) acknowledges that the DDR SDRAM standardization process was influenced by "a high level of cooperation *between the suppliers* within AMI, Inc. . . ." (CX 2767 at 3) (emphasis added). Mr. Rhoden made the same point in January and February 1999 e-mails urging the DRAM manufacturers to establish AMI2. In a January 18, 1999 e-mail, for example, he stated that AMI2 could "co-ordinate" and "lead" the JEDEC process by "maintain[ing] active leadership role in memory and related committees etc." (RX 1373 at 2, 3, 5). In his February 15, 1999 follow-up e-mail, Mr. Rhoden pointed out that the DRAM manufacturers "are stronger united together than we are individually" and stated that "[s]tandards leadership is one of the most important activities [AMI2] can be involved in . . . ." (CX 2729 at 3, 4). At the time, Mr. Rhoden was the Chairman of the Board of JEDEC *and* the Chairman of the JC 42 committee. (Rhoden, Tr. 285-88).

The question of whether JEDEC - and in particular the JC 42 committee - is or is not driven primarily by the interests of the DRAM manufacturers is important to the antitrust issues raised in this case. JEDEC's own leadership and EIA's General Counsel each agreed in the early 1990's that meeting of DRAM manufacturers *outside* of JEDEC to discuss standards under development within JEDEC were antithetical to JEDEC's true purpose and "probably" illegal. (JX 10 at 4; RX 575 at 17). As JEDEC Council Chairman Gordon Kelley stated in 1995,

"[m]ultiple company meetings to discuss JEDEC items is probably against the laws of the United States" and "exposes participating companies to legal action." (RX 575 at 17).

In sum, if a finding similar to that proposed by Complaint Counsel is needed, it should be phrased to reflect the weight of the evidence, as follows: "The evidence introduced at trial showed that JEDEC's purpose is to ensure that its standards primarily reflect the interests of DRAM manufacturers."

207. JEDEC standards ensure uniformity and reliability in products. (CX0419 ("uniform terms and definitions, common packages [and] interchangeability of logic [and] memory" to the industry); J. Kelly, Tr. 1791; Bechtelsheim, Tr. 5781 ("Well, the purpose was to develop standards that could be used by all memory manufacturers to manufacture devices that had the same functionality and thus could be used as a multivendor, multistandard device from multiple manufacturers."); Polzin, Tr. 3972 (JEDEC "defines standards that multiple manufacturers can design to have interoperable parts."); Calvin, Tr. 994 ("the expectation is when you buy something in the industry and you plug it into your system, that it's supposed to work. And so that's the purpose of the standardization body to get agreement across the industry members in terms of what the aspects of that standard are going to be.")).

Rambus's Response to Finding No. 207:

This proposed finding is irrelevant because it – and the cited testimony – speak in the present tense. The JEDEC standardization process during the time that Rambus was a member did not "ensure uniformity and reliability in products," as the proposed finding suggests. In particular, it is undisputed that the 1993 publication of JEDEC's SDRAM standard did not ensure interoperability. (MacWilliams, Tr. 4908). As a result, SDRAM devices built by one manufacturer were often not "plug-compatible" or interchangeable with those built by a different manufacturer. (Id.). As a result, Intel, rather than JEDEC, developed the new "PC SDRAM" standard in 1996. (MacWilliams, Tr. 4907-09). As the 1996 PC SDRAM standard stated, it was designed to be a "new Synchronous DRAM specification" that would, unlike the JEDEC

standard, result in "a 'fully compatible" device among all vendor designed parts." (RX 2103-14 at 9).

208. JEDEC standards are procompetitive because they lower costs and ensure broader participation in the market. (CX0419 ("What JEDEC standards mean to the industry is lower price and wider supply, consistent quality and reliability, uniform terms and definitions, common packages, interchangeability of logic, memory, etc."); J. Kelly, Tr. 1790-91 ("Because it is an open standard, any company wishing to comply can and can develop product to the standards, and that tends to mean more sources of supply, and because there's more competition in the manufacture of the product, it tends over time to drive the price down for the benefit of the supply chain as wee as OEMs and end user and in many cases consumers."); Polzin Tr. 3973 ("JEDEC allows manufacturers to all design to a common standard and basically enables the commodity marketplace. Everybody is designing compatible parts at the lowest possible cost competing on manufacturing cost.")).

Rambus's Response to Finding No. 208:

This proposed finding is irrelevant because it - and the cited testimony - all speak in the present tense. Moreover, as discussed above in response to Proposed Findings Nos. 206 and 207, there is substantial evidence that JEDEC standardization did *not* (at least for the SDRAM standard) ensure "interchangeability" or "uniform terms and definitions," and there is substantial evidence that at least in and after 1999, the JEDEC process was being driven not by a broad cross-section of industry participants but by DRAM manufacturers, acting together to influence JEDEC decisions. (RX 2103-14 at 9; CX 2767 at 3; RX 1424 at 1; CX 2729 at 3, 4; RX 1373 at 1, 3, 5). In addition, there is substantial evidence that the JEDEC standardization process was not pro-competitive while Rambus was a member. In April 1992, for example, a few months after Rambus joined JEDEC, JC 42.3 subcommittee chair Gordon Kelley co-authored an "assessment" of Rambus along with two other IBM employees. (RX 279 at 1). Kelley's "Rambus Assessment" stated that IBM's business interests would be best served if Rambus's RDRAM device did *not* become standardized at JEDEC. As Kelley explained, "[i]f Rambus

fails to become standard, then it is business as usual for BTV [the acronym for IBM's Burlington, Vermont operations] and the SDRAM has a significant chance of being standard." (RX 279 at 7).

Despite the obvious conflict of interest presented by Kelley's "Rambus Assessment," he made a unilateral decision two weeks later, at the May 1992 JC 42.3 meeting, to bar Rambus from even *presenting* its technology for standardization at JEDEC. (Kelley, Tr. 2649). Kelley testified that he barred Rambus from presenting its technology for standardization because it would not agree, *in advance* of presenting its technology, to license its related intellectual property on reasonable and non-discriminatory terms. (Kelley, Tr. 2649-50). He also testified that he understood in May of 1992 that it was EIA's policy, for legal reasons, that a member did *not* have to provide licensing assurances prior to *presenting* its technology for standardization. (Kelley, Tr. 2652). (See also CX 355 at 6-7 (ANSI Patent Policy Guidelines: "the patent holder is only required to provide assurances called for by the Patent Policy prior to the *final approval* of the proposed standard . . . .") (emphasis added)). Mr. Kelley testified that he believed, despite the EIA and ANSI policies to the contrary, that he had the right to bar Rambus from presenting its technologies because of a "hand vote" at a JC 42.3 meeting in May 1991 that resulted in a new, unwritten requirement that JEDEC presenters agree in advance to licensing restrictions. (Kelley, Tr. 2653-56).

There was no written evidence presented at trial of any such "hand vote," and the evidence shows that the requirements unilaterally imposed on Rambus by Mr. Kelley were never enforced to prevent *any* other JEDEC member from presenting its technology for standardization. (Kelley, Tr. 2657-58).

Putting to one side the question of whether the "hand vote" occurred, the fact that Mr. Kelley had a clear and undisclosed conflict of interest at the time that he barred Rambus from presenting its technology, and the evidence cited in reply to findings 206 and 207 above, demonstrate that Complaint Counsel's proposed finding that "JEDEC standards are procompetitive" is not supported by the weight of the evidence.

C. How JEDEC Is Organized.

1. Membership.

209. A company becomes a member of both JEDEC and EIA by completing and submitting one application and paying dues. (CX0601 (Rambus application); J. Kelly, Tr. 1801 ("one becomes a member of JEDEC by filling out a membership application and paying dues."); 1801-02 (Since at least 1990, when one becomes a member of JEDEC, one automatically becomes a member of EIA.); Rhoden, Tr. 294-95 ("Companies become a member of JEDEC by paying dues."); CX0208 at 7 ("Eligible organizations can become members of JEDEC by joining the EIA Solid State Products Division or by joining JEDEC directly," and paying annual dues.)).

Rambus's Response to Finding No. 209:

For this finding to be accurate and complete, it should reflect that during the time Rambus was a JEDEC member, dues were paid to EIA, not JEDEC, (CX 602 at 6, 7), and that there was no contractual relationship between JEDEC and Rambus. (Kelly, Tr. 2075).

210. During the 1990s, JEDEC had approximately 250 member companies who sent approximately 1800 individuals to participate in approximately 50 committees. (J. Kelly, Tr. 1774-75).

Rambus's Response to Finding No. 210:

Rambus has no specific response.

211. JEDEC membership is open to broad array of companies and individuals. (CX0208 at 6 ("[a]ny company, organization, or individual doing business in the United States that itself or through a related entity manufactures electronic equipment or electronics-related products, or provides electronics or electronics-related services, shall be eligible for membership" in JEDEC.); CX0203A at 4 (members can include "any and all companies having a relevant

commercial interest within the respective jurisdiction of the committees.")).

Rambus's Response to Finding No. 211:

This finding is unclear as to the time period it refers to. In 1992, when Rambus joined JEDEC, the membership application stated that:

> "JEDEC Committee membership is limited to companies and independent entities of companies that (1) manufacture solid state products, or provide related services or equipment, and (2) participate in the United States market."

(CX 602 at 2). This language should be used in lieu of the proposed finding.

212. JEDEC members represent a broad cross-section of the semiconductor supply chain. (CX0302 at 8 (members include chipset companies like Ali and VIA, microprocessor companies like AMD and Intel, packaging companies like Amkor, computer memory module companies like Celestica, memory suppliers like Elpida, Hynix, Samsung, Micron and Infineon, OEM companies like HP and IBM, networking companies like Lucent and cell phone companies like Motorola.); JX0028 at 1-3 (list of members attending and not attending); Rhoden, Tr. 293.).

Rambus's Response to Finding No. 212:

This proposed finding is irrelevant because it is framed in the present tense. CX 302, upon which this finding primarily relies, was not prepared until 2002. (Rhoden, Tr. 293).

213. JEDEC's membership includes companies from around the world. (Rhoden, Tr. 294 (noting companies from Korea, Germany, Taiwan and Japan companies.); CX0302 at 8.).

Rambus's Response to Finding No. 213:

This proposed finding is irrelevant because it is framed in the present tense. CX 302, upon which this finding primarily relies, was not prepared until 2002. (Rhoden, Tr. 293).

214. Membership entitles companies to attend meetings, receive minutes, vote, and receive copies of standards and other publications. (J. Kelly, Tr. 1805-06 (JEDEC "members can attend any meeting. They can receive meeting notices. They receive copies of minutes of

meetings. They have an opportunity to vote on a one-company/one-vote basis. They have the right to . . .receive copies obviously of standards and other publications that are distributed generally by JEDEC to members")).

Rambus's Response to Finding No. 214:

The proposed finding is incomplete because it omits the fact that companies not interested in the outcome of a particular issue were encouraged not to vote. (Rhoden, Tr. 304: ". . . we encourage you to abstain if you do not have any interest.").

215. During the early and mid-1990's, JEDEC minutes were regularly circulated to all members. (Crisp, Tr. 3139 ("Q. Now, Mr. Crisp, JEDEC regularly circulated minutes from the meetings. Isn't that right? A. I think that's correct.")).

Rambus's Response to Finding No. 215:

The minutes were also available in the early 1990's to non-members, with the possible exception of Russian companies. (Kelley, Tr. 2622-23).

216. Attendance by non-members is limited to one meeting. (J. Kelly, Tr. 1805-06).

Rambus's Response to Finding No. 216:

The cited testimony is misleading and incomplete because it omits the testimony by Mr. Kelly that non-members can attend *more* than one meeting simply by paying a "non-member participation fee." (Kelly, Tr. 1806). The cited testimony is also inconsistent with JEDEC manual 21-H, which gives committee chairs discretion to allow guests to attend meetings: "[a]ll JEDEC Committee meetings are open to members, their designated alternatives, and guests invited by the Committee. Others may attend meetings only with prior approval of the Chairman." (RX 1211 at 10).

217. A member can withdraw from JEDEC either by letter or by not paying dues for an extended period of time. (J. Kelly, Tr. 1808 ("A company can withdraw from JEDEC by either submitting a letter indicating their wish, their desire to withdraw, or by not paying their annual

dues."), 1808-09 ("we do not drop member companies for nonpayment of dues until around September 1, and the reason for that is that the nonpayment of dues is equivocal . . ., and it's not at all unusual for member companies to be six months late in paying their dues. We don't ever drop them without knowing to a reasonable degree of certainty that they don't intend to pay their dues.")).

Rambus's Response to Finding No. 217:

Rambus has no specific response to this finding, assuming that it is limited to present circumstances, as it suggests. Rambus also notes that contrary to the implications of this e-mail, its exit from JEDEC was well known at JEDEC by March 1996 even though it did not send a formal notice until June 1996. (RX 695 at 1 - 3/22/96 e-mail by Texas Instruments' JEDEC representative, Bill Vogley: {

} **(in camera)**.

218. Members who are late paying their dues still are entitled to attend meetings, vote, and receive minutes. (J. Kelly, Tr. 1809-10).

Rambus's Response to Finding No. 218:

Rambus has no specific response to this finding, assuming that it is limited to present day circumstances, as it indicates.

2. Management.

219. Prior to 2000, the JEDEC Council was the governing body of JEDEC. (J. Kelly, Tr. 1768). Today, the JEDEC board of directors is the governing body of JEDEC. (J. Kelly, Tr. 1770).

Rambus's Response to Finding No. 219:

The cited testimony is contradicted (as to the relevant dates) by JEDEC manual 21-K, which bears a February 2, 1999 publication date and which refers to the "JEDEC Board of

Directors" rather than the "JEDEC Council." (CX 214 at 1, 14). In addition, at least prior to 1998, the JEDEC Council could not unilaterally set or change policies without approval of the EIA Engineering Department Executive Council ("EDEC"). (Kelly, Tr. 2105).

220. The JEDEC board of directors consists of approximately 22-27 people. (Rhoden, Tr. 287). The members of the JEDEC board of directors are representatives of the DRAM industry, from electronics and semiconductors companies. (Rhoden, Tr. 287).

Rambus's Response to Finding No. 220:

Rambus has no specific response.

221. The chairman of the board of directors is elected by JEDEC members. (Rhoden, Tr. 286). The JEDEC chairman is not compensated by JEDEC. (Rhoden, Tr. 287-88). The JEDEC chairman is responsible for "the business aspect of JEDEC, trying to make sure that we [JEDEC] have office space, staff, relationships with other organizations, and to make sure that we take care of the business aspects of the corporation itself." (Rhoden, Tr. 286-87).

Rambus's Response to Finding No. 221:

To be complete and accurate, this finding should state that the current JEDEC chairman has, for most of the time in that position, been compensated by a private consortium called AMI2 whose board is comprised entirely of DRAM manufactures. As one of JEDEC board members observed in August 2000, at that time Mr. Rhoden's "whole company and existence depends upon the success of DDR," then in competition with Rambus's RDRAM. (RX 1692 at 1).

222. Desi Rhoden is the current Chairman of the JEDEC board of directors. (Rhoden, Tr. 283).

Rambus's Response to Finding No. 222:

Rambus has no specific response.

223. The president of JEDEC is responsible for supervising the JEDEC staff, managing the JEDEC budget, and implementing the policy directives of the JEDEC board of directors. (J. Kelly, Tr. 1754). Prior to 2000, the JEDEC president did not have any supervisory responsibilities for JEDEC staff. (J. Kelly, Tr. 1754-55).

Rambus's Response to Finding No. 223:

Rambus has no specific response, expect to note that there is no evidence that the position of JEDEC President existed during the time Rambus was a JEDEC member.

224. John Kelly is the president of JEDEC. (J. Kelly, Tr. 1750-51).

Rambus's Response to Finding No. 224:

Rambus has no specific response, expect to note that there is no evidence that the position of JEDEC President existed during the time Rambus was a JEDEC member.

225. The EIA general counsel is "the legal counsel for all of the operating units within EIA, including JEDEC." (J. Kelly, Tr. 1754).

Rambus's Response to Finding No. 225:

Rambus has no specific response.

226. The EIA general counsel is the person responsible for interpreting EIA rules and the JEDEC rules, including the JEDEC patent policy. (J. Kelly, Tr. 1813-14 ("a number of questions do arise from time to time about the patent policy of EIA and JEDEC, because that is part of -- and a very important part -- of the ground rules for the engineering function."), 1939 ("Q: . . . when either the staff or the committee leadership have interpreted EIA or JEDEC rules differently than you, whose interpretation controls? A: Mine does."); Sussman, Tr. 1348 ("Q. If a participant at JEDEC had raised any questions, who would you refer that person to for more precise answers on the patent policy? A. JEDEC legal counsel. None of us are lawyers.")). *Cf.* (J. Kelly, Tr. 2057-58 (Rambus never contacted EIA Legal Counsel concerning questions of interpreting the patent policy)).

Rambus's Response to Finding No. 226:

Rambus has no specific response, except to note that as Mr. Kelly acknowledged, while he may interpret the policies and rules, the EIA's Engineering Department Executive Council ("EDEC") establishes what the policies and rules are. (Kelly, Tr. 2078).

227. John Kelly has been the General Counsel of EIA since 1990. (J. Kelly, Tr. 1754).

Rambus's Response to Finding No. 227:

Rambus has no specific response.

228. Today, JEDEC employs a staff of ten persons to facilitate the meetings of JEDEC committees. (J. Kelly, Tr. 1792-93). During the early to mid-1990s, the size of JEDEC's staff was "considerably" smaller than the current size. (J. Kelly, Tr. 1795).

Rambus's Response to Finding No. 228:

Rambus has no specific response.

229. JEDEC's current budget totals $2.2 million, approximately half of which covers salaries. (J. Kelly, Tr. 1800).

Rambus's Response to Finding No. 229:

Rambus has no specific response.

3. Committees and Subcommittees.

230. JEDEC is organized into committees and subcommittees. (Landgraf, Tr. 1687 ("below the council are a series of committees which [the council] approve to exist")). Each committee or subcommittee has a chairman. (J. Kelly, Tr. 1794 ("The members of each committee and subcommittee elect from their membership a chairman and a vice-chairman.")).

Rambus's Response to Finding No. 230:

Rambus has no specific response.

231. The JC-42 committee is concerned with developing standards for the memory products. (Williams, Tr. 765-66 (The JC-42.3 membership consists of "[a]lmost all of the DRAM memory companies, SRAM memory companies, logic companies, customers of memory, as well as interconnect companies, such as socket manufacturers," and testing companies.); Rhoden, Tr. 288 (JC 42 is the committee responsible for developing standards relating to memory devices.)).

Rambus's Response to Finding No. 231:

Rambus has no specific response.

232. The JC-42 chairman is responsible for coordinating all the activities in the JC-42 committee and subcommittees, including the scheduling of meetings. (Rhoden, Tr. 288).

Rambus's Response to Finding No. 232:

Rambus has no specific response.

233. The JC-42 committee had several subcommittees focusing on particular specialized subject matters. (J. Kelly, Tr. 1769; Rhoden, Tr. 285 (JC-42 included subcommittees devoted to DRAM (42.3), SRAM (42.2), memory modules (42.5), flash memory and other types of programmable devices)).

Rambus's Response to Finding No. 233:

This finding is vague as to the time to which it refers.

234. JEDEC's JC-42.3 committee develops the predominant standards relating to dynamic random memory ("DRAM") products. (Peisl, Tr. 4381 (JEDEC subcommittee JC 42.3 "standardizes the DRAM interfaces and the packages of DRAM generations."); Rhoden, Tr. 283-84 ("JEDEC is the place where industry standards are set for the DRAM" industry.); Krashinsky, Tr. 2773 (JEDEC sets memory standards for the industry); (CX2107 at 23 (Oh FTC Dep) ("JEDEC is the committee which standardize all the standard products in the market."); MacWilliams, Tr. 4910-11 (Intel PC100 specification included programmable CAS latency and programmable burst length because features were already in the JEDEC specification.)).

Rambus's Response to Finding No. 234:

This finding is unobjectionable if the word "predominant" is excised. It is simply not true that the standards developed by the JC 42.3 subcommittee while Rambus was a member became "predominant," nor does the cited testimony offer support for such a finding. JEDEC's SDRAM standard, published in 1993, did not ensure interoperability and resulted in the manufacture of incompatible devices. (MacWilliams, Tr. 4908). Only after Intel developed the new "PC SDRAM" standard in 1996 did the SDRAM device win marketplace acceptance. *See* RPF 1518-19.

235. In late 1991, approximately 40-50 companies were represented on the JC-42.3 committee. (Rhoden, Tr. 340-41; JX0010 at 1-2 (minutes listing approximately 42 companies as members of JC-42.3)).

Rambus's Response to Finding No. 235:

Rambus has no specific response.

236. The JC-42 committee and its related subcommittees typically meet at least four times per year. (Rhoden, Tr. 340 ("there are four regular meetings, once a quarter, and depending upon the workload for the committee, the amount of work that we have to do, we often times hold special committee meetings in between meetings, and so somewhere between four and eight. In times of high activity, we will have eight meetings per year and almost always have five.")).

Rambus's Response to Finding No. 236:

Rambus has no specific response.

237. Minutes of JC-42 committee and its subcommittees are prepared by, Ken McGhee, a staff person. (Rhoden, Tr. 327).

Rambus's Response to Finding No. 237:

Mr. Rhoden also testified that there is a "review process" that goes on before the minutes are made official. (Rhoden, Tr. 591).

238. The minutes of JC-42 and its subcommittees record the key decisions that are made during the standard development process, including motions and votes. (Rhoden, Tr. 327-28).

Rambus's Response to Finding No. 238:

To be accurate and complete, this finding should reflect Mr. Rhoden's subsequent clarification that the minutes were intended to be a chronological statement of the events and occurrences in the meeting, although they were not "a transcript." (Rhoden, Tr. 590-91).

D. How JEDEC Standards Are Made.

239. The standard development process begins with discussions among the participants at a JEDEC meeting concerning subjects that members may feel should be considered for standards. (Rhoden, Tr. 406-07).

Rambus's Response to Finding No. 239:

The cited testimony does not support this proposed finding, and the other evidence submitted at trial does not support the proposition that JEDEC representatives come up with ideas at meetings that then become standards. For these reasons, Complaint Counsel's proposed finding no. 240 should be used in lieu of finding no. 239.

240. Typically, standardization at JEDEC involves a series of presentations. (CX0302 at 23; Williams, Tr. 772-73 ("[I]n order to get a point or feature to ballot, it required a first showing, which would happen at one meeting. You would then go to a second showing at the second meeting. You could then at the end of the second showing request that the item or the ballot -- the item be sent to ballot. The ballots would be issued. They would count the ballots at the third showing."); Rhoden, Tr. 406-07 ("Our procedure that we follow inside of the JC-42 committee is we typically have a first presentation, then followed by -- after some review, follow that by a second presentation.")).

Rambus's Response to Finding No. 240:

Rambus has no specific response.

241. Standardization proposals typically receive an item number after the first presentation. (Calvin, Tr. 1025).

Rambus's Response to Finding No. 241:

Rambus has no specific response.

242. A presentation might generate other proposals to solve the same problem. (Rhoden, Tr. 406-07 ("When someone has an idea that they'd like to bring into the committee, they will bring in a presentation, and then we will make presentations, and based on the presentations . . . the committee may generate other discussions and may also generate the development of other presentations for that matter."); CX0711 at 2 (Crisp of Rambus discussing corrupting SynchGDram proposals: "Desi made a comment at the end of the meeting that was in effect request for some of the folks to withdraw their proposals. He reminded folks that there are a lot of variants being proposed; VRAM, SGRAM, frame buffers on a chip, etc.")).

Rambus's Response to Finding No. 242:

Complaint Counsel have agreed that their description of the Crisp e-mail (CX 711 at 2) as

referring to "corrupting" proposals was an error; they meant to say "competing" proposals. In any event, the e-mail does not support the notion that the competing proposals had been generated *as a result of* presentations at JEDEC, as the finding suggests. Instead, the next two lines of the Crisp e-mail shows that Mr. Rhoden was in 1993 attempting to reduce competition in the marketplace – regardless of how it had arisen – by:

> "Stat[ing] that there was not enough market to justify all of these [devices] being standardized. He appealed to folks to really concentrate on one device for standardization."

(CX 711 at 2).

Mr. Rhoden's effort to reduce competition between the different technologies was in clear violation of the EIA Legal Guides, which state that:

> "EIA standardization programs . . . shall not involve any agreement, expressed or implied, to adhere, or require adherence to a standard . . . [and] shall not be proposed for or indirectly result in . . . restricting competition . . . or reducing product variations."

(CX 204 at 5).

243. JEDEC entertains a number of proposals by members when working toward a standard for a new device. (Rhoden, Tr. 415 ("[W]hen we're working on a particular device or whatever, there will be proposals that are made that come from usually a number of different companies. Sometimes multiple proposals or multiple ideas, if you will, come from a particular company, but more often than not, it comes from a variety of companies. So, you will have several different proposals that will be made inside JEDEC as to what path we should take for the next improvement cycle, if you will, of what we're working on").

Rambus's Response to Finding No. 243:

Rambus has no specific response, other than to note that JEDEC members are often

seeking to gain a competitive advantage through the standardization process, as Hyundai's Dr. Oh testified:

> "Q. What steps did Hyundai take to follow the work of JEDEC?
>
> A. We wanted to propose things to be adopted at the JEDEC meeting. That means if our proposal is – is adopted, that means we are ahead of our competitors, so we actively decided to attend and join the JEDEC committee."

(CX 2108, Oh Depo. at 23:24-24:5).

244. JEDEC members decide which of these ideas to pursue. (Rhoden, Tr. 415-416 ("Well, the differences of opinion are something that people have to investigate to see if particular -- if the particular proposals are viable or if they -- it usually winds up being that engineers themselves come up with the ideas, so they're almost always reasonable ideas, and it's just a question of then deciding which path they're going to take.")).

Rambus's Response to Finding No. 244:

There is substantial evidence that it is a *subset* of JEDEC members – the DRAM manufacturers – who are the principal decisionmakers on the question of which "ideas to pursue." (RX 1424 at 1: e-mail from a manufacturer representative to other manufacturer representatives, noting that JEDEC is "OUR organization and will approve whatever we decide to approve.") (capitalization in original).

245. In some cases, discussions of possible features generate a survey ballot that requests the members to give their views concerning different solutions. (JX0028 at 6 ("SDRAM Feature Survey Ballot"); Rhoden, Tr. 481 ("everything that shows up in a survey ballot is either from a presentation or from an earlier discussion that takes place in JEDEC."), 516 (survey ballot is "a collection of all of the topics that we had been discussing for some time, usually within JEDEC, and at some point we would need to make decisions, basically get a sense of the committee to see what path we would take moving forward."); Calvin, Tr. 1032 ("I also remember discussion before the survey was actually issued. Because this was an attempt to get a cross section from all the members. . . this survey was a result of trying to capture the top most things that were

necessary for SDRAM to continue to evolve. This had been discussed at numerous meetings before, and many inputs were coming in")).

Rambus's Response to Finding No. 245:

Rambus has no specific response, except to note Mr. Rhoden's subsequent clarification that a survey ballot "is essentially just to gauge interest level." (Rhoden, Tr. 587).

246. Survey ballots are official JEDEC work. (Landgraf Tr. 1716 ("in a JEDEC committee, there's a lot of official work that is documented, and survey ballots are considered to be official work."); Sussman, Tr. 1419 ("Q: Does the patent policy apply to a survey ballot based on your experience at JEDEC? A. And I've already answered that basically yes, as soon as possible in the discussion, we'd like to know.")).

Rambus's Response to Finding No. 246:

The weight of the evidence presented at trial supports a finding that survey ballots did not trigger any disclosure obligations relating to intellectual property. Mr. Rhoden testified that survey ballots contained no language requesting patent-related information because such information was not relevant at the survey stage:

> "Q. Do you see that there's no space on this survey ballot for anything relating to a patent disclosure? Do you see that?
>
> A. That is correct, *that was relevant to ballots*. This is a survey ballot, which is essentially just to guage interest level."

(Rhoden, Tr. 587) (emphasis added).

JC 42.3 chair Gordon Kelley similarly testified that in his understanding, disclosure was required only at the time of balloting and was merely "encouraged" prior to that time. (Kelley, Tr. 2707). In addition, the patent presentation routinely made at JC 42.3 meetings by Mr. Townsend did not list survey ballots in the list of those events where "patent status" should

be "resolve[d]." (JX 18 at 15; JX 20 at 15; JX 21 at 14; JX 22 at 12).

247. Following the conclusion of the second or subsequent presentations, the committee decides if it wants to create a ballot to vote on the substance of a proposed standard. (Rhoden, Tr. 406-07 (after the second presentation "we would decide if we want to have a ballot or not have a ballot.")).

Rambus's Response to Finding No. 247:

Rambus has no specific response.

248. JEDEC participants often had significant differences of opinion concerning the development of a standard. These differences of opinion drove heated debates concerning the merits of the various solutions to the technical challenges facing the JEDEC participants. (E.g., CX0711 at 14 (Regarding various proposals for SDRAM modules Crisp writes: "This was argued quite a lot . . . There was much wrangling etc and the conclusion is that they will all huddle once again to work out the details"), 33 (Regarding an HSTL ballot Crisp writes: "Another example of the flailing at JEDEC . Approximately three and a half hours was spent arguing about the resolution of the "No" ballots. The companies voting no are adamant about their objections and it appears there is basically an impasse"), 47 (Regarding a various pinout proposals Crisp writes: "The same issues came up as well as the usual pin naming and 'why don't you move pin xxx to yyy location.' Usually someone out in the audience seems to have some overwhelming reason why a particular pin should be in a particular position. Many times it really does not matter, but sometimes it does. *But always there are strong opinions!*") (emphasis added); CX0680 at 1 (Billy Garrett email from the September 1992 JC-42.3 meeting "This is not to say that there are not active, heated discussions on features and functionality. There are . . .NEC tried to introduce a second showing . . . but even the request for balloting was turned down due to several technical objections."), 2 ("Precharge and Autoprecharge were not resolved. Lots of disagreement on the effects on banks, and how autoprecharge will be done."); Rhoden, Tr. 434-35 ("if you give ten engineers a problem, you'll probably get 12 or 14 solutions, and the same is true inside the discussions inside the committee. People were proposing a number of other approaches to the same type of thing."); Sussman, Tr.1380 ("I had a lot of arguing to do to get the degree of programmable features into the part.")).

Rambus's Response to Finding No. 248:

Rambus has no specific response.

249. From time to time, ballots failed or was put on hold in the JEDEC committees because the committees did not reach a consensus. (JX0012 at 6 ("There was some discussion on the package size, but no consensus was gained. The ballot failed."), 12 ("ATT moved to put the ballot on hold until the two sided high pin count package issue was resolved. . . . Motion passed"); JX0019 at 10 ("In conclusion, NEC wanted to table the ballot. Fujitsu made motion to

send it to Council. Motion failed for lack of a second. Hitachi moved to take it off hold and send this ballot back to Committee. Apple seconded. The vote was unanimous."); JX0026 at 5 ("Motion to send to Council by Cypress, Xerox seconded. The vote was 5 yes, 8 no. Motion failed. The ballot was put on hold.")).

Rambus's Response to Finding No. 249:

Rambus has no specific response.

250. Ballots also may be put on hold for other reasons, including unresolved patent concerns. (G. Kelley, Tr. 2464-66 ("Because patent issues are almost terminal for a ballot to pass. If a patent issue comes up, unless it's able to be resolved at the meeting, it will -- the ballot will be put on hold or it will fail.")).

Rambus's Response to Finding No. 250:

Rambus has no specific response, except to note that the phrase "unresolved patent concerns" is ambiguous and unclear.

251. On other occasions, after long debate, ballots passed because they represented compromises that satisfied a majority, but not all, of the members. (JX0026 at 6 ("Micron: Vss and Vdd pins at the end of the package are not that useful. Vddq and Vssq can be organized better around the Dqs. . . Committee responded to Micron that this has been discussed for over a year. There are advantages and disadvantages of both implementations and this satisfies most.")).

Rambus's Response to Finding No. 251:

Rambus has no specific response.

252. If it preferred, a committee could pass items individually but place the individual items on hold until an entire list of related items that were needed to define a single standard was complete, and once that group of ballots was complete and passed, then together the committee could motion them to go to council for publication. (G. Kelley, Tr. 2554 (discussing the process for standardizing SDRAM); see also, e.g., JX0010 at 8-9 (V-PACK ballot failed due to patent concerns)).

Rambus's Response to Finding No. 252:

The citation to JX 10 (the December 1991 JC 42.3 minutes) is irrelevant to the proposed finding and in any event misstates the contents of the minutes, which refer to numerous concerns

regarding the balloted item.

253. After a JEDEC committee approves a standard, the proposed standard is sent by a ballot to the JEDEC board of directors, which then has to again by a consensus approve the ballot in order for the proposal to become a JEDEC the standard. (J. Kelly, Tr. 1785 ("Once the committee approves a standard . . .the proposed standard is sent by a ballot to the board of JEDEC, which then has to again by a consensus approve the ballot to adopt the standard."); Rhoden, Tr. 406-07 ("if the ballot were to pass [the committee], then we would move that ballot perhaps on to the final review process, which would be a procedural review to make sure that due process was followed at -- at that time it was the JEDEC Council, now it's the JEDEC board of directors.")).

Rambus's Response to Finding No. 253:

Rambus has no specific response.

254. JEDEC's consensus-based process means that the board of directors will consider any committee votes that were cast in opposition to the proposed standard. (J. Kelly, Tr. 1786 ("[t]he board will always discuss the fact that there are negative votes, particularly if there are unresolved negative votes.")).

Rambus's Response to Finding No. 254:

Rambus has no specific response.

255. JEDEC's consensus based process often requires years in order to adopt a new standard or change an existing standard. (CX0302 at 22 ("Complete process may take 2-3 years"); Polzin, Tr. 3977 ("JEDEC is open to any and all parties, so any and all parties have an opinion and can contribute or delay, or everybody has a vote, so it's not always the most straightforward thing to get a technical specification through. It's sometimes long, laborious, and you have to argue your points endlessly, probably much like Congress down the road, but it's successful and it works."); Peisl, Tr. 4453 ("JEDEC is traditionally a very slowly moving consortium, and there's a reason for that, because there's so many companies involved, it's basically the whole industry that produces parts for the PC and the laptop and the server business, so to try to reach consensus at JEDEC, based on my experience, have been incredibly hard and tough. In the last decade, essentially there were only two standards that emerged for SDR and DDR")).

Rambus's Response to Finding No. 255:

Rambus has no specific response.

256. During the standard development process, JEDEC prohibits members from public

discussion of committee deliberations. (G. Kelley, Tr. 2519 ("We specified that members were only to talk about JEDEC work within their companies."); CX0035 at 16)).

Rambus's Response to Finding No. 256:

This finding is irrelevant. There is no allegation in the complaint, and there was no evidence presented at trial, that Rambus engaged in "public discussion of committee deliberations." In addition, the JEDEC meeting minutes themselves were publicly available to anyone (except perhaps to Russian companies). (Kelley, Tr. 2622-23).

257. During the 1990s, JEDEC standards became more detailed. (CX0035 at 14-15 ("The work progressing on Synchronous DRAMs. . . is pushing our JC-42 scope- '. . . development of technical information and standards pertaining to pinouts, operational characteristics, test parameters, characterization and registration formats. . . If we do not do this, then we cannot create common parts that are plug compatible at 100Mhz operation and above. . . So, in addition to the design framework, we now are filling-in the details with timing diagrams that will impact, in a greater way, the chip design."); G. Kelley, Tr. 2390 ("the level of technical issues that we were dealing with [in 1992] on my DRAM pass-through was much greater than we had handled historically.")).

Rambus's Response to Finding No. 257:

Rambus agrees that during the 1990's, and particularly in connection with the DDR SDRAM standard, JEDEC "standardized" many more details than it had before. In fact, JEDEC standardized features and details that are not appropriate subject matters for groups of competitors to agree upon, for they do not relate to the professed goal of "interoperability." (Rhoden, Tr. 554-55; Polzin, Tr. 3972; Calvin, Tr. 1048; McAfee, Tr. 7234-35). In particular, in specifying an on-chip DLL as part of the DDR SDRAM standard, JEDEC overstepped its boundaries. An on-chip DLL is *not* required for interoperability. Rather, as Complaint Counsel's technical expert, Professor Jacob, explained, the DLL used in DDR SDRAMs is transparent to the DRAM interface. (Jacob, Tr. 5617-18). In other words, the rest of the system

is indifferent to whether there is a DLL or some other kind of circuitry on the DRAM so long as data from the DRAM arrives at the memory controller in the appropriate timing window. (Id.) To ensure interoperability, JEDEC should have simply specified the required timing parameters and left it up to the individual DRAM manufacturers to meet those requirements with whatever implementation they chose. (*See also* CX 204 at 5) (EIA Legal Guides prohibition against standardization activities that even "indirectly" result in "reducing product variations. . . .").

E. Why Companies Belong to JEDEC.

258. Formal standardization in the DRAM industry benefits the entire industry by ensuring quality and reliability in the products. (Prince, Tr. 9016-17 ("when something comes for formal standardization, it has the review of peers throughout the industry. Everyone gets a chance to review it and make comment, and if there are good and bad features, they can be modified. And what ultimately comes out for the users in the industry is the most adequate device that the industry collectively can prepare.")).

Rambus's Response to Finding No. 258:

As noted in response to finding no. 234, the evidence does not support a finding that JEDEC standardization (at least while Rambus was a member) "ensured quality and reliability in the products." The cited testimony does not support the finding in any event.

259. JEDEC is the most important standard-setting organization for DRAMs. (CX0035 at 14-15 ("This JEDEC standardization process creates the structure from which all DRAM designs begin. . . JEDEC is the fulcrum for DRAM standards in Asia, the Americas and Europe"); CX0419 (As of May 2000, "75% of the top 250 semiconductor manufacturers [were JEDEC] members, representing 80% of semiconductor sales. An estimated 90% of semiconductor standards in use are JEDEC standards."); Rhoden, Tr. 283-84 ("JEDEC is the place where industry standards are set for the DRAM" industry); Prince, Tr. 9016 ("JEDEC is the primary standardization body for RAMs."), 9021–22 (recalling only one RAM standard that was not formally standardized in either JEDEC or IEEE); Sussman, Tr. 1364; CX2773 at 9 (JEDEC standards are included in Micron's internal "Designer's Toolbox." web application.); CX2334 at 25 ("Pros" of DDR include fact that it is an open standard); CX2297 at 79 ("DDR SDRAM . . . Strong Points. . . JEDEC standardization in 1997."); CX0302 at 7 (JEDEC is the "World Leading technology standards association."), 16 ("Global JEDEC standards usage has skyrocketed."), 17 ("If you are not [at JEDEC], your competition may be deciding your future."); Peisl, Tr. 4384

("JEDEC's standards were the only source for our own specifications, meaning that . . . Infineon chip specifications were entirely directed towards the -- 100 percent compatibility towards the JEDEC specifications."), 4386 ("If we wouldn't have produced a chip that would not comply to the JEDEC specification, it would have not been able to work at the PC, at the server, at the laptop platforms at HP, IBM and all our other customers because of noncompliance issues, nontechnical issues, and we essentially would not have been able to sell anything"); (CX2080 at 194 (Karp, Micron Dep.) ("JEDEC's a bunch of competitors. They are not people that particularly like each other. *They are there because they have to be there* because it's part of – it's part of the business.")).

Rambus's Response to Finding No. 259:

This finding is irrelevant because it – and most of the cited testimony – are stated in the present tense. In addition, the weight of the evidence shows that during the relevant time period, JEDEC standardization was neither a necessary nor sufficient factor in achieving market success. (*See* RPF 1514-1523 and evidence cited therein).

260. JEDEC standards are very valuable to manufacturers. (CX0707 at 1 (Geoff Tate writes: "JEDEC is a bid deal to them [Samsung] because it [JEDEC] represents the big users."); Peisl, Tr. 4384 ("JEDEC's standards were the only source for our own specifications, meaning that . . . Infineon chip specifications were entirely directed towards the -- 100 percent compatibility towards the JEDEC specifications."), 4386 ("If we wouldn't have produced a chip that would not comply to the JEDEC specification, it would have not been able to work at the PC, at the server, at the laptop platforms at HP, IBM and all our other customers because of noncompliance issues, nontechnical issues, and we essentially would not have been able to sell anything"); Bechtelsheim, Tr. 5790 (monitored JEDEC's progress on SDRAM standard because "it was a prerequisite for, in my mind, for the memory manufacturers to actually produce and manufacture these JEDEC-compatible parts."); Williams, Tr. 763 (Micron's customers "require that they are able to buy products from multiple sources and that these products interoperate, and JEDEC is the body that sets those standards."); (CX2107 at 23 (Oh, FTC Dep) ("JEDEC is the committee which standardize all the standard products in the market.")).

Rambus's Response to Finding No. 260:

Rambus agrees that JEDEC standards are important today to DRAM manufacturers both for the content of the standard and because of the manufacturers' ability to control that content. As the NEC JEDEC representative stated in an e-mail to JEDEC representatives of other DRAM

manufacturers, "JEDEC is OUR organization and will approve whatever we decide to approve." (RX 1424 at 1) (capitalization in original).

261. JEDEC standards are valuable to customers because customers require competitive, effective devices with a competitive and reliable supply. (Landgraf, Tr. 1692-93 ("the utility of a [JEDEC] standard . . . is that from HP's perspective, we were a large user of memories, and we wanted to use the most competitive and most effective devices available, and we wanted them available from a number of suppliers. . . . So, we have a wide supply. We also have a competitive supply that -- the more suppliers you have, the better your selection is for -- and more competitive supply base you have. We also had assurance of supply going forward. HP -- many of HP's products are supported for a five to seven, maybe ten-year product life cycle, and in some cases that exceeds the manufacturing cycle for some suppliers, and so we -- by having a standard, we would have a greater chance of having continuity of supply for any time in production or even in support life."); G. Kelley, Tr. 2387-88 ("The DRAM is the largest single semiconductor used in [IBM], and the DRAM is probably the one that we spent more money on than any other. One of the realities of the DRAM, because of its proliferation, is that it must be low cost. To be low cost, it must be available for many suppliers, and it must be interchangeable from those suppliers, which means I can plug a component out from one supplier and plug the component in from another and they work equally well.); Heye, Tr. 3635-36 ("Q: Do you have an understanding as to why Apple chose to send a representative to the JEDEC memory committee? A: Yes. . . .in the early nineties, Apple was the largest consumer of semiconductors in the world outside of IBM. . . . So, when you're in that kind of volume in the '90s, you have got to ride the commodity curve. And by that I mean you have to ensure that your products, that is commodity parts, are using the parts that are the highest available lowest cost parts. . . . And so we had a person whose job was not only to be a member of JEDEC, but he would go literally around the world, I think at least twice a year, and talk to every memory vendor to understand the memory roadmaps."), 3716-17 ("AMD's use of open standards is absolutely critical for success in the marketplace."); Wagner, Tr. 3829 ("[nVidia] originally got involved with JEDEC, partially on request from memory vendors. We had -- we were making requests of them for certain features that JEDEC was trying to eliminate, they encouraged us to participate in JEDEC to ensure that those features didn't get dropped from the standards. So, we got involved at that point."); Peisl, Tr. 4409-10 (understood from discussion with customers concerning JEDEC standards that customers "were looking essentially for two major features . . . multisourcing [and] . . . interoperability.")).

Rambus's Response to Finding No. 261:

This finding is irrelevant because it is stated in the present tense. In addition, there is substantial evidence that JEDEC standardization is neither necessary nor sufficient for marketplace success, and that it was *Intel's* choice of memory technology, not JEDEC

standardization, that drove PC OEM purchasing decisions during the relevant time period.

(Gross, Tr. 2348-49; RFP 1513-1523).

262. JEDEC standards are valuable to third-party enablers. (Calvin, Tr. 999-1000 ("because of the standardization effort there, obviously anything that [Intel] wanted to use or make use of in the future, we wanted to be able to influence the direction, as well as to be able to understand what we would be getting as the part involved. So, [Intel] had a strong interest in knowing and being part of that development activity.); Polzin, Tr. 3973 ("AMD views the JEDEC standards process as crucial to its business. JEDEC allows manufacturers to all design to a common standard and basically enables the commodity marketplace. Everybody is designing compatible parts at the lowest possible cost competing on manufacturing cost.")).

Rambus's Response to Finding No. 262:

This finding is irrelevant because it is stated in the present tense. In addition, the phrase "third-party enablers" is vague. The cited testimony only refers to chipset manufacturers.

263. Customers insist on buying only JEDEC-compliant parts. (Peisl, Tr. 4409 ("The customers wanted to ensure that their systems, their platforms and servers, laptops and desktops, were sold at the best price and the best delivery situation, so they were looking essentially for two major features. One was the multisourcing, which JEDEC is ensuring. Because of the specified interface, they make sure that you have several DRAM vendors and several other vendors because they're all working towards the same interface. And the second issue is the interoperability. They of course wanted to make sure that our parts work together with all the other components in the system."); Becker, Tr. 1152-53 ("Q: Do you have an understanding as to why it is you only manufacture JEDEC-compliant products, DRAMs? A. My understanding is that that's all our customers are willing to buy. We talked about the DRAMs I manufacture as being a commodity product. Our customers, customers like Dell, IBM, Compaq, they're interested in buying DRAM modules or components from [Infineon], but not just [Infineon]. They want to be able to buy [Infineon] parts or Samsung's parts or Micron's part and use them interchangeably, and through the standards process, they get that benefit."); Sussman, Tr. 1363 ("Q. Have you ever had any customer indicate to you that they would only accept a JEDEC-compliant part for a particular application? A. I think we have had some military programs that they were insisting in their documents that they needed to be JEDEC standard."); Bechtelsheim, Tr. 5790 (monitored JEDEC's progress on SDRAM standard because "it was a prerequisite for, in my mind, for the memory manufacturers to actually produce and manufacture these JEDEC-compatible parts."); (CX2054 at 47-48 (Mooring, Infineon Dep.) (DRAM customers like Hewlett-Packard, Apple, and Sun told Rambus "we only use memories approved by JEDEC."); CX2079 at 117-18 (Mooring, Micron Dep.) (DRAM customers like Sun, Hewlett-Packard, Apple , and Compaq told Rambus "we don't use non-JEDEC standard memories"), 118 (" in the DRAM business, the only standard is JEDEC.")).

Rambus's Response to Finding No. 263:

The cited testimony provides scant support for this finding. The Peisl testimony says nothing about customers who will buy "only JEDEC-compliant parts." Peisl instead talks about having multiple sources and interoperability. Mr. Becker does say that his "understanding" is that Infineon's customers are only willing to buy JEDEC-compliant products, but he is a plant manager who has no foundation for testimony about customer preferences. Mr. Sussman says only that he "thinks" that some *military* customers wanted JEDEC-compliant devices. Mr. Bechtolsheim states that manufacturers needed to produce "JEDEC-compatible parts," but he did not say that they should produce *only* such parts. Finally, Mr. Mooring's testimony is misquoted. He did not attribute the quoted statements to each of the companies listed. Instead, he said there was a *range* of responses from these companies, including the quoted response and the response simply that "you ought to go take this to JEDEC." (CX 2079 at 118).

F. Members of the Industry Understand the Importance of JEDEC.

264. Even Rambus recognized the importance of JEDEC. In 1996, shortly after it withdrew from JEDEC, Rambus considered initiating a standards-related organization that it would control called "REDEC." (CX0902 at 1 ("We'd be responsive and open to their inputs, but it would be us making the real decisions"), 2 ("Get them away from Jedec and participating in our 'JEDEC.'"); CX0903 at 1 ("This is about pacification of our partners, pure and simple.")).

Rambus's Response to Finding No. 264:

Rambus did consider establishing a forum at which manufacturers and others would contribute ideas towards the implementation of the RDRAM devices. This proposal does not support the finding that Rambus "recognized the importance of JEDEC."

265. Although Rambus wanted to give the group the veneer of an open standards organization, Rambus fully intended to continue charging royalties for intellectual property generated by REDEC. (CX0902 at 1-2 ("My belief is that the name should NOT contain

Rambus, and should contain the words 'open standard'. . . First, we want royalties on what we do. . . All IP is shared. We get royalties."); CX0903 at 1-2 ("what should our answer to JEDEC be? First of all it would be beneficial if it were designed to give our partners a forum that they can participate in that makes them feel that they are as much in control of their own destiny as they currently are with JEDEC. I am not sure from a practical perspective how we could effect that and still remain in an ownership position with out patent rights. . . .Open standards seem at odds with our business model.")).

Rambus's Response to Finding No. 265:

This finding is both irrelevant and inaccurate. First, "open standards" is not inconsistent with the payment of royalties for intellectual property, as the EIA acknowledged in its January 1996 letter to the FTC. (RX 669 at 2-4). Moreover, Rambus has always sought for the RDRAM to become an "open" industry standard, meaning that it is available from numerous manufacturers who each manufacture compatible devices. *See* RPF 46-52.

266. Intel's PC-100/133 specifications adopted the JEDEC SDRAM standard and added parametric details. (Peisl, Tr. 4411 ("Intel's PC100 and PC133 specification essentially described some additives or addendums to the synchronous DRAM spec and it was JEDEC specification and it was later on added into the JEDEC specifications," and no inconsistency between the JEDEC standard and the Intel specification); Shirley, Tr. 4139-40 ("The Intel PC-100 specification added what I would call as a low level of detail about additional speed grades and additional current requirements that they saw as important to their use of our memory products."); MacWilliams, Tr. 4887 ("when [Intel] did the PC100 application, we made sure it was backwards compatible with the 66 megahertz"), 4906-07 ("PC100 was the effort by Intel to try and make the 100 megahertz SDRAM that met a spec referred to as PC100.")).

Rambus's Response to Finding No. 266:

This proposed finding is incomplete and misleading, because it implies that the existing SDRAM standard provided for parts interoperability and compatibility and was simply "tweaked" a bit by Intel to add some "details." The evidence is to the contrary. The publication of JEDEC's SDRAM standard was insufficient to ensure market success or even interoperability. Because of this, SDRAM products made by one DRAM manufacturer were not compatible with

those produced by another. (MacWilliams, Tr. 4908). Prompted by these incompatibilities, Intel - not JEDEC - developed the "PC SDRAM" standard in 1996. (MacWilliams, Tr. 407-09). As stated in that standard, "The objective of this document is to define a *new Synchronous DRAM specification* ('PC SDRAM') which will remove extra functionality from the current JEDEC standard SDRAM specification, so that it will be a 'fully compatible' device among all vendor designed parts." (RX 2103-14 at 9) (emphasis added). The Intel PC SDRAM specification set forth what would become the industry standard for PC100 SDRAM. (MacWilliams, Tr. 4908).

267. DRAMs produced in compliance with JEDEC standards have dominated the DRAM industry for the past decade. (CX0419 (As of May 2000, "75% of the top 250 semiconductor manufacturers [were JEDEC] members, representing 80% of semiconductor sales. An estimated 90% of semiconductor standards in use are JEDEC standards."); CX0302 at 16 ("Global JEDEC standards usage has skyrocketed."), 17 ("If you are not [at JEDEC], your competition may be deciding your future."); Peisl, Tr. 4384 ("JEDEC's standards were the only source for our own specifications, meaning that . . . Infineon chip specifications were entirely directed towards the -- 100 percent compatibility towards the JEDEC specifications."), 4386 ("If we wouldn't have produced a chip that would not comply to the JEDEC specification, it would have not been able to work at the PC, at the server, at the laptop platforms at HP, IBM and all our other customers because of noncompliance issues, nontechnical issues, and we essentially would not have been able to sell anything"); *see* DX0141; DX0219).

Rambus's Response to Finding No. 267:

The cited evidence does not support the finding. The fact that most manufacturers are JEDEC members does not mean that JEDEC standards "dominated the DRAM industry" or that most of the DRAMs sold in the 1990's were JEDEC-compliant. There is no evidence in the record on this latter point.

268. Paragraphs 268 to 299 are unused.

III. JEDEC's Purpose and Rules Are Designed to Develop Open Standards, Free of Hidden Intellectual Property Rights.

A. JEDEC Is Devoted to Open Standards.

300. The goal of JEDEC is to develop open standards. (CX2957 at 2 (Declaration of Joel Karp) ("My understanding of the EIA patent policy is that standards promulgated by standard-setting groups are 'open' standards"); CX0419 ("JEDEC standards are open (in terms of IP licensing)"); CX0449 at 2 ("JEDEC's core business is the development of open standards."); CX3089 at 13-14 ("one of the goals of setting open standards is to prevent a single entity from stifling competition"); Appleton, Tr. 6328 (JEDEC's "purpose is to develop an open standard [to which] companies and customers would have access . . . in order to develop their products"); Bechtelsheim, Tr. 5781-2, 5785 ("stated goal is to develop open industry standards"); Calvin, Tr. 995-96; Rhoden, Tr. 301, 536 ("the fundamental premise inside JEDEC is open standardization); J. Kelly, Tr. 1776-78 ("those [open standards] are the only kinds of standards that JEDEC generates"), 1782, 1787; Sussman, Tr. 1325; Williams, Tr. 761 (JEDEC creates "open standard[s] that everybody can use")).

Rambus's Response to Finding No. 300:

The parties agree that JEDEC's goal was to develop "open standards". The parties disagree, as discussed below, with respect to the definition of "open standards."

301. Open standards are free from hidden or restrictive intellectual property rights. (CX0903 at 2 (Richard Crisp writes: "The job of JEDEC is to create standards which steer clear of patents which must be used to be in compliance with the standard whenever possible."); CX0449 at 2 ("Open standards by definition are free of restrictive intellectual property (or 'IP') rights"); (CX2059 at 90 (Karp, Infineon Dep.) ("open is distinguished from something that's proprietary"); J. Kelly, Tr. 1777, 1898-99 ("EIA does not endorse a standard that contains hidden IP"); G. Kelley, Tr. 2393-96 ("first requirement was to avoid patents"); Kellogg, Tr. 5041-42; Rhoden, Tr. 536, 637; Tabrizi, Tr. 9118).

Rambus's Response to Finding No. 301:

While it is not clear what Complaint Counsel mean by "hidden or restrictive" rights, this finding would not be objectionable if it were rephrased to state that "'open' standards are those in which any intellectual property required to manufacture or use compliant products is available on reasonable terms to all who seek to utilize the standard." This re-phrasing would comport with

the testimony of most of the trial witnesses who addressed this point, including EIA General Counsel and JEDEC President John Kelly. Mr. Kelly was asked to explain what he meant by "restrictive intellectual property rights" in his March 2002 "Overview of the JEDEC Patent Policy," CX 449:

> "Q. And you say, 'open standards by definition are free of restrictive intellectual property or IP rights,' correct?
>
> A. Yes, sir.
>
> Q. And by 'restricted' you mean that there's no objection to having features [in] standards that are protected by valid patents as long as they're available to all comers on reasonable and non-discriminatory terms?
>
> A. Yes, sir."

(Kelly, Tr. 2072).

Numerous contemporaneous documents, and the evidence of JEDEC's actual practice, also make clear that "open" standards may, and often do, include patented features or technologies. As Mr. Kelly explained in a May 2000 letter to a prospective member, "JEDEC standards are open (in terms of IP *licensing*). . . ." (CX 419 at 1) (emphasis added). The EIA's January 1996 letter to the FTC confirms that an "open" standard is one where necessary patent licenses are available to all comers on reasonable terms. (*See* RX 669 at 4 (. . . "the important issue is the license availability to all parties on reasonable, non-discriminatory terms")). The EIA Legal Guides, which were required to be followed by JEDEC members (Kelly, Tr. 1829-30; CX 206 at 6), similarly provide that it is a "basic objective" of standards-setting that "[s]tandards are proposed or adopted by EIA without regard to whether their proposal or adoption may in any

way involve patents on articles, materials, or processes." (CX 204 at 4).

Any other policy – *e.g.*, a policy designed to avoid patent technology -- would hinder innovation and thwart progress, as the EIA recognized when it told the FTC in January 1996 that

> "[a]llowing patented technology in standards is procompetitive. . . . By allowing standards based on patents, American consumers are assured of standards that reflect the latest innovation and high technology [that] the great technical minds of this country can deliver."

(RX 669 at 2-3).

JEDEC's actual practices during the relevant time period also make it clear that JEDEC did not have a policy of avoiding patented technology. For example, when JEDEC added language to its ballots requesting certain information about issued patents, it emphasized that any responses would be "for information only and [would not] be checked to see who said what." (CX 3 at 6). Similarly, in the so-called "Quad Cas incident," where Texas Instruments ("TI") was accused of failing to disclose issued patents at the time of balloting of a JEDEC standard, all suggestions that the patented feature be withdrawn from the standard were *withdrawn* after TI agreed to license its patents on "RAND" terms. (JX 25 at 3). It is also undisputed that JEDEC routinely approved ballots despite an awareness of patents related to the proposed standards, and that it often did so *without* requesting or receiving RAND assurances. (RPF 1220-1238).

Finally, it is undisputed that JEDEC did "*not* require a certification by participating companies regarding potentially conflicting patent interests." (RX 740 at 1) (July 1996 letter by FTC Secretary Clark to EIA General Counsel John Kelly) (emphasis added). This was a deliberate policy decision, as JEDEC Secretary Ken McGhee's March 29, 1994 memorandum to

JC 42 Chairman Jim Townsend makes clear. McGhee stated in his memorandum that JEDEC's "legal counsel" had said that "he didn't think it was a good idea to require people at JEDEC standards meetings to sign a document assuring anything about their company's patent rights. . . ." (RX 486 at 1). McGhee's memorandum stated that "legal counsel" had stated that such a requirement would "have a chilling effect," would "slow[ ] down the business at hand," and would "need[ ] to come from a VP or higher" because "engineers can't sign such documents." (*Id*.). (*See also* RX 1582 at 1 – 2/11/00 McGhee e-mail to JC 42.4 members stating that "[d]isclosure of patents is a very big issue for Committee members and cannot be required of members at meetings.").

As the FTC recognized in its July 10, 1996 letter to the EIA, the difference between the EIA's policy, which did "not require a certification . . . regarding potentially conflicting interests," and the policy of the standard-setting body involved in the *Dell* case, which *did* require such a certification, meant that the "expectations of participants in the two standard-setting processes differ" with respect to intellectual property issues. (RX 740 at 1).

In sum, Complaint Counsel's proposed finding regarding the meaning of "open standard" is inaccurate, and it should be rephrased to state that "'open' standards are those in which any intellectual property required to manufacture or use compliant products is available on reasonable terms to all who seek to utilize the standard."

302. Open standards uphold the antitrust laws by ensuring that standards are free of discrimination and do not lead to monopolization. (CX0202 at 6 (basic rules prohibit activity that could violate the antitrust laws); CX0204 at 5 (EIA programs "shall not be proposed for or indirectly result in. . . restricting competition, giving a competitive advantage to any manufacturer, excluding competitors from the market. . ."); CX0302 at 9; J. Kelly, Tr. 1781-82 (open standards are not used to enhance market power); Rhoden, Tr. 302-03)). *See also* CX0711 at 16 (Richard Crisp email from JEDEC meeting stating "The meeting opened with a lot of

controversy regarding Patents. . . Micron says the policy exists due to anti-trust concerns. That if a group of companies wanted to keep out competition they could agree amongst themselves to standardize something that is patented and not license those that they do not want to compete with.")).

Rambus's Response to Finding No. 302:

If this finding incorporates the definition of "open standards" described in Rambus's response to finding no. 301, it is unobjectionable. As the EIA pointed out in its January 1996 letter to the FTC,

> "there is a positive and pro-competitive benefit to incorporating intellectual property in standards. As ANSI stated in its December 1, 1995 testimony (p. 10), 'when proprietary technology is incorporated into a standard, it is available to all competing companies. This spurs the rate of technology's implementation and enhances U.S. competiveness.'"

(RX 669 at 3).

In other words, the evidence shows that open standards further the interests of the antitrust laws by *incorporating* intellectual property and making it widely available, not by *excluding* intellectual property, as Complaint Counsel have suggested.

303. Open standards lower costs by avoiding patents and royalties. (G. Kelley, Tr. 2396 ("first requirement was to avoid patents"); Lee, Tr. 6595-96 ("There was also a policy . . .to try to avoid the use of patents, when possible, in defining a standard"); Peisl, Tr. 4476; CX2107 at 136-38, 158-60 (open standards important for cost-effectiveness) (Oh, Dep.); CX2297 at 79 (DDR DRAM strong points: "Open architecture without royalties or fees.")). *See also* CX0013 at 30 ("Problems in Intellectual Property - Some participants may look for commercial advantage. Late disclosure close to market interaction. Failure to indicate a patent is filed, pending or awarded . . . - Some participants might vote differently or develop different but equivalent standards if royalties were identified in the beginning as an objective."); CX0711 at 44 (Richard Crisp noting that Micron cited patents as reason for its "No" vote.); Heye, Tr. 3731 ("The second concern was a possible cost disadvantage we might incur in the infrastructure due to the incremental royalty fees")).

Rambus's Response to Finding No. 303:

The evidence in the record does not support the proposition that an effort to lower *manufacturing* costs by refusing to incorporate patented technologies in standards is pro-competitive or would advance consumer welfare. As the EIA itself explained to the FTC in January 1996, "allowing patented technologies in standards is procompetitive." (RX 669 at 2). The EIA also pointed out that standards in "high-tech industries must be based on the leading edge technologies. Consumers will not buy second-best products that are based only on publicly available information. They demand and deserve the best technology these industries can offer." (RX 669 at 4). The EIA letter also explains that "[e]ven if knowledge of a patent comes later in time due to the pending status of the patent while the standard was being created, the *important* issue is the licensing availability to all parties on reasonable, non-discriminatory terms." (RX 669 at 4) (emphasis added).

The evidence in the record does not, in any event, support the general proposition that "avoiding patents" will indeed lower manufacturing costs. That conclusion depends upon the costs of manufacturing alternative designs in lieu of the patented features. *None* of the cited testimony undertakes that analysis. Complaint Counsel thus did not meet their burden of proof on this issue. Moreover, the witnesses whose testimony is cited are almost all employed by DRAM manufacturers, who are interested in their company's profitability, not in the result might best serve overall consumer welfare. It might well be the case, for example, that a particular patented feature would improve the *efficiency* of a device (such as a microprocessor), so that from society's point of view, any increase in manufacturing costs would be outweighed by overall efficiency gains.

In short, a broad statement that excluding patented features from standards is pro-competitive or lowers costs is not supported by the trial record.

304. Open standards help ensure the use of the standard. (G. Kelley, Tr. 2398-99 (failure to disclose could block standard); Landgraf, Tr. 1694 ("worst thing to have" is a system you cannot produce because of infringement.)). *See also* CX0711 at 16 (Richard Crisp email from JEDEC meeting stating "The meeting opened with a lot of controversy regarding Patents. . . Micron says the policy exists due to anti-trust concerns. That if a group of companies wanted to keep out competition they could agree amongst themselves to standardize something that is patented and not license those that they do not want to compete with."), at 187 (Richard Crisp writes: "SSTL passed 30/0 and was sent to council. However Hitachi stated that they had a patent relating to it. This created a big ruckus. The major thrust of the criticism of Hitachi was that they waited until the ballots had been passed before mentioning that they had a patent")).

Rambus's Response to Finding No. 304:

The cited evidence has nothing at all to do with the proposed finding. The finding itself is otherwise unobjectionable if re-framed to state, in accord with the evidence, that an "open" standard – one available to all comers on reasonable terms – may be more widely available than one whose use is restricted to only certain companies.

B. JEDEC Operates Pursuant to Rules Which Govern Its Standard-Setting Activities.

305. Between 1991 and 1996, JEDEC was a part of EIA. (J. Kelly, Tr. 2075).

Rambus's Response to Finding No. 305:

The cited testimony states that between 1991 and 1996, JEDEC "was an activity within the EIA engineering department." (Kelly, Tr. 2075). This language should be used.

306. During the time when JEDEC was a part of EIA, the standard setting activities of JEDEC and other parts of EIA were governed by the written rules of the EIA as well as their own specific manuals and rules. (J. Kelly, Tr. 1824).

Rambus's Response to Finding No. 306:

The cited testimony does not support the proposed finding, for it does *not* refer to JEDEC

and instead refers to "divisions and sectors" of the EIA. (Kelly, Tr. 1824). There was no testimony that JEDEC was a "division" or a "sector" of the EIA while Rambus was a member.

307. EIA's basic rules relating to standard setting activities are found in the EIA Legal Guides, as well as in EP-3, EP-7. (CX0202 at 6; CX0203A at 20, CX0204 at 5, JX0054 at 8-9; J. Kelly, Tr. 1824-25).

Rambus's Response to Finding No. 307:

This finding is incomplete since it does not include EP-7-B, published in October 1995 (RX 616; Kelly, Tr. 2082).

308. The rules of JEDEC are provided in the EIA Legal Guides, EIA Manuals, and the JEDEC Manual of Organization and Procedure. (CX0202; CX0204; CX0203A; JX0054; CX0205; CX0205A; CX0208; J. Kelly, Tr. 1824-25 (citing EP-3, EP-7 and EIA Legal Guides)).

Rambus's Response to Finding No. 308:

This finding is not supported by the cited evidence and is vague as to which "JEDEC Manual of Organization and Procedure" it refers to. The cited testimony by Mr. Kelly does not refer to any JEDEC manuals. Mr. Kelly also testified that in the event of a conflict, any JEDEC manual would be subordinate to the EIA manuals. (Kelly, Tr. 1915-6). Mr. Kelly further testified that JEDEC manual 21-I (CX 208), which this finding cites, required approval by the EIA's Engineering Department Executive Council ("EDEC") to be effective. (Kelly, Tr. 2105). Mr. Kelly testified that he did not know whether such approval had ever been obtained. (Kelly, Tr. 2105). Complaint Counsel offered no testimony or other evidence to prove that such approval had been obtained. The resulting presumption is that the 21-H manual, which was published in 1988, was operative throughout the time that Rambus was a JEDEC member. (CX 205A at 1-2). The 21-H manual provides that "JEDEC standards are adopted without regard to whether or not their adoption may involve patents [on] articles, materials or processes."

(CX 205A at 11). It is undisputed that 21-H was the operative manual at the time the SDRAM standard was adopted in the spring of 1993. (CX 205A; CX 208).

309. EIA rules and JEDEC rules concerning disclosure and licensing of patents are consistent. (J. Kelly, Tr. 1915-16 ("I'm not aware of any conflicts between the JEDEC rules and the EIA rules"), 1919-20 ("I think that those terms were used interchangeably, EIA patent policy and JEDEC patent policy.")).

Rambus's Response to Finding No. 309:

The cited testimony does not support the proposed finding, for all that Mr. Kelly states is that he is not "aware" of any conflicts between the EIA and JEDEC manuals. In contrast, Gordon Kelley, who was the chair of the JEDEC Council and of the 42.3 subcommittee during much of the relevant time, testified that he understood there to be a basic conflict between the two manuals, for the EIA manuals intended the word "patents" to mean simply "patents," while the JEDEC manual (at least by 1993) supposedly intended the word "patents" to mean "patents and patent applications." (Kelley, Tr. 2686-7; 2695-7).

However, Rambus agrees that the proposed finding is, at bottom, accurate, for the weight of the testimony shows that: (1) both EIA and JEDEC standardization activities were governed by EIA's rules and policies, (Kelly, Tr. 1829-30, 1915-18; RX 1179 at 1; CX 204 at 4; Rhoden, Tr. 289, 667); (2) EIA encouraged, but did not require, the disclosure of patents or patent applications (RX 616 at 2; RX 669 at 2; RX 740 at 1; RX 742 at 1; RX 1582 at 1); and (3) both the EIA Legal Guides and the JEDEC manuals provided that standards were adopted "without regard" to whether their adoption "may in any way involve patents. . . ." (CX 204 at 4; RX 1211 at 20). The EIA and JEDEC rules were, therefore, consistent, as this finding states.

C. JEDEC Participants Must Act in Good Faith.

310. From 1991 to 1996, and continuing through today, EIA Basic Rule 1 required EIA/JEDEC participants to act in good faith. (CX0202 at 6 (Basic Rule 1); CX0204 at 5; CX0449 at 4; J. Kelly, Tr. 1840-41 ("[T]his provision is designed to prevent companies from acting in bad faith in connection with standard-setting activities"), 2053-55 ("all participants are under a duty under the EIA Legal Guides to act in good faith"; "clearly there are no intended loopholes"); CX2058 at 431 (Meyer 12/14/00 Dep.) (expected that JEDEC members, including Rambus, would act in good faith); Rhoden, Tr. 306-07; Sussman, Tr. 1330-32; Crisp, Tr. 2946-47; McGrath, Tr. 9272).

Rambus's Response to Finding No. 310:

This proposed finding misstates the language of the EIA Legal Guides, which uses the phrase "good faith" to refer to the policies and procedures adopted by the EIA and its various divisions, not to the obligations of members. The Legal Guides state that:

> "Section C. Basic Rules For Conducting Program.
>
> All EIA standardization programs shall be conducted in accordance with the following rules:
>
> (1) They shall be carried on in good faith under policies and procedures which will assure fairness and unrestricted participation. . . ."

(CX 202 at 6; CX 204 at 5).

It would stretch these words beyond reason to use them to impose additional obligations on anyone in an area (the patent policy) already covered by specific EIA rules. It would further stretch these words beyond reason to suggest that they were intended to impose any obligations on individual members. Given the location of this phrase within the Legal Guides, and the language used, it is apparent that this phrase is not directed to individual members but is instead a general directive to the administrators who "conduct" the EIA's standardization activities,

directing them to adopt "policies and procedures which will assure fairness and unrestricted participation." (*Id*.).

This conclusion is further buttressed by the fact that this phrase appears in "Part II" of the Legal Guides rather than "Part I." (*Id*.). The introduction to Part I states it includes "general guides" that are "required to be read and followed by all members of the association." (CX 204 at 3). The introduction to Part II *contains no such admonition to members* and refers to "legal policies," not "general guides." (CX 204 at 4).

311. Good faith imposes a duty on participants in EIA and JEDEC activities to familiarize themselves with and abide by the letter and the spirit of the patent policy. (CX0449 at 4; J. Kelly Tr. 2053-54 ("the patent policy is supposed to be complied with not just in terms of its written letter but also in terms of the spirit of the patent policy")).

Rambus's Response to Finding No. 311:

This proposed finding is irrelevant because it is phrased in the present tense. The cited document, CX 449, is similarly irrelevant, since it is a March 2002 "overview" of the JEDEC patent policy, prepared more than six years after Rambus attended its last JEDEC meeting and well after this dispute arose.

Complaint Counsel plainly knew how to refer to the relevant time period in their proposed findings when they wanted to, as in the immediate prior finding, no. 310.

No contemporaneous document supports the proposition that JEDEC members had a "duty" to comply with "the spirit of the patent policy," as this proposed finding suggests. Instead, JEDEC Secretary Ken McGhee's February 11, 2000 e-mail shows that the JEDEC leadership well understood that while JEDEC members may have been "encourage[d]" to go "beyond the patent policy" in making disclosures, they were not "required" to do so:

> "The JEDEC patent policy concerns items that are known to be patented that are included in JEDEC standards. Disclosure of patents is a very big issue for Committee members and cannot be required of members at meetings. However, if a company gives early disclosure on a patent they are working on, it definitely gives a lot of assurance to the Committee members regarding development of any standards affecting it. Therefore, in Micron's letter, *by giving early disclosure, they have gone one step beyond the patent policy and have complied with the spirit of the law. JEDEC encourages this type of activity from any member.*"

(RX 1585 at 1) (emphasis added).

312. Good faith requires fair treatment of other participants, trust, and honesty. (CX0449 at 4 (rules are "designed to promote openness, good faith, and fair dealing in the development of standards."); J. Kelly, Tr. 1841 ("[C]ompanies need to participate in the process openly and honestly and fairly and in good faith and not in bad faith, because bad faith undermines the confidence of everyone in the process."); G. Kelley, Tr. 2397 ("my mind translated [good faith] to fair treatment for all members"); Rhoden, Tr. 305-06 ("The term "good faith" as used in [the Legal Guides] is that the people. . . are coming under the premise that they're going to . . . work toward the benefit of the end user of the industry itself, and operating in good faith means that you would expect other people to do the same thing."); Sussman, Tr. 1330 ("Good faith, we're all competitors, we're all about ready to dice each other in the marketplace, but seeing we're talking about or about to talk on intellectual property, I trust you to do something, and I expect that same set of trust back.")).

Rambus's Response to Finding No. 312:

This finding should be amended to comport with the actual language used in the EIA Legal Guides. (CX 204 at 5). The finding should say "EIA standardization programs were required to be conducted 'in good faith under policies and procedures which will assure fairness and unrestricted participation.'" (*Id.*). The language actually used in the Legal Guides makes

clear that it is not directed to individual members but is instead a general directive to the administrators responsible for "conduct[ing]" EIA standardization activities. (CX 204 at 5).

Given the importance that Complaint Counsel attach to the "good faith" language from the EIA Legal Guides, it is useful to ask whether the record evidence supports a finding that the JEDEC leadership did in fact, and as required by the Legal Guides, utilize "procedures which will assure fairness and unrestricted participation." (*Id.*). The evidence shows that they did not. At Rambus's second meeting, for example, the chair of the 42.3B subcommittee, Gordon Kelley, unilaterally barred Rambus from presenting its technology for standardization, in purported reliance upon a special vote authorizing such an action. (Kelley, Tr. 2653-54). No one else recalled this vote at trial, and no trial exhibit refers to it. Moreover, Mr. Kelley had a clear conflict of interest: he made and enforced his unilateral decision to bar Rambus from presenting its technology *two weeks* after he wrote in an internal company document that his company's interests were threatened by the Rambus technology and were best served if Rambus "fails to become standard." (RX 279 at 7). He did not disclose this conflict to Mr. Crisp or to anyone else. (Kelley, Tr. 2656-57).

This undisclosed conflict of interest, and Chairman Kelley's attempt to justify it at trial by pointing to an entirely undocumented special vote allowing him this unilateral power, suggests strongly that the "good faith" requirement that Complaint Counsel rely upon was not adhered to in practice by JEDEC leadership.

Similarly, if Complaint Counsel intend to suggest that this "good faith" language should have been understood as imposing some requirement to disclose intellectual property, Mr. Kelley's contemporaneous conduct again throws doubt on any such contention. As set forth

at RPF 192-197, Mr. Kelley repeatedly took the position that IBM would "not confirm or deny any [intellectual property] rights" held by IBM and that it would "not come to the committee with a list of applicable patents on standards proposals." (RX 420 at 1; JX 18 at 8). According to the official JEDEC meeting minutes, Mr. Kelley explained that "[i]t is up to the user of the standard to discover which patents apply." (JX 18 at 8).

The evidence shows that true to his word, neither IBM's Kelley nor any IBM representative added any IBM patents or patent applications to the "patent tracking list" maintained by Jim Townsend between December 1993 (when Kelley's statement was made) and December 1995 (Rambus's last meeting). (JX 18 at 14-21; JX 19 at 17-23; JX 20 at 15-18; JX 21 at 14-18; JX 22 at 12-17; JX 25 T 18-26; JX 26 at 15-24; JX 27 at 20-25; JX 28 at 12-23).

These contemporaneous documents tell us two things about the "good faith" language that Complaint Counsel rely upon:

(1) the JEDEC committee leadership certainly did not understand the language as imposing any mandatory requirements with respect to intellectual property disclosure; and

(2) any JEDEC representative sitting in the room at JC 42.3 meetings and observing the positions taken by, and conduct of, the subcommittee's own chairman would not have understood the "good faith" language of the Legal Guides to impose any mandatory requirements with respect to intellectual property disclosure.

313. Bad faith undermines the standard-setting process. (J. Kelly, Tr. 1841-42 ("bad faith undermines confidence of everyone in the process"), 1846-48 (discussing example of bad faith by deliberately shielding representative from patent information); 2134-35 & 2167-68 (discussing example of bad faith by trying to stall standardization process); G. Kelley, Tr. 2523-24 (planting a press story concerning dissension in JEDEC is bad faith and "undermines the

JEDEC process.")).

Rambus's Response to Finding No. 313:

This proposed finding is too vague to allow a specific response. The cited testimony is irrelevant in any event, since there is no evidence in the record that Rambus engaged in *any* of the conduct referenced in that testimony.

314. EIA and JEDEC must rely on the good faith of participants in the process to surface patent issues. (J. Kelly, Tr. 1836-37 (EIA relies on "the participants in the process to surface patent issues to our attention, and when those are surfaced, then we identify them in the standard, but if we don't know, we're not in a position to go out and find out either through the U.S. PTO or otherwise what intellectual property may be there.")).

Rambus's Response to Finding No. 314:

The cited testimony does not refer to "good faith" and does not suggest that disclosure obligations that were not set out in EIA's manuals were ever imposed on EIA or JEDEC members. The evidence instead shows the clear understanding of the JEDEC leadership that JEDEC members were "encourage[d]" to go "beyond the patent policy" but were not "required" to do so. (RX 1585 at 1).

D. JEDEC Standard Setting Is Not to be Conducted in a Manner That Would Result in Anticompetitive Effects.

315. Between 1991 and 1996, and continuing through today, Basic Rule 5 required that EIA/JEDEC activities "not be proposed for or indirectly result in . . . restricting competition, giving a competitive advantage to any manufacturer, [or] excluding competitors from the market." (CX0202 at 6; CX0204 at 5; J. Kelly, Tr. 1842-44, 1848-49 (discussing example of bad faith that could lead to patent royalties on television sets); CX0711 at 16 (Richard Crisp email from JEDEC meeting stating "The meeting opened with a lot of controversy regarding Patents. . . Micron says the policy exists due to anti-trust concerns. That if a group of companies wanted to keep out competition they could agree amongst themselves to standardize something that is patented and not license those that they do not want to compete with."); CX1958 at 12 ("Two possible theories of non-enforcement [of patents]:. . . 2) Antitrust?"), 21 (discussing monopolization in context of standard-setting activities)).

Rambus's Response to Finding No. 315:

The cited rule does not refer to intellectual property. It is highly unlikely that the cited rule was intended to impose any implicit obligations relating to disclosure of intellectual property, for the Legal Guides do contain a *specific* reference to intellectual property, where they state that a "basic objective[ ]" of all EIA standardization programs is that:

> "Standards are proposed or adopted by EIA without regard to whether their proposal or adoption may in any way involve patents on articles, materials, or processes."

(CX 204 at 4).

It is obvious that the rule cited in this proposed finding, with its references to "restricting competition" and "excluding competitors" (CX 204 at 5), relates to cartel activity (such as price-fixing or joint efforts to boycott a new technology). This rule would also bar a committee chair's use of his authority to favor his own company over another company. For example, this rule would clearly prohibit JC 42.3B subcommittee chair Gordon Kelley from unilaterally barring Rambus from presenting its technology for standardization, as Kelley says he did in May 1992, given that he had concluded just two weeks earlier that the RDRAM device presented a "risk" to IBM and that if RDRAM failed to become a standard, it would be "business as usual" for IBM and the SDRAM would have a "significant" chance of being standardized. (RX 279 at 7-8).

In short, the cited evidence does not support the proposed finding.

E. JEDEC Participants Must Comply With Patent Disclosure and Licensing Assurance Rules Intended to Ensure Open Standards.

1. The Patent Rules Are Intended to Foster Free Use of JEDEC Open Standards.

316. Between 1991 and 1996, and continuing through today, JEDEC has ensured that its standards were open through the JEDEC patent policy. (CX0449 at 2; J. Kelly, Tr. 1908 ("If there's no disclosure, then there's no opportunity to request the assurances"); G. Kelley, Tr. 2398-99 (prevent IP from "blocking" standards), 2475 (discussing letter to Texas Instruments concerning Quad CAS issue (CX2384) and the need to prevent development of mediocre standards); Landgraf, Tr. 1694 ("the purpose of the patent policy is to disclose and make sure that standards do not have any conflicts down the road with their potential use."); Lee, Tr. 6598 ("the general goal [of the patent disclosure policy] was to develop a standard that was free from encumbrance from patents, and so the purpose to disclose it was to be able to allow the committee to avoid the use of patents and incorporating them in the standard.")).

Rambus's Response to Finding No. 316:

This proposed finding is unobjectionable if it is re-phrased, in accord with the weight of the evidence, to state that JEDEC has "attempted through its patent policy 'to encourage the early, voluntary disclosure of patents'" covering JEDEC standards. (RX 669 at 3). Moreover, as the cited testimony confirms, and as stated in the EIA's January 1996 letter to the FTC, "the important issue" under the patent policy is "the license availability to all parties on reasonable, non-discriminatory terms." (RX 669 at 4).

317. Early disclosure provided JEDEC participants with the opportunity to choose a different, but equivalent path for the standard. (CX0903 at 2 (Richard Crisp writes: "The job of JEDEC is to create standards which steer clear of patents which must be used to be in compliance with the standard whenever possible."); CX0711 at 187 (Richard Crisp writes: "SSTL passed 30/0 and was sent to council. However Hitachi stated that they had a patent relating to it. This created a big ruckus. The major thrust of the criticism of Hitachi was that they waited until the ballots had been passed before mentioning that they had a patent"); CX0013 at 30 ("Problems in Intellectual Property - Some participants may look for commercial advantage. Late disclosure close to market interaction. Failure to indicate a patent is filed, pending or awarded . . . - Some participants might vote differently or develop different but equivalent standards if royalties were identified in the beginning as an objective."); CX0711 at 44 (Richard Crisp noting that Micron cited patents as reason for its "No" vote.); CX3005 at 1

("We [Toshiba] understand from Micron and Cyrix there is also concern on the infringement of Intel's burst patent . . . a pin was dedicated to burst mode, making it selectable, *to side step the patent issue*.") (emphasis added); CX0083 at 5-6 (two ballots were put on hold pending resolution of status of patent owned by Sun Microsystems.); Sussman, Tr. 1343 ("The earlier that we have the information that something may have some IP on it, the better it turns out to be, so we don't waste time talking of this rather than an alternate."); Landgraf, Tr. 1693-94 ("The policy, as I understood it, was that if you as a member of JEDEC knew of a patent or application for a patent that would potentially be impacting the standard or proposed standard, you were to disclose it to the committee for -- for consideration so the committee could decide to either modify the standard proposal. . . so that it did not infringe with the application or the patent.")).

Rambus's Response to Finding No. 317:

To be accurate, this proposed finding should be re-phrased so that it refers to "early, voluntary disclosure. . . ." The weight of the evidence shows that the "early disclosure" referred to in this proposed finding was *encouraged*, but not required. JEDEC's official position on this issue is found in its February 2000 Board minutes:

> "D. Disclosure on Patents Pending
>
> Mr. Walther noted that Micron had sent a letter indicating they have patents pending on items that may affect committee standards. The issue was whether companies should make public that a patent is pending. The BoD discussed it and noted they *encourage* companies to make this kind of disclosures even though they were not *required* by JEDEC bylaws."

(RX 1570 at 13) (emphasis added). *See also* (RX 669 at 2) (statement in EIA 1/22/96 letter to FTC that the EIA "encourage[s] the early, voluntary disclosure of patents that relate to the standards in work"); (RX 742 at 1) (statement in JEDEC Secretary's 7/10/96 memorandum to JEDEC Council members that the EIA "encourage[s] early voluntary disclosure of any known essential patents"); (RX 740 at 1) (statement in 7/10/96 letter by FTC Secretary Donald Clark

that the EIA "encourage[s] the early, voluntary disclosure of patents, but do[es] not require a certification by participating companies regarding potentially conflicting patent interests"); (CX 3 at 6) (statement in JC 42.1 minutes from September 1989 that question regarding patents had been added to ballot form "for information only and was not going to be checked to see who said what"); (RX 1585 at 1) (statement in JEDEC Secretary's 2/11/00 e-mail that "[d]isclosure of patents is a very big issue for Committee members and cannot be required of members at meetings"); (JX 18 at 8) (statement in 12/93 JC 42.3 minutes that "IBM noted that in the future they will not come to the committee with a list of applicable patents on standards proposals. It is up to the user of the standard to discover which patents apply"); Wiggers, Tr. 10592-93 (testimony by JEDEC Council member Hans Wiggers that he and Gordon Kelley had each stated at a 42.3 meeting that they would not disclose patent applications).

2. JEDEC Participants Must Disclose Patents or Pending Patents That Might Be Involved In The JEDEC Work.

318. The JEDEC patent policy contains two distinct parts. First, all participants in the process are subject to a mandatory duty to disclose intellectual property that might be involved in the work of the committee. Second, the chairperson of the meeting has a duty to to ensure that no known patented or patentable material is included in a JEDEC standard unless the committee has received advance, written assurance from the owner of the intellectual property to that the owner will license the intellectual property for free or on reasonable and non-discriminatory terms. (CX0208 at 19; CX0208A at 19 (copy of 21-I Manual produced by Rambus); CX2076 at 80-81 (Brown Infineon Dep.) ("any members who are aware of any patent position or potential patent positions on the material should and are obligated to reveal that to the committee at that time."); CX2191 at 8 (JEDEC policy is to not standardize patented items without fair licensing; all participants are requested to reveal patents)).

Rambus's Response to Finding No. 318:

This proposed finding relies almost entirely upon the language of JEDEC manual 21-I (CX 208; CX 208A). It was Complaint Counsel's burden to prove that the 21-I manual became

effective. It was undisputed at trial that to be effective, the 21-I manual required EDEC approval. (Kelly, Tr. 2105). No witness testified that the 21-I manual had been approved by EDEC. EIA General Counsel John Kelly testified that although he had access to EDEC minutes, he did not know whether the 21-I manual had received EDEC approval. (Kelly, Tr. 2105). Accordingly, Complaint Counsel may not rely upon the language of the 21-I manual to show that JEDEC members agreed to mandatory disclosure obligations.

The deposition testimony by JEDEC consultant Reese Brown is similarly unreliable. Your Honor has previously found that Mr. Brown lacked the necessary foundation at the time of his *Infineon* deposition to opine about disclosure obligations at JEDEC. Moreover, after Mr. Brown was shown the 21-I manual at his deposition in this case, he revised his testimony to state that members had *no* disclosure obligation at the time of a first presentation. (CX 2110 at 63).

Moreover, the text of the 21-I manual does not support the broad disclosure obligation proposed by Complaint Counsel in any event. The operative language of Section 9.3.1 is directed only at JEDEC chairpersons, telling them how they are to communicate the EIA/JEDEC patent policy to members. (CX 208 at 19). 21-I indicates that this obligation of JEDEC chairpersons is, in fact, fully discharged by showing members a specific slide – "Appendix E" – whose text says *nothing* about a disclosure obligation. (CX 208 at 26-28). Of course, it is undisputed the JC 42 leadership did *not* routinely show the 21-I viewgraphs at meetings and instead used *EIA* policy language in their presentations. (*See*, *e.g.*, JX 20 at 15-16; JX 21 at 14-15; JX 22 at 12-13; JX 25 at 18-19; JX 26 at 15-16). This is strong evidence that 21-I never received the necessary EDEC approval and did not become effective.

Even if Complaint Counsel is correct, moreover, that the 21-I manual was both in force and required disclosure of patents and patent applications, it is undisputed that it was not published and therefore not effective before October 1993, *after* the SDRAM standard had passed all necessary committee and council ballots. (CX 208 at 1; CX 54 at 8-10; JX 15 at 4, 99).

In any event, there is overwhelming evidence from contemporaneous documents that JEDEC and its members understood that the disclosure of intellectual property interests was *encouraged* and *voluntary*, not required or mandatory. (RX 669 at 2) (statement in EIA 1/22/96 letter to FTC that the EIA "encourage[s] the early, voluntary disclosure of patents that relate to the standards in work"); (RX 742 at 1) (statement in JEDEC Secretary's 7/10/96 memorandum to JEDEC Council members that the EIA "encourage[s] early voluntary disclosure of any known essential patents"); (RX 740 at 1) (statement in 7/10/96 letter by FTC Secretary Donald Clark that the EIA "encourage[s] the early, voluntary disclosure of patents, but do[es] not require a certification by participating companies regarding potentially conflicting patent interests"); (CX 3 at 6) (statement in JC 42.1 minutes from September 1989 that question regarding patents had been added to ballot form "for information only and was not going to be checked to see who said what"); (RX 1570 at 13) (statement in 2/00 JEDEC Board minutes that "the BOD discussed" the question of whether "companies should make public that a patent is pending" and "noted they encourage companies to make this kind of disclosure even though they were not required by JEDEC bylaws"); (RX 1585 at 1) (statement in JEDEC Secretary's 2/11/00 e-mail that "[d]isclosure of patents is a very big issue for Committee members and cannot be required of members at meetings"); (JX 18 at 8) (statement in 12/93 JC 42.3 minutes that "IBM noted that in

the future they will not come to the committee with a list of applicable patents on standards proposals. It is up to the user of the standard to discover which patents apply").

319. The JEDEC patent disclosure policy is that:

> "The Chairperson of any JEDEC committee, subcommittee, or working group must call to the attention of all those present the requirements contained in EIA Legal Guidelines, and call attention to the obligation of all participants to inform the meeting of any knowledge they may have of any patents, or *pending patents*, that might be involved in the work they are undertaking."

(CX0208 at 19; CX0208A at 19) (emphasis added); (J. Kelly, Tr. 1837-38 (The EIA/JEDEC patent policy "requires an early disclosure of intellectual property; that is, patents or patent applications that are or may be related to the work of a standard-setting committee. And then once the disclosure -- the early disclosure is made, if the patent owner is willing to give reasonable assurances that I alluded to earlier, that is, reasonable and nondiscriminatory licensing terms or without charge."); Rhoden, Tr. 307 ("The JEDEC patent policy is essentially if you have IP, IP that may relate to any of the discussions that are going on inside JEDEC, that you are required to disclose that IP to the people who are participating."); Lee, Tr. 6595-96 ("[T]here was a requirement to disclose patents or patent applications in progress to the committee if the work that they were doing may relate or if the patent may relate to the work the committee was doing."); Sussman, Tr. 1333 ("Q. What is your understanding of the JEDEC patent policy that was in effect from the 1991 to '96 time period? A. Basically, if you have IP, you are to inform the group of that IP."); Landgraf, Tr. 1693-94 ("The policy, as I understood it, was that if you as a member of JEDEC knew of a patent or application for a patent that would potentially be impacting the standard or proposed standard, you were to disclose it to the committee. . . so the committee could decide to either modify the standard proposal. . .so that it did not infringe with the application or the patent, or the committee would then ask . . . the owner of the patent . . .whether they would comply with the JEDEC policy, which had to do with granting licenses either freely to all applicant requesters or offer the patent on reasonable terms and conditions. In a nutshell, that was the policy."), 1702 ("when I first joined JEDEC, [the manual containing the patent policy] was at Revision I, and subsequent it was revised to Revision J, but Manual 21-I is the standards and policies."); Williams, Tr. 771 ("if somebody had a patent or pending patent based upon the work that was being discussed at JEDEC, that there needed to be disclosure of sufficient information so that the council or the committee could determine whether or not what was being discussed was actually implied in the patent."), 790 ("I don't know exactly what the JEP stands for, but it is a manual that guides the policies of JEDEC, how the JEDEC ought to operate."); CX2076 at 80-81 (Brown Infineon Dep.) ("whenever material comes up in the committee for discussion and for voting, any members who are aware of any patent position or potential patent positions on the material should and are obligated to reveal that to the committee at that time."); Calvin, Tr. 1004 ("anyone who was aware of patend - - patented items, that could

affect policy, had an obligation to bring that awareness to the group.")).

Rambus's Response to Finding No. 319:

This proposed finding is not supported by the weight of the evidence. The only document cited in support of the finding is JEDEC manual 21-I. As noted in Rambus's responses to finding nos. 308 and 318, Complaint Counsel did not establish that manual 21-I ever received approval by the EIA's Engineering Department Executive Council, although it was undisputed that such approval was required before 21-I could become effective. (Kelly, Tr. 2105). Nor did Complaint Counsel establish that the language of the manual actually communicated a disclosure obligation in any event, given its statement that a committee chairman should discharge his duty to inform committee members of their own obligations by showing them a viewgraph that did not refer to a disclosure obligation. (CX 208 at 19, 27). For all of these reasons, Complaint Counsel may not rely upon the language of the 21-I manual to show that a disclosure obligation existed with respect to patent applications.

Moreover, the weight of the evidence demonstrates that: (1) disclosure of intellectual property interests was encouraged, but not required; and (2) if there was a disclosure obligation, it extended only to issued patents, not patent applications. *See* Wiggers, Tr. 10592-93 (testimony by JEDEC Council member Hans Wiggers that he and Gordon Kelley had each stated at a 42.3 meeting that they would not disclose patent applications); (RX 669 at 2) (statement in EIA ½2/96 letter to FTC that the EIA "encourage[s] the early, voluntary disclosure of patents that relate to the standards in work"); (RX 742 at 1) (statement in JEDEC Secretary's 7/10/96 memorandum to JEDEC Council members that the EIA "encourage[s] early voluntary disclosure of any known essential patents"); (RX 740 at 1) (statement in 7/10/96 letter by FTC Secretary Donald Clark

that the EIA "encourage[s] the early, voluntary disclosure of patents, but do[es] not require a certification by participating companies regarding potentially conflicting patent interests"); (CX 3 at 6) (statement in JC 42.1 minutes from September 1989 that question regarding patents had been added to ballot form "for information only and was not going to be checked to see who said what"); (RX 1570 at 13) (statement in 2/00 JEDEC Board minutes that "the BOD discussed" the question of whether "companies should make public that a patent is pending" and "noted they encourage companies to make this kind of disclosure even though they were not required by JEDEC bylaws"); (RX 1585 at 1) (statement in JEDEC Secretary's 2/11/00 e-mail that "[d]isclosure of patents is a very big issue for Committee members and cannot be required of members at meetings"); (JX 18 at 8) (statement in 12/93 JC 42.3 minutes that "IBM noted that in the future they will not come to the committee with a list of applicable patents on standards proposals. It is up to the user of the standard to discover which patents apply"); (RPF 242-273) (evidence that numerous JEDEC attendees who were named inventors on pending patent applications (including JEDEC Chairman Desi Rhoden) that were related to JEDEC's standard-setting work did not disclose those applications).

As these citations demonstrate, the overwhelming weight of the *contemporaneous* evidence supports a finding that disclosure was encouraged, but not required, as well as a finding that even if some members believed disclosure to be mandatory, any obligation did not extend to applications. The testimony to the contrary that Complaint Counsel cite is almost entirely from employees of DRAM manufacturers or others who would profit from the remedy sought in this case. Contemporaneous documents should be given greater weight than after-the-fact testimony by interested witnesses.

320. The JEDEC patent disclosure rule applied not only to issued patents, but also to patent applications and anything in the patent process. (CX0208 at 19; CX0208A at 19; JX0014 at 25; CX0306 at 1; CX0042A at 7 (Townsend memo produced by Rambus referring participants to "existing rules of EIA governing *patentable matters*) (emphasis added); CX2957 at 2 (Declaration of Joel Karp) ("contrary to industry practice and understanding for an *intellectual property* owner to remain silent during the standard-setting process – and then after a standard has been adopted and implemented – later attempt to assert that its *intellectual property* covers the standard") (emphasis added); CX2059 at 150-51 (Karp, Infineon Dep.) (verifying veracity of declaration); Calvin, Tr. 1006-07 (clear about fact that patent applications were required to be disclosed); Kellogg, Tr. 5024; J. Kelly, Tr. 1869-70; 1886-88 (term "patent" included patent applications), 1893-94, 1896-97 ("The industry probably moves even more quickly, particularly in high technology industries like the ones that EIA works with, and frequently patent applications move at a measured pace through the patent application policy to the issuance of final patents. So, if the work of the committee was held up, in effect, by the condition that only issued patents needed to be disclosed, then the standard development process could reach a very late stage or, in fact, already be concluded by the time a patent finally issued and there was disclosure that the patent was required to comply with the work by the committee on the standard under development, and that would produce exactly the same kind of anti-competitive result that we're trying to prevent by the disclosure."); G. Kelley, Tr. 2406-07 ("patent" as used by Mr. Townsend meant "an issued patent that was available from the patent office, patent applications that were being worked on with the patent office, and items that were probably going to become patents."), 2689 ("I would have thought that that new member would understand that it included patent applications from the beginning because we were dealing with patent applications from that new member's beginning and was clearly an issue at my meetings."); Landgraf, Tr. 1695-96 ("As soon as a member knew that they had -- either they had a patent of their own or applications or even a third party's patent or application, if you knew that and it was touching on some element of the standard or proposed standard, you were supposed to disclose that to the committee so that the committee has the earliest possible time to make changes or to have patent policy compliance."); Lee, Tr. 6595-96 ("the patent policy had a few aspects to it. First of all, there was a requirement to disclose patents or patent applications in progress to the committee if the work that they were doing may relate or if the patent may relate to the work the committee was doing. There was also a policy, as I understand, to -- to try to avoid the use of patents, when possible, in defining a standard."); CX2057 at 211-12 (Meyer 12/13/00 Dep.) (understood that "patents" included patent applications); Rhoden, Tr. 307, 317-21 ("patent" has always been applied to anything in the patent process), 336 ("patentable" includes whether or not a patent has been applied for), 618-19, 626-27; Sussman, Tr. 1333-34 ("issued patents, patent applications . . . if you were about to apply for a patent"), 1342 (understood in 1981 or 1982 that patent policy required disclosure of patent applications); Williams, Tr. 771 ("patent or pending patent"), 909-11); CX2076 at 80-81 (Brown Infineon Dep.) ("Issued patents and pending patent material"); McGrath, Tr. 9272-73 ("JUDGE McGUIRE: But also this obligation to act in good faith, did that incorporate the idea of disclosing patent applications as they were being developed? THE WITNESS: Yes, it would."); (CX2054 at 165 (Mooring, Infineon Dep.)). [note: R objection pending] ("if [Manual of Organization and Procedure 21-I] was the valid document, then there

would be requirement to disclose applications.")).

Rambus's Response to Finding No. 320:

The cited documents do not support the proposed finding, as is shown below:

- CX 208 and CX 208A are copies of the 21-I manual. Complaint Counsel did not prove that 21-I ever received the necessary EDEC approval. (Kelly, Tr. 2105).
- JX 14 refers to "draft" patent policy language; again, there was no evidence that the "draft" language ever received the necessary EDEC approval. (JX 14 at 3, 25).
- CX 306 is a blank, undated "Meeting Attendance Roster" that refers members not to manual 21-I but to the EIA Legal Guides and manuals. (CX 306 at 1-2). The second page of the "Roster" refers to "known patent[s]"; JEDEC Council chairman Gordon Kelley testified that he understood that the EIA used this phrase to refer to issued patents only. (Kelley, Tr. 2686-87; 2695-97).
- CX 42A is simply a set of 42.3 meeting minutes; like most minutes, it contains a Jim Townsend memorandum about patents that is addressed only to certain JEDEC members, not to Rambus, and that contains the EIA manual excerpts, not JEDEC manual excerpts. (CX 42A at 7-8).
- CX 2957 is a declaration by Joel Karp that refers to "intellectual property," not to patent applications or to what Complaint Counsel's proposed finding refers to as "anything in the patent process."(CX 2957 at 2).

In contrast to these unapproved manuals, drafts, and miscellaneous documents containing ambiguous language, there are numerous trial exhibits that state clearly that the disclosure of

patent applications or of intent to file or amend patent applications was, at most, *encouraged*, not required. (RX 1570 at 13) (statement in 2/00 JEDEC Board minutes that "the BoD discussed" the question of whether "companies should make public that a patent is pending" and "noted they encourage companies to make this kind of disclosure *even though they were not required by JEDEC bylaws*") (emphasis added); (RX 1585 at 1) (statement in JEDEC Secretary's 2/11/00 e-mail that a company that discloses patent applications has "gone one step beyond the patent policy," which JEDEC "encourages"); (RX 669 at 2) (statement in EIA 1/22/96 letter to FTC that the EIA "encourage[s] the early, voluntary disclosure" of patents); (RX 742 at 1) (statement in JEDEC Secretary's 7/10/96 memorandum to JEDEC Council members that the EIA "encourage[s] early voluntary disclosure of any known essential patents"); (RX 740 at 1) (statement in 7/10/96 letter by FTC Secretary Donald Clark that the EIA "encourage[s] the early, voluntary disclosure of patents, but do[es] not require a certification by participating companies regarding potentially conflicting patent interests"); (RX 616 at 2) (EIA manual 7-B, published in October 1995, provides that EIA standards are adopted "in accordance with the [ANSI] patent policy," which does not require disclosure of patent applications, *see* Kelly, Tr. 1958, 2074); (CX 353 at 1) (ANSI patent policy guidelines circulated to 42.3 members at Mr. Kelly's request); (RX 669 at 2) (1/22/96 EIA letter to FTC states that EIA "follow[s] the ANSI Intellectual Property Rights ("IPR") policy . . . ."); (RX 669 at 4) (1/22/96 EIA letter to FTC stating that ". . . if knowledge of a patent comes later in time *due to the pending status of the patent* while the standard was being crafted, the important issue is the license availability to all parties on reasonable, non-discriminatory terms") (emphasis added); (CX 3 at 6) (statement in JC 42.1 minutes from September 1989 that question regarding patents had been added to ballot form "for

information only and was not going to be checked to see who said what").

Complaint Counsel's proposed finding does find some support in the trial testimony it cites. Most of that testimony is from the representatives of manufacturers who would benefit from the remedy sought. The after-the-fact testimony of interested witnesses should be given less weight than contemporaneous documents. Much of the testimony is also so ambiguous to be of little probative value. Gordon Kelley's testimony that the disclosure obligation extended to "items that were probably going to become patents" is a disclosure standard that would be impossible to understand or implement, given the uncertainties of the patent process. (Kelley, Tr. 2406-07). Kelley's fellow IBM representative Mark Kellogg, who was the only JEDEC representative to testify that he had ever disclosed an intent to file an application, testified in his pre-trial deposition that he did *not* believe at the time that he made that disclosure that the disclosure was required by the JEDEC patent policy. (Kellogg, Tr. 5306). At trial, however, he amended his testimony to say that he understood that while disclosure was not required by the *written* JEDEC patent policy, he believed there to have been "more than one JEDEC patent policy" relating to such disclosures, including "an in-process modified policy" and "an expected policy." (Kellogg, Tr. 5306-07). The testimony on this issue by Intel's JEDEC representative, Sam Calvin, is similarly ambiguous and supports only a finding that memories fade over time:

> "There was – and I don't know when it occurred or how early it occurred, but there was a concern about not only patents, but applications for patents. And I'm then real foggy on this, because I knew it was an issue, but when exactly it went from an issue to understanding that to be JEDEC policy is unclear in my mind."

(Calvin, Tr. 1006).

Complaint Counsel also grossly misrepresent the nature of Mr. McGrath's testimony on this issue. Complaint Counsel quote only the first few words of an exchange between Your Honor and Mr. McGrath, the longtime JEDEC representative from Molex. Here is the portion quoted by Complaint Counsel in support of this finding:

> "JUDGE McGUIRE: But also this obligation to act in good faith, did that incorporate the idea of disclosing patent applications as they were being developed?
>
> THE WITNESS: Yes, it would."

(McGrath, Tr. 9273, *quoted in* Complaint Counsel's proposed finding No. 320). Here is the *full* exchange between Your Honor and the witness, in which the witness explains that he is referring to *presenters*:

> "JUDGE McGUIRE: But also this obligation to act in good faith, did that incorporate the idea of disclosing patent applications as they were being developed?
>
> THE WITNESS: Yes, it would. And I look at that as there's two scenarios that can occur in that good faith: One, if I'm the person doing the proposal for this technology and I'm developing technology that I'm going to patent I think it's my responsibility to tell the group that that's what I'm doing.
>
> If I'm developing technology and I'm one of the attendees listening to somebody else present something and – what I do at that point is I – I

may not know enough information from this first showing or even the second showing to see where this technology is going, and I don't want to disclose what I'm doing in confidence within the company until I'm sure that these two things are going to cross at some point.

So there's – *the good faith that I'm talking about is if I'm making the presentation, if I'm trying to take JEDEC down this particular technology road, that's what I'm referring to*."

(McGrath, Tr. 9273-4) (emphasis added).

Mr. McGrath's testimony thus does not support a finding that *non*-presenters were obligated or expected to disclose patent applications. Instead, it supports a finding that some JEDEC members expected that if another member was "making the presentation [and] trying to take JEDEC down this particular technology road," that member should in good faith disclose that it has applied for patent coverage. (*Id*.). Such a view is consistent with traditional principles of equitable estoppel and with the advice Lester Vincent had given Rambus. It is undisputed, however, that such expectations were never triggered with respect to Rambus, for Rambus made no presentations at JEDEC and did not encourage JEDEC to adopt any feature or technology over which it later claimed patent coverage.

321. The EIA/JEDEC patent policy did not change during the 1990s. (J. Kelly, Tr. 1920 (since 1990 "sometimes the words have changed, but the substance has not.")).

Rambus's Response to Finding No. 321:

Mr. Kelly's testimony about the unchanging nature of the "EIA/JEDEC patent policy" is contrary to the weight of the evidence. Many of the JEDEC representatives who testified said

that they understood the policy to be undergoing transformation and to be in flux during the early and mid 1990's. (Calvin, Tr. 1006 – "foggy" recollection of changes involving applications); (Kelley, Tr. 2669, 2686-87, 2692 – recollection of wholly undocumented "hand vote" at 42.3 meeting in 1991 that supposedly *added* new disclosure obligations regarding applications); (Kelley, Tr. 2678 – recollection that only *some* JEDEC committees required disclosure of patent applications prior to October 1993); (Kellogg, Tr. 5306-07 – referring to at least three *simultaneous* versions of the JEDEC patent policy: the written policy, the "in-process modified policy," and the "expected policy"). The ambiguous and "foggy" nature of the various witnesses' recollections demonstrates three important points: (1) the need to rely upon the language of contemporaneous documents rather than 10-year-old recollections of interested witnesses; (2) the absence of any common understanding among JEDEC members, or even among JEDEC leaders, about the contents of the JEDEC patent policy; and (3) the ultimate correctness of the Federal Circuit's description of that policy as having a "staggering lack of defining details." *Rambus Inc. v. Infineon Technologies*, 318 F.3d 1081, 1102 (Fed. Cir. 2003).

322. The EIA Legal Guides prohibit the sharing of future plans at EIA sponsored meetings. (CX0202 at 4). There is no tension between the prohibition on discussing future plans and the requirement to disclose patent applications that might relate to JEDEC standards. (J. Kelly, Tr. 1989 ("I don't see that there's any tension there at all."). The future plans that are subject to the prohibition in the EIA Legal Guides are discussions of plans that would result in a violation of the antitrust laws. (J. Kelly, Tr. 1989 ('t]he future plans that were referred to in the EIA Legal Guides are discussions that could result in conduct prohibited by the antitrust laws.")).

Rambus's Response to Finding No. 322:

As noted above, the weight of the evidence does not support a finding that there was a "requirement to disclose patent applications," as the second sentence of this finding states. *See* RRFF 311 and 317-320. The EIA Legal Guides – the only authority referred to in this finding –

make no reference to disclosure of patent applications *or* patents.

The cited evidence also does not support the second sentence. Mr. Kelly did not draft the Legal Guides. Even using *his* description of the "future plans" referred to in the Legal Guides ("discussions that could result in conduct prohibited by the antitrust laws"), the rules would plainly discourage or prohibit the discussion of future intentions with respect to intellectual property. It is unlawful for manufacturers to reach agreement on the price they will pay for licensing intellectual property. It is also unlawful for manufacturers to reach agreement not to license a particular company's technology. The evidence nevertheless shows that top executives of DRAM manufacturers met in Japan in January 1997 and talked about whether Rambus's RDRAM royalty rates were "acceptable" or too high. (CX 2250 at 2 – Terry Lee's notes of the 1/97 meeting showing that Siemens executive Dr. Von Zitzewitz told the other executives that a license "is ok" for a "niche" memory, "but not for main memory," and that "0.1% royalty would have been ok," but that Rambus "is not acceptable." (CX 2250-2).

Given this evidence, and the other substantial evidence of concerted activity among the DRAM manufacturers who attend JEDEC meetings, it is certainly possible that unlawful agreements regarding royalty rates, or unlawful agreements to exclude a company's products, "could result" from disclosures at JEDEC about a company's future intentions with respect to intellectual property. If a company were required to disclose, for example, that it might someday apply for intellectual property rights with respect to a certain feature, the manufacturers could in private agree to pay no more than a certain royalty rate before standardizing the technology. That prospect is more than sufficient to trigger Mr. Kelly's definition of the "future plans" whose discussion is prohibited by the Legal Guides. (Kelly, Tr. 1989: "[t]he future plans that were

referred to in the EIA Legal Guides are discussions that *could* result in conduct prohibited by the antitrust laws.") (emphasis added).

3. Disclosure is Mandatory.

323. Membership in JEDEC is voluntary. (J. Kelly, Tr. 1966 ("The entire process is voluntary, and as a voluntary standards development organization, we really don't have the power to impose sanctions against members who don't comply with the policy."); Rhoden, Tr. 615 ("participation in the committees is always voluntary.")).

Rambus's Response to Finding No. 323:

Rambus has no specific response.

324. Once a member joins JEDEC, however, the obligations that participants assume are mandatory requirements of participation. (CX0208 at 19 ("the obligation of *all participants* to inform the meeting of any knowledge they may have of any patents, or pending patents that might be involved in the work they are undertaking") (emphasis added); J. Kelly, Tr. 1903-04 ("is it optional on the part of someone with knowledge of a patent or patent application to disclose or not disclose, *the answer is absolutely no, it is not optional*"), 1979 ("any time a participant has knowledge of relevant intellectual property, patent or patent application, that is or may be required to comply with the work underway, then that participant has an absolute duty to disclose it."); Lee, Tr. 6595-96 ("there was a *requirement* to disclose patents or patent applications in progress to the committee if the work that they were doing may relate or if the patent may relate to the work the committee was doing."); Rhoden, Tr. 319, 615 (disclosure is an obligation); Sussman, Tr. 1346 ("Q. Again, based on your experience, did you view this patent disclosure policy we have been discussing as a voluntary option or was it a mandatory requirement on JEDEC members? A. *It's required.*"); CX2057 at 200 (Meyer 12/13/00 Dep.) (disclosure is an obligation); CX0711 at 188 (Richard Crisp noting that "So the conclusion I reach here is that we can abide by the patent policy on a case by case basis. . . As long as we mention that there are potential patent issues when a showing or ballot comes to the floor, the we have not engaged in 'inequitable behavior. . . The things we should not do are to not speak up when we know that there is a patent issue.")).

Rambus's Response to Finding No. 324:

This proposed finding is contrary to the weight of the evidence. The application form that Rambus filled out when it joined JEDEC said nothing at all about any disclosure obligations. (CX 601 at 1-2). The JEDEC manual that was in effect at the time Rambus joined and at the

time the SDRAM standard was approved said only that JEDEC standards were adopted "without regard" for whether they involve patents. (CX 205A at 11). When JEDEC added language on its ballot form asking members to "please" inform the committee of "patents involving this ballot," the members were explicitly told that they need not be concerned about inaccurate or incomplete disclosures: "the question was added on ballot voting sheets for information only and was not going to be checked to see who said what." (CX 3 at 6 – 9/13/89 JC 42.1 official meeting minutes).

Numerous other contemporaneous documents state explicitly that members were only "encouraged" to make "voluntary" patent-related disclosures. (RX 669 at 2; RX 740 at 1; RX 1570 at 13; RX 1585 at 1; JX 18 at 8; RX 742 at 1). *See* RPF 128-185. JEDEC manual 21-I (CX 208), on the other hand, the *only* JEDEC document that this finding cites, was never shown to have become effective. (Kelly, Tr. 2105).

This finding also cites a portion of a December 1995 e-mail by Richard Crisp. The truncated quotation is highly misleading. The e-mail itself shows that Mr. Crisp was discussing what he understood Rambus should do *if it decided* to bring the Rambus module to JEDEC for standardization. (CX 711 at 188; Crisp, Tr. 3479-3485: "I was referring to what we would have to do and what we should not do in the event that we were to propose the R-module as a standard.").

Complaint Counsel's failure to note that in the last sentence of the quote from Mr. Crisp's e-mails, they had *cut off* the quote in the middle of the sentence, is troubling, for it changes the meaning of Mr. Crisp's comments in a way that appears intentional. Here are the two versions of the finding's last sentence:

CCFF 324

"The things we should not do are to not speak up when we know that there is a patent issue."

Complaint Counsel chose to use a period, not an ellipsis, to end the sentence, even though the sentence in the e-mail continues. Here is the actual comment from the Crisp e-mail:

CX 711 at 188

"The things we should not do are to not speak up when we know that there is a patent issue, to intentionally propose something as a standard and quietly have a patent in our back pocket we are keeping secret that is required to implement the standard and then stick it to them later (as WANG and SEEQ did). I am unaware of us doing any of this or of any plans to do this."

(CX 711 at 188)

Clever editing is no substitute for evidence. The e-mail is about *presenting* and *advocating* a technology for standardization. The e-mail is consistent with settled principles of equitable estoppel and with Lester Vincent's advice to Mr. Crisp about his involvement with JEDEC. It is undisputed that Rambus did not encourage, advocate or promote the adoption of any technology at JEDEC. Complaint Counsel's efforts to twist the meaning of this e-mail are inappropriate.

4. The Disclosure Obligation Does Not Include A Duty to Conduct a Patent Search.

325. EIA and JEDEC did not require members to conduct patent searches. (J. Kelly, Tr. 1869-70, 1966-67; G. Kelley, Tr. 2457-58 (IBM did not agree to provide a list of patents because

IBM was concerned that bringing a list to JEDEC might erroneously be construed as a complete catalog of IBM patents in a particular area); Williams, Tr. 895-96 (discussing IBM's statement); CX2057 at 193 (Meyer 12/13/00 Dep.)). *See also* (RX1712 at 8 (no duty to search under ANSI Guidelines)).

Rambus's Response to Finding No. 325:

Rambus agrees with the finding as stated.

326. From time to time, however, JEDEC participants made requests for other participants to clarify their companies' patent position relating to specific items. In these instances, participants fulfilled their obligations under the patent policy by acting in good faith. For example, at the May 1992 JC-42.3 meeting, patent issues were raised concerning Hitachi's LOC package proposal. Hitachi's representative, Mr. Tabrizi, did not know about the patent, but promised the committee that he would check on it. (CX0034 at 8). At the July 1992 JC-42.3 meeting, concern about patent coverage was noted relating to a Hitachi presentation. (JX0013 at 13). At the September 1992 JC-42.3 meeting, Hitachi noted that it did not have a patent on the proposal. (CX0042 at 9). Ultimately, JEDEC chose a different path to develop the standard because of the difficulty in reviewing the patent issues on the matter. (JX0015 at 4).

Rambus's Response to Finding No. 326:

None of the cited exhibits refer to good faith or to any obligations under the patent policy. In addition, the last sentence of this proposed finding is plainly false. JX 15 – the March 1993 42.3 meeting minutes – do not state that *JEDEC* "chose a different path to develop the standard. . .," as the finding asserts. Instead, the minutes state that *Hitachi* "had chosen to use EIAJ as a path to develop its standard. . . ." (JX 15 at 4).

327. Similarly, among the patent matters discussed at the March 1993 Committee meeting was an inquiry made to IBM concerning whether IBM would disclose to the Committee all patents and patent applications held by the company worldwide. (G. Kelley, Tr. 2449-50; JX0015 at 6). Because of the breadth and difficulty of the company-wide search that would be required for such a listing, there was a risk that any such listing would be incomplete and misleading, therefore IBM stated that it would not undertake such a listing. (G. Kelley, Tr. 2450-51).

Rambus's Response to Finding No. 327:

The proposed finding adopts Gordon Kelley's explanation at trial of the statements

attributed to him in the official March 1993 JC 42.3 meeting minutes. Those minutes state that:

> "IBM noted that their view has been to ignore patent disclosure rule because their attorneys have advised them that if they do then a listing may be construed as complete."

(JX 15 at 6).

Mr. Kelley testified at trial that this passage was inaccurate and that what *really* happened was that the 42.3 committee asked him to provide a list of *all* patents and applications that IBM might have relating to "all issues at all levels of the computer business." (Kelley, Tr. 2450). Mr. Kelley testified that he declined to provide such a list. (*Id*.).

The minutes contain no reference to any request that IBM list every single computer-related patent or patent application filed by IBM, and it is illogical, and inconsistent with other testimony and with the actual language of the minutes, to think that such a request occurred. Mr. Kelley's fanciful explanation of the unambiguous language of the minutes is not just inconsistent with the minutes; it is also inconsistent with other contemporaneous documents. In August 1993, for example, Mr. Kelley sent a memorandum to JEDEC entitled "BGA/Patent/License Rights" that states in part that:

> "It is the responsibility of the producer to evaluate the subject and work out the proper use of rights. So, I can not confirm or deny any IPL [intellectual property law] rights."

(RX 420 at 2).

Mr. Kelley cannot claim that the memorandum is inaccurate, for he prepared and sent it. The memorandum says nothing about there being too many patents to review or disclose. It says,

in plain English, that it is up to the *manufacturer* to figure out what patent-related rights are involved and to "work out the proper use" of those rights. (*Id.*). This same theme – that manufacturers have an obligation to consider and resolve patent issues – appears in the EIA's 1/22/96 letter to the FTC, which explains that "[a]ll companies will review the final standard that emerges if they intend to build product to that standard. They will check the state of the art and patent situation to assess which patent rights will require licensing." (RX 669 at 4).

Additional evidence regarding the true nature of Mr. Kelley's comments is found in the December 1993 JEDEC meeting minutes, which state that "IBM noted that in the future they will not come to the Committee with a list of applicable patents on standards proposals. It is up to the user of the standard to discover which patents apply." (JX 18 at 8).

The consistency of these statements, and the unlikeliness that the 42.3 Committee would have ever asked IBM for a list of every single computer-related patent or patent application it held, render less than credible Mr. Kelley's attempts to deny or explain away the statements.

And the proof is in the pudding. After these statements appeared in the minutes, no IBM patent or patent application was added to the "patent tracking list" maintained by JC 42 Chairman Jim Townsend, at least prior to Rambus's departure from JEDEC). (JX 18 at 14-21; JX 19 at 17-23; JX 20 at 15-18; JX 21 at 14-18; JX 25 at 18-26; JX 26 at 15-24; JX 27 at 20-25; JX 28 at 12-18). This shows that IBM acted for years in accordance with the statements attributed to Mr. Kelley in the minutes.

In short, Complaint Counsel's proposed finding, which accepts Mr. Kelley's implausible, after-the-fact explanation of statements contained in JEDEC meeting minutes, is sharply contradicted by the weight of the evidence.

328. Despite the fact that IBM was under no duty to search its patent portfolio, IBM representatives agreed to inform the JC-42 committee of any relevant patents, patent applications or items in the patent process of which they were aware, and to investigate IBM's position with respect to any patent that other JEDEC participants could describe. (G. Kelley, Tr. 2450-51 ("they were asking me to provide the committee with a list of all issued patents and patent applications, and I was warning the committee that that was not something that I could do. It was just not a possible task for me to know what was going on all over the world for the IBM Corporation. I then went on to promise the committee that I would alert the committee to any information that I had that applied to the JEDEC task at hand and if a question came up, I would get them information on any patent that they could describe to me."); Kellogg, Tr. 5024-26 ("one of the things that [IBM] felt impossible for us to do would be to study/evaluate the entire patent portfolio from IBM"; "I believe Gordon [Kelley] stated at least once and actually followed up. . . that if we were requested to evaluate the possibility of patents and if we were able to do so, we would investigate.")).

Rambus's Response to Finding No. 328:

As noted in response to Complaint Counsel's proposed finding no. 327, the cited testimony is sharply contradicted by numerous contemporaneous documents and by IBM's own actions over a period of years with respect to disclosure.

329. The issue concerning IBM's position on listing all its patents was raised again at the December 1993 Committee meeting. (JX0018 at 3; G. Kelley, Tr. 2471-73). IBM reiterated it's position as stated to the Committee in March 1993 that it was impossible reliably to conduct a search to provide such a company-wide listing, and so would not attempt to do so. (JX0018 at 3; G. Kelley, Tr. 2471-73).

Rambus's Response to Finding No. 329:

This finding cites to the wrong page of the December 1993 JC 42.3 meeting minutes. At page 3, which this finding cites, IBM is reported to have stated that it will not "list all of its patents on BGA due to length." (JX 18 at 3). There is a *separate* and much more general statement attributed to IBM at page 8 of the minutes:

> "IBM noted that in the future they will not come to the Committee with a list of applicable patents on standards proposals. It is up to the user of the

standard to discover which patents apply."

(JX 18 at 8).

In short, and as explained in more detail in response to proposed finding no. 327, the cited explanations by Mr. Kelley are inconsistent with the language of the minutes and with other contemporaneous documents.

5. All JEDEC Participants Must Disclose.

330. The JEDEC disclosure policy imposed an obligation on "*all participants* to inform the meeting of any knowledge they may have of any patents, or pending patents, that might be involved in the work they are undertaking." (CX0208 at 19 (emphasis added); CX0202 at 4 ("They [the "General Guides Applicable to All EIA Activities"] are required to be read an followed by all members of the Association and staff, chairmen and members of all committees, sections, divisions, and other EIA sponsored groups."); Calvin, Tr. 1005-06 (for presenters "it wasn't a different obligation"); J. Kelly, Tr. 1865, 1969-70 ("All participants in the work of the committee have a shared responsibility to disclose any information of which they have personal knowledge of intellectual property that may relate to the working committee. It's not limited to members, it's not limited to the IP owner. It's across the board."); Landgraf, Tr. 1700 ("I don't think there was any distinction, whether you were a member presenting ideas for standardization or you're a member just observing the direction the committee is going, because . . .the committee is the collective intelligence of its membership, . . . So, the obligation is not only on the person making a presentation but also on the membership to point out improvements that can be done or issues with the direction that the committee is going. And so the dialogue and feedback is important, and that includes the idea of disclosures of patents and applications."); Rhoden, Tr. 319-20 ("it's everyone who is a member either in attendance or not in attendance, a guest, a -- whoever is either in the room at the time discussions are held or has access to any of the JEDEC information outside of the meetings themselves.")). *See also* RX1712 at 8 (ANSI Guidelines suggest standards organizations adopt rules to ensure that any participant, not just the patent holder, identifies patents that may be required)).

Rambus's Response to Finding No. 330:

The proposed finding is not supported by contemporaneous documents and is in conflict with the weight of the evidence. Even the documents cited by the finding do not support it. CX 202 – the EIA Legal Guides – contain no disclosure requirement and instead state that EIA standards are adopted without regard for patents. (CX 202 at 5-6). Complaint Counsel did not

establish that CX 208 – the 21-I manual – received the necessary EDEC approval, and the 21-I "viewgraphs" that members were supposed to (but did not) see did not refer to any disclosure requirement in any event.

The cited testimony also offers no support for the proposition that there was a *commonly understood* set of obligations, as each of the cited witnesses expressed a different understanding about who possessed the purported disclosure obligation. For example, Desi Rhoden testified that the obligations ran to those members "in attendance or not in attendance" (Rhoden, Tr. 319-320), while Gordon Kelley testified that they ran to the persons "present in the room" during the JEDEC meeting. (Kelley, Tr. 2700). The evidence also shows that although named inventors on patent applications were often "in the room" at JEDEC meetings while proposals relating to those applications were being discussed, the inventors did *not* disclose those applications to JEDEC. *See* RPF ¶¶ 243-247 (SyncLink Consortium members did not disclose); 248-251 (Fujitsu did not disclose); 252-254 (IBM did not disclose); 255-258 (Micron did not disclose); 259-260 (Mitsubishi did not disclose); 261-264 (Samsung did not disclose); 265-269 (Texas Instruments did not disclose); 270-272 (Toshiba did not disclose). This evidence supports the conclusion that JEDEC attendees did not understand that they had an obligation to disclose patent applications relating to the work of the committee.

6. Meaningful Information Must be Disclosed.

331. The JEDEC patent policy required that a participant disclose sufficient information to put the committee on notice as to the nature of the relationship between the proposed standard and the intellectual property that might relate to the proposed standard. (Calvin, Tr. 1010-12 ("tell the subject matter of the patent or patent applications, as the case may be"; "the policy would be to follow up to understand those aspects of claims that might affect the patent, or might affect the development of the standard."); J. Kelly, Tr. 1870-71 ("[A]s long as enough information is provided to the committee that it understands the nature of the technology and

how it applies to the standard, that's enough."), 1994, 2004 ("the explanation includes identification of the technology and how it relates to the work of committee."), 2136-37; Rhoden, Tr. 627 ("sufficient technical information would be required to be disclosed, such that the formulating committee can understand what has been claimed"); Sussman, Tr. 1375-76 ("give us the concept and. . . at least enough information to know what you're doing."); Williams, Tr. 771-72, 774-75 (no requirement to provide copies of patent applications), 793-94 ("you needed to know sufficient information to make an informed decision whether or not it applied. . .You needed to know sufficient information so that you could make a decision")).

Rambus's Response to Finding No. 331:

This purported requirement is not supported by *any* contemporaneous document. In fact, this finding cites to no documents at all, contemporaneous or otherwise. The JEDEC meeting minutes certainly do not support the notion that patent-related disclosures were ever accompanied by an explanation of the claims asserted in a patent or a patent application. EIA General Counsel John Kelly's testimony about the nature of the information provided carries no weight, for he has never attended a single JEDEC meeting. (Kelly, Tr. 1821). JEDEC Board Chairman Desi Rhoden testified, in contrast, that it would be sufficient for a member simply to state that it "might have IP relating" to its presentation. (Rhoden, Tr. 1304-05). JC 42.3 and JEDEC Council chair Gordon Kelley similarly testified that it would be sufficient for a JEDEC member simply to provide the number of the patent, because that would give enough information to allow engineers to research the details relating to the patent. (Kelley, Tr. 2700).

332. Disclosures that did not provide the committee with an understanding of the relevance of the technology to the are insufficient. (J. Kelly, Tr. 2134-35 (discussing Echelon example), 2158-63 (disclosure made to block standard is made in bad faith); Kellogg, Tr. 5060 ("JUDGE McGUIRE: Well, then let me ask a question. Under your understanding of the patent policy, when one discloses a patent, are you saying then that if they haven't also disclosed the implications of the patent, have they I guess adequately then disclosed the patent under the patent policy? THE WITNESS: No. That's kind of my point, and I appreciate the clarification.. . .Within the context of the patent policy at JEDEC, disclosure of a number I don't believe meets the patent policy. If the number is disclosed not in any context of anything else."); G. Kelley, Tr. 2578-79 (comment of "no comment" is inadequate.); Sussman, Tr. 1413-14 (Rambus disclosure

relating to SyncLink was inadequate because "I do not have enough information to know what you have. All I can do is determine that you have something. . . . you're telling me that you do have something. But I don't know what it is.")).

Rambus's Response to Finding No. 332:

The purported requirement to explain "the relevance of the technology" is not supported by any contemporaneous document. The JEDEC meeting minutes do not show that patent-related disclosures were *ever* accompanied by an explanation of the claims asserted in a patent or a patent application. JC 42.3 and JEDEC Council chair Gordon Kelley testified, moreover, that it would be sufficient for a JEDEC member simply to provide the number of the patent, because that would give enough information to allow the engineers to research the details relating to the patent. (Kelley, Tr. 2700). JEDEC Board Chairman Desi Rhoden similarly testified that it would be sufficient for a member simply to state that it "might have IP relating" to its presentation. (Rhoden, Tr. 1304-05).

7. The Duty to Disclose Is Triggered by the Participant's Knowledge or Belief of A Relevant Patent or Application.

333. The duty to disclose was triggered by the knowledge or belief of the JEDEC participant. (Calvin, Tr. 1012 ("as you began to realize that the direction the standard was going could be affected by those [patents or patent applications], you would have a similar obligation [to disclose]."); J. Kelly, Tr. 1980-82 (subjective belief or judgement of participant that there is a sufficient relationship between the IP and the standard triggers disclosure obligation); CX2057 at 200 (Meyer 12/13/00 Dep.) ("sufficient knowledge to be aware that there was coverage" triggers obligation to disclose)).

Rambus's Response to Finding No. 333:

Contrary to this proposed finding, the overwhelming weight of the evidence shows that *if* there was a disclosure obligation, it was triggered only when a JEDEC representative had "actual knowledge" of the intellectual property and its relationship to a standard. JEDEC Board

Chairman Desi Rhoden testified that the disclosure obligations under the JEDEC patent policy were "triggered by the actual knowledge of the people that were involved. . . ." (Rhoden, Tr. 624). EIA General Counsel John Kelly testified that the disclosure obligations applied "to all participants with actual knowledge." (Kelly, Tr. 1970).

Mr. Rhoden did not know what obligation might exist where a representative had a *question* about whether his company might have intellectual property interests relating to a particular feature under discussion, but did not know if those interests existed. (Rhoden, Tr. 625). In fact, no witness testified that a JEDEC representative who had a question about whether his company might have intellectual property interests relating to a feature under discussion at JEDEC meetings had an obligation to disclose that he had that question.

The EIA's January 10, 1996 comment letter to the FTC also spoke to the "actual knowledge" requirement and noted the "chilling effect" that a broader disclosure obligation would have:

> "EIA and TIA strongly agree that the FTC must limit the application of the *Dell* rule to cases involving *actual knowledge* of the existence of a patent and intentional failure to disclose the patent interest.

(RX 669 at 3) (emphasis added).

334. A company could not deliberately shield its representative from knowledge of relevant patents. (J. Kelly, Tr. 1983 (such conduct would violate duty of good faith)).

Rambus's Response to Finding No. 334:

This finding is irrelevant, for Complaint Counsel do not contend that Rambus engaged in such conduct.

8. The Duty to Disclose Extends to Any Patent or Application That Might Be Involved in JEDEC Work.

335. The EIA/JEDEC patent policy required disclosure of patents and patent applications that "*might be involved*" in the standards under development. (CX0208A at 19 ("obligation of all participants to inform the meeting of any knowledge they may have of any patents, or pending patents, that might be involved in the work they are undertaking") (emphasis added); G. Kelley, Tr. 2705 ("there were many work items that occurred on the committee that did not become standards. . . My definition says that any claim that might apply to the work of the committee it was required to disclose."); Landgraf, Tr. 1693-94 (disclose patents or applications "that would *potentially* be impacting the standard or proposed standard."); Lee, Tr. 6595-96; Rhoden, Tr. 307; Sussman, Tr. 1346 (participants must disclose where there is a "gray" area); CX2057 at 203-04 (Meyer 12/13/00 Dep.) (disclosed patent when "sufficiently close" to work of JEDEC.); Williams, Tr. 909-11 (if "there would be a reasonable possibility that the patent was going to be associated with the work of JEDEC, that you ought to say, hey, I've got something I'm patenting here or there's something that you're talking about that I've got some IP on.")).

Rambus's Response to Finding No. 335:

This finding is inaccurate. Assuming that JEDEC members were obligated to disclose *some* intellectual property interests at JEDEC meetings while Rambus was a member, the weight of the evidence, including all of the contemporaneous documents, shows that that obligation could have extended only to patents that were "essential" to a standard, *i.e.*, those patents that were necessary for the manufacture or use of a product that complied with the standard.

- EIA Manual EP-3-F refers only to standards that "*call for the use* of patented items." (CX 203A at 11) (emphasis added).
- EIA Manual EP-7-A refers only to standards "that *call for the exclusive use* of a patented item or process." (JX 54 at 9) (emphasis added).
- The EIA's January 1996 letter to the FTC states that the EIA "follow[s] the ANSI intellectual property rights ("IPR") policy as it relates to *essential* patents." (RX 669 at 2) (emphasis added).

- JEDEC Secretary Ken McGhee's July 10, 1996 memorandum to JEDEC Council members and alternates states that the EIA encourages disclosure of "known *essential* patents." (RX 742 at 1) (emphasis added).
- When writing on behalf of the EIA in August 1995 to an EIA member called Echelon, EIA General Counsel John Kelly explained that the "ANSI and EIA patent policy . . . requires an SDO to secure a commitment to license a patented item or process from a patent holder when a standard refers to a patented technology *or, as a practical matter, conformance to a standard requires use of the patented technology*." (RX 2299 at 2) (emphasis added).
- The operative language of JEDEC's policy manual JEP 21-I – even if it had been approved by EDEC – refers *only* to standards that "*require the use* of patented items." (CX 208 at 19) (emphasis added).

The weight of the trial testimony supports the same conclusion as the contemporaneous documents. Infineon's JEDEC representative Willi Meyer testified that it was his understanding the disclosure duty applied only to patents "related to the work at JEDEC in the sense that it described features that were *necessary to meet the standard*." (CX 3136, Meyer, 5/7/01 *Infineon* Trial Tr. at 117:12-14) (emphasis added). Hewlett-Packard representative Thomas Landgraf testified that he understood the patent policy to involve disclosure if "the standard required someone else's idea to be used . . . in order for it to operate." (Landgraf, Tr. 1693-5).

JEDEC 42.3 subcommittee chairman and IBM representative Gordon Kelley similarly testified that the disclosure duty was triggered by a patent claim that "reads on or applies" to the standard, meaning that "if you exercise the design or production of the component that was being

standardized [it] would require use of the patent." (Kelley, Tr. 2706-7). Another IBM JEDEC representative, Mark Kellogg, testified that his understanding was that "you have to disclose intellectual property that reads on the standard." (Kellogg, Tr. 5310-1). Mr. Kellogg also stated that "[s]ometimes we disclose intellectual property that doesn't [read on the standard] and one would question why. It adds confusion." (Kellogg, Tr. 5311).

336. In 1994, Texas Instruments sought clarification of the of the EIA/JEDEC patent policy. (CX0353 at 2-5) (March 9, 1994, memo from requesting that the JEDEC Council and Legal Counsel provide guidance to the committee concerning whether the patent policy applied only to patents that must be used to comply with the standard). *Cf.* (J. Kelly, Tr. 2057-58 (Rambus never contacted EIA Legal Counsel concerning questions of interpreting the patent policy)).

Rambus's Response to Finding No. 336:

Rambus has no specific response to the language used in this finding, although it notes that the words "of the" are repeated.

337. On March 29, 1994, Mr. Kelly responded that "[w]ritten assurances must be provided by the patent holder when it appears to the committee that the candidate standard may require the use of a patented invention." (CX0353 at 1 (underline in original); J. Kelly, Tr. 1941-42). Furthermore, it was not necessary for the committee to make a factual determination that the use of the patented invention is, in fact, required to meet the standard. (CX0353 at 1; J. Kelly, Tr. 1941-42). *See also* (J. Kelly, Tr. 1945 (assurance should come as soon as "it appears that the technology is or may be required to comply with the standard under development.")).

Rambus's Response to Finding No. 337:

The cited language from CX 353 refers to licensing assurances, not to a disclosure trigger. *See also* RRFF 335.

338. The Federal Circuit erred on the facts when it appeared to say that the only intellectual property that was required to be disclosed was that which, in fact, is required to meet or to comply with the final issued standard. Participants are unable to make an on-the-spot infringement analysis of what the final standard will look like and whether or not the patent or patent application covers the proposed standard. (CX3089 at 18; J. Kelly, Tr. 2064-66 (the majority "appeared to say that the only intellectual property that. . .needed to be disclosed was

that which in fact is required to meet or to comply with the final issued standard, and the concern we have there is that it basically requires participants in the process to make an on-the-spot infringement analysis of what the final standard will look like."); Williams, Tr. 771-72 ("and none of us were lawyers there, so we couldn't determine . . . if it infringed or not. I mean, that wasn't the purpose."); CX2059 at 201 (Karp, Infineon Dep.) (disclose intellectual property that might be involved in the work; no expectation that participants would conduct an infringement analysis)).

Rambus's Response to Finding No. 338:

The Federal Circuit's conclusion comports with the clear weight of the evidence, as demonstrated in detail in Rambus's response to proposed finding no. 335.

9. The Duty to Disclose Arises As Soon As a Participant Knows of A Relevant Patent or Application.

339. A participant is under a duty to disclose at the very moment the participant knows that his or her own company or anyone else's company has patents or patent applications that might involve the work of JEDEC. (Calvin, Tr. 1012-13 ("as you began to realize that the direction the standard was going could be affected by those [patents or patent applications], you would have a similar obligation [to disclose.]"); J. Kelly, Tr. 1837; 1945 (disclose as soon as "it appears that the technology is or may be required to comply with the standard under development."),1983-84 ("if there is any suggestion that the committee's work should move in a certain direction or any information that's presented with that as the intent, then the duty to disclose arises."); Landgraf, Tr. 1695-96 ("as soon as a member knew that they had -- either they had a patent of their own or applications or even a third party's patent or application, if you knew that and it was touching on some element of the standard or proposed standard, you were supposed to disclose that to the committee"); Rhoden, Tr. 356-57 ("my understanding always was as early as possible. That's the way it has always been stated and the way we have always used it. You are required as soon as you have knowledge of a discussion taking place, a presentation, discussion, ballot, whatever, as soon as you become aware that a topic is being discussed for which you know that there is IP, you are obligated to disclose."), 654 (disclose as early as possible); Williams, Tr. 772 ("as soon as you knew that there was a possible patent the could apply to what was being discussed"), 909-11 (as soon as you could if you thought it [a patent or patent application] was going to be applicable)).

Rambus's Response to Finding No. 339:

As demonstrated by the consistent use of the word "know" in this proposed finding and in the cited testimony, any disclosure obligation that may have existed was always tied to the

"actual knowledge" of the JEDEC representative, not to his beliefs, hopes or desires. (Rhoden, Tr. 624; Kelly, Tr. 1970, 2172; RX 669 at 3).

The evidence also shows that any obligation that may have existed was not triggered until the time that a proposal was balloted for approval. (Kelley, Tr. 2707 - testimony by JC 42.3 and JEDEC Council Chairman Gordon Kelley that as he understood the JEDEC patent policy, disclosure was required only at the time of balloting, although it was encouraged earlier in the process); (CX 2057, Meyer 12/13/00 Depo. Tr., p. 211) (testimony by Siemens JEDEC representative Willi Meyer that although it was "good practice" to notify the committee before balloting, "the ballot was considered the deadline when it should have been done"). The viewgraphs that were routinely shown at JC 42.3 meetings reinforced this view, since they asked the committee chair to "resolve patent status prior to (choose one)," followed by a list of events, almost all of which relate to balloting. (*See, e.g.*, JX 20 at 15-18; JX 21 at 14-18; JX 22 at 12-17). (*See also* Kelly, Tr. 1981) (timing of disclosure involves "gray area[s]" and the exercise of "judgment" on the part of the participant, especially where the standard is still "evolving."). (*See also* RRFF 317 and evidence cited therein).

340. The duty to disclose was not tied to any procedural formality in the JEDEC process. (CX0208A at 19 ("The Chairperson of any JEDEC committee, subcommittee, or working group must call to the attention of all those present the requirements contained in EIA Legal Guidelines, and call attention to the obligation of all participants to inform the meeting of any knowledge they may have of any patents, or pending patents, that might be involved in the work they are undertaking.") (emphasis added); J. Kelly, Tr. 1945, 1983-85 ("it's not tied to any procedural formality in the process at all"); Rhoden, Tr. 488-89 (duty triggered by "discussion, presentations, ballots, anything that's taking place inside the committee."); Landgraf, Tr. 1716-17 ("in a JEDEC committee, there's a lot of official work that is documented, and survey ballots are considered to be official work."); Lee, Tr. 6987-88 ("Q. Was it your understanding in April 1997 that the required time of disclosure for intellectual property known to the representative was time of balloting, but it was encouraged earlier? A. No."); Sussman, Tr. 1343 ("Basically any discussion. The earlier that we have the information that something may have some IP on it, the

better it turns out to be, so we don't waste time talking of this rather than an alternate.")).

Rambus's Response to Finding No. 340:

The weight of the evidence shows that any disclosure obligation that may have existed was not triggered until the time that a proposal was actually *balloted* for approval:

- JC 42.3 Committee Chairman Gordon Kelley testified that as he understood the JEDEC patent policy, disclosure was required only at the time of balloting, although it was encouraged earlier in the process) (Kelley, Tr. 2707);
- Siemens JEDEC representative Willi Meyer that although it was "good practice" to notify the committee before balloting, "the ballot was considered the deadline when it should have been done" (CX 2057, Meyer 12/13/00 Depo. Tr., p. 211);
- The viewgraphs that were routinely shown at JC 42.3 meetings asked the committee chair to "resolve patent status prior to (choose one)," followed by a list of events, almost all of which relate to balloting. (*See, e.g.*, JX 20 at 15-18; JX 21 at 14-18; JX 22 at 12-17);
- EIA General Counsel John Kelly testified that the timing of disclosure involves "gray area[s]" and the exercise of "judgment" on the part of the participant, especially where the standard is still "evolving." (Kelly, Tr. 1981). (*See also* RRFF 317 and 339 and evidence cited therein).

341. The disclosure duty is triggered by discussions at task group meetings. (Sussman, Tr. 1386 ("The same rules apply."); Macri, Tr. 4661 ("At the beginning of every task group meeting, we always say that the full JEDEC rules are in effect, and during discussions with these companies, I said, of course, you would have to abide by the JEDEC rules.")).

Rambus's Response to Finding No. 341:

The quoted testimony refers to JEDEC rules, not to a purported "disclosure duty."

342. Early disclosure promotes efficiency in standards development practices. (J. Kelly, Tr. 1955-56 ("by encouraging early disclosure of patents and obviously in EIA's case also patent applications, we get as much information, as I said before, as early in the process as possible to allow it to move forward expeditiously and efficiently without concern about unknown, undisclosed patents that may impede the work of the committee.")). *See also* (RX1712 at 6-7 (encouraging early disclosure of patents and patent applications promotes "greater efficiency in standards development practices.")).

Rambus's Response to Finding No. 342:

Both the cited document and the cited testimony refer to "encouraging" early disclosure of intellectual property interests. Rambus agrees that the EIA "encourage[d] the early, voluntary disclosure of patents that relate to the standards in work," as its January 1996 letter to the FTC stated. (RX 669 at 3). The evidence does not, however, support a finding that early disclosure was required rather than "encouraged."

343. A company that deliberately withdraws from JEDEC for the purpose of avoiding its patent disclosure obligations had violated both the patent policy and the duty of good faith. (J. Kelly, Tr. 1907 ("every participant in the process with knowledge of relevant IP has a continuing duty to disclose that IP and relevant technical information."), 1993 ("the violation [of the patent policy] would occur at that time there was knowledge that triggered the duty to disclose. . . the withdrawal itself, if it was motivated by bad faith, would certainly violate the Legal Guides."); G. Kelley, Tr. 2758 ("Q: Again, Mr. Kelley, based on your understanding of the disclosure policy between 1991 and 1996, if a company observed a presentation while that company was a member and then chose to withdraw before the matter came to ballot, would the member's withdrawal relieve it of any obligation to disclose relevant patents or patent applications? A. No.")).

Rambus's Response to Finding No. 343:

The cited testimony does not support the proposed finding. The finding is irrelevant in any event, since the Complaint does not claim that Rambus engaged in such conduct.

344. Resigning from JEDEC does not relieve a company of the duty to disclose relevant intellectual property that might relate to JEDEC work conducted while the company was a

member. (G. Kelley, Tr. 2758 ("Q: Again, Mr. Kelley, based on your understanding of the disclosure policy between 1991 and 1996, if a company observed a presentation while that company was a member and then chose to withdraw before the matter came to ballot, would the member's withdrawal relieve it of any obligation to disclose relevant patents or patent applications? A. No."); J. Kelly, Tr. 1907 ("every participant in the process with knowledge of relevant IP has a continuing duty to disclose that IP and relevant technical information."), 1992-94 (violation of the duty to disclose occurs at the time of the participant's knowledge, which would be prior to withdrawal; party withdrawing must identify technology and its relationship to the standard.)).

Rambus's Response to Finding No. 344:

The proposed finding cites to no by-law, manual, statement of policy, or contractual provision for support. Instead, it finds support only in the after-the-fact "understandings" of two interested witnesses. Gordon Kelley's testimony offers no support at all, for he did not testify that there was any "obligation to disclose" prior to balloting. He testified instead that JEDEC members were only "encouraged," and *not* "required," to make intellectual property disclosures prior to balloting. (Kelley, Tr. 2707). John Kelly's testimony, on the other hand, is wholly improbable. Not only is it linked to no contemporaneous document, but also there is no evidence that any former member was ever asked to comply with such an ongoing requirement. In addition, such an unbounded duty – without limit in time even in the event of a withdrawal – would seem to implicate the very same fears of "chilling" JEDEC participation that caused JEDEC to decide not to ask members for written assurances with respect to intellectual property. (RX 486 at 1).

345. The Federal Circuit majority was in error on the facts when it tried to pinpoint an exact moment in time when disclosure might be or was required. (CX3089 at 18; J. Kelly, Tr. 2064-65 (the majority "tried to pinpoint an exact moment in time when disclosure might be/was required, and I believe the majority said that that moment in time was when a formal ballot was presented for a vote in JEDEC, and that. . . is absolutely not the case. The rule is as early as possible in the process and there is no procedural point, identifiable point, at which disclosure is required")).

Rambus's Response to Finding No. 345:

Contrary to John Kelly's after-the-fact testimony, the contemporaneous evidence fully supports the Federal Circuit's conclusion that any disclosure obligation that existed was triggered at the time of balloting, and not before. *See* RRFF 317, 339 and 386 and evidence cited therein.

10. The Duty to Disclose is Continuing.

346. The EIA/JEDEC patent policy applied with equal force to situations involving: 1) the discovery of patents that may be required for use of a standard subsequent to its adoption, and 2) the initial issuance of a patent after the adoption of a standard. (CX0208 at 29 ("the EIA Patent Policy applies with equal for to situations involving: 1) the discovery of patents that may be required for use of a standard subsequent to its adoption, and 2) the initial issuance of a patent after the adoption of a standard."); J. Kelly, Tr. 1985 (once a standard has been finalized and adopted, members have a continuing duty to disclose patents or patent applications relevant to the final standards.); Rhoden, Tr. 323 ("the EIA patent policy has applied to patents even after the fact, those granted after the issuance of a standard."); Sussman, Tr. 1344-45).

Rambus's Response to Finding No. 346:

Complaint Counsel did not show that CX 208 (the 21-I manual) ever became effective. (Kelly, Tr. 2105). Rambus does agree, however, that the EIA/JEDEC *licensing* policy is supposed to be triggered if JEDEC learns of intellectual property after a standard is passed. As the EIA's 1/22/96 letter to the FTC stated, "[e]ven if knowledge of a patent comes later in time due to the pending status of the patent while the standard was being created, the important issue is the license availability to all parties on reasonable, non-discriminatory terms." (RX 669 at 4). JEDEC appears to have ignored or violated its own policy in choosing never to request "RAND" assurances from Rambus despite its longstanding knowledge of Rambus's intellectual property.

11. In Addition to Disclosure, JEDEC Participants Must Comply With Licensing Assurance Requirements.

347. JEDEC rules prohibit it from including patented or patentable material in JEDEC standards without written assurances from the owner of the intellectual property that it will grant

licenses for free or on reasonable and non-discriminatory ("RAND") terms. (CX0203A at 11 ("The committee chairman must have also received a written expression from the patent holder that he is willing to license applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination."); CX0208 at 19 ("the committee chairperson must receive the written assurance of the organization holding rights to such patents that a license will be made available without compensation to applicants. . . or that a license will be made available to all applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination"); JX0054 at 9; CX2191 at 8 ("JEDEC has a policy of not making standards on items that have been patented, unless the patent holder agrees to certain restrictions regarding fair royalties and not restricting companies that can be licensed"); Bechtelsheim, Tr. 5897-98 (using patented technology "is okay as long as the patent holder would commit to licensing their required patents under reasonable and nondiscriminatory terms"); J. Kelley, Tr. 1868-69; 1884-86 (the rule is "firm" and JEDEC committees are forbidden to adopt standards with known patents), 1895-96, 1907-08 ("The patent owner is free to give or not to give the written assurances. If the patent owner does not give the written assurances, then the committee can take no further action with respect to the patented technology."); G. Kelley, Tr. 2393; Landgraf, Tr. 1693-94 (the committee would ask the patent owner "whether they would comply with the JEDEC policy, which had to do with granting licenses either freely to all applicant requesters or offer the patent on reasonable terms and conditions."); Lee, Tr. 6991 (when patents were identified "the JEDEC member also had a responsibility to agree on reasonable, nondiscriminatory license fees"); Rhoden, Tr. 307-08; Williams, Tr. 793-794 (the intellectual property "needed to be licensed on a reasonable and nondiscriminatory basis"); Grossmeier, Tr. 10951 ("If there were patents declared or disclosed, the committee chair would advise . . . that proposal or that standard could not proceed to the JEDEC Council for approval until a letter was received by the JEDEC office from the patent holder saying that it. . .would comply with the EIA guidelines on accessibility of the patent, with reasonable terms and nondiscriminatory access.")). *See also* (Kellogg, Tr. 5046 (obligated to terminate consideration of Quad CAS once committee became aware of patents; begin considering "work-arounds."); CX0711 at 171 (Richard Crisp noting that "There are no second showings at this meeting of the SyncLink material . . . Off-line Dave Barnum of Augat. . . said that he thinks that the reason there will not be second showings is that we have cast doubt over the patent issue.")).

Rambus's Response to Finding No. 347:

This proposed finding misstates the evidence it cites. The finding refers to "patented or patentable material;" the evidence does not. (*See, e.g.*, CX 2191 at 8 – "JEDEC has a policy of not making standards on items that have not been patented, unless the patent holder" agrees to "RAND" terms).

As the EIA explained in its January 22, 1996 letter to the FTC, where so-called

"patentable" material is involved, its approach is to seek "RAND" assurances *after* the issuance of the patent:

> ". . . if knowledge of a patent comes later in time due to the pending status of the patent while the standard was being created, the important issue is the license availability to all parties on reasonable, non-discriminatory terms."

(RX 669 at 4).

The IEEE – which, like the EIA, follows the ANSI Patent Policy – has explained to the FTC why this approach makes sense:

> "Standards committees realize that until a patent has been issued there is very little value to disclosure since the scope of valid patent claims has not been determined. This is why it is not appropriate to group issued patents and applications together, especially in the context of antitrust policy where governmental action could have a significant impact on standards-setting procedures."

(RX 2011 at 5).

348. RAND licensing helps to ensure open standards. (J. Kelly, Tr. 1895-96 ("licensing assurances are designed to ensure that the process is open and that the end product of the process is open and . . . that the end product of the process, which is a standard or a technical publication, will not include" unlicensed or restrictive IP.")).

Rambus's Response to Finding No. 348:

The cited testimony is misquoted and contains no reference to "unlicensed" IP. (Kelly, Tr. 1895-96).

12. The Licensing Assurances Must Be in Writing.

349. Oral statements relating to licensing assurances are not enough to comply with JEDEC/EIA policy. (J. Kelly, Tr. 1880-81 ("We would require in addition a written expression of the company's willingness to license [on reasonable and non-discriminatory terms] signed by a person in a position of authority to bind the company.), 2004-05 (JEDEC requires "the commitment of the company, not the commitment of the participant, and that of necessity requires that there be something in writing on company letterhead signed by an official with the authority to bind the company.")).

Rambus's Response to Finding No. 349:

The evidence shows that in practice, JEDEC often accepted vaguely worded oral assurances of RAND licensing and often went forward after a patent disclosure without even asking for RAND assurances. *See* RPF, ¶¶ 1220-1238.

350. The wording on the written assurance letter needs to be consistent with the language found in Section 3.4 of EP-7-A, the EIA Style Manual, with no substantial modifications or additions. (JX0054 at 9; J. Kelly, Tr. 1881 ("the wording needs to be in the words that you see in Section 3.4 [of EP-7] with no substantial modifications or additions."), 1898-99 (the RAND requirement is related to good faith)).

Rambus's Response to Finding No. 350:

The evidence shows that in practice, JEDEC often accepted vaguely worded oral assurances of RAND licensing and often went forward after a patent disclosure without even asking for RAND assurances. *See* RPF, ¶¶ 1220-1238.

351. EIA general counsel is responsible for determining whether a written assurance complies with EIA policy. (J. Kelly, Tr. 1882 ("Q. And who within EIA determines whether licensing assurance letters satisfy the organization's rules? A. I do.")).

Rambus's Response to Finding No. 351:

The proposed finding is irrelevant to the issues in the case.

352. Assurances should come as soon as it appears that the technology is or may be required to comply with the standard. (J. Kelly, Tr. 1945 (" if it appears that the technology is or may be required to comply with the standard under development, then the assurances should be

forthcoming at that point."); CX0353 at 1 ("[w]ritten assurances must be provided by the patent holder when it appears to the committee that the candidate standard may require the use of a patented invention.") (underline in original)).

Rambus's Response to Finding No. 352:

The finding would only be supported by the cited evidence if the words "to the committee" are inserted after "it appears." (CX 353 at 1). Rambus also notes in response to this proposed finding that JEDEC has never requested that Rambus provide RAND assurances with respect to the patents at issue here, despite JEDEC's longstanding awareness of those patents.

353. Once written assurances are received, then JEDEC may consider including patented technology in a standard. (J. Kelly, Tr. 1839-40 ("when the best approach to a technological problem is patented technology, then we, of course, will adopt the patented technology as part of the standard. . . provided there is disclosure of the existence of the IP early in the process and provided that we obtain the licensing assurances."), 1988 ("if the patent is disclosed early and the assurances are given, there is no reason not to move forward with the best technological approach, even if it's patented or subject to a patent application.")).

Rambus's Response to Finding No. 353:

The contemporaneous documents take a different approach. As the EIA informed the FTC in its ½2/96 comment letter,

> "Even if knowledge of a patent comes later in time due to the pending status of the patent while the standard was being created, the important issue is the license availability to all parties on reasonable, non-discriminatory terms."

(RX 669 at 4).

13. Assurance Must be Given of Reasonable Royalty Rates.

354. Actual royalty rates are not discussed in JEDEC. (CX2058 at 235-36 (Meyer 12/14/00 Dep.)).

Rambus's Response to Finding No. 354:

This proposed finding is inaccurate. Mark Kellogg presented IBM's "actual royalty rates" to JEDEC when he presented the IBM Worldwide Licensing policy at a 42.5 meeting on December 2, 1991. (JX 9 at 24; Kellogg, Tr. 5232, 5238-39). The IBM Worldwide Licensing Policy sets forth royalty rates from 1-5% of selling price: "The royalty for use of IBM's patents may be based on the licensee's selling price of each product covered by one or more licensed patents or on the royalty portion selling price of such product, the choice being left to the licensee. . . . The royalty rates are 1% of the selling price if the product is covered by one Category I patent, and 2% of the selling price if the product is covered by two or more Category I patents. If the product is covered by one, two or three or more Category II patents, the royalty will be, respectively 1%, 2% or 3% of the selling price, added to any royalty incurred for Category I patents." (JX 9 at p. 24; Kellogg, Tr. 5238-9; Kelley, Tr. 2618-20). No witness testified that anyone objected to these rates as unreasonable.

355. EIA and JEDEC do not determine what is a reasonable royalty rate. (CX2089 at 174-75 (Meyer Infineon Tr.) (reasonable "was up to the negotiations"); J. Kelly, Tr 1882-83 (JEDEC does not "have the expertise to be able to determine what's commercially reasonable in the context of any industry, no less semiconductors. . . That expertise resides in the industry. So, that's why in the first instance we leave it to the parties themselves to work out what's reasonable.")).

Rambus's Response to Finding No. 355:

Rambus has no specific response.

356. Determination of a reasonable royalty rate is left to negotiation and market forces or the courts. (CX2089 at 174-75 (Meyer Infineon Tr); J. Kelly, Tr. 1882-83, 2073-74 (JEDEC and EIA "don't get into the definition, the further definition of reasonable and nondiscriminatory at all. We leave that to the parties to work out or the courts.")).

Rambus's Response to Finding No. 356:

Rambus has no specific response.

F. JEDEC Informs Participants of the Disclosure and Licensing Obligations.

357. JEDEC informed participants of their obligations under the patent policy through discussions at JEDEC meetings, manuals, minutes, ballots, the JEDEC sign-in sheet, and advice from John Kelly. (Rhoden, Tr. 324) (stating that JEDEC informed participants of the patent policy by: (1) reviewing the patent policy at every committee meeting; (2) making available to everybody the Manual of Organization and Procedure; and (3) reiterated the patent policy on the sign-in sheet). *See also* (CX2057 at 95 (Meyer 12/13/00 Dep.) (Describing various ways of learning about the patent policy)).

Rambus's Response to Finding No. 357:

The proposed finding is inaccurate; the cited testimony does not refer to "obligations." In addition, while there was testimony that JEDEC manuals were "available," there was also testimony that they were not actually *sent* to members. The passage from Mr. Meyer's deposition transcript that Complaint Counsel cite, for example, contains this exchange:

> "Q. Excluding whatever was in the minutes, did anybody ever send you, anybody from JEDEC or EIA send you a policy document or a procedure document between 1990 and 1997?
>
> A. Other than attached to the minutes, no."

(CX 2057, Meyer 12/13/00 Depo. at 95:4-12)

1. Meeting Presentations.

358. The chairperson of each JEDEC committee, subcommittee, or working group was required to call to the attention of all those present the requirements contained in the EIA legal guides to inform the meeting on any knowledge they may have of patents or pending patents that might be involved in the work of the meeting. (CX0208 at 19; CX0208A at 19).

Rambus's Response to Finding No. 358:

Complaint Counsel cite no authority other than the 21-I manual for this finding. Complaint Counsel did not meet their burden of proving that CX 208 (the 21-I manual) ever became effective. (Kelly, Tr. 2105). The great weight of evidence also shows that the portion of 21-I quoted herein neither articulated JEDEC policy authority nor purported to communicate that policy to JEDEC members. *See* RRFF 317, 318 and 330.

359. Jim Townsend of Toshiba was the chairman of the JC-42.3 committee during the relevant time period. He was elected chairman at the December 1991 meeting. (JX0010 at 12 (noting Mr. Townsend's election)).

Rambus's Response to Finding No. 359:

This proposed finding is incomplete because it does not reflect the organizational changes within the JC 42 committee over time. In the early 1990s, the JC 42.3 subcommittee was divided into several task groups that were eventually given letter denominations. Gordon Kelley was chair of the DRAM Task Group (responsible for all dynamic RAM devices, including SDRAM), from at least 1991 through 1995. (CX 2089, Meyer Inf. Trial Tr. 4/26/01 at 134:15-17; CX 35 at 14-15; JX 21 at 7). Mr. Townsend was the *overall* chair of the JC 42.3 RAM Committee between January 1992 (JX 11 at 2) and December 1995, when Gordon Kelley assumed that position. (JX 28 at 3 – "Election results: Gordon Kelley: JC 42.3 Chairman. . .").

360. Mr. Townsend ensured that the committee participants were informed of their obligations with respect to the patent policy. (CX2078 at 38-39 (Karp, Micron Dep.) ("I believe it was a personal crusade by Jim Townsend); G. Kelley, Tr. 2399 ("Jim Townsend made it a very big issue that the committee needed to deal with patents and what he called patent applications in the work of the committee so that we could avoid whenever possible."); Lee, Tr. 6597 (Townsend "was pretty vocal at the beginning of meetings to state the policy and to clarify if any question came up."); Rhoden, Tr. 325 ("Generally, during that period of time, it would have been Mr. Jim Townsend who would have made those [patent] presentations"); Williams, Tr. 771 ("Q. Between late 1991 through 1993, how did you learn about JEDEC's patent policy? A. Mainly

by the presentations that were given at every meeting by Mr. Townsend.")).

Rambus's Response to Finding No. 360:

The weight of the evidence shows that Townsend did not discuss patent applications at the outset of each meeting. Indeed, only *one* of the witnesses cited in support of this finding mentioned applications in the cited testimony. And that witness – Mr. Kelley – did not say whether patent applications should be disclosed by non-presenters as well as presenters. The JC 42.3 minutes show that Townsend routinely did not use or show the viewgraphs attached to the 21-I manual, and instead displayed viewgraphs containing the language of EIA manuals EP-3-F, EP-7-A and EP-7-B. (*See*, *e.g.*, JX 20 at 15-16; JX 21 at 14-15; JX 22 at 12-13; JX 25 at 18-19; JX 26 at 15-16). This shows that Townsend was aware either that the EIA manuals supplied the controlling patent policy or that the 21-I manual had not received EDEC approval, or both.

361. Other chairmen also presented the patent policy to their respective committees. (JX0029 at 2 ("Mr. Kelley noted verbally what is the patent policy of EIA/JEDEC."); Sussman, Tr. 1347-48 ("As a chair, as I opened the meeting, I would mention the JEDEC patent policy, and I would flash a transparency on the screen.")).

Rambus's Response to Finding No. 361:

The cited evidence is not probative because it says nothing about *what* information was presented to members or whether there was any mention of patent applications. The cited 42.3 meeting minutes simply note, for example, that Mr. Kelley "noted verbally what is the patent policy. . . ." (JX 29 at 2). Mr. Sussman's testimony is just as ambiguous and, like Kelley's testimony, describes a presentation far more cursory than what the proposed finding implies:

"As the meeting opened, I would wave the patent policy, and there would

be a transparency up on the projector with the page with the patent policy on it."

(Sussman, Tr. 1348).

362. The Wang litigation sensitized the JC-42 committee to patent issues. (G. Kelley, Tr. 2401-02 (after *Wang* "Jim had become a general with a flagpole patent, and at every meeting and every sub-meeting for a week of meetings, Jim emphasized each group's need to make sure that we gave time for disclosure of patents and discussion of patents and resolved any patent issues that could be resolved at the committee meeting for the purposes of meeting the requirements of an open standard."); Landgraf, Tr. 1698-99 (*Wang* "served to reinforce the seriousness of the policy. At this point, it became crystal clear to me and I think other people that when you're developing standards, the idea is to expand the number of suppliers and the number of potential users for it, and if you are going to participate in an open standard formulation body, you need to disclose everything that is applicable or potentially impacting the standards that you're going to adopt."); Sussman, Tr. 1353 (Townsend "was very sensitized by the WANG case and started to compile a [patent tracking] list."); Williams, Tr. 786-87 (Chairman Townsend and the rest of the board wanted to ensure [that *Wang*] never happened again, and so that's why there was so much emphasis placed upon why the policy was where it was and why there was discussion upon it and why it was at length discussed that this was so important, so that the industry was not held hostage again like it was under the WANG case.")). *See also* (CX0013 at 4 (noting that Mr. Townsend brought in a lawyer, gave a presentation, and made suggestions as to what could be done to avoid *Wang* problems in the future)).

Rambus's Response to Finding No. 362:

The *Wang* litigation involved a company that had *promoted* its technology for standardization, unlike Rambus. (CX 711 at 188). Moreover, none of the cited testimony refers to patent applications rather than issued patents.

363. Between May 1991 and September 1995, presentations on the patent policy were given at each meeting of the JC-42.3 subcommittee. (JX0005 at 3-4 (May 1991) ("Toshiba recommended that at each meeting a showing be made to explain what the intellectual property policies are . . . The important thing is disclosure"); Calvin, Tr. 1007-09 (essentially every meeting; gave presentation at each meeting during the week of meetings); G. Kelley, Tr. 2407; Rhoden, Tr. 325, 330; Williams, Tr. 785-86 (early presentation were quite lengthy); CX3136 at 134 (Meyer Infineon Tr.); JX0007 at 3 (September 1991); JX0010 at 11 (December 1991); JX0012 at 5 (February 1992); CX0034 at 3 (May 1992); JX0013 at 4 (July 1992); CX0042 at 3 (September 1992); JX0014 at 3 (December 1992) (noting that a draft of the revisions to the Manual or Organization and Procedure was shown); CX0045A at 2 (December 1992); JX0015 at

4 (March 1993); CX0050A at 2 (March 1993); JX0016 at 5 (May 1993); JX0017 at 3 (September 1993); CX0057A at 2; (September 1993); JX0018 at 3 (December 1993); CX0060A at 2 (December 1993); JX0019 at 4-5 (March 1994); JX0020 at 4 (May 1994); JX0021 at 4 (September 1994); JX0022 at 3 (December 1994); JX0025 at 3 (March 1995); JX0026 at 4 (May 1995); JX0027 at 4 (September 1995)).

Rambus's Response to Finding No. 363:

Rambus has no specific response.

364. The patent policy was presented at other JC-42 subcommittee meetings. (CX0018 at 7 (JC-42.5) ("It was suggested that at the beginning of each meeting the patent disclosure requirements be shown. Committee agreed."); CX0021 at 3 (JC-42.5); CX0030 at 3 (JC-42.5); CX0044 at 3 (JC-42.5); CX0052 at 4 (JC-42.5)).

Rambus's Response to Finding No. 364:

Rambus has no specific response.

365. Beginning with the December 1995 meeting, participants discussed the patent policy during the plenary session. (JX0028 at 3 ("Patent Policies. This subject was covered in the Plenary Session in December 4")).

Rambus's Response to Finding No. 365:

Rambus has no specific response.

366. Mr. Townsend cautioned participants to disclose "relevant patent applications." (RX0356 at 2 ("members are cautioned to disclose their relevant patent applications."); G. Kelley, Tr. 2406-07 (The JEDEC patent policy as explained by Jim Townsend required members to disclose "an issued patent that was available from the patent office, patent applications that were being worked on with the patent office, and items that were probably going to become patents."); Rhoden, Tr. 332 ("Mr. Townsend would always make reference that disclosure was required of patent applications."); Williams, Tr. 788-89; CX3136 at 134 (Meyer Infineon Tr.)).

Rambus's Response to Finding No. 366:

The use made by Complaint Counsel in this finding of Mr. Kelley's testimony violates Your Honor's July 10, 2003 Order On Post Trial Briefs, which bars the parties from offering testimony for the truth of the matter asserted if the testimony was admitted for another purpose.

Mr. Kelley was allowed to testify to his "understanding" of Mr. Townsend's message, but only after Your Honor explained that "I am not going to allow hearsay that tries to prove an out of [court] statement. That's pretty clear, Mr. Oliver." (Kelley, Tr. 2406). In any event, Mr. Kelley's description – that he thought members needed to disclose "items that were probably going to become patents" is a description of a policy that was never expressed anywhere in writing and that would be virtually impossible to implement given the uncertainties of the patent system. Mr. Kelley's testimony is also inconsistent with the Patent Tracking Lists – which show that no IBM patents *or* patent applications were added between the fall of 1993 and the fall of 1995, despite the enormous number of patents received by IBM in that time period. (JX 18 at 14-21; JX 19 at 17-23; JX 20 at 15-18; JX 21 at 14-18; JX 25 at 18-26; JX 26 at 15-24; JX 27 at 20-25; JX 28 at 12-18). Mr. Kelley's testimony is also inconsistent with statements repeatedly attributed to IBM in the JEDEC minutes to the effect that IBM would *not* disclose patents or "intellectual property law" rights. (JX 15 at 6; RX 420 at 1; JX 18 at 8). (*See also* Wiggers, Tr. 10592-4 – testimony by Hewlett-Packard representative and JEDEC Council member Hans Wiggers that he was present at a 42.3 meeting when Kelley said that IBM would not disclose patent applications, and that he, Wiggers, announced at the meeting that Hewlett-Packard would take the same position).

The three other witnesses cited in support of this finding are employed by DRAM manufacturers (or, in Mr. Rhoden's case, by a consortium of DRAM manufacturers), who have a strong financial interest in the outcome. In contrast to the after-the-fact testimony of these interested witnesses, the written evidence shows that disclosure of applications was only encouraged, not required. *See* RRFF 318-322 and evidence cited therein; RPF 204-273 and

evidence cited therein.

2. The Patent Tracking List.

367. In addition to his presentations of the patent policy, Mr. Townsend also kept a patent tracking list, which was his compilation of patents and pending patents concerning which he had been made aware of through the course of the work inside JEDEC. (Rhoden, Tr. 325 (Townsend "also distributed copies of. . . .his notes about patents that he had been made aware of through the course of the work inside JEDEC. He called that his patent tracking list"); Sussman, Tr. 1355 (JUDGE McGUIRE: Okay, now, whose job was it to transcribe any information on these sheets, these tracking sheets? I mean, who had that responsibility? Jim Townsend? THE WITNESS: Jim Townsend."); McGrath, Tr. 9247 ("As I recall there were at times things that were listed just as a patent application on his list.")).

Rambus's Response to Finding No. 367:

Rambus has no specific response.

368. The patent tracking list had multiple purposes, including record-keeping, a reminder to other participants of the patent issues that were on, and as an educational tool for those who were newcomers to the committee. (G. Kelley, Tr. 2407-08).

Rambus's Response to Finding No. 368:

In the cited passage, Mr. Kelley testified about his "understanding of the purpose" behind the list. (Kelley, Tr. 2407). He did *not* testify that he had personally prepared the list or that he had personal knowledge of its genesis. (*Id.*). In any event, he *certainly* did not testify that the list was intended as a reminder to "participants," as this proposed finding states. Instead, he testified that the list "was a reminder *to me* as we opened the meeting to remember the patent issues that were on the list." (Kelley, Tr. 2408) (emphasis added).

369. The patent tracking list was not a complete list of all patents and patent applications disclosed to the JC-42 committee. (G. Kelley, Tr. 2408 ("I know of instances where patent issues did not make the list.")). *See, e.g.,* (CX0034 at 7 (Fujitsu LOC package patent application disclosed in May 1992 did not appear on patent tracking list as of December 1995); CX0711 at 169 (Fujitsu SSTL patent application disclosed in September 1995 did not appear on patent tracking list as of December 1995); JX0027 at 7-8 (Stacktek patent disclosed by Hewlett-Packard in September 1995 did not appear on patent tracking list as of December 1995)). *Cf.* (JX0028 at

15-18 (December 1995 patent tracking list)).

Rambus's Response to Finding No. 369:

Rambus has no specific response.

370. A memorandum sometimes was shown and circulated with the patent tracking list. The memorandum referred participants to the "existing rules of the EIA governing *patentable* matters" and reminded participants of their obligation to indicate "the intent of your company to patent or not patent the subject matter." (CX0042A at 7) (emphasis added). *See also* (CX0336; CX0342; CX0347).

Rambus's Response to Finding No. 370:

This proposed finding is false. The memorandum to which this finding refers was always addressed to *specific companies*, not to all "participants," as Complaint Counsel asks Your Honor to find. (CX 42 at 13). The memorandum also says nothing at all about "obligations" on the part of "participants" or anyone else with respect to patents or "patentable matters." (*Id.*). Instead, the memorandum requests that its recipients – specific, identified companies that *never* included Rambus – to "please . . . research your company's position" on the items listed "next to your company's name. . . ." (*Id.*).

In other words, the memorandum asked specific companies to research and state their position on specific subject matters. No disclosure requirements are mentioned or implied. Because it was and is undisputed that there was *no* obligation on the part of JEDEC members to research anything about patents (*see* CCFF 325), this memorandum would naturally have been understood by JEDEC members as encouraging *voluntary* action, not as stating or imposing obligations.

371. Although the memorandum apparently was addressed only to participants representing companies with patents already on the patent tracking list, inclusion of the patent tracking list in the minutes assured that every participant was aware of the rules. (CX0042 at 16-

17). Rambus received copies of the patent tracking lists that were included in the minutes. (CX0042A) (original bates numbers indicate that these minutes were produced from Rambus's files)).

Rambus's Response to Finding No. 371:

There is no evidence in the record that the patent tracking list was addressed to those companies with patents on the list, and it is obvious from a simple comparison of the list of patents and the list of recipients that Complaint Counsel's speculation in this regard is unfounded. After Rambus's '703 patent was added to the tracking list, for example, it was *not* added to the list of addressees to whom Mr. Townsend sent his memorandum with its request for information. (JX 18 at 14-21; JX 19 at 17-23; JX 20 at 15-18; JX 21 at 14-18; JX 25 at 18-26; JX 26 at 15-24; JX 27 at 20-25; JX 28 at 12-18).

Moreover, the finding's assertion that the patent tracking list "assured that every participant was aware of the rules" is also unfounded. The only "rules" referenced in the memorandum are the *EIA* policies set out in EP-3 and EP-7A. (CX 42 at 14-15). Those "rules" reference no disclosure obligations at all. And even Gordon Kelley testified that as he understood these provisions (which were attached to virtually every set of JC 42.3 meeting minutes while Rambus was a member), they did *not* require disclosure of patent applications. (Kelley, Tr. 2686-7, 2695-7).

372. The patent tracking list, memoranda and other patent policy related documents were included in the package of minutes and attachments. (JX0007 at 21-23; JX0012 at 28-30; CX0034 at 13-21; JX0013 at 14-18; CX0042 at 13-17; CX0042A at 7-9; JX0014 at 21-30; JX0015 at 24-30; JX0016 at 21-29; JX0017 at 12-14; JX0018 at 14-21; JX0019 at 17-30; JX0020 at 15-25; JX0021 at 14-25; JX0022 at 12-20; JX0025 at 18-26; JX0026 at 15-28; JX0027 at 20-27; JX0028 at 12-23; CX0021 at 12-21; CX0030 at 12-20; CX0044 at 8-16; CX0052 at 11-14; CX0079A at 6-10; JX0009 at 13-16; JX0012 at 28-30).

Rambus's Response to Finding No. 372:

A review of these materials shows that in virtually every case, excerpts from the EIA manuals were shown, not the JEDEC manuals..

3. New Member Orientation.

373. JEDEC conducted new member orientations that included discussions of the patent policy when the new members had questions. (Rhoden, Tr. 341-42).

Rambus's Response to Finding No. 373:

Mr. Rhoden testified that such discussions occurred "occasionally, not often." (Rhoden, Tr. 341-42).

374. New members received copies of the JEDEC Manual of Organization and Procedure. (CX0208; Landgraf, Tr. 1702-04).

Rambus's Response to Finding No. 374:

Mr. Landgraf's testimony is not probative of any issue in this case, since he testified that he did not start attending JEDEC meetings until 1994. (Landgraf, Tr. 1687). Testimony by other JEDEC members about earlier time periods shows that the manuals were not routinely distributed to members. (CX 2057, Meyer 12/13/00 Depo. at 94-95). In any event, if this finding is accurate, it would prove only that Rambus had received the 21-H manual, which was in effect when Rambus joined JEDEC. (CX 205A). The only reference in the 21-H manual to intellectual property is this:

> "JEDEC standards are adopted without regard to whether or not their adoption may involve patents on articles, materials or processes."

(CX 205A at 11). This language also appears in the EIA Legal Guides and is described there as a "basic objective" of all EIA standardization programs. (CX 204 at 4).

4. Sign-In Sheets.

375. Participants at each JEDEC meeting were required to record their names on the Meeting Attendance Roster or sign-in sheet. (CX0306; CX3136 at 135 (Meyer Infineon Tr.) ("Q. This [sign-in sheet] is what the members signed whenever they came to a JEDEC meeting, is that right, Mr. Meyer? A. They sign that sheet, yes."); CX0356).

Rambus's Response to Finding No. 375:

Rambus has no specific response.

376. The attendees listed on the front page of each set of minutes was taken from the sign-in sheets. Thus, participants who appear as having attended the meeting necessarily must have signed the sign-in sheet. (Rhoden, Tr. 343 ("the people sign in, and then. . . they are transferred from this sheet then to the printed document, and you see at the head of all of the meeting minutes, the names that appear at the head of the meeting minutes would necessarily have signed a sheet just like this to be transferred to that point."); Calvin, Tr. 1014-15 ("the policy is that there's a sign-up sheet that is sent around, and you sign in, either as a member, or as an associate. And that's how they track.")).

Rambus's Response to Finding No. 376:

Rambus has no specific response.

377. After the Wang case (see CCFF 362, 434), JEDEC also revised the sign-in sheet to further clarify the rule requiring disclosure of patent applications that may relate to JEDEC work. (CX0306 at 1; J. Kelly, Tr. 1934-35 ("the language that I'm referring to is 'subjects involving patentability or patented items shall conform to the EIA policy'. . . I think that first appeared on the sign-in sheet in the early 1990s time frame, around the time of the WANG case."); CX0317 at 2 (March 1991 letter from Jack Kinn to Jim Townsend stating "Finally, subject to concurrence by our legal counsel, I will have a statement on patents, included on the reverse of the sign-in sheet plus suggest to Council a statement go on the front, requesting the chairmen to read the excerpts at the beginning of every meeting.")).

Rambus's Response to Finding No. 377:

The finding is not supported by the weight of the evidence. First, the 1991 Kinn memorandum refers to a statement "on patents," not patent applications. (CX 317 at 2). Gordon Kelley testified to his understanding that EIA consistently used the word "patents" to refer only to issued patents. (Kelley, Tr. 2686-7; 2695-7). Second, if JEDEC wanted to use the

sign-in sheets to tell members of some obligation to disclose patent applications, it presumably would have done three things: (1) used words like "disclose;" (2) used words like "obligated"; and (3) used the phrase "patent application." Instead, the sign-in sheet simply states that "subjects involving patentable or patented items shall conform to *EIA policy*." (CX 306 at 1) (emphasis added). The "EIA policy" on the reverse side of the sign-in sheet talks about *licensing* assurances, not disclosure obligations. (CX 306 at 2).

In short, the referenced language on the sign-in sheet at most was there to remind JEDEC members of EIA policies regarding licensing assurances.

378. The sign-in sheet used during at least part of the relevant time period contained a written reminder at the top of the first page that "[s]ubjects involving *patentable* or patented item shall conform to EIA Policy." (CX0306 at 1) (emphasis added); J. Kelly, Tr. 1934-35 (language appeared around the time of the *Wang* litigation)). Mr. Crisp recalled having seen the sign-in sheet with this language at some point while attending JEDEC meetings. (CX2094 at 439-40 (Crisp, Dep.)).

Rambus's Response to Finding No. 378:

See RRFF 377.

379. The term "patentable," as used in the sign-in sheet, referred to anything over which an individual company claimed ownership or anything that they claimed could be patentable. (J. Kelly, Tr. 1935-36 ("patentable" meant patent applications), 1856-57 (sign-in sheet incorporates language from EIA Legal Guides); Rhoden, Tr. 344 ("My understanding is anything that an individual company claimed ownership, anything that they claimed could be patentable, then that references the patentable terminology that you see here."); Sussman, Tr. 1350-51 (language in sign-in sheet is "all inclusive.")).

Rambus's Response to Finding No. 379:

None of the three witnesses whose testimony is cited regarding their understanding of the meaning of the word "patentable" on the sign-in sheet had any involvement in the choice of that word, so their testimony is necessarily limited to their own personal understanding. In any event,

the sentence as a whole, given its reference to the EIA licensing policy on the reverse side and the absence on the reverse side of any reference to a disclosure obligation, is *at best* a reminder about the licensing assurances requested when the committee learns of intellectual property issues. *See* RRFF 377.

380. The sign-in sheet also referred participants to EIA general counsel concerning any doubtful questions. (CX0306 at 1; J. Kelly, Tr. 1857-58, 1937-38 (receives questions concerning the patent policy approximately once every other month)).

Rambus's Response to Finding No. 380:

Rambus has no specific response.

381. EIA general counsel is the official responsible to final interpretation of the patent policy. (J. Kelly, Tr. 1857-58, 1915, 1939 (Mr. Kelly's interpretation controls)).

Rambus's Response to Finding No. 381:

Mr. Kelly testified that he "believes" that he has "the last word" in "interpreting EIA rules." (Kelly, Tr. 1857-58). He also testified, however, that EDEC, not himself, drafts those rules. (Kelly, Tr. 2078 – "EDEC drafts the policy.").

If Mr. Kelly is correct that he represents the "last word" with respect to EIA patent policy interpretation, then the 1/22/96 letter to the FTC that he co-signed, and its unambiguous statement that the EIA "encourage[s] the early, voluntary disclosure of patents that relate to the standards in work," ought to be binding upon EIA and JEDEC, or at least given great weight. (RX 669 at 3; Kelly, Tr. 2092-3).

5. Meeting Minutes.

382. JEDEC meeting minutes contained discussions of the terms of the patent policy. (CX0045A at 13) (showing proposed revisions of the JEDEC Manual of Organization and Procedure); CX0064A at 2 (discussion of request by Texas Instruments for clarification of the patent policy)).

Rambus's Response to Finding No. 382:

Rambus has no specific response.

6. Ballots.

383. JEDEC ballots required that participants who were "aware of patents involving this ballot, please alert the Committee accordingly during your voting response." (JX0059 at 2).

Rambus's Response to Finding No. 383:

The evidence shows that JEDEC's ballots neither imposed nor described a disclosure obligation. When the ballot language regarding patents was first added to JEDEC ballots, a JEDEC member asked about the purpose of the new language. The minutes of the JC 42.1 meeting held on September 13, 1989 state that:

> "Council discussed patent issue at their June meeting at the request of JC-42.3. The result was not to change EIA legal requirements as outlined in document EP-7, but to add some wording on JEDEC ballot voting sheets about informing the Committee if any patent covers the balloted material. TI was concerned that Committee members could be held liable if they didn't inform Committee members correctly on patent matters. *Committee responded that the question was added on ballot voting sheets for information only and was not going to be checked to see who said what*."

(CX 3 at 6) (emphasis added).

The statements in the official JEDEC meeting minutes that the patent-related question on the ballot was added "for information only" and that the ballots were "not going to be checked to see who said what" are entirely inconsistent with the proposition that the ballot language was

intended to, or did, express any mandatory disclosure obligation. (CX 3 at 6).

384. The term "patents" as used in JC-42.3 subcommittee ballots (see, e.g., JX0059 at 2) is not limited to issued patents; it includes all IP for which a patent had been applied for or was about to be applied for, as well as issued patents. (Sussman, Tr. 1391-92).

Rambus's Response to Finding No. 384:

This finding relies solely upon the understanding of a single interested witness whose employer would benefit from the remedy sought. Mr. Sussman's testimony lacked not just credibility but also foundation; he did not testify that he had had any role or responsibility in connection with drafting the language that appeared on the ballot forms.

Moreover, the contemporaneous documents do not support the proposition that the word "patent" as used on the ballots really meant patents *and* patent applications, not to mention something Complaint Counsel call "IP for which a patent . . . was about to be applied for." *See* RPF 204-273 and evidence cited therein. The official minutes of the JEDEC Board of Directors are more reliable than the testimony of a single interested witness, especially with respect to a policy issue. The February 2000 JEDEC Board minutes state the following:

> "D. Disclosure on Patents Pending
>
> Mr. Walther noted that Micron had sent a letter indicating they have patents pending on items that may affect committee standards. The issue was whether companies should make public that a patent is pending. The BoD discussed it and noted they *encourage* companies to make this kind of disclosures even though they were not *required* by JEDEC bylaws."

(RX 1570 at 13) (emphasis added).

385. This language was included on every ballot during the time Rambus was a member.

(Rhoden, Tr. 355-56 (ballots between 1991 and 1996); Williams, Tr. 812-13 (ballots included this "verbiage" between 1991 and 1993)).

Rambus's Response to Finding No. 385:

The language about patents did not appear on "every ballot," as this finding states. As Mr. Rhoden acknowledged, the referenced language did *not* appear on *survey* ballots, which were "just trying to gauge interest level." (Rhoden, Tr. 587). Mr. Rhoden testified that he had "meant to exclude" survey ballots from the very same testimony that Complaint Counsel now cite. (*Id.*).

386. A participant was required to disclose patent information at this point in the process if "it had not been disclosed to the committee before" this time. (Rhoden, Tr. 356-57 (ballot did not mark the time that participants were required to disclose)). *See also* Williams, Tr. 812-13 ("This is like a last ditch effort to get a disclosure and to remind people that they have that obligation even when voting").

Rambus's Response to Finding No. 386:

This finding should be re-phrased to comport with the evidence and to say that there is substantial evidence that if disclosure *was* required, it was not required until time of balloting. As JEDEC Council and 42.3 Chairman Gordon Kelley understood it, disclosure was required only at the time of balloting, although it was "encouraged" earlier in the process. (Kelly, Tr. 2707). Siemens' JEDEC representative Willi Meyer similarly testified that while it was "good practice" to alert the committee prior to balloting, the "deadline" was "the ballot." (CX 2057, Meyer 12/13/00 Depo. at 211). The evidence of actual JEDEC behavior also supports this conclusion, for patent disclosures were more likely to occur at the time of balloting than at any earlier time. *See* RPF 1224-1237.

7. Manuals.

387. The rules of JEDEC are provided in the EIA Legal Guides, EIA Manuals, and the JEDEC Manual of Organization and Procedure. (CX0202; CX0204; CX0203A; JX0054;

CX0205; CX0205A; CX0208; J. Kelly, Tr. 1824-25 (citing EP-3, EP-7 and EIA Legal Guides)).

Rambus's Response to Finding No. 387:

This proposed finding is identical in every respect to proposed finding no. 308. Like no. 308, it is unsupported by the evidence. *See* RRFF 308.

388. EIA rules and JEDEC rules concerning disclosure and licensing of patents are consistent. (J. Kelly, Tr. 1915-16 ("I'm not aware of any conflicts between the JEDEC rules and the EIA rules"), 1919-20 ("I think that those terms were used interchangeably, EIA patent policy and JEDEC patent policy.")).

Rambus's Response to Finding No. 388:

This proposed finding is identical, word-for-word, to CCFF 309. It is inaccurate for the reasons set out in RRFF 309.

(A). EIA Legal Guides.

389. EIA participants are required to comply with the rules and policies set forth in the EIA Legal Guides. (J. Kelly, Tr. 1829-32 (participants obligated to read and follow EIA Legal Guides)).

Rambus's Response to Finding No. 389:

Rambus has no specific response.

390. The Legal Guides were made available to all EIA and JEDEC participants. (J. Kelly, Tr. 1830-31 ("Copies of this document were also available through my office, as well as through the Publications Index.")).

Rambus's Response to Finding No. 390:

Rambus has no specific response.

391. Part I of the EIA Legal Guides includes "general guides applicable to all Electronic Industries Association activities. They are required to be read and followed by all members of the Association and staff, chairmen and members of all committees, sections divisions, and other EIA-sponsored groups." (CX0202 at 4; CX0204 at 3; J. Kelly, Tr. at 1830).

Rambus's Response to Finding No. 391:

Rambus has no specific response.

392. Part II of the EIA Legal Guides "are special guides that relate to engineering standardization programs uniquely." (CX0202 at 5; CX0204 at 4; J. Kelly, Tr. 1828).

Rambus's Response to Finding No. 392:

Rambus has no specific response.

393. Parts I and II of the EIA Legal Guides apply directly to JEDEC activities and the activities of JEDEC Committees. (J. Kelly, Tr. 1829).

Rambus's Response to Finding No. 393:

Rambus has no specific response.

394. Part III of the EIA Legal Guides relate to market research activities. Because JEDEC has never engaged in market research activities, Part III of the EIA Legal Guides is not applicable to JEDEC. (J. Kelly, Tr. 1828-29).

Rambus's Response to Finding No. 394:

Rambus has no specific response.

395. The Legal Guides set forth the basic rules under which EIA and JEDEC programs must operate, including the duty to act in good faith and the requirement that EIA and JEDEC programs be operated in a manner that does not result anticompetitive effects. (CX0205 at 5).

Rambus's Response to Finding No. 395:

This proposed finding misstates the language of the EIA Legal Guides, which uses the phrase "good faith" to refer to the policies and procedures adopted by the EIA and its various divisions, not to the obligations of members. The Legal Guides state that:

> "Section C. Basic Rules For Conducting Program.
>
> All EIA standardization programs shall be conducted in accordance with the following rules:

(1) They shall be carried on in good faith under policies and procedures which will assure fairness and unrestricted participation. . . ."

(CX 202 at 6; CX 204 at 5).

This language shows no intention to impose obligations on individual members, who have no say over the "policies and procedures" used to "conduct" EIA programs. Given its location within the Legal Guides, and the words used, it is apparent that this section is a general directive to the *administrators* who "conduct" the EIA's standardization activities to adopt "policies and procedures which will assure fairness and unrestricted participation." (*Id.*).

This conclusion is further buttressed by the fact that this phrase appears in "Part II" of the Legal Guides rather than "Part I." (*Id.*). The introduction to Part I states it includes "general guides" that are "required to be read and followed by all members of the association." (CX 204 at 3). The introduction to Part II *contains no such admonition to members* and refers to "legal policies," not "general guides." (CX 204 at 4).

(B) EP-3.

396. EP-3 is the EIA Manual for Committee, Subcommittee and Working Group Chairmen and Secretaries. (CX0203A at 1; J. Kelly, Tr. 1859-60 (purpose of EP-3 was to guide chairs on how to conduct meetings)).

Rambus's Response to Finding No. 396:

Rambus has no specific response.

397. EP-3 prohibits the inclusion of patented items in EIA/JEDEC standards unless the patent information has been disclosed and the patent owner has agreed to grant licenses on RAND terms. (CX0203A at 11 ("No program of standardization shall refer to a product on which there is a known patent unless all the technical information covered by the patent is known to the [committee]. The committee chairman must have also received a written expression from the patent holder that he is willing to license applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination.") (also cross-referencing EP-7)).

Rambus's Response to Finding No. 397:

The proposed finding misstates the evidence. The language says nothing about disclosure and only refers to "known patents." A more appropriate finding would simply quote the language from the manual.

398. EP-3 was made available to all EIA and JEDEC participants. (J. Kelly, Tr. 1878).

Rambus's Response to Finding No. 398:

This finding should track the language used in the cited testimony, which was that the manual was provided to JEDEC committee members *if they asked for it.* (Kelly, Tr. 1862).

(C) EP-7-A.

399. EP-7 is the Style Manual for Standards and Publications of EIA, TIA, and JEDEC. (JX0054 at 1).

Rambus's Response to Finding No. 399:

Rambus has no specific response, except to note that the cited manual is EP-7-A, which was replaced in 1995 by EP-7-B. (RX 616 at 1; Kelly, Tr. 2081-82).

400. EP-7 requires JEDEC members to avoid patented items or process unless disclosure has been made and the owner of the intellectual property agrees to RAND licensing. (JX0054 at 9 ("Avoid requirements in EIA standards that call for the exclusive use of a patented item or process. No program standardization shall refer to a patented item or process unless all the technical information covered by the patent is known to the [committee]. The committee chairman must have also received a written expression from the patent holder that he is willing to license applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination")).

Rambus's Response to Finding No. 400:

The proposed finding misstates the evidence. The language says nothing about "disclosure," as the finding suggests. A more appropriate finding would simply quote the language from the manual.

401. The term "patent" as used in EP-7 means issued patents as well as patent applications. (J. Kelly, Tr. 1886-88).

Rambus's Response to Finding No. 401:

This proposed finding is not supported by the weight of the evidence. Rambus has provided citations to a large number of contemporaneous documents showing that the EIA encouraged, but did not require, the disclosure of patent applications. *See* RRFF 320.

402. EP-7 was made available to all EIA and JEDEC participants. (J. Kelly, Tr. 1878).

Rambus's Response to Finding No. 402:

This finding should be modified to reflect Mr. Kelly's actual testimony, which was that the manual was provided to JEDEC committee members if they requested it. (Kelly, Tr. 1862).

(D) JEDEC Manual of Organization and Procedure.

403. The JEDEC Manual of Organization and Procedure was directed to all members. (CX0205 (JEP21-H) CX0208 (JEP21-I); J. Kelly, Tr. 1913-14 (purpose of JEP21 was to provide sector-specific guidance to JEDEC engineering committees); 1914-15 (the JEDEC manual was "made available to all new members at the time they became members. It was also made available to committee chairs when they assumed their responsibility as committee chairs. It was also brought to meetings by the staff people who were responsible for the committees and available at the meeting if anyone cared to review the document."); Sussman, Tr. 1349 (never heard of Manual of Organization and Procedure referred to as "Chairman's Manual."); Landgraf, Tr.1702-04 (never heard of Manual or Organization and Procedure referred to as "Chairman's Manual;" "it was given out by Mr. Townsend to all new members from companies. So, every time a company either joined JEDEC or they changed members, they would get a new copy of this, this document."); Rhoden, Tr. 313 ("never" heard of Manual of Organization and Procedure referred to as "Chairman's Manual.")).

Rambus's Response to Finding No. 403:

Rambus has no specific response, except to note that Complaint Counsel did not establish that manual 21-I had ever received the EDEC approval that it needed to become effective and that any JEDEC manual during the time Rambus was a member was necessarily subservient to

the governing EIA manual. (Kelly, Tr. 2105; RX 1179 at 1; Kelly, Tr. 1915-18).

404. The Manual of Organization and Procedure is the manual by which all JEDEC activities are conducted. (Rhoden, Tr. 313 ("This is the manual that is for all of the participants inside JEDEC to operate and for JEDEC committees to operate under."); Landgraf, Tr.1702 ("Manual 21-I is the standards and policies."); G. Kelley, Tr. 2385 ("I would control the agenda and make sure that. . . the meeting was run by JEDEC's manual of operation and procedures."); Williams, Tr. 790 ("I don't know exactly what the JEP stands for, but it is a manual that guides the policies of JEDEC, how the JEDEC ought to operate" including the patent policy)).

Rambus's Response to Finding No. 404:

Rambus has no specific response, except to note that: (1) Complaint Counsel did not establish that the 21-I manual had ever received the necessary EDEC approval; and (2) any JEDEC manual during the time Rambus was a member was necessarily subservient to the governing EIA manual. (Kelly, Tr. 2105; RX 1179 at 1; Kelly, Tr. 1915-18).

(1) JEP21-H.

405. JEDEC Manual of Organization and Procedure 21-H ("JEP21-H") was the version in effect between 1991 and late 1993. (J. Kelly, Tr. 1913-14 (21-H was in effect in 1990); CX0208 at 1 (published October 1993)).

Rambus's Response to Finding No. 405:

Because Complaint Counsel did not establish that manual 21-I had ever received the EDEC approval that it needed to become effective, there is no record evidence that 21-H ceased to be the effective JEDEC manual. (Kelly, Tr. 2105).

406. JEP21-H specifically incorporates the EIA Legal Guides. (CX0205 at 14; J. Kelly, Tr. 1916)).

Rambus's Response to Finding No. 406:

Rambus has no specific response.

407. JEP21-H noted that EIA Legal Counsel was authorized to advise the committees concerning interpretation of the Legal Guides. (CX0205 at 14 ("EIA Legal Counsel can advise

the Counsel and Committees from time to time concerning interpretation of Legal Guides"); J. Kelly, Tr. 1916-17)).

Rambus's Response to Finding No. 407:

Rambus has no specific response.

(2) JEP21-I.

408. Beginning as early as January 1992, JEDEC began considering making revisions to its manual of organization and procedure. (JX0011 at 5; CX0035 at 9 ("the secretary [of the JEDEC Council] outlined the genesis for the changes the fact that a new set of policy statements and guidelines have been written that will be circulated to the Council for review and comment")).

Rambus's Response to Finding No. 408:

Rambus has no specific response.

409. The 1993 revisions were motivated by the allegations that Wang made that it did not understand the patent policy to apply to patent applications. This caused immediate concern in the JEDEC organization, and there was an initiative almost from that moment forward, when that defense or allegation was first raised, to clarify the patent policy so that it would be clear in the future that "patent" meant patents and patent applications. (J. Kelly, Tr. 1930-32 ("there was litigation that arose out of a JEDEC standard-setting activity involving WANG Technologies. . . one of the defenses or allegations that WANG made in that case was that they did not understand the patent policy to apply to patent applications. This caused immediate concern in the JEDEC organization, and there was an initiative almost from that moment forward. . .to clarify the patent policy so that it would be clear in the future that 'patent' meant patents and patent applications, and there would never be a repetition of the situation presented in the WANG case.")).

Rambus's Response to Finding No. 409:

Complaint Counsel did not meet their burden of establishing that the "1993 revisions," by which they presumably mean the 21-I manual, ever received the necessary EDEC approval. (Kelly, Tr. 2105).

410. The proposed revisions were shown and discussed at JEDEC meetings. (JX0014 at 25; Williams, Tr. 791 (discussions led by Mr. Townsend), 892 ("I do know that we did discuss [the revisions] at multiple meetings."); J. Kelly, Tr. 1936-37 (Mr. Townsend was personally involved in revision process)).

Rambus's Response to Finding No. 410:

Complaint Counsel did not meet their burden of establishing that the "proposed revisions," by which they presumably mean the 21-I manual, ever received the necessary EDEC approval. (Kelly, Tr. 2105).

411. The proposed revisions to the language of the Manual of Organization and Procedure were discussed at the December 1992 42.3 meeting. (CX0045A at 11-14; JX0014 at 23-27; G. Kelley, Tr. 2416-17).

Rambus's Response to Finding No. 411:

Complaint Counsel did not meet their burden of establishing that the "proposed revisions," by which they presumably mean the 21-I manual, ever received the necessary EDEC approval. (Kelly, Tr. 2105). The cited minutes show that the material that was presented was described as a "draft." (CX 45A at 2).

412. The final revisions to the language of the Manual of Organization and Procedure were discussed at the September 1993 JC-42.3 meeting. (JX0017 at 12-14).

Rambus's Response to Finding No. 412:

Complaint Counsel did not meet their burden of establishing that the "final revisions," by which they presumably mean the 21-I manual, ever received the necessary EDEC approval. (Kelly, Tr. 2105). The cited minutes show that the material that was presented was described as a "draft" that "has not been approved. . . ." (JX 17 at 12).

413. Richard Crisp of Rambus attended meetings at which the revisions were shown and discussed (JX0014 at 1; JX0017 at 1). David Mooring of Rambus also attended the December 1992 meeting. (JX0014 at 1-2).

Rambus's Response to Finding No. 413:

Rambus has no specific response.

414. In October 1993, version "I" of the JEDEC Manual of Organization and Procedure was published. (CX0208 at 1).

Rambus's Response to Finding No. 414:

Rambus agrees that the 21-I manual bears a publication date of October 1993. (CX 208 at 1). Complaint Counsel did not establish that the manual ever became effective.

415. The 1993 revisions make more explicit that the disclosure rule applied to applications and conformed with the manner in which the EIA/JEDEC patent policy had been interpreted and applied prior to October 1993. (J. Kelly, Tr. 1927-28 ("This manual [21-I] made more explicit the requirement to disclose both issued patents as well as patent applications"); G. Kelley, Tr. 2411 ("another change was the inclusion of patent applications in the wording of the patent section of our document")).

Rambus's Response to Finding No. 415:

This proposed finding, and its reliance upon the testimony of John Kelly and Gordon Kelley, presents a useful example of just how murky and inconsistent the witnesses' understandings were of the patent policy in the early 1990's, for John Kelly and Gordon Kelley directly contradicted each other on these very basic issues. John Kelly testified that he had always understood that patent applications had to be disclosed under the EIA's interpretation of the word "patent." (Kelly, Tr. 1886-87). Gordon Kelley, on the other hand, testified to exactly the opposite. He said that he understood that the EIA used "patent" to mean "patent" and that the EIA policy had *not* required JEDEC members to disclose patent applications. (Kelley, Tr. 2676-79). He also testified that preparation of the 21-I manual required most JEDEC committees to change their practice, which was "difficult to do" under "existing laws," meaning the EIA and ANSI legal guides. (*Id.*).

416. One of the revisions provided additional clarity that the patent policy required disclosure of patent applications. While the wording the manual was revised, it did not reflect a substantive change in the policy. (CX2191 at 5 (notes of NEC representative describing "main"

change to the manual without any mention of the patent policy); G. Kelley, Tr. 2415-16 ("Q. Based on your understanding of the JEDEC policy in the early 1990s, and based on your understanding as one of the individuals involved in working on the addition to the JEDEC manual, did you understand that the work that you were doing in the manual would change in any way the substance of the JEDEC disclosure policy? A. No."); J. Kelly, Tr. 1927 ("this was a restatement of the patent policy, and it in no way varied the policy itself. It changed some of the verbiage."); CX2057 at 177-78 (Meyer 12/13/00 Dep.) ("Q. But did the written policy itself change at any time between January of '91 and December of '96? A. We changed it. JEDEC council changed the wording. Q. Did that in your mind change the policy? A. No, it did not change the policy."); Williams, Tr. 791-92 ("the policy wasn't what was being revised; only the manual was being revised. The policy, even from my very first time at JEDEC, was always the same, and that is you needed to disclose if you felt that you had IP. . . on something that was being discussed at JEDEC.")).

Rambus's Response to Finding No. 416:

As noted in Rambus's response to CCFF no. 415, during cross-examination Gordon Kelley revised the testimony cited here and testified that the provisions contained in the 21-I manual *did* mean a change for most of the JEDEC committees and was "difficult to do" under "existing laws" as a result. (Kelley, Tr. 2676-79). Moreover, Complaint Counsel did not establish that EDEC – which had responsibility for those "existing laws" – ever approved the 21-I manual. (Kelly, Tr. 2105).

417. Beginning in January 1992, the JEDEC Council worked on a set of revisions for the JEDEC manual. One of the revisions included a specific reference to patent applications in the wording of the patent section of the manual. (JX0011 at 5; G. Kelley, Tr. 2410-11). Throughout 1992 and into 1993, the Council circulated and discussed draft revisions to the manual. (CX0035 at 9; CX0039 at 12; CX0046 at 9; G. Kelley, Tr. 2411-16, 2419-23). In May 1993 and again in September 1993, the JEDEC Council reviewed and approved the revisions to the JEDEC manual. (CX0054 at 7; CX0055 at 2; G. Kelley, Tr. 2423-28).

Rambus's Response to Finding No. 417:

Rambus has no specific response to this finding, other than to note that it does not refer in any way to EDEC approval of the 21-I manual.

418. JEP21-I was made available to all JEDEC participants. (J. Kelly, Tr. 1923-24;

Landgraf, Tr. 1702-04 ("I'm not sure if I received this at my first meeting or second or third meeting, but it was given out by Mr. Townsend to all new members from companies"); Richard Crisp, Rambus' JEDEC representative, was provided a copy of the JEDEC 21-I Manual. (Crisp, Tr. 2977-78; CX0208A)).

Rambus's Response to Finding No. 418:

Mr. Crisp did not receive a copy of the 21-I manual until the summer of 1995. (Crisp, Tr. 3475).

G. Remedies for Violations.

419. There is no mechanism for EIA or JEDEC to force members to comply with the patent policy or any other rule. (J. Kelly, Tr. 1966 ("the entire process is voluntary, and as a voluntary standards development organization, we really don't have the power to impose sanctions against members who don't comply with the policy."), 2006-07 ("we could write to the company and say we're very disappointed in your behavior. What we couldn't do is to impose sanctions against the company. . . as a practical matter, there is very little we can do other than a slap on the wrist to enforce these rules."); Rhoden, Tr. 610-11 ("your actions, by definition, have to be voluntary, because there is no way that EIA or any of the organizations could, in fact, force you to do it.")).

Rambus's Response to Finding No. 419:

Rambus has no specific response.

420. JEDEC is unable to impose sanctions on companies because participation in JEDEC provides a competitive advantage to companies and, therefore, must be open even to companies that violate the patent disclosure rules. (J. Kelly, Tr. 2006-07 ("participation in a JEDEC standard-setting activity confers a significant competitive advantage on the participants, and were we to act in a way that would deny them that competitive advantage, EIA and JEDEC would be subject to lawsuits for violation of the antitrust laws ourselves.")).

Rambus's Response to Finding No. 420:

This is a legal conclusion, not a finding of fact. It seems unlikely that as a matter of contract or of antitrust law, JEDEC would be required to allow companies to attend meetings if they insisted on engaging in price-fixing or other cartel behavior during meetings.

421. JEDEC's primary recourse is to remove the subject intellectual property from its

standards. (J. Kelly, Tr. 2007-08 ("we could withdraw the standard"); G. Kelley, Tr. 2431-32 ("If the JEDEC organization . . . had found out that there was patent material that applied to a standard that we had approved without the knowledge of that patent material, then the validity of that standard was in question and we often either we removed the standard or expected the patent issue to be resolved."), 2464 ("patent issues are almost terminal for a ballot to pass")). *See, e.g.,* CX0346 at 1 ("TI did not disclose to the Committee that they had this patent until JEDEC approved some standards. The Committee is very suspicious of TI because TI did not pursue any requests for royalties until after the JEDEC standard was approved. . . A new ballot was issued . . . to rescind the standards affected by the TI patent.").

Rambus's Response to Finding No. 421:

The proposed finding is inconsistent both with the contemporaneous documents and with JEDEC's behavior in connection with the TI "Quad Cas" issue cited in support of the finding. All ballots to withdraw the Quad Cas feature were themselves *withdrawn* once TI had issued a RAND letter. (JX 25 at 3; Kellogg, Tr. 5220-26). JEDEC's behavior in this regard is consistent with the policy statement provided by the EIA to the FTC in its 1/22/96 letter:

> "Even if knowledge of a patent comes later in time due to the pending status of the patent while the standard was being created, the important issue is the license availability to all parties on reasonable, non-discriminatory terms."

(RX 669 at 4).

422. JEDEC members, including Rambus, understood that failure to disclose means that the patent owner may be unable to enforce the patent against the standard. (CX1942 at 1 ("I [Lester Vincent] said there could be equitable estoppel problem if Rambus creates impression on JEDEC that it would not enforce its patent or patent [applications]."); CX1937 (billing records of Lester Vincent noting "Conference with Richard Crisp and Allen Roberts concerning equitable estoppel issue with respect to JEDEC."); CX1990 at 1 (Lester Vincent forwarding materials to Rambus concerning Dell consent decree); CX0858 at 2 ("I [Richard Crisp] understand the concerns about the patent policy and some potential exposure we could have in the event of future litigation. [Equitable Estoppel and Laches]); Appleton, Tr. 6329 ("if [a company] fail[ed] to disclose [patents or patent applications], then. . . they couldn't come back later and try to enforce those against the standard that had been developed"); Lee, Tr. 6598-99 ("if [a company]

failed to disclose the patent that may relate to the work of the committee and if it was adopted into the standard, that [company] would forego their right to enforce the patent against the standard."); Rhoden, Tr. 611-12 ("any company that did not disclose necessarily gave up their right to that IP as it related to the standard. That is what I understood.")).

Rambus's Response to Finding No. 422:

The evidence does not support a finding that Rambus understood that a mere failure to disclose might result in an inability to enforce its patents. The evidence cited by Complaint Counsel supports only the proposition that there could be a problem if "Rambus creates impression on JEDEC that it would not enforce" its intellectual property. (CX 1942 at 1). (*See also* Crisp, Tr. 3470-71 – Crisp understood from Vincent that "we should not mislead JEDEC into thinking that we wouldn't enforce our property rights.").

The evidence shows that Mr. Crisp followed Mr. Vincent's advice by openly refusing to comment about Rambus's intellectual property position at the May 1992 and September 1995 JEDEC meetings. *See* RPF 492-514 and evidence cited therein. The evidence also shows that Rambus said nothing and did nothing to mislead JEDEC members into believing that Rambus would not seek or enforce intellectual property rights over features incorporated in JEDEC standards. *See* RPF 464-558.

This proposed finding also relies upon testimony by Micron CEO Steve Appleton, Micron engineer Terry Lee, and AMI2 President Desi Rhoden. The financial interests of these witnesses is apparent, and their personal understanding of the law of equitable estoppel is irrelevant.

H. Incidents of Non-Disclosure & JEDEC's Response.

423. There have been occasions in which JEDEC participants did not disclose patent information that might related to JEDEC work. These incidents have resulted in either (1)

rescission of the standard (Quad CAS); (2) the selection of an alternative standard (SEEQ); or (3) litigation (Wang). (See CCFF following).

Rambus's Response to Finding No. 423:

This proposed finding falsely states that standards incorporating the Quad Cas technology were rescinded. They were not. Once Texas Instruments provided a "RAND" letter, all ballots that had *proposed* to withdraw the technology from standards were themselves withdrawn. (JX 25 at 3). In any event, this finding is irrelevant and improper since it offers no evidentiary support for this proposition – or for the other two propositions it advances.

1. Quad CAS.

424. The Quad CAS incident involved the alleged failure of Texas Instruments to disclose properly its issued patent relating to Quad CAS technology. The issue arose at the JC-42.3 subcommittee meeting in September 1993, when Micron accused Texas Instruments of having failed to comply with the JEDEC disclosure policy. (JX0017 at 6; CX0346 at 1 (JEDEC Secretary Ken McGhee writing to John Kelly that "TI did not disclose to the Committee that they had this patent until JEDEC approved some standards. The Committee is very suspicious of TI because TI did not pursue any requests for royalties until after the JEDEC standard was approved."); CX0452 (McGhee 11/3/93 Letter distributed to all JC-42.3 members a memo, discussed by Jim Townsend at the September 1993 meeting, drawing their attention to "the existing rules of the EIA governing patentable matters," and reminding them of their obligation to relevant "patents held and applied for"); Williams, Tr. 776-77 ("this was a case where it was found out that TI had. . . had a patent on the quad CAS device that had just been standardized or was in the process of being standardized, and it did pass, became a standard. . . I can't remember exactly where it was, but I remember a great uproar in the committee based upon it."); Sussman, Tr. 1335 ("they proposed a quad CAS, and after the part was standardized, after some modules were standardized, then the company revealed its patent position, and we were rather upset. We had spent a lot of time and energy, wasted a lot of time and energy.")).

Rambus's Response to Finding No. 424:

Rambus has no specific response, except to note Mr. Sussman's testimony that TI had themselves "proposed" the Quad Cas standard. Rambus never presented any technology to JEDEC for standardization or advocated the adoption of any feature or device.

425. Micron Corporation notified the Committee that TI had asserted patent claims against it and that TI was going to charge license fees and royalties for the use of the concept of Quad CAS. (G. Kelley, Tr. 2464). At the time there were pending Committee ballots pertaining to the use of Quad CAS as part of the SDRAM standard; when TI refused to comment on the patent issues pertaining to these ballots, the Committee determined unanimously to place the ballots on hold until the patent issue was resolved. (JX0017 at 6; G. Kelley, Tr. 2465-66). The Committee also voted to prepare a ballot to rescind portions of previously-passed standards pertaining to Quad CAS. (JX0017 at 7; G. Kelley, Tr. 2466-68). (CX2059 at 181-82 (Karp, Infineon Dep.) (Samsung, most likely Joel Karp, seconded the Micron motion to remove the Quad CAS standards.)).

Rambus's Response to Finding No. 425:

Rambus has no specific response.

426. The Quad CAS issue arose again at the December 1993 meeting of the JC-42.3 subcommittee, when there was an extensive discussion of the issue. Members stated that the key issue was the disclosure to the JC-42.3 subcommittee of the relevant patents and that Texas Instruments was not following the JEDEC disclosure policy. (JX0018 at 8 (Mr. Kelley noted that the letter from TI [explaining its position] does not address the key issue that the Committee was not informed of TI's patent. TI was asked why the Committee was not informed of the patents. TI did not respond because litigation is going on. . . . –Samsung: We are reluctant to vote yes [on the ballot relating to the proposed standard] because we do not think TI is following the patent policy. . . . Micron noted that all companies should have equal access to a standard developed by the Committee. . . . –Sanyo: It is understood that if and when TI conforms to the EIA policy, work should continue. . . . if TI has knowingly and intentionally violated the EIA/JEDEC patent policy, EIA may need to consider additional actions/discussions with TI.); G. Kelley, Tr. 2475 (IBM may not participate if information being hidden); G. Kelley, Tr. 2470-72 (describing discussion that took place at the meeting)). *See also* (CX2955 at 2 (Joel Karp letter voting to rescind Quad CAS standards because "TI is unwilling to provide such a demonstration [of reasonable terms and conditions free of unfair discrimination] for review by potential licensees.")).

Rambus's Response to Finding No. 426:

The cited evidence does not support the second sentence of the proposed finding. Most of the remarks focus on the availability of licenses on reasonable terms, not disclosure. As Micron explained it, "all companies should have equal access to a standard developed by the Committee." (JX 18 at 8). The Sanyo remark also shows that the key question was availability

of the patent on "RAND" terms. (*Id.*). As previously noted, once TI agreed to provide a "RAND" letter, all ballots that had proposed to withdraw the Quad Cas technology were themselves withdrawn. (JX 25 at 3; Kellogg, Tr. 5220-26).

Complaint Counsel also omit a relevant passage from the page of the December 1993 minutes that they cite. Just before the Sanyo comment, an IBM comment appears:

> "IBM noted that in the future they will not come to the Committee with a list of applicable patents on standards proposals. It is up to the user of the standard to discover which patents apply."

(*Id.*).

EIA General Counsel John Kelly testified that he reviewed and approved the draft minutes containing the IBM comment. (Kelly, Tr. 2117; CX 348 at 1: "Ken – the draft minutes are fine.").

427. The following month, Gordon Kelley of IBM wrote to Buf Slay of Texas Instruments, expressing concern that TI's conduct could have and adverse impact on JEDEC's work. (CX2384 ("I am and have been concerned that this issue can destroy the work of JEDEC. If we have companies leading us into their patent collection plates, then we will no longer have companies willing to join the work of creating standards; i.e., widely used designs. . . .If we allow JC-42 standards to be used for patent collection purposes, then we do a great disservice to the very sort of industry that feeds us. . . .If we on JEDEC council do not deal with [this issue] completely, we set ourselves up for bigger problems in the future."); CX3136 at 142 (Meyer Infineon Tr.) (recalling Mr. Kelley's "patent collection plate" testimony); Appleton, Tr. 6331-32 (failure to disclose would discourage Micron from participating)).

Rambus's Response to Finding No. 427:

The evidence shows that JEDEC routinely approved ballots despite awareness of patents relating to the proposed standards, and that it often did so without even *requesting* RAND assurances. RPF 1220-1238. Moreover, regardless of the language of Mr. Kelley's letter, the

undisputed truth is that as soon as TI agreed to issue a "RAND" letter, the dispute ceased and all ballots seeking to withdraw the Quad Cas technology were withdrawn. (JX 25 at 3; Kellogg, Tr. 5220-26). It is evident that "the important issue is the license availability to all parties on reasonable non-discriminatory terms." (RX 669 at 4).

428. At the following meeting in March 1994, the issue was revisited. TI requested a clarification of the Committee's interpretation of the patent policy; in response to a question from the chairman, members stated unanimously that the policy was clear. (JX0019 at 5 ("Applicability of patents to use of JEDEC standards was discussed. The issue is warning, IBM noted. Failure to disclose a patent prevents the Committee from considering the standard. The Committee was asked if the patent policy is clear. The Committee felt it was clear."); CX2375 at 1-2 (notes of Mark Kellogg summarizing the Quad CAS discussion at the March 1994 meeting); Kellogg, Tr. 5028-29 (recalling that vote was unanimous that patent policy was clear)).

Rambus's Response to Finding No. 428:

The proposed finding is incomplete. The minutes, and the pertinent testimony at trial, show that Chairman Kelley's principal response was that the motion was improper:

> "TI then made the motion [for clarification]. The Committee did not second the motion and felt it may be beyond the scope of this Committee. IBM noted that the issue should have been taken to the JEDEC Council because Council has been working on patent policies for some time and are beyond the scope of the Committee."

(JX 19 at 4). (*See also* Kellogg, Tr. 5224-26) ("Gordon was stating that the – any modification to the patent policy was within the scope of council, not the committee. . . . If the words change, that is the council. That's policy."

429. EIA legal counsel issued a memorandum stating that "[w]ritten assurance must be provided by the patent holder when it appears to the committee that the candidate standard may require the use of a patented invention.') (CX0353 at 1 (emphasis in original); *see also* CX0355 (memorandum from JC-42 Secretary, Ken McGhee, forwarding Mr. Kelly's memorandum to all

members of the JC-42 committee. (CX0355).

Rambus's Response to Finding No. 429:

Rambus has no specific response.

430. Richard Crisp was present at the September 1993, December 1993, and March 1994 JC-42.3 subcommittee meetings, and reported details of the Quad CAS discussion back to others at Rambus. (CX0710 at 1 (TI was chastised for not informing JEDEC that it had a 1987 patent on quad CAS devices. . . . The bottom line is that all quad CAS devices will be removed from standard 21C.)).

Rambus's Response to Finding No. 430:

Rambus has no specific response.

431. Pursuant to these discussions, the JC-42.3 subcommittee rescinded the Quad CAS standard. (JX0018 at 9 (ballot to remove standard passed); CX0710 at 1 (Richard Crisp noting that the standard will be rescinded); G. Kelley, Tr. 2479-80 (conveying to the committee the importance the Quad CAS lesson in light of rescission of standard); Williams, Tr. 776-77 (standard rescinded).

Rambus's Response to Finding No. 431:

Rambus has no specific response.

432. In early 1995, Texas Instruments agreed to comply with the JEDEC patent policy and removed their representative who failed to provide the Quad CAS disclosure. (JX0025 at 3 ("A letter from TI was received at JEDEC complying with the EIA patent policy"); G. Kelley, Tr. 2486). The Quad CAS ballot was taken off hold. (JX0025 at 3).

Rambus's Response to Finding No. 432:

As this finding demonstrates, once Texas Instruments agreed to provide RAND assurances, the technology remained in the standard. (JX 25 at 3; Kellogg, Tr. 5220-26).

2. SEEQ.

433. A company named SEEQ proposed a JEDEC standard called silicon signature. (Sussman, Tr. 1338). SEEQ owned two patents relating to the technology, but disclosed and offered to license only one. (Sussman, Tr. 1338-39 (SEEQ "was telling us about silicon signature and offering it as a royalty-free license to anyone who wanted it, hoping that just as

soon as we standardized this, the second patent, which would be die trace, which he had not said anything about, but because it was almost identical, would be insisted upon by the customers, and [SEEQ] could put a tax on us.")). Upon learning of SEEQ's second patent, the committee was willing to standardize the SEEQ technology, provided that SEEQ agreed to reasonable licensing terms. (CX0003 at 4 ("The Committee felt they would like to proceed with [the SEEQ technology] for PLDs as long as reasonable rates for use remained and that Seeq would put their position in writing. There was some question about whether die trace was included in the patent release.")). When the committee learned that the second patent was not included in the patent release, JEDEC chose to standardize on a different technology. (Sussman, Tr. 1338-39 ("What we did, as we found out about the second application, is that we did not standardize either of [the SEEQ patents]. We standardized an alternate methodology."); *see also* CX0711 at 188 ("So the conclusion I reach here is that we can abide by the patent policy on a case-by-case basis. . . The things we should not do are to not speak up when we know that there is a patent issue, to intentionally propose something as a standard and quietly have a patent in our back pocket we are keeping secret that is required to implement the standard and then stick it to them later (as WANG and SEEQ did).")).

Rambus's Response to Finding No. 433:

The SEEQ story shows that it is the availability of intellectual property on reasonable terms to all comers that is "the important issue," as the EIA's ½2/96 letter states. (RX 669 at 4).

3. Wang.

434. Failure to disclose a relevant patent application precipitated litigation in the Wang matter. Wang failed to disclose a patent relating to memory modules and later attempted to enforce the patent against the industry. (Williams, Tr. 787 ("they [Wang] were part of the committee, they had helped set a standard, and then they went out and enforced their patents against everybody in the industry who used a SIMM module."); Sussman, Tr. 1338 ("that ended up in a rather lengthy litigation, crossed multiple houses and cost the industry millions of dollars before the patent was found to be invalid."); Landgraf 1697-98; JX0020 at 4 ("It as noted that the WANG patent case is coming up for trial on June 14.")).

Rambus's Response to Finding No. 434:

None of the cited evidence refers to a failure to disclose a patent application. The finding therefore lacks any evidentiary basis.

I. The Relationship to the ANSI Rules.

435. The American National Standards Institute ("ANSI") is an umbrella organization

that accredits standards-setting organizations. (J. Kelly, Tr. 1947-48 ("ANSI is one of several organizations in the United States that accredits other organizations to develop standards.")).

Rambus's Response to Finding No. 435:

Rambus has no specific response.

436. ANSI also has the authority to adopt certain of the standards that are submitted to it by its qualified organizations for adoption as American national standards. (J. Kelly, Tr. 1947-48).

Rambus's Response to Finding No. 436:

Rambus has no specific response.

437. EIA has been a dues-paying member of the American National Standards Institute since the late 1970s. (J. Kelly, Tr. 1948-49). EIA forwards certain standards developed by EIA sectors to ANSI for adoption as American National Standards. (J. Kelly, Tr. 1948-49).

Rambus's Response to Finding No. 437:

Rambus has no specific response.

438. John Kelly was a member of the ANSI patent policy working group from 1990 until 2002 and was personally involved in the discussions and deliberations leading to the final approval of the ANSI guidelines. (J. Kelly, Tr. 1950-51 ("I got involved at a relatively late stage in the process, but I participated fairly actively in the discussions and the deliberations that led up to the final approval of the guidelines by the working group. And I have been also been involved in a number of discussions over the ensuing ten years about the guidelines and proposed amendments to the guidelines.")).

Rambus's Response to Finding No. 438:

Rambus has no specific response.

439. The EIA patent policy is in compliance with, but not identical to, the ANSI patent policy guidelines. (J. Kelly, Tr. 1957-58).

Rambus's Response to Finding No. 439:

This proposed finding is too vague to be meaningful. Mr. Kelly testified that the *wording* of the ANSI and EIA patent policies was "essentially identical:"

"Q. Now, the EIA patent policy in this time period, 1994, the wording was essentially identical to the ANSI patent policy, right?

A. Very close, yes.

Q. Can you agree with the words, 'essentially identical?'

A. Essentially identical, I will accept your phraseology, yes, sir."

(Kelly, Tr. 2077-78).

It is also undisputed that by October 1995, at the latest, the EIA had adopted the ANSI Patent Policy in toto. EIA Manual EP-7-B, published in October 1995, provides that "[s]tandards and publications are adopted by EIA in accordance with the American National Standards Institute (ANSI) Patent Policy." (RX 616 at 2).

440. ANSI has audited EIA and has always found EIA in compliance with ANSI patent policy during those audits. (J. Kelly, Tr. 2148-49 ("The patent policy is consistent with the ANSI patent policy, and my basis for saying that is that EIA has been audited by ANSI in general in terms of the record retention and also in terms of its written policies and never been found not to be in compliance with the ANSI patent policy."), 2154-55 ("my understanding is we are in compliance with the policy and have been.")).

Rambus's Response to Finding No. 440:

Rambus has no specific response, except to note that neither the finding nor the cited evidence indicates when the audits occurred.

441. The ANSI patent policy guidelines do not require rigid adherence to every single aspect of the ANSI patent policy. (RX1712 at 3 (ANSI guidelines "are suggestions -- adherence is not essential for standards developers to be found in compliance with ANSI's patent policy. Rather, this is an effort to identify possible procedures that a standards developer may wish to adopt, either in whole or in part, for purposes of effectively implementing the patent policy. Additional or different steps may also be selected for such purposes."); J. Kelly, Tr. 1956-57 ("we were trying, as a member of the patent policy group, to establish some general guidance for the benefit of standards developers that they could either follow or not follow, in whole or in part, and we're emphasizing here that. . . standard developers had the option of adopting additional or different steps from those suggested from the guidelines that might be appropriate

in the case of their own standards development activities.")).

Rambus's Response to Finding No. 441:

The proposed finding is irrelevant, for it is undisputed that:

(1) the language of the EIA Patent Policy and that of the ANSI policy are "essentially identical," (Kelly, Tr. 2077-78);

(2) the EIA adopted the ANSI Patent Policy in toto no later than October 1995, when EP-7-B was published, (RX 616 at 2); and

(3) the EIA informed the FTC in January 1996, on behalf of JEDEC and its other standard-setting activities, that it "follow[ed] the ANSI intellectual property rights (IPR) policy." (RX 669 at 2).

442. One aspect of the EIA/JEDEC patent policy that goes beyond the requirements of ANSI's patent policy is that the EIA/JEDEC policy requires the disclosure of patent applications as well as issued patents, whereas the ANSI patent policy requires the disclosure only of issued patents. (CX0208 at 19; J. Kelly, Tr. 1957-58 ("there is a material difference between the ANSI policy and the EIA/JEDEC policy, and that is that the EIA/JEDEC policy requires the disclosure of patent applications as well as issued patents.")).

Rambus's Response to Finding No. 442:

Rambus agrees that the ANSI Patent Policy does not require the disclosure of patent applications, and that the ANSI policy also did not require such disclosure in the early to mid-1990's. Rambus disagrees with the statement in this proposed finding that the "EIA/JEDEC policy requires the disclosure of patent applications . . . ." The great weight of evidence is to the contrary, as set out in detail at RPF 204-273. In particular, it is undisputed that in January 1996, in a formal comment letter to the Federal Trade Commission, the EIA stated on behalf of JEDEC and its other standard-setting activities that it "endorse[d] and follow[ed] the ANSI intellectual

property rights (IPR) policy." (RX 669 at 2). Moreover, in June 1996, when the Federal Trade Commission responded to the EIA's January 22, 1996 letter, the FTC stated that the "EIA and TIA, *following ANSI procedures*, encourage the early, *voluntary* disclosure of patents, but *do not require* a certification by participating companies regarding potentially conflicting patent interests." (RX 740 at 1) (emphasis added).

This exchange of formal letters shows clearly that at the precise time of Rambus's departure from JEDEC, both the standards body that it had been a member of, and the federal agency that is now prosecuting it, understood with great clarity that the EIA "follow[ed]" the ANSI Patent Policy. (RX 669 at 2; RX 740 at 1). The parties agree that the ANSI Patent did *not* require disclosure of patent applications. CCFF 441.

Even in 2000, *after* JEDEC had become an independent organization with its own rules, one basic rule had not changed: the disclosure of patent applications was still "not required," as the minutes of the February 2000 meeting of JEDEC's board of directors state. (RX 1570 at 13). (*See also* RX 1582 at 1 – February 2000 e-mail by JEDEC Secretary Ken McGhee stating that a JEDEC member's disclosure of a patent application went "one step beyond" the patent policy).

443. The EIA/JEDEC patent policy is consistent with the ANSI patent policy guidelines, notwithstanding the different treatment of patent applications. (J. Kelly, Tr. 1959). ANSI guidelines specifically acknowledge that a standards development organization may wish to at least consider including patent applications as well as patents in their patent disclosure policy. (RX1712 at 8 ("Similarly, a standards developer may wish to encourage participants to disclose the existence of pending U.S. patent applications relating to a standard under development."); J. Kelly, Tr. 1959-60, 2154 ("there are options that individual standard developer organizations can adopt that are not identical to the ANSI policy to address specific issues. . . an example that we specifically give in these guidelines is that standard developers may elect to require the disclosure of patent applications as well as issued patents.")).

Rambus's Response to Finding No. 443:

For the reasons set out in RRFF 439-442, the EIA/JEDEC Patent Policy and the ANSI Patent Policy are, in fact, consistent, in part because neither requires the disclosure of patent applications. *See also* RPF 204-273.

444. Paragraphs 444 to 499 are unused.

IV. The Development of JEDEC DRAM Standards.

A. The First Generation SDRAM Standard.

1. The Origins of the Standard.

500. "Asynchronous DRAM" is a term that is used to describe DRAMs that are driven off the RAS and CAS signals where the RAS and CAS actually control the operation of the DRAM rather than a clock. (Jacob, Tr. 5394).

Rambus's Response to Finding No. 500:

Rambus has no specific response.

501. Page mode and extended data out or "EDO" DRAMs are types of asynchronous DRAM (Sussman, Tr. 1469; Polzin, Tr. 4031; Horowitz, TR. 8581). In the late 1980's page mode and EDO DRAMs were commonly used in the industry. (Sussman, Tr. 1361). Page mode and EDO DRAMs were standardized at JEDEC. (Sussman, Tr. 1362; Prince, Tr. 9020-9021).

Rambus's Response to Finding No. 501:

Rambus has no specific response.

502. In the late 1980's, microprocessors were demanding more performance out of DRAMs. (Kelley, Tr. 2388-2389).

Rambus's Response to Finding No. 502:

The proposed finding is misleading in suggesting that this situation was peculiar to the late 1980s. It is a matter of common knowledge that microprocessor speeds, and hence the performance demanded of DRAMs, have been increasing since well before the late 1980s. DRAMs were, however, still able to keep up with the increased demands in the late 1980s.

In the late 1980s, Michael Farmwald foresaw that, if the trends continued, there would be a memory "bottleneck" in the future, with memory unable to keep pace with processor speeds. (Farmwald, Tr. 8068-69). This was before others recognized that such a memory bottleneck was on the horizon. (*E.g.* McWilliams, Tr. 4929 ("Q. When did you first come to recognize the

existence of such a bottleneck? A. We [Intel] saw the bottleneck coming about '95, at which time we decided we needed to do something to make memories speed up more quickly.")).

503. In order to respond to this demand and to ensure that the new JEDEC standard would result in common parts that were plug compatible, the JC-42.3 subcommittee began to standardize certain aspects of DRAM performance and design relationships. (CX0035 at 14; G. Kelley, Tr. 2390-2391). Prior to that time, JC-42.3 work had generally focused on standardizing the location of pins, also known as pin-out diagrams. (G. Kelley, Tr. 2388).

Rambus's Response to Finding No. 503:

The proposed finding is incomplete. While the original impetus for going beyond standardization of pinouts may have been to ensure plug compatibility (i.e. interoperability) of more complex designs, the JC-42.3 subcommittee later overstepped these boundaries and began standardizing certain technologies that are unrelated to interoperability. An on-chip DLL, for example, as included in the DDR SDRAM standard is *not* required for interoperability. Rather, as Complaint Counsel's technical expert, Professor Jacob, explained, the DLL used in DDR SDRAMs is transparent to the DRAM interface. (Jacob, Tr. 5617-18) In other words, the rest of the system is indifferent to whether there is a DLL or some other kind of circuitry on the DRAM so long as data from the DRAM arrives at the memory controller in the appropriate timing window. (Id.) To ensure interoperability, all JEDEC needed to do was to specify the required timing parameters, which would have left it up to the individual DRAM manufacturers to meet those requirements with whatever technology they chose.

504. A new generation of memory was needed because the industry anticipated that microprocessor and computer speeds would increase and the industry demanded memory that could operate at the same speeds. (CX2088 at 291-292 (Meyer, Infineon Trial Testimony, April 25, 2001).

Rambus's Response to Finding No. 504:

The proposed finding is incomplete. The industry's recognition that increasing microprocessor speeds would outstrip the capabilities of current memory technology lagged behind Rambus's recognition of this problem. (RRFF 502).

505. JEDEC entertains a number of proposals by members when working toward a standard for a new device. (Rhoden, Tr. 415 ("[W]hen we're working on a particular device or whatever, there will be proposals that are made that come from usually a number of different companies. Sometimes multiple proposals or multiple ideas, if you will, come from a particular company, but more often than not, it comes from a variety of companies. So, you will have several different proposals that will be made inside JEDEC as to what path we should take for the next improvement cycle, if you will, of what we're working on").

Rambus's Response to Finding No. 505:

Rambus has no specific response, other than to note that JEDEC members are often seeking to gain a competitive advantage through the standardization process, as Hyundai's Dr. Oh testified:

> "Q. What steps did Hyundai take to follow the work of JEDEC?
>
> A. We wanted to propose things to be adopted at the JEDEC meeting.
>
> That means if our proposal is – is adopted, that means we are ahead of our competitors, so we actively decided to attend and join the JEDEC committee."

(CX 2107, Oh Depo. Tr., 23:24-24:5).

506. JEDEC members then decide which of these ideas to pursue. (Rhoden, Tr. 415-416 ("Well, the differences of opinion are something that people have to investigate to see if particular -- if the particular proposals are viable or if they -- it usually winds up being that engineers themselves come up with the ideas, so they're almost always reasonable ideas, and it's just a question of then deciding which path they're going to take.")).

Rambus's Response to Finding No. 506:

There is substantial evidence that it is a *subset* of JEDEC members – the DRAM manufacturers – who are the principal decisionmakers on the question of which "ideas to pursue." (RX 1424 at 1: e-mail from a manufacturer representative to other manufacturer representatives, noting that JEDEC is "OUR organization and will approve whatever we decide to approve.") (capitalization in original).

507. One option considered by the JC-42.3 subcommittee was to continue to develop a new generation of EDO DRAMs. (CX0711 at 1 ("HP, Micron and Mitsubishi are now saying that EDO is the right thing to do that it offers better performance than DRAM at a much lower cost than SDRAM.").

Rambus's Response to Finding No. 507:

The proposed finding is misleading to the extent that it implies that the option of developing a new generation of EDO DRAMs was not pursued. Complaint Counsel cite an e-mail from Richard Crisp dated October 5, 1993 for this proposed finding. *After* that time, a new generation of EDO DRAMs, called "Burst EDO" was developed and standardized at JEDEC in mid-1995. (Williams, Tr. 873, 879-80; RX 585 at 1). However, Burst EDO failed in the marketplace in competition with SDRAM. (Williams, Tr. 829). As Dr. Oh of Hyundai testified regarding Burst EDO: "[T]his is enhanced version of EDO, and we wanted to convince our customers the advantages of this part, but was not accepted by our customers." (CX2108, Oh Depo., at 236).

508. JEDEC also began to consider a DRAM that had been developed by IBM called "High Speed Toggle" (G. Kelley, Tr. 2584-2585). High speed toggle is also known as "HST". (Kelley, Tr. 2441).

Rambus's Response to Finding No. 508:

Rambus has no specific response to this finding, except to note that it is vague as to when JEDEC supposedly considered the "High Speed Toggle" device.

509. HST was a partially asynchronous and partially synchronous part, in that it had asynchronous inputs but synchronous outputs. (Kellogg, Tr. 5173 ("So what high-speed toggle was was a memory device that had asynchronous inputs. In other words, it had the fastest possible access path and clocked outputs, and the clock itself was a clock that transferred data on both edges, such that we could run a relatively low-speed clock in the memory device. So asynchronous, command and address, clocked output, clocking data on both edges of the clock.")); Rhoden, Tr.437 (Q. Now, was IBM proposing a synchronous device or asynchronous device or was it something different? A. Well, in terms of data, it was a synchronous device because of the nature of how -- remember I said, I said it's a CAS clock. It's a function that's fundamentally synchronous. So, as we would toggle the CAS signal, column, clock, whatever -- whichever name you want to call it, you would get data out on -- from the rising edge and from the falling edge in a synchronous fashion.)).

Rambus's Response to Finding No. 509:

The proposed finding is incorrect. According to the definition provided by Complaint Counsel's expert, HST was an asynchronous part. Professor Jacob testified that an asynchronous DRAM is one where asynchronous RAS and CAS signals control the operation of the DRAM rather than a clock. (CCFF 500.) Since RAS and CAS were *asynchronous* in HST, it follows from Professor Jacob's definition that HST was asynchronous. (Rhoden, Tr. 568; Kellogg, Tr. 5173). Indeed, a January 1992 document written by Willi Meyer of Siemens states: "IBM presented generic high speed toggle mode in Sep'90 *which was asynchronous*." (CX2431 at 1 (emphasis added)).

510. In HST, IBM proposed to transfer data on both edges of the clock signal. (Kellogg, Tr.5173; Sussman, Tr. 1381; Rhoden, Tr. 436-437); CX2080 at 242 (Karp, Micron Dep.)(recalls that the toggle mode presentations had " some relationship to both edges of a clock.").

Rambus's Response to Finding No. 510:

The proposed finding is incorrect. HST did not transfer data on both edges of the clock signal, but on both edges of a "toggle" signal. While some witnesses loosely referred to this toggle signal as a "clock," it was not a free running clock like the system clock in a synchronous memory such as SDRAM or DDR SDRAM. (Rhoden, Tr. 437 (the HST toggle signal is not in constant operation, as opposed to the system clock in SDRAM); Sussman, Tr. 1471 (in HST, "data is synchronous with their -- I'm calling it a clock, but basically both on the rise and the falling edge of their input signal, whatever we are going to call it, I have data")).

511. IBM and other companies continued to make HST presentations at JEDEC during 1990 and 1991. (JX0002 at 92 (IBM presentation of high speed toggle); JX0003 at 56-57 (IBM presentation of high speed toggle); JX0003 at 7 (motion to send IBM HST out on survey passed unanimously); CX0316 at 1 (DRAM TASK GROUP TOGGLE MODE Questionnaire); JX0004 at 6 (approval of issuance of HST survey ballot); CX0314).

Rambus's Response to Finding No. 511:

The proposed finding that "other companies" besides IBM made HST presentations is not supported by the evidence. There is evidence only that one company besides IBM, namely Siemens, made a toggle mode presentation that was similar in some ways to IBM's HST presentation. (CCFF 512).

512. At the May 9, 1991 JC-42.3 meeting, the subcommittee passed a motion to ballot the IBM HST presentation. (JX0005 at 12). At the same meeting Siemens also made a HST presentation that was like the IBM HST except it used a G\ pin instead of a new toggle pin. (JX0005 at 12).

Rambus's Response to Finding No. 512:

The proposed finding is incomplete. Although IBM made presentations about High Speed Toggle and it was balloted, it was not a viable option. As an IBM researcher later wrote,

the High Speed Toggle DRAM was "very big, very hot, and very nonstandard." (RX 2099-7 at 16; Soderman, Tr. 9399-9400). The researcher went on to conclude that "in the commodity market, these attributes are disastrous." (*Id*.).

2. The Decision to Adopt a Fully Synchronous DRAM Standard and a Single Edge Clock.

513. At the JEDEC JC-42.3 meeting in May 1991, Howard Sussman of NEC proposed a fully synchronous DRAM to JEDEC for the first time. (Sussman, Tr. 1364; CX2088 at 272-275 (Meyer, Infineon Trial)).

Rambus's Response to Finding No. 513:

Rambus has no specific response.

514. Mr. Sussman proposed to use a single edge clock to input and output data and a programmable mode register to set CAS latency and burst length. (Sussman, Tr. 1365-1367 and 1373-1375).

Rambus's Response to Finding No. 514:

The evidence does not support the proposed finding. Mr. Sussman, who was NEC's JEDEC representative at the relevant time, did not testify that he proposed to use a programmable mode register to set CAS latency and burst length during his initial synchronous DRAM presentation in May 1991. The available documentation strongly suggests that these features were added to his proposal after that time. There was no documentation about the NEC proposal attached to the May 1991 minutes. (JX0005). A few months later, however, in August 1991, Mr. Sussman held an unauthorized meeting of JEDEC members in Boxborough, Massachusetts to discuss his synchronous DRAM proposal. (Sussman, Tr. 1369-70; CX0020). A report about that meeting prepared by Mr. Sussman was intended to provide "a consensus of where we were." (Sussman, Tr. 1370.) The description of the features of Mr. Sussman's

synchronous DRAM proposal does not include *any* mention of a mode register, programmable CAS latency, or programmable burst length. (CX0020 at 1). A report about the Boxborough meeting prepared by Gordon Kelley of IBM makes clear that Mr. Sussman was proposing a *fixed* CAS latency at this time. (RX0173 at 3 ("NEC: . . . Data Out has a four clock latency from RE\ [RAS] and a 2 clock latency from CE\ [CAS]")). Mr. Kelley's list of the main features of the NEC proposal makes no mention of a mode register or programmable burst length. (*Id.*).

At the September 1991 JEDEC meeting, Mr. Sussman made a second showing of his synchronous DRAM proposal. (JX0007 at 9). The presentation materials do not mention a mode register, programmable CAS latency, or programmable burst length. (JX0007 at 160-62).

It was not until October 1991, at a second unauthorized meeting of JEDEC members in Portland, Oregon, that Mr. Sussman's presentation materials indicate that latency and burst length should be programmable. Both programmable CAS latency and programmable burst length are included in a list of key features of the proposed device. (JX0010 at 50 ("The latency of data to the clock should be programmable;" "wrap length should be programmable."); Sussman, Tr. 1373-75). A timing diagram, a version of which had been used by Mr. Sussman at the August 1991 non-JEDEC meeting as well as the September 1991 JEDEC meeting, had the following language *added* to the right-hand column when it was used at the non-JEDEC meeting in October 1991: "Latency is programmable." (*Compare* JX0010 at 51 *with* CX0020 at 3 *and* JX0007 at 160).

Toshiba also made a presentation for a synchronous DRAM including programmable CAS latency (JX0010 at 67), causing Howard Kalter of IBM to remark that "programmable latency was the cleverest item Toshiba ever created." (RX0199 at 2). By this time, Toshiba was

a Rambus licensee and was working on the design of the first RDRAM chip. (RPF 643). Indeed, Rambus attended its first JEDEC meeting, in December 1991, at Toshiba's recommendation and as Toshiba's guest. (RPF 446).

515. At the next JC-42.3 meeting on September 18, 1991 , the subcommittee voted in favor of the IBM HST technology. However, there were four no votes and a number of comments. NEC and Samsung commented that the use of two clock edges can limit speed. (JX0007 at 8 ("NEC: Two edge trigger limits speed. . . . Samsung: Clock generation is difficult – two edge clock limits speed")). The subcommittee decided to put the ballot on hold until more resolution to the comments could be made. (JX0007 at 9).

Rambus's Response to Finding No. 515:

The proposed finding is misleading in its reference to "two clock edges," without more. IBM's HST proposal used a separate "toggle" signal which was not a free-running clock as used in synchronous DRAMs. (*See* RRFF 510).

516. Also at the JC 42.3 meeting on September 18, 1991, Mr. Sussman made a second presentation of NEC's SDRAM proposal. (JX0007 at 13 and 160-162; CX2088 at 276 (Meyer, Infineon Trial Tr. ((4/25/01)). A number of other companies also presented synchronous DRAM proposals at this meeting, including Texas Instruments (JX0007 at 13 and 163-176 (first showing of an SDRAM proposal)), Toshiba (JX0007 at 13 and 177 (a first showing with a similar package and pinout to the NEC proposal)) and Hewlett Packard (JX0007 at 013(a presentation on SDRAM features)).

Rambus's Response to Finding No. 516:

Rambus has no specific response.

517. At the first JEDEC JC-42.3 meeting on December 4-5, 1991 (the first JEDEC meeting attended by Rambus (see CCFF 867)), Mark Kellogg of IBM made a presentation comparing HST to synchronous DRAMs. (JX0010 at 5 and 84 ("Options: 1) high speed toggle (already passed ballot, on hold)"); Kellogg, Tr. 5172-5173).

Rambus's Response to Finding No. 517:

Rambus has no specific response.

518. Also at the JC-42.3 meeting of December 4-5, 1991, Howard Sussman presented the

results of a non-JEDEC meeting that had been held in Portland, Oregon on October 24, 1991 to discuss high bandwidth DRAM. (JX0010 at 4; Sussman, Tr. 1373). The conclusion from that meeting was that a fully synchronous DRAM with all signals referenced to a single positive clock edge would best meet system requirements. (JX0010 at 50).

Rambus's Response to Finding No. 518:

Rambus has no specific response.

519. At the next JC-42.3 meeting held on February 27-28, 1992 NEC, Hitachi, Fujitsu, Toshiba, Mitsubishi and Sun all made presentations proposing to use fully synchronous DRAMs. (JX0012 at 39, 42 (NEC presentation); JX0012 at 69 (Hitachi presentation); JX0012 at 76 (Fujitsu presentation); JX0012 at 94 (Toshiba presentation); JX0012 at 60 (Mitsubishi presentation); (JX0012 at 110 (Sun Presentation)).

Rambus's Response to Finding No. 519:

The proposed finding is misleading in suggesting that the companies listed were proposing to "use fully synchronous DRAMs" rather than other devices. There was no such "either/or" decision to be made. The listed companies made presentations regarding synchronous DRAM devices that they proposed to develop. They continued to also make presentations regarding asynchronous DRAMs that they proposed to develop as well. For example, at the February 1992 JC-42.3 meeting, Toshiba made two presentations regarding "address compression" for asynchronous DRAMs, Fujitsu made a presentation regarding an asynchronous DRAM in a new kind of packaging, and NEC made a presentation regarding an asynchronous DRAM with a "revolutionary pinout." (JX0012 at 10-11).

520. No further action on HST was taken at the February 1992 JC-42.3 meeting. High Speed Toggle items continued to be listed, however, on an active items list presented at the February 1992 meeting by the Subcommittee Chairman. (JX0012 at 19 ("Item 312.1 … Toggle Mode, Ballot 91-119, IBM"), 20 ("Item 358 . . . G\Toggle Mode, Siemens")).

Rambus's Response to Finding No. 520:

Rambus has no specific response.

521. At a DRAM Task Group meeting of April 9-10, 1992, NEC, Fujitsu, Toshiba, Samsung, Hitachi and Mitsubishi presented proposals for a fully synchronous DRAM. (CX0034 at 33 (NEC presentation; Fujitsu presentation), at 35 (Toshiba presentation; Samsung presentation; Hitachi presentation); at 36 (Mitsubishi presentation).

Rambus's Response to Finding No. 521:

Rambus has no specific response.

522. At the April 1992 DRAM Task Group meeting, IBM proposed a slightly modified version of its HST technology. (CX0034 at 32 ("IBM: … A Synchronous RAS/CAS with Synchronous DQ * dual clock edge…"); Kellogg, Tr. 5175).

Rambus's Response to Finding No. 522:

Complaint Counsel have altered the language used in the summary of the IBM presentation they cite in a way that changes the meaning of the presentation. The presentation does not say "A Synchronous RAS/CAS," but, rather "A-Synchronous RAS/CAS," meaning that the RAS and CAS signals are asynchronous." (Kellogg, Tr. 5175 (the presentation involved "asynchronous inputs for address and command"; Jacob, Tr. 5542-43 (the presentations stated "asynchronous RAS/CAS")).

523. Following the April 1992 DRAM Task Group meeting, the JC-42.3 subcommittee decided to pursue a fully synchronous DRAM rather than IBM's toggle mode. (G. Kelley, Tr. 2515).

Rambus's Response to Finding No. 523:

The proposed finding is misleading in suggesting that the JC-42.3 subcommitee could only choose to pursue synchronous DRAM or IBM's toggle mode. In fact, the JC-42.3 subcommittee continued to develop various asynchronous DRAMs while it was also standardizing synchronous DRAMs. (Rambus's Responses to Findings Nos. 507, 519). It is true that the JC-42.3 subcommittee decided to proceed with the standardization of a synchronous

DRAM. It is true that it decided not to proceed with the standardization of IBM's HST DRAM. It is *also* undisputed that, as an IBM researcher later wrote, the High speed Toggle DRAM was "very big" and "very hot" and "very nonstandard," which attributes were "disastrous" for it. (RX 2099-07 at 16).

524. Following the April 1992 DRAM Task Group meeting, the JC-42.3 Subcommittee decided to use a single edge rather than a dual edge clock (i.e., to input and output data only on the rising edge of the clock, rather than on both the rising and falling edges of the clock). (G. Kelley, Tr. 2515) The concept of using dual edge clocking "had generated quite a bit of interest." Rhoden, Tr. 462-63 (". . . actually we came very close to including it in the original SDRAM standard . . .).

Rambus's Response to Finding No. 524:

The proposed finding is not supported by the weight of the evidence. The evidence shows that there was some discussion of potentially using a dual-edge clock in synchronous DRAMs at an August 1991 *non*-JEDEC meeting that Rambus did not attend. (CX0020 at 1). By the time Rambus attended its first JEDEC meeting in December 1991, Howard Sussman was reporting the consensus that "A fully synchronous DRAM with *all signals referenced to a single (positive) clock edge* would best meet system requirements." (JX0010 at 50 (emphasis added)). The only evidence that of the purported consideration of "dual-edge clocking" that Complaint Counsel point to after this time is IBM's HST presentations; these presentations did *not* propose including dual-edge clocking in synchronous DRAMs, but, rather, proposed a different, asynchronous DRAM that would output data on both edges of a "toggle" signal. (*See* RRFF 509-10).

525. The subcommittee decided to postpone implementing dual edge clocking until a later standard in part because the subcommittee believed current requirements could be met with a single edged clock. (G. Kelley, Tr. 2515 ("At the meeting, we discussed the advantages of a double-edged clock versus a single-edged clock and we decided as a group that we could meet

the requirements of the high-performance systems for the next-generation DRAM without needing a double-edged clock for that doubling of the performance and that we would reconsider the double-edged feature in the next generation."); Rhoden, Tr. 463-464)

Rambus's Response to Finding No. 525:

The proposing finding is misleading in suggesting that dual-edged clocking was simply "postpone[d]" until a later standard, as though JEDEC members believed that it was a foregone conclusion that it would be included. To the contrary, when JEDEC distributed a survey ballot in late 1995 regarding possible features to include in the next generation synchronous DRAM standard, a majority of respondents voted *against* dual-edged clocking. (JX0028 at 45) (showing 9 votes against dual-edged clocking; only 7 in favor).

526. Another factor in the decision to postpone implementing dual edge clocking until a later standard was that a number of companies had difficulty perfecting the clock signal to permit using both the rising and the falling edges. (Prince, Tr. 9024; Kellogg, Tr. 5180; Sussman, Tr. 1371).

Rambus's Response to Finding No. 526:

The proposed finding is misleading in suggesting that dual-edged clocking was simply "postpone[d]" until a later standard, as though JEDEC members believed that it was a foregone conclusion that it would be included. *See* RRFF 525.

3. The Decision To Include Programmable CAS Latency and Burst Length.

527. At the JC-42.3 meeting of December 4-5, 1991, Howard Sussman of NEC presented the results of a separate meeting in Portland concluding that the latency of data to the clock and the burst length should be programmable. (JX0010 at 50 ("The latency of data to the clock should be programmable. Implied setup with WCBR equivalent") ("Burst sequence...and wrap length should be programmable")). At the same meeting, Texas Instruments made a second showing of its SDRAM proposal that also included programmable CAS latency and programmable burst length. (JX0010 at 56 ("FEATURES TO BE PROGRAMMED IN WCBR CYCLE: . . . WRAP LENGTH . . . DATA CLOCK LATENCY)); Rhoden, Tr. 419-420). Toshiba also made a second showing that included programmable CAS latency and burst length.

(JX0010 at 67; Rhoden, Tr. 424). Wrap length and burst length are the same thing. (Rhoden, Tr. 419-420; Williams, Tr. 812-813; Sussman, Tr. 1374-1375).

Rambus's Response to Finding No. 527:

The proposed finding is misleading in referring to the Texas Instruments' and Toshiba presentations as "second showing[s]," without more. In fact, the Texas Instruments' presentation was designated as a "revised presentation" rather than a "second showing." (JX0010 at 4). Moreover, neither of the "first showings" at the September 1991 included programmable CAS latency and programmable burst length. (JX007 at 163-77).

528. The JC-42.3 Subcommittee considered a number of alternative methods of determining the CAS latency and burst length, including using a fixed burst length, using pins to set the CAS latency and burst length, and using fuses to set CAS latency and burst length. (Rhoden, Tr. 425-434; Kellogg, Tr. 5099-5102 and 5130-5131).

Rambus's Response to Finding No. 528:

The proposed finding is incomplete. The alternative methods considered at JEDEC were quickly rejected. Indeed, there is no evidence that any even made it past the "first showing" stage. *See* RRFF 529-31.

529. At the December 1991 JC-42.3 meeting, Samsung presented a proposal for SDRAMs that included fixed CAS latency and burst length. Samsung proposed using a single CAS latency of 2 and a single burst length of 8. (JX0010 at 71; Rhoden, Tr. 425-28; Kellogg, Tr. 5099-5101).

Rambus's Response to Finding No. 529:

The proposed finding is incomplete. The Samsung presentation was a first showing (JX0010 at 5), and there is no evidence that it ever progressed beyond the first showing stage.

530. The Samsung proposal also included a fuse option to select between two different burst options. (JX0010 at 71; Rhoden, Tr. 427-428).

Rambus's Response to Finding No. 530:

The proposed finding is incomplete. The Samsung presentation was a first showing (JX0010 at 5), and there is no evidence that it ever progressed beyond the first showing stage.

531. At the December 1991 JC-42.3 meeting, Mitsubishi presented a proposal for an SDRAM that would use two pins, BT and WP, to set the burst length and burst type. (JX0010 at 74; Kellogg, Tr. 5102). In its proposal, Mitsubishi provided for two burst length options, a burst length of 4 and 8. (JX001 at 64; Rhoden, Tr. 430-34).

Rambus's Response to Finding No. 531:

The proposed finding is incomplete. The Mitsubishi presentation was designated as a "first time presentation." (JX0010 at 5). There is no evidence that it ever progressed beyond this stage.

532. At the December 1991 JC-42.3 meeting, Texas Instruments presented a proposal using the WCBR cycle to program the mode register to determine burst length and CAS latency. (JX0010 at 50 and 56). WCBR indicates a situation where the write signal is low and a CAS signal is sent before the RAS signal. While common in a test or refresh operation, CAS before RAS differs from a normal read or write operation where the RAS would be sent before the CAS. (Kellogg, Tr. 5107-5109).

Rambus's Response to Finding No. 532:

Rambus has no specific response.

533. WCBR was a cycle that had been used in fast page mode and EDO DRAMs to reflect a means by which a test mode could be entered and remain for some period of time. (Kellogg, Tr. 5106-5107).

Rambus's Response to Finding No. 533:

Rambus has no specific response.

534. The use of WCBR to program CAS latency and burst length appealed to JEDEC members because it was a familiar concept, was evolutionary and could easily be achieved. (Kellogg, Tr. At 5109-10 (Texas Instrument's proposal to use WCBR "had two key messages to me. One is that it indicated I could use an evolutionary concept. In other words, I could use something I was familiar with and I'd been using for some period of time. It also implied that

setting modes in a programmable method could be easily achieved."); Sussman, Tr, 1382-83 (WCBR "is the same test mode methodology, programmable, that we have had for years.")).

Rambus's Response to Finding No. 534:

The proposed finding is misleading in its suggestion that the "use of WCBR to program CAS latency and burst length . . . was a familiar concept." The testimony cited indicates only that the use of a WCBR cycle for the purpose of entering test mode was familiar, not that the use of that cycle to program CAS latency and burst length was familiar. To the contrary, Howard Kalter of IBM remarked that "programmable latency was the cleverest item Toshiba ever created." (RX0199 at 2).

535. At the JC-42.3 meeting of February 27-28, 1992 NEC, Hitachi, Fujitsu, Toshiba and Mitsubishi all made SDRAM proposals that included programmable CAS latency and burst length. (JX0012 at 39 (NEC: "FEATURE. . . Programmable wrap-length (2,4,8,16, Full Page) . . . Programmable RAS,CAS latency using WCBR+Address-key") and JX0012 at 42 (NEC: diagram indicating mode register programmability including programmability of CAS latency and burst length); JX0012 at 69 (Hitachi: "Programmable wrap length . . . . Programmable RAS, CAS latency") (Sussman, Tr. 1382-1383); JX0012 at 76 (Fujitsu: "Features: ... Programmable burst type and wrap length (4, 8, Full Column)"); JX0012 at 91 (Fujitsu: diagram indicating mode register programmability including programmability of CAS latency and burst length); JX0012 at 94 (Toshiba: "Basic Features of Synchronous DRAM: ... 3. Sequential column access with programmable wrap length . . . 6. Programmable latency"); JX0012 at 60 (Mitsubishi: "Target Specification of Synchronous DRAM: ... 2. *Programmable Wrap length 4 & 8 bit (Selectable by Address Key)").* At the same meeting, Sun presented comments on what features it would like to see included in SDRAMs, including programmable CAS latency and burst length. (JX0012 at 110 ("Synchronous DRAM requirements . . . WCBR programming (latency, wrap len, etc. . .").

Rambus's Response to Finding No. 535:

Rambus has no specific response.

536. At a DRAM Task Group meeting of April 9-10, 1992, NEC, Fujitsu, Toshiba, Samsung, Hitachi, Mitsubishi and IBM presented proposals that included programmable burst length. (CX0034 at 33 ("NEC: ... programmable Wrap 1,2,4,8, full page"); CX0034 at 33 ("Fujitsu: ... programmable wrap and burst of 1, 4,8, full page length); CX0034 at 35 ("Toshiba: ... programmable Wrap and burst of 4 and 8"); CX0034 at 35 ("Samsung: ... programmable

Wrap and burst of 4, 8 full page length"); CX0034 at 35 ("Hitachi: ... programmable Wrap and burst of 1,2,4,8, full page"); CX0034 at 36 ("Mitsubishi: ... programmable Wrap and burst of 4,8,16,32, full page"); CX0034 at 32 ("IBM: ... Programmable Wrap of 2,4 or 8 words").

Rambus's Response to Finding No. 536:

Rambus has no specific response.

537. At the next meeting of JC-42.3 on May 7, 1992, the minutes of the April DRAM Task Group meeting were presented to the full JC-42.3 subcommittee. (CX0034 at 4 and 30-37).

Rambus's Response to Finding No. 537:

Rambus has no specific response.

538. At the May 1992 meeting of the JC-42.3 Subcommittee, Samsung, NEC, Toshiba, Hitachi and Mitsubishi all made SDRAM presentations that included programmable CAS latency and burst length. (CX0034 at 44 (Samsung - Mode register field table showing programmability of CAS latency and burst length); CX0034 at 63 (NEC - Mode register table showing programmability of CAS latency and burst length); CX0034 at 83 (Toshiba - "Programmable Latency Clock Times . . . CAS Latency") and 85 (Diagram indicating mode register programmability including programmability of burst length and CAS latency); CX0034 at 99 (Hitachi - "1. Feature . . . *Programmable wrap length (1,2,4,8, Full Page). . . *Programmable RAS, CAS latency. . ."); CX0034 at 108 (Mitsubishi - Access latency table showing programmability of CAS latency and burst length); CX0034 at 140 (Fujitsu -Register programming table including programmability of CAS latency and burst length).

Rambus's Response to Finding No. 538:

Rambus has no specific response.

539. At the May 1992 JC-42.3 meeting, Cray gave a presentation that proposed the use of fuses to choose between two different CAS latencies, 2 and 3, and two burst lengths, full page and 8, for an SDRAM part. (CX0034 at 149 (proposing feature sets, which included CAS latency and Wrap Length, for two SDRAM configurations and stating, "[d]efault [s]et fuse programmable by supplier"); Sussman, Tr. 1388; Kellogg, Tr. 5103-5105). There were no other presentations of alternatives to programmable CAS latency and burst length at this meeting. (*See generally* CX0034).

Rambus's Response to Finding No. 539:

The proposed finding is misleading and incomplete. The referenced presentation by Cray

did not involve independent choices between two CAS latency values and two burst length values; rather, Cray was proposing to use a fuse to select between a set of features for a single bank configuration and a set of features for a dual bank configuration, where the feature set included, *inter alia*, the CAS latency value and burst length value. (CX0034 at 149.) This would not have yielded the flexibility of programmable CAS latency and programmable burst length because these values could not be adjusted independently of each other and numerous other features. Moreover, the Cray presentation was not even identified as a first showing in the minutes (CX0034 at 3-12), and there is no evidence that it ever progressed even to a first showing.

540. On June 11, 1992, four SDRAM ballots were sent out to all members. (CX0252A at 1). One ballot sought approval for use of a programmable mode register to set CAS latency and burst length. (CX0252A at 1 ("Item 376.3 "Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register" JC-42.3-92-85"); Crisp, Tr. 3075-3076; Rhoden, Tr. 448; Williams, Tr. 811-812; Sussman, Tr. 1390-1391).

Rambus's Response to Finding No. 540:

The proposed finding is misleading. The ballot sought approval of a particular implementation of a mode register which was used to program CAS latency and burst length, as well as other features. (CX0252A at 3).

541. Crisp voted (for technical reasons) against all four of the ballots, including the proposal for the mode register. (JX0013 at 9-11). The ballot required anyone aware of patents involving the ballot to alert the Subcommittee during their response. Committee Ballot, JC-42.3-92-85, item 376.3 (June 11, 1992) (Proposed Standard for 16M bit x 4 Sync DRAM Mode Register). At the time that the mode register ballot was being considered, Crisp never said anything with respect to potential Rambus patents relating to that ballot. (Crisp, Tr. 3087; Williams, Tr. 819-820).

Rambus's Response to Finding No. 541:

The proposed finding misrepresents the evidence. With regard to patents, the ballot

states: "If anyone receiving this ballot is aware of patents involving this ballot, please alert the Committee accordingly during your voting response." (CX0252A at 2). The ballot forms did not "require[]" patent disclosure. JEDEC committee members were told at the time the quoted language was added to the ballot form that it was added "for information only" and that the ballots were "not going to be checked to see who said what". (CX 3 at 6). (*See also* RPF 182-85). Moreover, the ballot forms did not require, or even mention, "potential" patents, that the proposed finding implies Rambus should have disclosed.

The proposed finding is also misleading because it suggests that there existed a Rambus patent or patent application for Mr. Crisp to disclose. In fact, Rambus had no issued patents at this time. Moreover, Complaint Counsel has stipulated that, prior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had *no* claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard. (Parties' First Set of Stipulations, No. 9.)

542. The results of the vote on the mode register ballot were presented at the next JC-42.3 meeting on July 21, 1992. (JX0013 at 9-12; Sussman, Tr. 1393). The initial tally showed 14 members in support of the proposal, 5 against and 7 abstentions. (JX0013 at 10). Various Subcommittee members offered comments, especially with respect to the need for a CAS latency of 4. (JX0013 at 10-11 ("-Hitachi: We don't like latency of 4 four. NEC agreed to review its need for the CAS latency of four cycles. There was a lot of discussion about this. Some felt it should be made optional."). Finally, it was agreed to re-ballot the mode register proposal with an optional latency mode of four. (JX0013 at 11).

Rambus's Response to Finding No. 542:

Rambus has no specific response.

543. At the September 16-17, 1992 JC-42.3 meeting Sun made an SDRAM presentation that included programmable CAS latency and burst length. (CX0042 at 39-40 (Mode register

table showing programmability of CAS latency; "Programmable Options: Several programmable options are associated with read and write accesses, as specified in the Mode Register. ... Wrap Length. Wrap length specifies the length of the burst for a read or write cycle")).

Rambus's Response to Finding No. 543:

Rambus has no specific response.

544. On January 21, 1993, the DRAM Task Group made minor technical edits to the NEC mode register that included programmable CAS latency and burst length and had previously been balloted as "Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register" JC-42.3-92-85 (item 376.3). The DRAM Task Group decided that a re-ballot was not necessary and added the ballot to the pass-hold category. (CX0047 at 3 ("This ballot had been passed but was shown as up for re-ballot. The ballot will not be reissued but will be editorially changed.").

Rambus's Response to Finding No. 544:

Rambus has no specific response.

4. Other Technologies Considered In Connection With JEDEC Work on the SDRAM Standard.

(A) Low Voltage Swing Signaling.

545. During 1992 Jedec work included a number of presentations that included low voltage swing signaling. At the February 27, 1992, JC 42.3 meeting, NEC, Fujitsu, Mosaid, Sun and Intel all made proposals that included low-voltage swing signaling. (JX0012 at 39, 76, 104, 111, 113; Crisp, Tr. 3045-46). At this same meeting, the JC-42.3 Committee discussed GTL technology for use with SDRAM. (JX0012 at 36, 56-58, 60, 101-02, 104, 111).

Rambus's Response to Finding No. 545:

The proposed finding is irrelevant. Complaint Counsel's apparent purpose in seeking findings relating to low voltage swing signaling is to argue that Rambus should have disclosed intellectual property relating to this technology to JEDEC. (*See* CCFF 3121-36.)

However, there is no evidence that any of the low voltage swing signaling presentations that Complaint Counsel cite were incorporated into the SDRAM standard, *or, indeed, ever even balloted for inclusion*. Complaint Counsel assert that JEDEC included low swing signaling

technology in SDRAM (CCFF 564, 3135), but the assertion is not supported by the evidence cited. The only cite offered by Complaint Counsel that relates to SDRAM (CX0234 at 116) states: "Electrical interface – TTL or lower level interface consistent with the value of VDD chosen." This offers no support for the proposition for which it is cited.

Moreover, Complaint Counsel have introduced no evidence whatsoever to show that Rambus ever had any patents or patent applications with claims covering any of the presentations they cite in this or the next three proposed findings. The only patent filing that Complaint Counsel cite with respect to low voltage swing signaling is a preliminary amendment that was filed in application serial no. 847,532. (CCFF 3126 (citing to Crisp testimony concerning this preliminary amendment); see also Crisp, Tr. 3032-33 (referencing claim 151 of '532 application); CX3102). Claim 151 of the preliminary amendment in question reads:

> "A complementary metal oxide semiconductor (CMOS) dynamic random access memory (DRAM) coupled to a multiline bus, wherein a first line of the multiline bus is a terminated transmission line, the CMOS DRAM comprising:
>
> (A) a CMOS memory array;
>
> (B) a bus line driver for producing a low voltage swing signal on the first line of the multiline bus, wherein the low voltage swing signal swings between an upper voltage and a lower voltage, wherein the difference between the upper voltage and the lower voltage is less than one volt, wherein the bus line driver comprises an N channel metal oxide semiconductor (NMOS) transistor having a first end, a second end, and a gate, wherein the first end of the NMOS transistor is coupled to ground, wherein the second end of the NMOS transistor is coupled to

the first line of the multiline bus, wherein the first line of the multiline bus has a more positive voltage then ground, and wherein the gate is coupled to the CMOS memory array."

(CX3102 at 171-72).

Complaint Counsel have introduced no evidence that *any* of the numerous limitations of this claim were satisfied by *any* of the presentations that they cite. Indeed, even with respect to the "low voltage swing" limitation, there is a failure of proof. As claim 151 demonstrates, "low voltage swing" is a vague and relative term. In claim 151, it is defined for purposes of the claim as swings of less than one volt. Complaint Counsel have introduced no evidence relating to the magnitude of the swings involved in the presentations that they cite.

In the absence of any evidence that Rambus had any pending claims relating to low voltage swing presentations at JEDEC, there can be no relevance to findings about those presentations.

546. At the April 8, 1992, Special SDRAM Task Group meeting, the JC 42.3 Subcommittee considered SDRAM proposals that included low voltage swing signaling. (CX0034 at 32 (IBM), 33 (NEC, Fujitsu), 35 (Samsung, Hitachi), 36 (Mitsubishi).

Rambus's Response to Finding No. 546:

The proposed finding is irrelevant. (*See* RRFF 545).

547. At the May 7, 1992, JC 42.3 meeting, the Subcommittee considered SDRAM proposals that included low voltage swing signaling. (CX0034 at 59 (NEC), 122-123 (Fujitsu)).

Rambus's Response to Finding No. 547:

The proposed finding is irrelevant. (*See* RRFF 545).

548. At the September 16-17, 1992, JC 42.3 meeting, the Subcommittee considered Sun's 15 meg SDRAM specification which included low voltage swing signaling (CX0042 at

31) ("It is proposed that LVTTL be used for I/O drivers and receivers.")).

Rambus's Response to Finding No. 548:

The proposed finding is irrelevant. (*See* RRFF 545).

(B) Dual Bank Design.

549. During 1992 and 1993 Jedec work included a number of presentations that included dual bank design. At the February 1992 JC 42.3 meeting, the Subcommittee addressed the topic of multiple active subarrays in two presentations (JX0012 at 34, 37) and multibank or dual bank design in other presentations (*See, e.g., id.* at 60). The Subcommittee considered proposals for multibank, or dual bank, design from NEC, Mitsubishi, Fujitsu, and Sun. (JX0012 at 39, 60, 76, 110).

Rambus's Response to Finding No. 549:

The proposed finding is irrelevant. Complaint Counsel's apparent purpose in seeking findings relating to dual bank design is to argue that Rambus should have disclosed intellectual property relating to this technology to JEDEC. (*See* CCFF 3138-50.) However, Complaint Counsel have introduced no evidence whatsoever to show that Rambus ever had any patents or patent applications with claims covering a. dual bank design. Indeed, Complaint Counsel agree that in June 1993 Lester Vincent expressed doubt that a claim broad enough to cover dual bank design "can extract this claim from the teachings of [Rambus's '898 application]." (CX0702; CCFF 3145). Mr. Vincent's notes of a July 1993 meeting with Richard Crisp and Fred Ware of Rambus indicate that that claim was "dead." (CX1963 at 4 (notes regarding potential claims referenced by numbers in an earlier list at CX0702)).

There is no evidence that Rambus ever filed or obtained claims to dual bank designs after the notion of filing such claims had been pronounced "dead" by Mr. Vincent in 1993. The only pending claim that Complaint Counsel assert relates to dual bank designs is claim 182 in a

Preliminary Amendment to application serial no. 08/222,646. (CCFF 3148; CX1466 at 12). Claim 182 states:

> "A dynamic random access memory (DRAM) wherein the DRAM is addressable over a range of addresses, the DRAM comprising:
>
> a plurality of independently addressable memory sections, wherein each of the independent memory sections is assigned a portion of the range of addresses, each of the memory sections comprising:
>
> an array of memory cells connected in rows and columns; and a plurality of sense amps, each sense amp being coupled to a column of the array of memory cells; each sense amp for sensing data stored in a selected memory cell;
>
> a plurality of address registers coupled to the plurality of memory sections, each address register for storing information indicating a portion of the range of addresses that corresponds to a memory section, wherein the plurality of address registers are independently addresssed to access data stored in corresponding memory sections, and wherein the DRAM is formed on a single semiconductor substrate."

(CX1466 at 12). Complaint Counsel quote the reference to "a plurality of independently addressable memory sections" while ignoring the rest of this length claim. (CCFF 3148). In particular, the claim requires the key feature that each such section be associated with an "address register for storing information indicating a portion of the range of addresses that corresponds to a memory section." The benefits of such address registers are explained at length in the '898 application. (CX1451 at 16-17). There is no evidence that SDRAMs contain any

such address registers. In the absence of any evidence that Rambus had any pending claims relating to dual bank design, there can be no relevance to findings about presentations relating to dual bank design.

550. At the May 7, 1992, JC 42.3 meeting, the Subcommittee considered SDRAM proposals that included dual bank design. (CX0034 at 59 (NEC), 122-123 (Fujitsu)). During that meeting, Mr. Kelley of IBM, prompted by Mr. Meyer of Siemens, asked Mr. Crisp whether Rambus might have patent claims that related to dual bank design. (CX2089 at 130, 131, 136-137 (Meyer, Infineon Trial Tr.). Mr. Crisp gave no verbal response, but rather shook his head. Mr. Kelley then commented to the group that "they don't have anything to say about that." (*Id.*).

Rambus's Response to Finding No. 550:

The proposed finding that the JC-42.3 subcommittee considered proposals including dual bank design is irrelevant. (*See* RRFF 549). The rest of the proposed finding is incorrect, misleading and not supported by the evidence. The proposing finding alters the question that Mr. Kelley asked Mr. Crisp to make it appear that, by shaking his head, Mr. Crisp was denying that Rambus might have relevant patent claims. To the contrary, as Mr. Meyer makes clear in the very testimony cited by Complaint Counsel: "The way how Mr. Kelley formulated the question was: Do you want to give a comment on this?" (CX2089, Meyer Infineon Trial Tr., at 136). Thus, Mr. Meyer's testimony that Mr. Crisp shook his head in response shows that Mr. Crisp was declining to comment on Rambus's patent position.

Complaint Counsel's description of the May 1992 exchange between Mr. Kelley and Mr. Crisp is especially misleading since every witness who testified about the exchange, and every contemporaneous document that describes it, states that Crisp had declined to comment about Rambus's intellectual property. (*See, e.g.*, RX 290 at 3 – notes of 5/92 meeting taken by IBM's Mark Kellogg say "Siemens: kernel of chip similar to Rambus. Patent concerns? (No

Rambus comments)". This evidence is set out in more detail at RPF 493-511.

551. At the September 16-17, 1992, JC 42.3 meeting, the Subcommittee considered Sun's 15 meg SDRAM specification which included a dual bank design (CX0042 at 30) ("The 4M x 4 device is organized internally as two banks.").

Rambus's Response to Finding No. 551:

The proposed finding is irrelevant. (*See* RRFF 549).

(C) Auto-Precharge.

552. At a number of meetings during the course of 1992, the JC-42.3 Subcommittee discussed using the auto-precharge technology in the SDRAM standard. (February 1992: JX0012 at 37, 39 (NEC), 76 (Fujitsu), 94 (Toshiba), 108 (Sun); April 1992: CX0034 at 32 (IBM), 33 (NEC), 35 (Hitachi); May 1992: CX0034 at 6, 150).

Rambus's Response to Finding No. 552:

The proposed finding is irrelevant. Complaint Counsel's apparent purpose in seeking findings relating to auto-precharge is to argue that Rambus should have disclosed intellectual property relating to this technology to JEDEC. (*See* CCFF 3152-60.) However, the only patent claim that Complaint Counsel raise as purportedly related to auto-precharge is claim 193 which was briefly pending in application serial no. 08/222/646. (CCFF 3159). In fact, claim 193 was filed on September 6, 1994 and withdrawn from further consideration at Rambus's election as of January 24, 1995. (CX1466 at 15, 19; CX1493 at 197, 201, 212, 214). Thus, claim 193 was only pending for a few months, over two years after the presentations cited by Complaint Counsel.

553. At the September 16-17, 1992, JC-42.3 meeting, the Subcommittee considered Sun's 15 meg SDRAM specification which included an "autoprecharge" option CX0042 at 45). Auto-precharge was incorporated as a feature in the JEDEC SDRAM 21-C standard, issued in November 1993. (JX0056 at 115).

Rambus's Response to Finding No. 553:

The proposed finding is irrelevant. (*See* RRFF 552).

(D) Source Synchronous Clocking.

554. At the April 1992 JC-42.3 Special Task Group meeting, the DRAM Task Group discussed the issue of source synchronous clocking. CX1708 at 2 ("Hitachi brought up the issue of source synchronous clocking."); Crisp, Tr. 3053-54 (recalling that a discussion on source synchronous clocking had taken place at this meeting)).

Rambus's Response to Finding No. 554:

The proposed finding is irrelevant. Complaint Counsel's apparent purpose in seeking findings relating to source synchronous clocking is to argue that Rambus should have disclosed intellectual property relating to this technology to JEDEC. (*See* CCFF 3175-80.) Even if the fact that a JEDEC member "brought up [an] issue" at a task group meeting were enough to trigger a disclosure obligation (there is no evidence to support such a duty), Complaint Counsel have introduced no Rambus patents or patent applications with claims that they allege cover an externally supplied reference voltage.

(E) Externally Supplied Reference Voltage.

555. At the February 27, 1992, JC 42.3 meeting, Samsung proposed an externally supplied reference voltage. (JX0012 at 58; Crisp, Tr. 3043, acknowledging that "vref" refers to externally supplied reference voltage).

Rambus's Response to Finding No. 555:

The proposed finding is irrelevant. Complaint Counsel's apparent purpose in seeking findings relating to externally supplied reference voltage is to argue that Rambus should have disclosed intellectual property relating to this technology to JEDEC. (*See* CCFF 3163-73.) There is no evidence, however, that the presentations relating to an externally supplied reference

voltage that Complaint Counsel cite were ever incorporated into the SDRAM standard or even balloted for inclusion. An externally supplied reference voltage is not part of the SDRAM standard; indeed, Terry Lee testified that even in some SDRAM configurations where an externally supplied reference was included as an option, it was not actually used. (Lee, Tr. 11035). In addition, Complaint Counsel have introduced no Rambus patents or patent applications with claims that they allege cover an externally supplied reference voltage.

556. At the May 1994 JC-42.3 Subcommittee meeting, Mr. Crisp observed various presentations regarding specific SDRAM configurations. Mr. Crisp wrote in an e-mail to Mark Johnson, an attorney for Rambus, "Note that many of the SDRAMs use an externally supplied reference voltage in the input buffers. I believe we have a claim we added to cover this configuration. We should make note of this." (CX0711 at 26, 27). Later in the same May 1994 meeting, Mr. Crisp noted, "(again we need to check claims about 'DRAM with input receivers using an externally supplied reference voltage'). We may be able to slow down or stop (or at least collect from) all of the CTT, GTL and HSTL devices if this claim is allowed (Allen, I believe this was one of the claims you, Lester, Tracy and I wrote up in late '91, right?)." (CX0711 at 26, 31).

Rambus's Response to Finding No. 556:

The proposed finding is irrelevant. (*See* RRFF 555). The proposed finding is also incorrect in identifying Mark Johnson as a Rambus attorney. Mark Johnson was a Rambus engineer. (Diepenbrock, Tr. 6165).

557. On March 14, 1995, Fujitsu gave a presentation on "STBUS" signaling technology to the JC-16 Subcommittee. (CX0711 at 53, 54; *see also* CX0082 at 13). In an e-mail to Rambus executives and others, Mr. Crisp stated that Rambus had claims that anticipated Fujitsu's STBUS proposal because it was a proposal for a current source device that relied on an externally supplied reference voltage. (CX0711 at 53, 54 ("Taken along with the fact that they rely on an externally bussed reference (this should be anticipated by some of our claims), I would say that this proposal may well infringe our work.")).

Rambus's Response to Finding No. 557:

The proposed finding is irrelevant. *See* RRFF 555.

5. Adoption of the SDRAM Standard.

558. At the JC-42.3 meeting on March 3-4, 1993, the subcommittee voted unanimously to send 14 SDRAM ballots to Council to become approved as a comprehensive standard for SDRAMs intended for publication as Release 4 of the 21-C standard. JX0015 at 14 ("VLSI moved to send all pass/hold ballots on to Council. Seconded by TI. The vote was: 26 yes, 0 no. Motion passed."). The ballots were in fact sent to Council after the vote. (G. Kelley, Tr. 2554-2555; JX0016 at 5).

Rambus's Response to Finding No. 558:

The proposed finding is misleading in referring to the SDRAM ballots as providing for a "comprehensive" standard. In fact, the JEDEC SDRAM standard was not sufficiently comprehensive to ensure interoperability and led to incompatibility between SDRAMs from different manufacturers. (RPF 1518). This prompted Intel to develop it own specification to ensure interoperability. (RPF 1519-23).

559. The subcommittee agreed to issue a press release stating that the Sync DRAM standard has been approved by subcommittee. (JX0015 at 14; G. Kelley, Tr. 2555). A copy of the release was attached to the minutes of the March meeting. (JX0015 at 99) ("Press Release … At the March 4 meeting here the EIA/ JEDEC JC-42.3 Subcommittee on Memory unanimously approved 14 Synchronous DRAM ballots. These will be submitted to the JEDEC Council for their approval before publishing as a JEDEC standard. … the following list of ballots [are included] … 4 16M/18M SDRAM Mode Register Bit Definitions."). Among the features included in this standard was programmable CAS latency and burst length. (JX0056 at 114).

Rambus's Response to Finding No. 559:

Rambus has no specific response.

560. At the JC-42.3 meeting on May 19-20, 1993, Gordon Kelley of IBM reported to the full JC-42.3 subcommittee that the SDRAM ballots had gone to Council and that all council members apart from AT&T had supported the ballots. He attached to the minutes a letter responding to ATT's concern by proposing additions to the Mode Register. (JX0016 at 5 and 36-37(IBM) (table showing programmability of mode register including programmable CAS latency and burst length). Kelley also distributed copies of the ballots to the subcommittee. (JX0016 at 5; G. Kelley, Tr. 2557-2558).

Rambus's Response to Finding No. 560:

Rambus has no specific response.

561. On May 24, 1993 the JEDEC Council formally approved adoption of the comprehensive standard in Release 4 of the 21-C standard. (CX0054 at 8-10; G. Kelley, Tr. 2559-2560).

Rambus's Response to Finding No. 561:

The proposed finding is misleading in referring to the SDRAM ballots as providing for a "comprehensive" standard. (RRFF 558).

562. In November, 1993 JEDEC published the SDRAM standard as JEDEC Standard No. 21-C Release 4 (JX0056; Williams, Tr. 801). The standard included a programmable mode register that includes programmable CAS latency and burst length. (JX0056 at 114 (mode register table showing programmability of three elements, including latency mode and burst length); Rhoden, Tr. 456-458; Williams, Tr. 801-03; Sussman, Tr. 1399-1400).

Rambus's Response to Finding No. 562:

Rambus has no specific response.

563. For a manufacturer to produce JEDEC-compliant SDRAMs, the standard requires the manufacturer to design and produce SDRAMs with programmable CAS latency and burst length on a mode register. (Sussman, Tr. 1399-1401; see CCFF 25-28 and 114-116 discussing need for compatibility and interoperability).

Rambus's Response to Finding No. 563:

Rambus has no specific response.

564. The SDRAM and DDR SDRAM standards include low swing signaling (CX0234 at 116, 189-195), dual bank (CX0234 at 116, 145), source synchronous clocking (CX0234 at 164; Lee, Tr. 6682) and auto-precharge (CX0234 at 145, 151) features, and allows optional use of an externally supplied reference voltage (CX0234 at 84 (pin 40), 85 (pin 40), 86 (pin 49) and 87 (pin 49).

Rambus's Response to Finding No. 564:

The proposed finding is irrelevant, vague and misleading. Complaint Counsel's apparent

purpose in seeking findings regarding these technologies is to argue that Rambus should have disclosed related intellectual property to JEDEC. (*See generally* CCFF 3121-74). Complaint Counsel has not, however, even attempted to make a showing that Rambus *had* any relevant intellectual property to disclose. (*See generally* RRFF 545-57). The finding simply lists various vague terms that could each apply to a host of different technologies, all of which are irrelevant absent some showing, that has not been made, that Rambus had claims directed to the specific technology incorporated in JEDEC standards.

The finding is also simply incorrect and not supported by the evidence cited in certain respects. For example, the SDRAM standard did not include any of the various forms of low swing signaling. The cited page of the SDRAM standard states simply: "Electrical interface – TTL or lower level interface consistent with the value of VDD chosen." This indicates, at most, that SDRAMs could be manufactured with a variety of different forms of electrical interfaces, some with lower voltage swings and some with higher, and still comply with the standard. Likewise, there is no evidence that SDRAM included any form of source synchronous timing; the cited evidence does not relate to SDRAM but to the data strobe in DDR SDRAM.

6. Subsequent JEDEC Work Relating to the SDRAM Standard.

565. Work continued in the JC-42.3 subcommittee after the publication of the SDRAM standard in November, 1993. That work included improvements to the SDRAM standard and work on future generation of devices. (Rhoden, Tr. 460 ("Q. Now, what standard-setting work, if any, did the JC-42.3 subcommittee do between May of 1993 and June of 1996? A. Oh, a tremendous amount. The work -- inside JEDEC, there is a continuous time line of activity. Work -- it's -- while there are snapshots and we do collect groups of ballots at times, the work is continuous. We're always working on the improvements to what we have, improvements to what we've seen before and future generation of devices. So, that's three things we're always working on.").

Rambus's Response to Finding No. 565:

The proposed finding is misleading to the extent that it suggests that consideration of the DDR SDRAM began prior to December 1996. Complaint Counsel rely on the testimony of Desi Rhoden for this proposed finding, but Mr. Rhoden's testimony in this regard is not reliable. A March 9, 1998 e-mail from Mr. Rhoden recapping the DDR SDRAM standardization effort states in part:

> "[W]e could have finished the DDR standard sooner if only we had started earlier. Let us recap what has transpired with DDR:
>
> 1. A lot of private and independent work *outside of JEDEC* for most of 1996 (here is where we missed a good opportunity to start early).
>
> 2. December 96 – A single overview presentation of a DDR proposal at a JC 42 meeting."

(CX0375 at 1 (emphasis added)). Thus, Mr. Rhoden's e-mail makes clear that, although there was some work earlier in 1996 outside of JEDEC, JEDEC's consideration of DDR SDRAM did not begin until December 1996. The weight of the evidence is in accord with the timeline described in Mr. Rhoden's March 1998 e-mail. *See* RPF 399-413.

566. SDRAMs were not immediately adopted by the marketplace and as late as 1995 asynchronous DRAMs continued to make up approximately 97% of the market with Fast Page Mode approximating 87.2% and EDO's 9.9% of the market. (Rapp, Tr. 10248).

Rambus's Response to Finding No. 566:

The proposed finding is not supported by the evidence cited. Mr. Rapp did testify that Fast Page Mode and EDO accounted for, approximately, 87.2% and 9.9% of the DRAM market

by revenue in 1995; he did not, however, testify that this was the result of not being "immediately adopted by the marketplace," as opposed to other possible factors, such as availability.

567. JEDEC members noted that SDRAMs were not being produced due to their overhead and yield issues. (JX0027 at 12 ("NEC noted that the amount of overhead for the JEDEC SDRAM made it unusable so it was not produced. Yield was the major issue also. Presently SDRAMs are being made, but a clear market is not there yet.") and 13 ("It was noted that as compared to EDO, SDRAM is harder to make and the yields are lower.").

Rambus's Response to Finding No. 567:

Rambus has no specific response.

568. JC-42.3 members showed a continued interest in asynchronous DRAMs and at the January 5, 1995 JC-42.3 meeting, Micron made a presentation of an asynchronous DRAM called Burst EDO that was based upon a page mode DRAM. (JX0023 at 69-79; Williams, Tr. 821 and 825-826).

Rambus's Response to Finding No. 568:

Rambus has no specific response.

569. Brett Williams of Micron testified that Burst EDO lost support, however, and was abandoned due to momentum behind SDRAM. (Williams, Tr. 829). He further testified that if Burst EDO had been adopted more work would have been done on it to improve its performance. (Williams, Tr. 829-830; see Jacob, Tr. 5395-5396 (discussing advantages of continuing to develop asynchronous over synchronous memory.).

Rambus's Response to Finding No. 569:

The proposed finding is misleading and incomplete. Although Burst EDO was standardized by JEDEC (Williams, Tr. 873, 879-80; RX 585 at 1), it failed in the marketplace in competition with SDRAM. (Williams, Tr. 829; CX2108, Oh Depo., at 236 ("[T]his is enhanced version of EDO, and we wanted to convince our customers the advantages of this part, but was not accepted by our customers.")). It was generally understood in the 1990s that asynchronous memories, such as Burst EDO, were not capable of reaching the speeds that would be required

for future DRAMs. (RPF 897-901). Indeed, even Micron admitted that Burst EDO would most likely be limited to speeds of 100 MHz and below. (RRFF 2231). The vague testimony of Mr. Williams, one of the proponents of Burst EDO, that Burst EDO might have been improved, without offering any specific suggestions, is not supported by the weight of the evidence. (RRFF 2233).

570. Other JEDEC members made proposals aimed at reducing the costs of SDRAMs. At the March 15, 1995, JC-42.3 meeting, TI proposed reducing test cost by making CAS latency of 1 optional. The proposal included a mode register with programmable CAS latency and burst length. (JX0025 at 107 (Mode register table showing programmability of CAS latency and burst length)).

Rambus's Response to Finding No. 570:

The proposed finding is misleading in stating that the TI proposal included a mode register with programmable CAS latency and burst length. Other than making the CAS latency value of 1 optional rather than required, the TI proposal simply retained the then-current features of SDRAM, including a mode register with programmable CAS latency and burst length. (JX0025 at 14, 107).

571. At the May 24, 1995, JC-42.3 meeting, TI made a second showing of its proposal to make CAS latency of 1 optional. (JX0026 at 9). The proposal continued to include a mode register with programmable CAS latency and burst length. (JX0026 at 62 (SDRAM mode register table showing programmable CAS latency and burst length)). A motion to ballot the TI proposal was unanimously accepted. (JX0026 at 9). Crisp sent an e-mail from the meeting stating that "TI would prefer to eliminate the requirement for supporting CAS latency = 1 to reduce cost of speed testing by removing some testing permutations." (CX0711 at 70).

Rambus's Response to Finding No. 571:

The proposed finding is misleading in stating that the TI proposal continued to include a mode register with programmable CAS latency and burst length, when it simply retained those features from the then-current SDRAM standard. (*See* RRFF 570).

572. At the September 11, 1995, JC-42.3 meeting, NEC made an SDRAM Lite presentation that proposed an SDRAM with a reduced feature set aimed at saving costs. (Rhoden, Tr. 475-6; Lee, Tr. 6625-27). That proposal suggested using a fixed CAS latency of 3 and a single fixed burst length. (JX0027 at 13, 66; Lee, Tr. 6626, 6629-30, 6632, 11,017; Sussman, Tr. 1416-17).

Rambus's Response to Finding No. 572:

The proposed finding is not supported by the weight of the evidence. The NEC SDRAM lite presentation did not include a single fixed burst length, but rather two burst lengths of 1 and 4. While the feature set in the NEC presentation cited by Complaint Counsel (JX0027 at 66) is completely illegible, a slightly better version of the same presentation makes clear that both burst lengths of 1 and 4 have check marks beside them. (CX0091A at 33). Moreover, the minutes of the meeting at which the presentation was made confirm that NEC wanted to retain burst lengths of both 1 and 4 in SDRAM lite. (JX0027 at 13 ("Need burst of 1 . . . NEC . . . 10) Burst of 4: . . . NEC . . . ."). The SDRAM lite proposal was ultimately rejected. (Sussman, Tr. 1416-17).

573. There was initial support for SDRAM Lite at the meeting with 23 members voting that an SDRAM Lite standard was needed and 4 voting against. (JX0027 at 12). It was agreed at the meeting that Desi Rhoden would prepare a survey ballot that JEDEC would issue. (JX0027 at 14).

Rambus's Response to Finding No. 573:

The proposed finding is misleading to the extent that it suggests support for any particular SDRAM lite feature set. The vote cited, under the heading "SDRAM Lite Features Task Group," was, as Complaint Counsel also note, a vote that an "SDRAM standard was needed," with the features of that standard yet to be determined. (JX0027 at 12).

574. At the JC-42.3 meeting on December 6, 1995, SDRAM Lite was further discussed. (JX0028 at 6; CX0711 at 191-92 (Crisp e-mail (12/6/95)).

Rambus's Response to Finding No. 574:

The proposed finding is incomplete. The discussion of SDRAM Lite at the December 1995 meeting indicated that "PC users" would not be satisfied with a single CAS latency of 3. (CX0711 at 191).

575. On January 31, 1996, there was an interim meeting of JC-42.3 where results of the SDRAM Lite survey ballot were discussed. Included in the discussion was having fixed CAS latency and burst length. (JX0029 at 13, 14 ("Survey Ballot Results . . . Does your company want to include CAS latency of 2 in the reduced specification? . . . Does your company want to include Burst Length of 1 in the reduced specification?. . . "); Lee, Tr. 6630, 6632, 11018-11019). The survey ballot also asked members if they wanted to include auto-precharge in the reduced specification. (JX0029 at 15).

Rambus's Response to Finding No. 575:

The proposed finding is incomplete. The results of the survey ballot indicate that more respondents wanted to retain multiple CAS latency and burst length values than not. (JX0029 at 13).

576. According to Terry Lee of Micron, the SDRAM Lite proposal lost support and was abandoned because it was recognized that the cost adder in the full SDRAM technology was not as great as initially thought and because members were frustrated at the length of time it was taking to get a standard. (Lee, Tr. 6634-6635).

Rambus's Response to Finding No. 576:

Rambus has no specific response.

577. SDRAMs began selling in volume in 1997, accounting for 33.5% of the DRAMs sold, and became the dominant product in the market in 1998, accounting for 60.8% of DRAMs sold. By that stage full page mode DRAMs had declined to 8.8% and EDO to 27.6% of DRAMs sold. (Rapp, Tr. 10248-10249).

Rambus's Response to Finding No. 577:

The proposed finding is misleading and incomplete. Although SDRAM represented a relatively small percentage of the DRAM market in 1996, it was certainly "volume" production.

(Rapp, Tr. 10248 (SDRAM was 4.3% of the DRAM market by revenue in 1996). Mr. Rapp testified that the figures cited in the proposed finding were the DRAM market shares measured by revenue.

B. The Next Generation SDRAM (DDR SDRAM).

1. The Beginnings of Work on the Standard.

578. JEDEC work on the next generation SDRAM that would eventually be named DDR SDRAM began with consideration of IBM's HST proposals in the late 1980's and early 1990's. (G. Kelley, Tr. 2584-2585 ("Q. Mr. Kelley, based on your recollection and your participation within JEDEC, what is your understanding of when JEDEC began work on the standard that became the JEDEC DDR SDRAM standard? A. In my mind, the consideration of using a double-edged clock actually began when I made the first presentation in 1988 and IBM reproposed in 1990 and 1991 and several other companies picked up in that -- on that concept in 1991. I think we had five companies showing what they called their own toggle mode in their presentations on the consideration of the first-generation synchronous DRAM. So in my mind, the consideration of the dual-edge clock began in 1988 and was essentially tabled because it was felt by the committee that it was not needed for the first generation part and that we would pick up the idea for consideration of the second generation part, which is now called DDR SDRAM."); Sussman, Tr. 1427- 1428).

Rambus's Response to Finding No. 578:

The proposed finding is not supported by the weight of the evidence, which makes clear that JEDEC consideration of the DDR SDRAM standard began in December 1996. (RPF 399-413).

In particular, the proposed finding that IBM's HST proposals constituted DDR SDRAM standard setting work is not supported by the weight of the evidence. The HST proposal was for an asynchronous DRAM, not a synchronous DRAM. (RRFF 509). In the HST proposal, data was transferred on both edges of a toggle signal, rather than on the edges of a free running clock. (RRFF 510). It is also worth noting that although IBM held patents on HST (Kelley, Tr. 2715), there is no evidence that they disclosed them in connection with DDR SDRAM. If, as Complaint

Counsel elsewhere assert, Mr. Kelley's practice was to inform the committee of IBM patents related to the work of the committee (see CCFF 338, then his failure to do so here shows that he did not believe the (asynchronous) HST device was related to the DDR device that was eventually standardized by JEDEC.

579. After the publication of the first generation SDRAM standard in November 1993, JEDEC worked both on implementations of and improvements on the SDRAM standard, including pin-out diagrams for specific SDRAM configurations, and on the standard for the next generation SDRAM. (Rhoden, Tr. 460-61 ("Q: Now, what standard-setting work, if any, did the JC-42.3 subcommittee do between May of 1993 and June of 1996? A: Oh, a tremendous amount. . . . We're always working on the improvements to what we have, improvements to what we've seen before and future generation of devices. . . . Q: Now, with respect to the SDRAM standard, what would future generation devices refer to? A: Well, we call[ed] them future generation DRAM –SDRAM . . .. Sometimes it was referred to as SDRAM II, sometimes it was just future DRAM. . . . Q: What standard did [that work] lead to? A: Well, the next generation standard would have been the DDR standard that actually came out later."); G. Kelley, Tr. 2566-67 ("Q: . . . After adoption of the series of SDRAM ballots, what did the JC-42.3 subcommittee do next? A: I believe that the next item that we pursued was the next generation of synchronous DRAM. Q: What do you mean by 'the next generation of synchronous DRAM? A: The one that we had just approved was the first synchronous DRAM in our JEDEC standards and we had already discussed at the early discussion of the synchronous DRAM that we would probably need to take some of the ideas of that first discussion and generate a second generation. We were now beginning that process."); Sussman, Tr. 1402 ("Q: . . . What did the JC-42.3 committee do next [after it completed work on the SDRAM standard]? A: Start on the next evolutionary part."); Williams, Tr. 820 ("Q: . . . after JEDEC published [the SDRAM standard], what work did it move on to next? A: It took up several different options, mainly looking at the next standard, the next generation of memory."); *see also* CX0700 at 2 (Crisp e-mail from the May 19-20, 1993 JC-42.3 meeting: "Apple . . . is saying that the committee is rushing ahead to get a next generation standard before finding out the problems with the first generation standard."); CX0711 at 52, 54 (Crisp e-mail of March 1995 quoting Hans Wiggers as saying that JEDEC had been working for over two years to standardize a high-speed interface and has not yet reached consensus); MacWilliams, Tr. 4815 (". . . we first heard about DDR in '95 when we went out to ask for options, which was one of the options we considered, the higher-speed SDRAM. One of the options was DDR.")).

Rambus's Response to Finding No. 579:

The proposed finding is not supported by the weight of the evidence. Despite detailed minutes taken at each JEDEC meeting about what presentations were made and what topics

discussed, Complaint Counsel are unable to point to any discussion of "next generation SDRAM" until late 1995, when a "Future Synchronous DRAM (SDRAM) Features" survey ballot was issued. (CX0260 at 1). Actual consideration of a DDR SDRAM did not begin until December 1996 when a first showing was made. All of the contemporaneous documentation that refers to the history of the DDR SDRAM standard setting indicates that discussions regarding DDR SDRAM began in mid-1996 outside of JEDEC and was not considered at JEDEC until December 1996. (RPF 399-413).

Indeed, Mr. Rhoden, one of the leaders of the DDR SDRAM standardization effort, whose testimony Complaint Counsel cite in support of this finding, made clear in a March 1998 e-mail that DDR standard setting did not begin at JEDEC until "December 96 – A single overview presentation of a DDR proposal at a JC 42 meeting." (CX0375 at 1; RRFF 565).

Much of the evidence cited by Complaint Counsel is misleading and does not actually support the proposed finding. Complaint counsel cite an e-mail written by Richard Crisp in May 1993 in which he states that "Apple . . . is saying that the committee is rushing ahead to get a next generation standard before finding out the problems with the first generation standard." (CX0700 at 2). However, the context of the statement, which related to the number of banks that higher density SDRAMs should contain, makes clear that Mr. Crisp was using "next generation" or "future generation" here to refer to those future, higher density SDRAMs, not what eventually became DDR SDRAMs. For example, Mr. Crisp stated during the same discussion that "Micron also proposed that future generation SDRAMs increase the number of banks. They propose 64meg has 4 banks and propose 8 banks for 256meg." (*Id.*)

Complaint Counsel also cite a March 1995 e-mail from Mr. Crisp in which he quotes

Mr. Wiggers as saying that JEDEC had been working for over two years to standardize a high-speed interface. (CX0711 at 54). However, in the very next line Mr. Crisp states that "[t]his servers [sic] to further underscore the fact that the JC16 committee (led by Farhad Tabrizi of Hyundai) is not delivering on its responsibilities." (CX0711 at 54). Thus, Mr. Wiggers' statement was in reference to the work of JC16, *not* in reference to some undefined new kind of SDRAM within the JC-42.3 subcommittee. Mr. Crisp explained the reference at trial:

> "Q. What did you understand his statement to be about when he says a 'high speed interface'?
>
> A. He was talking about the signaling technology that could be used on almost any kind of a chip.
>
> Q. And was that something that was within JC-16 as opposed to 42.3?
>
> A. Yes, that's correct."

(Crisp, Tr. 3520-21).

Finally, Complaint Counsel cite the testimony of Peter MacWilliams of Intel who testified that he "first heard about DDR in '95." (MacWilliams, Tr. 4815). The testimony says nothing about JEDEC, however. Mr. MacWilliams may well have been referring to what Mr. Rhoden had described as "private and independent work *outside of JEDEC* for most of 1996. . . ." (CX 375 at 1) (emphasis added). It is also likely that Mr. MacWilliams was simply confused about the year. Complaint Counsel concede that the term "DDR" was not coined until 1996 (CCFF 583), so Mr. MacWilliams could not have heard it in 1995. Moreover, since the JEDEC future SDRAM survey ballot was not issued until late 1995 (CX0260), with the results not presented at JEDEC until December 1995 (JX0028 at 6), it is unlikely that MacWilliams was

aware in any JEDEC-related context, prior to that time, of what features might even *potentially* be in a next generation standard.

580. Work on what became the DDR SDRAM standard was referred to as "next generation SDRAM," "SDRAM II" or "future SDRAM." The standard was later named DDR SDRAM after Fujitsu coined the term "DDR" in December 1996. (Rhoden, Tr. 408-09 (" . . . what DDR was originally called by a lot of people that worked on it, we called it SDRAM II, and it wasn't until Fujitsu actually coined the term DDR that we came up with a different name, called it DDR as opposed to SDR II or something like that."); Kelley, Tr. 2581 ("Q: What was your understanding of what Samsung Electronics meant by 'future SDRAM' [in a JEDEC presentation made in March 1996]? A: The committee always needs to be looking ahead to determine what they want for the generation of DRAM that they're presently working on, which at this time I believed was the one we called DDR SDRAM . . .."); (Lee, Tr. 6636 ("This is a JEDEC survey ballot for future synchronous DRAM features, which later became known as DDR")).

Rambus's Response to Finding No. 580:

The proposed finding is not supported by the weight of the evidence. Complaint Counsel attempt to reconcile their current position with the contrary documentary evidence showing that DDR SDRAM standard setting at JEDEC did not begin until the first showing by Fujitsu in December 1996 (RPF 399-413), by suggesting that only a name changed was involved at that time. This suggestion simply does not comport with the evidence. For example, in a March 1998 e-mail by Desi Rhoden, one of the leaders of the DDR standardization effort, on whose testimony Complaint Counsel rely for this proposed finding, Mr. Rhoden wrote:

> "[W]e could have finished the DDR standard sooner if only we had started earlier. Let us recap what has transpired with DDR:
>
> 1. A lot of private and independent work outside of JEDEC for most of 1996 (here is where we missed a good opportunity to start early).

2. December 96 – A single overview presentation of a DDR proposal at a JC 42 meeting."

(CX0375 at 1). Here Mr. Rhoden is bemoaning the fact that DDR standard setting work did *not* begin at JEDEC until December 1996. Quite clearly Mr. Rhoden was *not* suggesting that "we could have finished the DDR standard sooner if only" the *name* "DDR" had been coined earlier.

An IBM presentation on DDR SDRAM dated March 17, 1997 similarly notes that "Industry has been working on DDR definition [outside of JEDEC] for 6-9 months," and it also points to the December 1996 "first showing" by Fujitsu. (RX 892 at 1). A March 10, 1997 Mitsubishi memorandum regarding the "Planning History" of DDR confirms that DDR efforts began outside of JEDEC in the summer of 1996, with "eight companies . . . meeting once every 2 weeks to quickly plan DDR specifications." (RX 885A at 1). Like the IBM document and the Rhoden e-mail, the Mitsubishi document dates JEDEC work relating to DDR SDRAM to the first showing by Fujitsu in December 1996. (RX885A at 1). Since the IBM and Mitsubishi presentations each use the term "DDR" to refer to the earlier work outside of JEDEC before Fujitsu had "coined the term," it is quite clear that they were not focusing on nomenclature, but on the actual standard-setting work.

581. The work begun by JEDEC after adoption of the SDRAM standard included revisiting the dual edge clock that had been proposed by IBM as part of its HST presentations in the late 1980's and early 1990's. (Rhoden, Tr. 462-463, Sussman, Tr. 1403; G. Kelley, Tr. 2567 ("Well, clearly one of the ideas was the dual-edged clock control of the output that we had earlier called toggle mode and now was called dual-edge clock and became what we called DDR or double data rate.").

Rambus's Response to Finding No. 581:

The proposed finding, that the dual edge clocking feature in DDR SDRAMs was simply

"revisiting" IBM's HST presentations is misleading and not supported by the weight of the evidence. (See RRFF 578).

582. The work begun by JEDEC after adoption of the SDRAM standard included discussion on adding on-chip PLLs. (Rhoden, Tr. 463; Sussman, Tr. 1403).

Rambus's Response to Finding No. 582:

The proposed finding is misleading to the extent that it suggests significant discussion of on-chip PLLs and incomplete. In fact, the only proposal that Complaint Counsel raise that related in any way to putting a PLL on a DRAM is a September 1994 NEC presentation regarding "PLL Enable Mode." (JX0021 at 87; CCFF 604). The NEC presentation was a "first showing" (JX0021 at 87), and there is no evidence that it ever progressed beyond that point. Rambus had no patents or pending patent applications with claims covering an SDRAM with a PLL built according to the NEC proposal during the time it was a member of JEDEC. (RRFF 1187-93).

583. The various features that members had been talking about were gathered together in a presentation given by Fujitsu at JEDEC in December 1996. This was when the term DDR was first used. (Rhoden, Tr. 1197-1198 ("This was the Fujitsu presentation where they had taken a collection of the discussions that had taken place throughout -- in -- within previous meetings for the past decade or so, and they had pulled them together in a unified approach to the next generation part. Rather than talking about these features independently, they actually pulled them together, and that is a presentation from Fujitsu. They also happened to coin the name DDR. That's the first time that the DDR name shows up, is in the Fujitsu presentation.")).

Rambus's Response to Finding No. 583:

The proposed finding is misleading and not supported by the weight of the evidence to the extent that it suggests that work at JEDEC on the DDR SDRAM standard began prior to the Fujitsu presentation in December 1996. (RRFF 579-80).

584. The first use of the term "DDR SDRAM" in late 1996 did not mark the beginning

of the work on what became the DDR SDRAM. (G. Kelley, Tr. 2582 and 2585-86 ("Q: Mr. Kelley, would you agree that the first use of the term 'DDR SDRAM' in late 1996 marked the beginning of the work on what became the DDR SDRAM standard? A: Not in my mind."); Rhoden, Tr. 408-09 and 1200; Sussman, Tr. 1429 ("Q. In the 1994 to 1996 time frame, you were attending the JEDEC meetings obviously. A. Yes, sir. Q. In that time frame, was there ongoing JEDEC work that led to the DDR standard? A. Yes."); Lee, Tr. 6636).

Rambus's Response to Finding No. 584:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 579-80; RPF 399-413).

585. The JEDEC patent disclosure policy and obligation of good faith applied to work relating to technologies incorporated in what ultimately became known as the DDR SDRAM standard before the name "DDR SDRAM" was first used in December 1996. (G. Kelley, Tr. 2586-87 ("QUESTION: Mr. Kelley, based on your understanding of the JEDEC disclosure policy, was a member's duty to disclose patents and patent applications relating to dual-edge clock technology triggered only by presentations occurring during or after December 1996? THE WITNESS: No. In my mind, we had been considered -- considering toggle mode, which is a dual-edge clock, in the early considerations of SDRAM in the 1990, 1991, 1992 time frame significantly. There were lots of presentations that included consideration in those early '90 years, so it did not begin with the later consideration of what the committee called DDR."); Rhoden, Tr. 468, 492, 514; Sussman, Tr. 1381-1382, 1386, 1406-1407, 1409; G. Kelley, Tr. 2571; Landgraf, Tr. 1717, 1720; *see also* J. Kelly, Tr. 1983-1984 (For the duty to disclose to arise, it is not necessary that there be some formal activity within the relevant standard-setting committee that involves the technology or technologies covered by the patent or patent application) and 1984-1985 (The duty to disclose is "not tied to any procedural formality in the process at all.")).

Rambus's Response to Finding No. 585:

The proposed finding is misleading and not supported by the weight of the evidence. First, the proposed finding suggests that DDR SDRAM standard setting work began before December 1996 and that the significance of December 1996 is only that this was when "the name 'DDR SDRAM' was first used." This is contrary to the weight of the evidence which shows that DDR SDRAM standard setting work began at JEDEC in December 1996. (*See* RRFF 579-80; RPF 399-413).

Second, the proposed finding is contrary to the weight of the evidence to the extent that it suggests that any and every discussion at JEDEC triggers a patent disclosure obligation. To the contrary, the evidence shows that during the time Rambus was a member of JEDEC the manuals and policies of JEDEC encouraged, but did not require, disclosure of intellectual property interests. Moreover, to the extent that there was any disclosure duty, it applied only to issued patents that were essential to practice a standard, and the disclosure obligation arose only at the time of balloting. (*See generally* RPF 108-317).

2. The Decision to Use Programmable CAS Latency and Burst Length.

586. Because the next generation SDRAM standard was designed as a follow-on to the first SDRAM standard, the JC-42.3 subcommittee's assumption was that the features contained in the SDRAM standard would be carried over into the future, or next generation, SDRAM standard. (Peisl, Tr. 4378- 4379)

Rambus's Response to Finding No. 586:

The proposed finding mischaracterizes the evidence. Mr. Peisl testified as follows:

> "[W]e knew pretty much about the DDR design right from the beginning because we knew that JEDEC would take many of the features over, and some features were not yet defined at that point in time and we scheduled the design accordingly to start with all the features that we knew and put on those that are still in discussion on the JEDEC level towards the end of the design."

(Peisl, Tr. 4378-79). Mr. Peisl did not say that there was an assumption that the features contained in SDRAM would be carried over to the next generation; he simply stated that many features would be carried over while others were undefined. The proposed finding is also belied

by evidence of the DDR2 SDRAM standardization effort, in the course of which various features of DDR SDRAMs, such as programmable CAS latency, programmable burst length and dual edge clocking, were reevaluated and extensively discussed prior to their inclusion in the standard. (RPF 751-52, 755-56, 760-61).

587. When it began work on the next generation SDRAM standard, the JC-42.3 subcommittee assumed that programmable CAS latency and programmable burst length would be carried over into the next generation standard. (Rhoden, Tr. 491).

Rambus's Response to Finding No. 587:

The proposed finding is incomplete. As Complaint Counsel note, the JC-42.3 subcommittee had considered, and rejected, fixing CAS latency in connection with the SDRAM Lite proposal in late 1995. (CCFF 572). To the extent that there was an assumption that programmable CAS latency and programmable burst length would be carried over into the next generation standard, it was presumably because the benefits of those features had recently been discussed.

588. In October 1995, JEDEC staff distributed to subcommittee members, including Rambus, a survey ballot requested at the September 1995 JC-42.3 meeting. (CX0260). The subject of the survey was "Future Synchronous DRAM (SDRAM) Features." (CX0260 at 1). The survey ballot assumed that the future SDRAM standard would include programmable CAS latency and burst length. The ballot asked whether members thought it important to add any additional latency values to those already available. (CX0260 at 9 ("There are currently 4 reserved states in the mode register's CAS latency field that could logically accommodate CAS latencies of 5, 6, 7, and 8. . . .Does your company believe it is important to standardize CAS latencies beyond a CAS latency of 4?")). The survey ballot also asked members whether they wanted the "wrap" functionality to be programmable. (CX0260 at 11 ("There may be advantages to eliminating the "wrap" functionality or making it programmable.")).

Rambus's Response to Finding No. 588:

The proposed finding is misleading. The "wrap" functionality discussed in the ballot is unrelated to programmable burst length but, rather, has to do with the order in which data bits are

read out of memory for a given burst length. (CX0260 at 11). There is no assumption of programmable burst length evident from the survey ballot.

589. The results of the SDRAM Features Survey Ballot that had issued on October 30, 1995 were tallied at the same meeting on December 6, 1995. (JX0028 at 36-48). Mosaid made a presentation on the results of the survey. (JX0028 at 6). The CAS latency portion of the survey results showed that JC-42.3 members strongly supported adding into the mode register CAS latencies in excess of four. (JX0028 at 42). The results of the burst wrap survey were also presented. (JX0028 at 44).

Rambus's Response to Finding No. 589:

The proposed finding is misleading to the extent that it means to suggest that "burst wrap" is related to programmable burst length; it is not. (*See* RRFF 588).

590. At the March 20, 1996, JC-42.3 meeting, the RAM features and functions subcommittee made a presentation that included use of programmable CAS latency and burst length. (JX0031 at 64). Desi Rhoden, who made the presentation, assumed that JEDEC would continue to use programmable CAS latency and burst length in the next standard. (Rhoden, Tr. 491-492).

Rambus's Response to Finding No. 590:

The proposed finding is incomplete. To the extent that there was an assumption that JEDEC would continue to use programmable CAS latency and burst length in the next standard, it was presumably because a proposal to eliminate programmable CAS latency and restrict programmable burst length had recently been rejected in connection with SDRAM Lite. (CCFF 587). The March 20, 1996 presentation underscores the importance of programmable CAS latency since it indicates that different CAS latencies would be required at different clock speeds. (JX0031 at 64).

591. At the June 5, 1996, JC-42.3 meeting, EIA made two presentations that included programmable CAS latency and burst length. (JX0033 at 41- 46 and JX0033 at 47-49).

Rambus's Response to Finding No. 591:

The proposed finding is incomplete and incorrect. The presentations were made by Oki on behalf of EIAJ, not EIA. (JX033 at 7). The presentations for 100-150 MHz SDRAM included three required burst length values and four required CAS latency values. (JX033 at 41, 45, 47, 48).

592. At the September 10, 1997 JC-42.3 meeting, the subcommittee voted unanimously to send a DDR mode register to Council. (JX0040 at 7-8; Lee, Tr. 6640-6641). That mode register included programmable CAS latency (CX0234 at 150; JX0057 at 12; Lee, Tr. 6641) and burst length (CX0234 at 150; JX0057 at 12).

Rambus's Response to Finding No. 592:

Rambus has no specific response.

593. The mode register was approved by Council and included in Release 9 of the 21-C standard published by JEDEC in August 1999 and subsequently in the consolidated DDR SDRAM Specification (JESD79) that was published by JEDEC in June 2000. (CCFF 657).

Rambus's Response to Finding No. 593:

Rambus has no specific response.

3. Consideration of On-Chip PLL/DLL.

594. After the release of the SDRAM standard, JEDEC began working on the next "evolutionary part". (Sussman, Tr. 1402). JEDEC was considering on-chip PLL/DLLs as part of that work. (Sussman, Tr. 1403).

Rambus's Response to Finding No. 594:

The proposed finding is inaccurate and incomplete. JEDEC did not begin work on what became the next generation standard, DDR SDRAM, until December 1996. (RPF 399-413). It is true that there was recognition in the mid-1990s among JEDEC members that, as bus speeds increased, an on-chip PLL or DLL would become necessary. (Soderman, Tr. 9408-10; Rhoden,

Tr. 546 ("I don't think we ever had any question whether we would use the technology [on-chip PLL or DLL]. It was just a question of when.")).

595. PLLs are very similar to DLLs. (Jacob, Tr. 5443).

Rambus's Response to Finding No. 595:

The proposed finding is misleading. PLLs are similar to DLLs in that they can be used for similar purposes in some applications. (Jacob, Tr. 5617). They are, however, different types of circuits: A PLL uses a voltage controlled oscillator while a DLL uses variable delay lines. (Jacob, Tr. 5616-17).

596. Rambus co-founder Horowitz testified that a DLL is a type of PLL. (Horowitz, Tr. 8607).

Rambus's Response to Finding No. 596:

The proposed finding is misleading in its suggestion that the terms DLL and PLL are generally used in this way. In fact, Dr. Horowitz's use of the terms is non-standard. Since both phase locked loops (PLLs) and delay locked loops (DLLs) can be used to achieve the same functional result of locking the phases of two signals together, Dr. Horowitz considers "phase lock loop [to be] a generic term that means any circuit that uses feedback to adjust phase of two signals to be coincident or in some fixed relation." (CX2116, Horowitz FTC Depo. at 84-85.) Dr. Horowitz then separates when he terms PLLs into two types: "There are those that are based on oscillators, which I generally call VCO, voltage-controlled oscillator phase lock loops, and there are also those that depend on delay lines, which I call delay line phase lock loops or DLL." (*Id.* at 85).

The general use of the terms, however, as Complaint Counsel's experts testified, restricts

PLLs to what Professor Horowitz calls "VCO" phase lock loops, so that PLLs and DLLs are distinct categories of circuits. (Nusbaum, Tr. 1637) ("I understand that the terminologies may be used in terms of their functional result differently, but a phase locked loop is typically a device that's got a variable oscillator and a phase comparator and a delay locked loop does not necessarily have such components."); (Jacob, Tr. 5443) ("The primary difference is that a PLL contains an oscillator and a DLL doesn't."); (Jacob Tr., 5617). ("Q. A DLL uses variable delay circuitry to delay one signal so that it is in sync with another signal; correct? A. Correct. Q. And a PLL uses an oscillator instead of varying the delay circuitry; right? A. Correct.") (Soderman, Tr. 9401) ("The difference is that -- DLL is a delay locked loop. A PLL generates -- has an oscillator that generates an internal clock that can be synchronized with some other signal. The DLL delays the clock to a particular value that would synchronize with some signal. The difference is one has an oscillator, one doesn't.")

597. The JEDEC subcommittee members used the terms PLL and DLL interchangeably. (Rhoden, Tr. 492).

Rambus's Response to Finding No. 597:

The proposed finding is not supported by the weight of the evidence. While PLLs and DLLs could be used for some similar purposes, they are different circuits. (RRFF 595). Once JEDEC chose a DLL, the evidence shows it was always referred to as a "DLL," never as a "PLL." (*See*, *e.g.*, CX0234 at 176; JX0057 at 5, 12, 16).

598. The predominant purpose of JEDEC considering placing a PLL or a DLL on a memory device was to guarantee that the memory controller would capture data during the data valid window. (Jacob, Tr. 5442-5443; Kellogg, Tr. 5154-5155; Lee, Tr. 6662-6664)

Rambus's Response to Finding No. 598:

The proposed finding is misleading and incomplete. SDRAMs and DDR SDRAMs both had to guarantee that the memory controller would capture data during the data valid window, but SDRAMs operating at lower data transfer rates did not require a PLL or DLL. (See Jacob, Tr. 5441 (as data transfer rates increase, the data valid window shrinks)). As the window becomes smaller, it becomes important to align the data closely with the clock so that the data is read in the window where it is valid. (Soderman, Tr. 9404-05). Thus, while a PLL or DLL does ensure that the memory controller captures valid data, the predominant purpose of considering an on-chip PLL or DLL was to allow higher data transfer rates.

599. An on-chip PLL/DLL would account for delays occurring within the DRAM itself but would not account for delays that occur between the DRAM chip and the controller. (Kellogg, Tr. 5154).

Rambus's Response to Finding No. 599:

Rambus has no specific response.

600. The duty to disclose patents or patent applications relating to use of on-chip PLL or on-chip DLL technology was triggered while Rambus was still a member of JEDEC. (G. Kelley, Tr. 2587 ("Q. Again, Mr. Kelley, based on your understanding of the JEDEC disclosure policy, was a member's duty to disclose patents and patent applications relating to use of on-chip PLL or on-chip DLL technology triggered only by presentations occurring during or after December 1996? A. No. They had to be disclosed when the presentations were first considered in the '95, possibly even '94 time frame. I specifically remember '95.")).

Rambus's Response to Finding No. 600:

The proposed finding is not supported by the weight of the evidence. *See* RRFF 601-616.

601. During the course of 1994, Richard Crisp of Rambus observed discussions in the JEDEC JC-42.5 subcommittee regarding using PLLs on memory modules to remove clock skew from the module. (CX0711 at 13, 14 (Crisp e-mail (3/8/94): the 200 pin DIMM (Dual In-line Memory Module) includes "an on-board PLL clock generator to remove clock skew from the module."), at 31, 35 (Crisp e-mail (7/13/94): Mark Kellogg "argues that the PLLs, buffers, etc

must be moved off the DIMM. They are still needed, but the idea is to put them on the motherboard.")).

Rambus's Response to Finding No. 601:

The proposed finding is irrelevant. Discussions at JEDEC relating to PLLs on memory *modules* could not trigger any duty to disclose Rambus patents or patent applications, because there is no evidence that Rambus had any patents or patent applications relating to this technology. To the contrary, Complaint Counsel assert that a PLL or DLL on the module is an *alternative* to Rambus technology. (CCFF 2366).

602. During the course of 1994, Richard Crisp of Rambus was present when the JC-42.3 subcommittee discussed putting PLLs on other types of memories, including SDRAMs. (JX0021 at 39 (Motorola SRAM Sleep and Doze Mode Proposal diagram shows "Phase Locks"); JX0022 at 34 (NEC SRAM Sleep and Doze Mode (informal) proposal table showing PLL)).

Rambus's Response to Finding No. 602:

The proposed finding about putting PLL on types of memories other than SDRAMs is irrelevant to this matter. The proposed finding about putting PLLs on SDRAMs is not supported by the evidence cited, which relates to PLLs on SRAMs, not SDRAMs. It is true that there was one presentation by NEC regarding a "PLL Enable Mode" which included a diagram showing a PLL on an SDRAM. (CCFF 604). The NEC presentation was a "1st showing" (JX0021 at 87), and there is no evidence that it ever progressed beyond that point. Finally, Rambus had no patents or pending patent applications with claims covering an SDRAM with a PLL built according to the NEC proposal during the time it was a member of JEDEC. (RRFF 1187-93).

603. Richard Crisp and others at Rambus appreciated that memory manufacturers could incorporate PLLs/DLLs on SDRAMs to correct for clock skew. (CX0711 at 22, 23 (Crisp e-mail (5/24/94): "The use of DLL/PLL technologies could be incorporated by anyone to solve" one aspect of clock skew)).

Rambus's Response to Finding No. 603:

The proposed finding is misleading to the extent that it suggests that this knowledge was peculiar to Rambus or that incorporating PLLs or DLLs on SDRAMs could be easily done. It was generally understood in the mid-1990s that on-chip PLLs or DLLs would be required at some point to limit clock skew sufficiently to achieve higher data transfer rates. (RRFF 2369). Nevertheless, many in the industry were resistant to incorporating on-chip PLLs or DLLs due to the difficulties involved. When Rambus first presented its technology to DRAM manufacturers in the 1989-90 time frame, many felt that it was not possible to put a PLL on a DRAM. (Horowitz, Tr. 8517 ("A phase-lock loop was even worse. This is a very tricky analog circuit. You couldn't put this on a DRAM. You couldn't get the I/O speeds, the circuitry to run. You know, you name it, people were kind of skeptical.")). As late as 1997, well after Rambus had proven that PLLs and DLL could be placed on DRAMs and very high data transfer rates achieved, many DRAM manufacturers remained daunted by the difficulties involved. In a November 1997 e-mail, for example, Hans Wiggers of Hewlett-Packard explained that DLLs would be "essential" for the data rates that they hoped to achieve, while recognizing that "I know everyone is afraid of DLLs." (RX1040).

604. At the September 13-14, 1994, JC-42.3 meeting, NEC made a presentation regarding PLLs on SDRAMs. NEC's presentation showed an on-chip PLL circuit and proposed to include a PLL-enable bit in the mode register in order to enable on-chip PLLs. (JX0021 at 87 (Mode Register diagram showing PLL Enable Mode), 91 (diagram comparing access time with and without on-chip PLL) and 92 (slide discusses advantages and disadvantages of on-chip PLL); Rtthoden, Tr. 466 ("NEC was proposing including a PLL on board the chip to actually synchronize the phased relationship of the internal clock to the external clock."); G. Kelley, Tr. 2569-70 (The "PLL enable mode is for the addition of a feature called phase lock loop. . . . The proposal on the left [of JX0021, page 91] asks us to consider not putting the PLL on chip, in other words, doing the phase lock loop operation with another device. And then the proposal on the right as a comparison shows us the option of putting the phase lock loop on the DRAM chip

as a new feature. And the comparison shows why the inclusion of the phase lock loop on the chip buys performance.");

Rambus's Response to Finding No. 604:

The proposed finding is incomplete. The NEC presentation was a "1st showing" (JX0021 at 87), and there is no evidence that it ever progressed beyond that point. Rambus had no patents or pending patent applications with claims covering an SDRAM with a PLL built according to the NEC proposal during the time it was a member of JEDEC. (RRFF 1187-93).

605. Richard Crisp sent an e-mail from the September 1994 JC-42.3 meeting stating that NEC was proposing putting a PLL on an SDRAM. (CX0711 at 36-37 ("(NEC PROPOSES PLL ON SDRAM!!!) . . .**** They plan on putting a PLL on board their SDRAMs . . . ****I believe that we have now seen that others are seriously planning inclusion of PLLs on board SDRAMs. . . . What is the exact status of the patent with the PLL claim? ****") (emphasis in original)).

Rambus's Response to Finding No. 605:

The proposed finding is incomplete. In fact, Rambus had no patents or pending patent applications with claims covering an SDRAM with a PLL built according to the NEC proposal during the time it was a member of JEDEC. (RRFF 1187-93).

606. Members viewing this presentation were under an obligation to disclose patents or patent applications relating to use of on-chip PLL technology. (G. Kelley, Tr. 2571; *see also* Rhoden, Tr. 468 (this presentation triggered a disclosure obligation)) Furthermore, members had an expectation that a member with any intellectual property relating to on-chip PLL should disclose that interest at the meeting. (Sussman, Tr. 1406-1407).

Rambus's Response to Finding No. 606:

The proposed finding is not supported by the weight of the evidence. The evidence shows that during the time Rambus was a member of JEDEC the manuals and policies of JEDEC encouraged, but did not require, disclosure of intellectual property interests; moreover, to the extent that there was any disclosure duty it applied only to issued patents that were essential to

practice a standard, and the disclosure obligation arose only at the time of balloting. (*See generally* RPF 108-317). The NEC presentation was a "1st showing" (JX0021 at 87), and there is no evidence that it ever progressed beyond that point. Before being balloted, the presentation would have required a second showing, as well as a vote to approve the ballot. (Williams, Tr. 773; Grossmeier, Tr. 10949). Moreover, Rambus had no patents or pending patent applications with claims covering an SDRAM with a PLL built according to the NEC proposal during the time it was a member of JEDEC. (RRFF 1187-93).

The proposed finding also misstates the evidence if it is suggesting that members had an "expectation" that "any" other member with "any" intellectual property "relating to" on-chip PLL would disclose that intellectual property in response to the NEC presentation. At most, the evidence supports a finding that *some* members expected that *presenters* (here, NEC) who had patents or applications that would need to be used to build or use the proposed device would or should disclose. As Mr. McGrath explained, in response to questions by Your Honor:

> "[I]f I'm the person doing the proposal for this technology and I'm developing technology that I'm going to patent I think it's my responsibility to tell the group that that's what I'm doing.
>
> . . .
>
> So there's – the good faith that I'm talking about is if I'm making the presentation, if I'm trying to take JEDEC down this particular technology road, that's what I'm referring to."

(McGrath, Tr. 9273-74).

It is undisputed that Rambus never presented its technology for standardization.

607. In terms of implementation, there was essentially no difference in the PLL proposed by NEC in September 1994 and a DLL. (Rhoden, Tr. 467-468).

Rambus's Response to Finding No. 607:

The proposed finding is not supported by the weight of the evidence. As both Complaint Counsel's technical expert and Rambus's technical expert made clear, PLLs and DLLs are implemented differently – the former uses a voltage controlled oscillator, while the latter uses variable delay lines. (RRFF 595; Soderman, Tr. 9401).

608. At the May 24, 1995 JC-42.3 meeting, Hyundai, Texas Instruments and Mitsubishi made a presentation of the proposed Ramlink/Synclink standard at JEDEC. (JX0026 at 10-11). That presentation included discussion of on-chip PLLs, which the RamLink/SyncLink was planning to avoid. (JX0026 at 97 ("Avoid using PLL in DRAM components")).

Rambus's Response to Finding No. 608:

The proposed finding is irrelevant. A presentation that, as Complaint Counsel admits, related to *not using* on-chip PLLs or DLLs, could hardly have triggered any disclosure duty with respect to *using* on-chip PLLs or DLLs.

609. Discussions of features for the future SDRAM standard led to a request at the JC-42.3 meeting held on September 11, 1995 for a survey ballot to determine the features for the next-generation DRAM. On-chip PLLs were one of the features that had been discussed that led to the request for the survey ballot. (JX0027 at 14 ("A survey ballot was requested on the next generation issues stated above. Mr. Allen agreed to prepare the survey."); Calvin, Tr. 1032 (" . . . this survey was a result of trying to capture the top most things that were necessary for SDRAM to continue to evolve. This had been discussed at numerous meetings before, and many inputs were coming in and, well, this seems to be a big problem area, we should do this. And PLL/DLL was one of those discussions. So, this was just an attempt to say, how important is it, how would you rate it, in terms of need.")).

Rambus's Response to Finding No. 609:

The proposed finding is not supported by the weight of the evidence. The issues that led to the request to issue the survey ballot are listed in the minutes of the September 1995 meeting;

on chip PLLs was not among them. (JX0027 at 14). In any event, the evidence shows that a survey ballot did not trigger a disclosure obligation. (RPF 346; RRFF 339-40, 385).

610. In October 1995, JEDEC staff distributed to subcommittee members, including Rambus, the survey ballot requested at the September 1995 JC-42.3 meeting. (CX0260). The subject of the survey was "Future Synchronous DRAM (SDRAM) Features." (CX0260 at 1). Question 3.9-1 asked members whether they believed that use of an on chip PLL or DLL was important to reduce the access time from the clock for future generations of SDRAMs future generations of DRAMs (CX0260 at 12 ("Does your company believe that on chip PLL or DLL is important to reduce the access time from the clock for future generations of SDRAMs?").

Rambus's Response to Finding No. 610:

The proposed finding is irrelevant because the evidence shows that a survey ballot did not trigger a disclosure obligation. (RPF 346; RRFF 339-40, 385).

611. At the JC-42.3 meeting of December 6, 1995, the tally of the votes cast in the Future SDRAM Features Survey Ballot was announced. Eleven members voted "yes" and four members "no" to the question as to whether their company believed that "on chip PLL or DLL is important to reduce the access time from the clock for future generations of SDRAMs" (JX0028 at 45). On-chip PLL/DLL was included among issues with "strong support" in the conclusion of the SDRAM Feature Survey Ballot. (JX0028 at 35 ("ISSUES WITH STRONG SUPPORT . . . On chip PLL/DLLs to reduce clock access time")).

Rambus's Response to Finding No. 611:

The proposed finding is irrelevant because the evidence shows that a survey ballot did not trigger a disclosure obligation. (RPF 346; RRFF 339-40, 385). The proposed finding is also incomplete. Despite the survey ballot, there remained significant opposition to including on chip PLLs or DLLs in the standard because of the difficulties involved. As late as November 1997, Hans Wiggers of Hewlett-Packard explained to those still opposed that DLLs were "essential" for the data rates that they hoped to achieve, while recognizing that "I know everyone is afraid of DLLs." (RX1040). In recapping the DDR SDRAM standardization process, Desi Rhoden wrote that they had "saved a few of the toughest issues [like the DLL enable/disable] for last," and the

issue was not resolved until March 1998. (CX0375 at 2).

612. Mosaid presented the results of the survey. Mosaid disclosed a pending patent application with claims relating to on-chip DLL technology, but stated that the patent likely to result from the application may not be necessary to use a standard. (JX0028 at 6 ("MOSAID noted that they had a patent pending on DLL and noted that it was a particular implementation and may not be required to use the standard."); CX0711 at 192 (Crisp e-mail (12/6/95): Richard Foss of Mosaid "stated that MOSAID has a pending patent application for PLL/DLL on SDRAMs. His suspicion is that his patent will probably end up being an implementation patent rather than a concept patent. In the event the patent winds up being a concept patent, he says they will be compliance with the JEDEC patent policy.*****")).

Rambus's Response to Finding No. 612:

The proposed finding is incomplete and misleading in suggesting that Mosaid made a voluntary disclosure of a patent application. To the contrary, Mosaid's comment was in response to a specific question from Hyundai. (JX0028 at 45 ("Wondering DLL may be Mosaid patent.")). It is also useful to note that Mosaid only agrees to comply with the patent policy if the patent ends up as a "concept patent," not if it ends up as an "implementation patent." (CX 711 at 192). The exchange thus confirms that to the extent there was any disclosure duty, it applied only to essential patents, that is, patents that are "necessary to use a standard." (See generally RPF 274-85). Rambus had no patents or patent applications that covered the general concept of an on-chip PLL/DLL, as opposed to a specific implementation. (*See* RRFF 1183).

613. At the January 31, 1996, JC-42.3 interim meeting, Micron presented a proposal discussing the potential use of on-chip PLL/DLLs and echo clocks in Future SDRAMs. (JX0029 at 17 ("PLL/DLL circuits are being considered to reduce the apparent access time (i.e. as measured from the external clock) for read accesses"). Micron proposed using a single PLL on the controller or clock chip and echo clocks rather than on-chip PLLs. (JX0029 at 18 ("FUTURE SDRAM - CLOCK ISSUES PLL/DLL Circuits . . Use centralized PLL/DLL (e.g. in clock chip) to generate two phases of clock signal"); Rhoden, Tr. 487). The Micron presentation triggered a duty to disclose under the JEDEC patent policy. (Rhoden, Tr. 488).

Rambus's Response to Finding No. 613:

The proposed finding is irrelevant. Even if, contrary to the weight of the evidence, a presentation like Micron's could trigger a duty to disclose intellectual property, it certainly could not trigger a duty to disclose intellectual property unrelated to the presentation. Here, Complaint Counsel concede that the Micron presentation proposed "a single PLL on the controller or clock chip . . . rather than on-chip PLL/DLLs." Complaint Counsel have introduced no evidence that Rambus had intellectual property related to PLLs or DLLs on the *controller*; to the contrary, Complaint Counsel assert that a PLL or DLL on the controller is an *alternative* to Rambus's technology. (CCFF 2366).

614. At the JC-42.3 meeting of March 20, 1996, Desi Rhoden, on behalf of the JC-42.3C RAM Features and Functions Letter Committee, made a presentation that included on–chip PLL/DLL**.** (JX0031 at 64 (table showing SDRAM features that includes on chip PLL/DLL); Rhoden, Tr. 492). This presentation triggered a disclosure under the JEDEC patent policy. (Rhoden, Tr. 493).

Rambus's Response to Finding No. 614:

The proposed finding is misleading and incomplete. Mr. Rhoden's presentation was not a proposal for a device; it simply provided information regarding what features might be required in the future and confirmed the general knowledge that to achieve high data transfer rates, an on-chip PLL or DLL would be required. (JX0031 at 64; see RRFF 2369). Even if, contrary to the weight of the evidence, such general discussion could trigger a disclosure obligation, Rambus had no patents or patent applications that covered the general concept of an on-chip PLL/DLL as opposed to a specific implementation. (*See* RRFF 1183).

615. Samsung also made a Future SDRAM proposal that included discussion of alternatives to on-chip PLL/DLL. (JX0031 at 68-72; Rhoden, Tr. 513-514; Lee, Tr. 6691). This presentation triggered disclosure under the JEDEC patent policy. (Rhoden, Tr. 514).

Rambus's Response to Finding No. 615:

The proposed finding is irrelevant. Even if, contrary to the weight of the evidence, a presentation like Samsung's could trigger a duty to disclose intellectual property, it certainly could not trigger a duty to disclose intellectual property unrelated to the presentation. Here, Complaint Counsel concede that the Samsung presentation related to "*alternatives* to on-chip PLL/DLL" (in fact, like the Micron presentation cited above (CCFF 613), it proposed a PLL on the memory controller (JX0031 at 71)). Complaint Counsel have introduced no evidence that Rambus had intellectual property related to PLLs or DLLs on the *controller*; to the contrary, Complaint Counsel assert that a PLL or DLL on the controller is an *alternative* to Rambus's technology. (CCFF 2366).

616. At the JC-42.3 meeting of June 5, 1996, EIA made two presentations involving on/off-chip DLL. (JX0033 at 42 ("Latency, in the case of DLL on chip") and 48 ("Latency (without DLL)").

Rambus's Response to Finding No. 616:

The proposed finding is irrelevant. EIAJ (not EIA) was simply presenting information as to what the timing parameters would be for a 100-150 MHz SDRAM with and without an on-chip DLL. It did not consider the case of an off-chip DLL, as stated in the proposed finding, and was not proposing that a DLL be included in the standard. (JX033 at 42, 48).

617. During the course of its work relating to what ultimately became the DDR SDRAM standard, the JC-42.3 subcommittee also considered, as an alternative to on-chip PLL/DLL, the use of vernier circuits. (JX0036 at 58, 64; CX0367 at 3 (Presentation of Desi Rhoden: "The inclusion of the vernier in the memory for read data timing manipulation is good for all but the simple one memory device system."); Kellogg, Tr. 5168 ("My recommendation was in support first of all for the vernier. We seriously felt that that was the optimal solution, looking at the total data capture issue."); *see also* Lee, Tr. 6676-6678).

Rambus's Response to Finding No. 617:

The proposed finding is incomplete. A vernier would not have been a viable alternative to an on-chip PLL or DLL. (RRFF 2389-99).

618. During the course of its work relating to what ultimately became the DDR SDRAM standard, the JC-42.3 subcommittee also considered, as an alternative to on-chip PLL/DLL, the use of an edge-aligned, bi-directional data strobe. (CX0368 at 1, 4 (Micron presentation regarding an edge-aligned, bi-directional data strobe: An edge-aligned strobe allowed implementation without DLL); CX0370 at 2(Silicon Graphics presentation for a unidirectional data strobe for read operations; "DLLs introduce instability, cut into dram core cycle time.") and 3; CX2713 at 2; Lee, Tr. 6651, 6654).

Rambus's Response to Finding No. 618:

The proposed finding is incomplete. Although DDR SDRAMs have a "bidirectional data strobe (DQS)," they still use a DLL to align the strobe with the clock. (JX0057 at 5).

619. By the time of the JC-42.3 meeting of December 9-10, 1997, the subcommittee had decided to include an on-chip DLL in the DDR standard that could be turned on or off (Lee, Tr. 6680-6681). At this meeting the subcommittee discussed the timing of a device where the on-chip DLL was disab
led or enabled. (JX0041 at 18; Lee, Tr. 6680-6681).

Rambus's Response to Finding No. 619:

The proposed finding is not supported by the weight of the evidence. In recapping the DDR SDRAM standardization process in a contemporaneous e-mail, Desi Rhoden wrote that they had "saved a few of the toughest issues [like the DLL enable/disable] for last" and the issue was not resolved until March 1998. (CX0375 at 2).

4. Consideration of Dual Edge Clocking.

620. Dual edge clocking means capturing data off both edges of the clock. (Lee, Tr. 6688).

Rambus's Response to Finding No. 620:

The proposed finding is vague. "Dual edge clocking" can refer to a number of different technologies and implementations.

621. In a DDR SDRAM, data transitions on both the rising and falling edge of the clock. (Rhoden, Tr. 389; Polzin, Tr. 3995 ("DDR techniques allowed you to capture the data on the falling edge and the rising edge to effectively double the data rate, hence the word "double data rate" or "DDR."); Peisl, Tr. 4397 ("Both, the rising and falling edge of the clock. That's the essential of the DDR standard.").

Rambus's Response to Finding No. 621:

The proposed finding is misleading. In DDR SDRAMs, the clock is all but ignored during writes to the DRAM; the DRAM samples incoming data not with respect to the system clock, but with respect to another signal known as the DQS data strobe. (Jacob, Tr. 5642).

622. In a DDR SDRAM read operation, data is driven by a data strobe, or strobe clock, which transmits data in time with the rising and falling edges of the system clock. (Rhoden, Tr. 513 (Samsung was proposing a "strobe clock, which is essentially what we have [in DDR SDRAMs]."); Peisl, Tr. 4397 (data is being transmitted on the rising and falling edges of the clock); Sussman, Tr. 1427 (page 5 of the DDR SDRAM standard refers to two data transfers per clock cycle); Kellogg, Tr. 5172 (the DDR SDRAM standard called for transmission of data on both the rising and falling edges of the clock)).

Rambus's Response to Finding No. 622:

The proposed finding is misleading. The data strobe is not a "clock." A "clock" is a "free-running" signal, that is running all the time, while the data strobe in DDR SDRAMs is not free-running. (Macri, Tr. 4634).

623. JEDEC consideration of the dual edge clocking technology that was included in the DDR SDRAM standard began in 1988 when IBM presented its first HST proposals. (G. Kelley, Tr. 2584-85 ("In my mind, the consideration of using a double-edged clock actually began when I made the first presentation in 1988 and IBM reproposed in 1990 and 1991 and several other companies picked up in that -- on that concept in 1991. I think we had five companies showing what they called their own toggle mode in their presentations on the consideration of the first-generation synchronous DRAM. So in my mind, the consideration of the dual-edge clock

began in 1988 and was essentially tabled because it was felt by the committee that it was not needed for the first generation part and that we would pick up the idea for consideration of the second generation part, which is now called DDR SDRAM.") and 2586-87 ("In my mind, we had been considered -- considering toggle mode, which is a dual-edge clock, in the early considerations of SDRAM in the 1990, 1991, 1992 time frame significantly. There were lots of presentations that included consideration in those early '90 years, so it did not begin with the later consideration of what the committee called DDR.")

Rambus's Response to Finding No. 623:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 578).

624. Dual edge clocking continued to be considered at JEDEC as IBM and other members made further HST proposals in 1990 and 1991. (G. Kelley, Tr. 2584-85; CCFF 511)

Rambus's Response to Finding No. 624:

The proposed finding is misleading in referring to HST as "dual edge clocking." HST did not transfer data on both edges of the clock signal, but on both edges of a "toggle" signal. While some witnesses loosely referred to this toggle signal as a "clock," it was not a free running clock like the system clock in a synchronous memory such as SDRAM or DDR SDRAM. (Rhoden, Tr. 437 (the HST toggle signal is not in constant operation, as opposed to the system clock in SDRAM); Sussman, Tr. 1471 (in HST, "data is synchronous with their -- I'm calling it a clock, but basically both on the rise and the falling edge of their input signal, whatever we are going to call it, I have data")).

625. On January 3, 1991, the JC-42.3 subcommittee issued a survey ballot regarding a proposed standard for HST. (CX0251). It included questions on dual edge clocking. (CX0316 at 1 ("TOGGLE MODE offers increased data rate (Writes or Reads) by clocking data from all of the DRAM I/Os at both the falling and the rising edges of the 'toggle' pin . . . Do you think that this kind of performance enhancement needs to be offered as a standard" yes (hand written).").

Rambus's Response to Finding No. 625:

The proposed finding is misleading in referring to questions relating to HST as involving

"dual edge clocking." As the evidence quoted by Complaint Counsel makes clear, in HST data is transferred on "both the falling and the rising edges of the 'toggle' pin," not the clock. (CX0316 at 1; *see* RRFF 624). The proposed finding is also unrelated to any issue in this case since Rambus did not attend its first JEDEC meeting until December 1991. (CCFF 758).

626. At the May 9, 1991 JC-42.3 meeting, the subcommittee passed a motion to ballot the IBM toggle mode presentation. (JX0005 at 12). At the same meeting Siemens also made a toggle mode presentation that was like the IBM toggle mode except it used a G\ pin instead of a new toggle pin. (JX0005 at 12).

Rambus's Response to Finding No. 626:

The proposed finding is irrelevant since Rambus did not attend its first JEDEC meeting until December 1991. (CCFF 758).

627. At the September 18, 1991 JC-42.3 meeting, the subcommittee voted in favor of the IBM toggle mode technology. However, there were four no votes and a number of comments. For example, NEC and Samsung commented that the use of two clock edges can limit speed. (JX0007 at 8). The subcommittee therefore decided to put the ballot on hold until more resolution to the comments could be made. (JX0007 at 9). At the same meeting Siemens made a second showing of its toggle mode technology. A motion to ballot was not made. (JX0007 at 10).

Rambus's Response to Finding No. 627:

The proposed finding is irrelevant since Rambus did not attend its first JEDEC meeting until December 1991. (CCFF 758).

628. At the JC-42.3 Subcommittee meeting held on December 4-5, 1991, Mark Kellogg of IBM made a presentation comparing High Speed Toggle to synchronous DRAMs. (JX0010 at 5 and 84 ("Options: 1) high speed toggle (already passed ballot, on hold)")).(Kellogg, Tr. 5172-5173) The HST being presented by Kellogg was basically the same thing as dual edge clocking. (Sussman, Tr. 1380-1381; Prince, Tr. 8992 ("Q. And when you talk here about another method, was that -- are you describing dual-edged clocking? A. Yes, although at the time I would have said I was describing toggle mode. Yes. Q. And by that would mean using the rising edge and the falling edge of the clock to – A. Yes, sir.") The Kellogg presentation created an obligation on a member to disclose relevant patents or patent applications. (G. Kelley, Tr. 2506). A JEDEC member listening to this presentation with claims covering dual edge clocking should

have disclosed those claims. (Sussman, Tr. 1381-82).

Rambus's Response to Finding No. 628:

The proposed finding is not supported by the weight of the evidence to the extent that it means to suggest that HST is "basically the same thing as dual edge clocking" as used in DDR SDRAMs or as described in Rambus's '898 application. HST's asynchronous technology was quite different from the synchronous technology in DDR SDRAMs and described in Rambus's '898 application. (See RRFF 578). Indeed, although IBM held patents on HST (Kelley, Tr. 2715), there is no evidence that they disclosed them in connection with DDR SDRAM. Moreover, the Patent and Trademark Office has issued Rambus patents covering the form of dual edge clocking described in the '898 application despite considering whether IBM's HST technology constituted prior art. (*See* RRFF 2364).

The proposed finding that the Kellogg presentation triggered an obligation to disclose dual edge clocking claims is likewise not supported by the weight of the evidence. First, as noted above, HST, as discussed in the Kellogg presentation, is different from dual edge clocking as used in DDR SDRAMs and as described in the '898 application. Second, JEDEC policies cannot be stretched to attach a disclosure obligation in connection with presentations like Mr. Kellogg's. (*See generally* RPF 108-317). Third, the cited evidence does not support the finding. In the cited testimony, Mr. Sussman responded that it would have been "useful" if dual edge clocking claims had been disclosed, in response to a question asking whether it would "have been relevant to know if another member had IP claims on dual edge clocking technology." (Sussman, Tr. 1381-82). Moreover, Mr. Kellogg testified that he did not believe that the written JEDEC patent policy in effect at the time required the disclosure of patent applications in connection

with his presentation. (Kellogg, Tr. 5306-07).

The proposed finding is also irrelevant. There is no evidence that Rambus had any patents or patent applications covering any form of dual edge clocking technology in December 1991. Indeed, the first Rambus claim that Complaint Counsel raise as relating to dual edge clocking was filed in September 1994. (CCFF 1205).

629. At a special meeting of the JC-42.3 Subcommittee Task Force held on April 14, 1992, IBM indicated a desire to have dual edge clock technology in the first-generation SDRAM standard. (CX0034 at 32 ("IBM: … A Synchronous RAS/CAS with Synchronous DQ * dual clock edge…"); Rhoden, Tr. 443 (Mr. Hardell was "proposing using both edges of the clock for the transition of data and information inside the Synchronous DRAM."); G. Kelley, Tr. 2514 (Mr. Hardell was proposing that JEDEC use the IBM invention, "an asynchronous DRAM with a synchronous output using both edges of the clock, the rising edge of the clock and falling edge of the clock, to output data."); Sussman, Tr.1386 ("Hardell . . . is still pushing a double edge clock version of the part).

Rambus's Response to Finding No. 629:

The proposed finding is misleading. At the task force meeting, IBM proposed a "slightly modified version of its HST technology." (CCFF 522). This proposal was for an asynchronous DRAM. (RRFF 509; RPF 338). Thus, it makes no sense to say that this was a proposal about features to incorporate in the first generation SDRAM, or *synchronous* DRAM, standard. Indeed, as noted above, Mark Kellogg had recently given a presentation contrasting HST and synchronous DRAM. (CCFF 628).

The evidence cited in support of the proposed finding misquotes the summary of the IBM presentation, thereby entirely changes the meaning. The presentation does not say "A Synchronous RAS/CAS," but, rather "A-Synchronous RAS/CAS," meaning that the RAS and CAS signals are asynchronous." (Kellogg, Tr. 5175 (the presentation involved "asynchronous inputs for address and command"; Jacob, Tr. 5542-43 (the presentations stated "asynchronous

RAS/CAS")).

The proposed finding is also misleading in referring to the IBM proposal as proposing "dual edge clocking." (*See* RRFF 628).

630. Mr. Sussman's expectation as a JEDEC member was that a member with intellectual property relating to dual edge clocking technology would disclose that intellectual property. (Sussman, Tr. 1386). The same JEDEC disclosure rules apply to JEDEC task force meetings like this one as to regular JEDEC committee meetings. (Sussman, Tr. 1386)

Rambus's Response to Finding No. 630:

The proposed finding is not supported by the weight of the evidence, to the extent that "dual edge clocking" is intended to encompass the form of dual edge clocking described in Rambus's '898 application. This form of dual edge clocking was very different from the IBM presentation in April 1992. (*See* RRFF 628-29).

The proposed finding is also irrelevant. There is no evidence that Rambus had any patents or patent applications covering any form of dual edge clocking technology in April 1992. Indeed, the first Rambus claim that Complaint Counsel raise as relating to dual edge clocking was filed in September 1994. (CCFF 1205).

631. The attendees at the meeting discussed the advantages of a dual edged clock against a single edged clock and decided that a dual edge clock was not needed to meet the requirements of the SDRAM standard that it was currently working on and that it would reconsider the dual edge clocking technology in the next generation standard (G. Kelley, Tr. 2515 ("At the meeting, we discussed the advantages of a double-edged clock versus a single-edged clock and we decided as a group that we could meet the requirements of the high-performance systems for the next-generation DRAM without needing a double-edged clock for that doubling of the performance and that we would reconsider the double-edged feature in the next generation."); Rhoden, Tr. 462).

Rambus's Response to Finding No. 631:

The proposing finding is misleading in referring to the IBM proposal in April 1992 as

"dual edge clock." (*See* RRFF 628).

632. The proposal made by IBM at the April 14, 1992 Task Force meeting eventually wound up in the DDR standard. (Rhoden, Tr. 445-446 ("The differences [between Mr. Hardell's presentation in April 1992 and the dual edge clock proposed for the DDR SDRAM ballot] was almost none. What Mr. Hardell was proposing is essentially what we ultimately wound up with in the standard for DDR."); Rhoden, Tr. 483; Kellogg, Tr. 5176).

Rambus's Response to Finding No. 632:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 628).

633. At a meeting of the JC-42.3 subcommittee held on May 24, 1995, Hyundai, Texas Instruments and Mitsubishi all made presentations relating to the Synclink technology. (JX0026 at 10-11 and 95-108 (Hyundai presentation); JX0026 at 10 and 109-110 (Texas Instruments presentation)); JX0026 at 11 and 111-112 (Mitsubishi presentation)).

Rambus's Response to Finding No. 633:

Rambus has no specific response.

634. The SyncLink presentations included proposals to use dual edge clock technology. (JX0026 at 112 ("Strobe in Reference Clock both edge for input, positive edge for output") (Mitsubishi presentation); Rhoden, Tr. 472 ("Mitsubishi was proposing here a reference clock. Both edge for input is basically, if you want to think about it, it's a dual edge input. Both edge for input and positive edge for output, they were using a combination, if you would."); Calvin, Tr. 1026-1027; Sussman, Tr. 1405, 1408; G. Kelley, Tr. 2575 ("I understood that this was proposing a new concept of double-edge clock. It was similar to the concept that we had discussed for some time called toggle mode where you use the double-edge clock on output control. This was using a double-edge clock on input control with data coming into the DRAM."); *see also* CX0711 at 156-57 (e-mail from Don Stark to all Rambus staff noting SyncLink's use of both the rising and falling edges of the clock for data input)).

Rambus's Response to Finding No. 634:

The proposed finding is misleading. As explained in the JEDEC minutes, the Synclink technology was being standardized under the auspices of the IEEE, not JEDEC, and was being brought to JEDEC simply to standardize the pinout. (JX0026 at 10).

635. Mr. Sussman's expectation was that a member with intellectual property relating to dual edge clocking should disclose that interest in response to this presentation. (Sussman, Tr.

1409).

Rambus's Response to Finding No. 635:

The proposed finding is misleading to the extent that it suggests that Rambus did not disclose intellectual property interests in the Synclink technology. To the contrary, after the Synclink presentation at JEDEC, Richard Crisp of Rambus disclosed that Rambus believed that it had intellectual property covering aspects of Synclink. (*See generally* RPF 536-48). For example, in August 1995, Mr. Crisp told a Synclink working group, whose members were mostly JEDEC representatives, that "SyncLink may violate RamBus patents that date back as far as 1989." (RX0592 at 2; RPF 542-43). At the next JEDEC meeting in September 1995, Mr. Crisp presented a statement of Rambus's position. That statement made clear that Rambus believed that its work predated Synclink and then stated:

> "At this time, Rambus elects to not make a specific comment on our intellectual property position relative to the Synclink proposal. Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property."

(JX0027 at 26). Rambus's statement was taken by JEDEC members as a warning that Rambus may have intellectual property relating to Synclink. (RPF 545-48).

636. JEDEC never standardized the Synclink architecture. (G. Kelley, Tr. 2579; Sussman, Tr. 1415).

Rambus's Response to Finding No. 636:

The proposed finding is misleading and incomplete. The Synclink architecture had not been proposed for standardization at JEDEC; only the pinout had been brought to JEDEC for standardization. (JX0026 at 10). At a JEDEC meeting on December 9-10, 1997, the SLDRAM pinout standard ballot was approved by the JC-42.3 subcommittee. (JX 41 at 22, 24; RX 1114 at 1; Rhoden, Tr. 1206-08).

637. In October 1995, JEDEC staff distributed to subcommittee members, including Rambus, a survey ballot requested at the September 1995 JC-42.3 meeting. (CX0260). The subject of the survey was "Future Synchronous DRAM (SDRAM) Features." (CX0260 at 1). Question 3.9-4 asked members whether they believed future generations of DRAMs could benefit from using both edges of the clock for sampling inputs. (CX0260 at 12 ("Does your company believe that future generations of SDRAMs could benefit from using BOTH edges of the clock for sampling inputs")). This question related dual edge clocking. (Calvin, Tr. 1033; Lee, Tr. 6689).

Rambus's Response to Finding No. 637:

The proposed finding is irrelevant because the evidence shows that a survey ballot did not trigger a disclosure obligation. (RPF 346; RRFF 339-40, 385).

638. At a meeting of the JC-42.3 Subcommittee held on December 6, 1995, the results of the survey ballot were tabulated and announced. No clear consensus on the proposed use of dual edge clock in the next generation standard was reached, with seven members responding that the next generation of SDRAMs would benefit from using dual-edge clock technology and nine members responding that it would not. (JX0028 at 45.). Two specific comments relating to dual edge clock technology were recorded in the results of the survey ballot, both supportive of using the technology. ((JX0028 at 45) ("Mitsubishi . . . Dual CLK input/output is simple and effective.") ("HP … Use positive edge for address/command & both edges for data.")).

Rambus's Response to Finding No. 638:

Rambus has no specific response.

639. At a meeting of the JC-42.3 Subcommittee held on March 20, 1996, Samsung made a presentation proposing to use dual edge clock technology in the future SDRAM standard. (JX0031 at 71 ("Future SDRAM - Proposal – Proposed Clocking Scheme … – Data in sampled

at both edge of Clock into memory … – Use both edge of the Strobe clock to sample the memory Data into Controller"); Rhoden, Tr. 512; Calvin, Tr. 1035; Landgraf, Tr. 1719-1720; G. Kelley, Tr. 2581-2582; CX2114 at 85 (Karp, FTC Dep.)).

Rambus's Response to Finding No. 639:

The proposed finding is incomplete. The Samsung presentation on "future SDRAM concepts" is not identified in the minutes as either a first showing or second showing, but simply as a "presentation." (JX0031 at 9). There is no evidence that the Samsung presentation ever progressed any further.

640. This presentation triggered disclosure under the JEDEC patent policy. (Rhoden, Tr. 514; G. Kelley, Tr. 2582; Landgraf, Tr. 1720 ("Q. Based on your understanding of the JEDEC patent policy, would a member who held patents or patent applications on dual edge clock have been required to disclose that information at this time? A. Yes, the committee had been discussing for a number of meetings what the next generation of Synchronous DRAM should be looking like and what kind of features, and a result of MOSAID's survey ballot as well as other discussions and meetings, the committee was driving towards a set of features for next generation SDRAM for higher performance, and all of these were in the direction of a proposed standard. So, all these presentations were bits and pieces that ended up into the double data rate standard.").

Rambus's Response to Finding No. 640:

The proposed finding is not supported by the weight of the evidence. To the contrary, the evidence shows that during the time Rambus was a member of JEDEC the manuals and policies of JEDEC encouraged, but did not require, disclosure of intellectual property interests. Moreover, to the extent that there was any disclosure duty it applied only to issued patent that were essential to practice a standard, and the disclosure obligation arose only at the time of balloting. (*See generally* RPF 108-317). Finally, Rambus did not have patents or patent applications that covered the Samsung presentation. (*See* RRFF 1207-19).

641. At the same meeting in March 1996, JEDEC considered running a single-edged clock faster in order to double the data rate. (JX0031 at 64; Rhoden, Tr. 542-43 (VLSI proposed

using higher speed clocks to achieve data rates of up to 300 mhz)).

Rambus's Response to Finding No. 641:

The proposed finding is not supported by the evidence. Mr. Rhoden's presentation was not a proposal for a device; it simply provided information regarding what features would be required in the future if certain clock speeds were eventually implemented (JX0031 at 64; Rhoden, Tr. 542-43). It clearly is not a proposal that single edge clocks at those speeds actually be implemented in order to double the data rate and Mr. Rhoden did not so testify.

642. During the course of its work relating to what ultimately became the DDR SDRAM standard, the JC-42.3 Subcommittee also considered, as an alternative to dual edge clocking, the use of a single edged clock. (CX0371 at 3; Lee, Tr. 6710-13 (showing and discussing two Texas Instruments presentations, one proposing to use a high-speed single-edged clock, and one proposing to use a lower speed single-edged clock with an on-chip clock frequency doubler to double the clock speed of the external clock signal).

Rambus's Response to Finding No. 642:

The proposed finding is incomplete. The use of a single edged clock as an alternative to dual edge clocking was not a viable alternative. (*See* RRFF 2325-43).

643. At the September 10, 1997, JC-42.3 meeting, the subcommittee voted to send a ballot including dual edge clocking to Council. (JX0040 at 8; Lee, Tr. 6714-6715).

Rambus's Response to Finding No. 643:

The proposed finding is not supported by the evidence which relates to a ballot involving using both edges of a data strobe, not both edges of the clock. The data strobe is not a "clock." A "clock" is a "free-running" signal, that is running all the time, while the data strobe in DDR SDRAMs is not free-running. (Macri, Tr. 4634).

644. In 1999-2000, Jedec considered interleaving SDRAM chips on the module in order to double the data rate. (CX0150 at 109-117). In December 1999, Kentron made a proposal to Jedec to interleave SDRAM chips on the module. (CX0150 at 115) ("Operate each bank with its

individual CLK . . . Provide/Sample data for every rising edge of both CLKs.").

Rambus's Response to Finding No. 644:

The proposed finding is incomplete. Interleaving banks on the module was not a viable alternative. (RRFF 2351-55).

5. Other Technologies Considered In Connection With the DDR SDRAM Standard.

(A) Externally Supplied Reference Voltage.

645. At the May 1994 JC-42.3 meeting and the March 1995 JC-16 meeting Richard Crisp of Rambus observed presentations regarding externally supplied reference voltage. (CX0711 at 25, 27; CX0711 at 52, 54).

Rambus's Response to Finding No. 645:

The proposed finding is irrelevant. (RRFF 555).

646. JEDEC included externally supplied reference voltage as an optional feature in the DDR SDRAM standard. (CCFF 564).

Rambus's Response to Finding No. 646:

The proposed finding is incorrect. Some SDRAM pinouts included an optional VREF pin, making it clear that an externally supplied reference voltage was not required for the SDRAM standards; DDR SDRAM pinouts contain a VREF pin. The proposed finding is also irrelevant. (RRFF 555, 564).

(B) Source Synchronous Clocking.

647. During the March 15, 1995 JC 42.3 meeting, Mr. Crisp recorded a Fujitsu representative's suggestion that it would be necessary to use two clocks, a clock-in and clock-out, for high speed operation. (CX0711 at 58). In an e-mail sent to Rambus executives and others, Mr. Crisp stated, "It appears that they are starting to figure out that we have a very good idea with respect to source synchronous clocking. Of course they may get into patent trouble if they do this." (*Id.*).

Rambus's Response to Finding No. 647:

The proposed finding is irrelevant. (*See* RRFF 554).

648. JEDEC included a bidirectional data strobe, or DQS strobe, as part of the DDR SDRAM standard. (CX0234 at 164). The data strobe might be considered to be a form of source synchronous clocking. (Lee, Tr. 6682).

Rambus's Response to Finding No. 648:

The proposed finding is irrelevant. (*See* RRFF 554, 564). The vague language of the proposed finding, that the data strobe *might* be considered to be a *form* of source synchronous clocking, underscores the point that source synchronous clocking is not a single well-defined technology. Complaint Counsel has made no showing that Rambus had any pending claims covering any JEDEC work relating to some type of source synchronous clocking.

6. Adoption of the DDR SDRAM Standard.

649. In August 1999 JEDEC issued Release 9 of the 21-C standard. (CX0234).

Rambus's Response to Finding No. 649:

Rambus has no specific response.

650. Release 9 expanded the original SDRAM standards to include DDR SDRAMs. (CX0234 at 143). It included programmable CAS latency and burst length as well as on-chip DLL and dual edge clocking. (CCFF 653-658)

Rambus's Response to Finding No. 650:

The proposed finding is misleading in the suggestion that the original SDRAM standards were simply "expanded . . . to include DDR SDRAMs." The DDR SDRAM standard retained some features of SDRAM (such as programmable CAS latency), changed others (such as outputting data on both edges of the clock instead of just a single edge), and added others (such as the on-chip DLL).

651. Users requested that JEDEC take everything that related to DDR out of Release 9 and put it in a separate specification. (Rhoden, Tr. 1293-1294). In response to user requests, JEDEC took all of the DDR specifications that had previously issued in Release 9 of the 21-C standard (CX0234) and put them together in one document. (Rhoden, Tr. 1293-1294). That document, entitled "Double Data Rate (DDR) SDRAM Specification" and numbered "JESD79" was published in June 2000. (JX0057; Rhoden, Tr. 1293-1294).

Rambus's Response to Finding No. 651:

Rambus has no specific response.

652. Apart from the possibility of some slight updating and clean-up, JESD79 contains the same DDR related material as in Release 9 of the 21-C standard. (Rhoden, Tr. 1294).

Rambus's Response to Finding No. 652:

Rambus has no specific response.

7. The Content of the Adopted DDR SDRAM Standard.

653. The DDR SDRAM Standard incorporated in Release 9 of 21-C and JESD79 included many features that had been previously adopted in the first generation SDRAM standard as well as new features such as dual edge clocking and on-chip DLLs. (Sussman, Tr. 1428-1429 ("Many of the features of the Synchronous DRAM are part of the double data rate Synchronous DRAM. Key items that we've added is that now the customer base, the user base, has more experience with higher edge clocks. We're using both edges of the clock rather than just a single edge. Now that we're going faster, we've added this DLL/PLL that used to be on the system board for only some of the systems. So, basically we're adding other system-level features that we know about and arguing about adding them into the component."); Gross, Tr. 2296-2297 (DDR "was an improvement and had a lot in common with the prior technology SDRAM relative to the way it was utilized to get data in and out of the device."); Peisl, Tr. 4429 ("DDR was an evolutionary concept in regards to SDR on JEDEC level. Several features of SDR had been taken over into DDR, so it was more or less a logical step for the industry committee to go from SDR to DDR and this is meant by the engineering word "easier"); McWilliams, Tr. 4822 ("DDR is perceived to be evolutionary in that it added some strobes for the data bus but preserved most of the paradigms of SDRAM."); Bechtelsheim, Tr. 5871- 5872 (DDR is "a modest design change from the original synchronous DRAM in terms of the conceptual similarity of the two designs."); CX2451 at 20).

Rambus's Response to Finding No. 653:

Rambus has no specific response.

654. All of the features included in the DDR SDRAM standard had been considered in the first generation SDRAM standard. (CX2767 at 5 ("Everything that exists within DDR was considered in the previous SDRAM generation but postponed to make sure we could keep the final cost in line with the previous technology (EDO).")

Rambus's Response to Finding No. 654:

The proposed finding is not supported by reliable evidence. In an effort to obtain a sweeping finding that finds no support in the contemporaneous documents or in any trial testimony, Complaint Counsel rely on a comment by an interested witness, Desi Rhoden, in a media interview in the summer of 2000, after Rambus had asserted its patents. It is notable that Complaint Counsel did not ask Mr. Rhoden to repeat his statement at trial, under oath and subject to cross-examination.

(A) On-chip DLL.

655. The DDR SDRAM standard requires use of on-chip DLLs. (CX0234 at 176 ("DLL Enable/Diasable Mode for DDR SDRAM/SGRAM . . . The following defines the DLL disable/enable bit in the Extended Mode Register") and at 197 ("DDR SDRAMs/SGRAMs incorporate an internal DLL (Delay Lock Loop) or equivalent circuitry to shift the output data in time such that the output data is nominally aligned with the input clock, CK."); JX0057 at 8 (Functional block diagram showing an on-chip DLL); Lee, Tr. 6643 ("Q. Based on your understanding, does the JEDEC DDR SDRAM standard require the inclusion of on-chip DLL? A. Yes"); Rhoden, Tr. 564 ("Q. So, on-chip DLL is not really a requirement for JEDEC Standard 21-C is it? A. Oh, quite the contrary, sir. It is a requirement.") and 1295; Sussman, Tr. 1427; Peisl 4391-4392)

Rambus's Response to Finding No. 655:

The proposed finding is incomplete. The inclusion of a DLL in the standard was improper because an on-chip DLL is not required for interoperability. (*See* RRFF 503). As Complaint Counsel argue, the importance of standard-setting is to ensure interoperability. (See CCFF 25-28, 114-116). Since the DLL is not required for interoperability, there was no legitimate reason for JEDEC to favor an on-chip DLL over other circuits, such as a PLL, that

could serve the same purpose. (*See* RRFF 595). Indeed, although Rambus disagrees, Complaint Counsel assert that yet other circuits, such as vernier circuits could have done just as well. (*See* CCFF 2389-99).

(B) Dual Edge Clocking.

656. The DDR SDRAM standard requires use of dual edged clocking. (JX0057 at 24; Kellogg, Tr. 5172) The JESD79 DDR SDRAM specification covers SDRAMs that have dual edge clocking. (JX0057 at 5; Sussman, Tr. 1427; Kellogg, Tr. 5172) (JX0057 at 21 ("Each subsequent data-out element will be valid nominally at the next positive or negative clock edge.").

Rambus's Response to Finding No. 656:

The proposed finding is vague. DDR SDRAM requires a particular implementation of dual edged clocking in which read data is aligned with the rising and falling edges of the clock, but write data is not. (RRFF 621).

(C) Programmable CAS Latency and Burst Length.

657. The DDR standard requires the use of programmable CAS latency and burst length. (CX0234 at 150 (mode register table includes SDRAM and DDR SDRAM CAS latency and burst length values); Geilhufe, Tr. 9742-9744; Lee, Tr. 6625)). In June 2000, JEDEC published a Double Data Rate (DDR) SDRAM Specification (JESD79), which was unique to DDR SDRAM. It continued to include a programmable mode register to define CAS latency. (JX0057 at 12 ("The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst, type, a CAS latency, and operating mode, as shown in Figure 1. The Mode Register is programmed via the MODE REGISTER SET command . . . and will retain the stored information until it is programmed again of the device loses power. . .").

Rambus's Response to Finding No. 657:

The proposed finding is vague. The DDR standard requires a particular implementation of programmable CAS latency and burst length according to which these values are programmed in specific bits of a mode register. (CX0234 at 150).

8. The Implementation of the Standard.

658. The JEDEC SDRAM and DDR SDRAM standards determined what features were required to be present in JEDEC-compliant DRAMs. (Peisl, Tr. 4384 ("JEDEC's standards were the only source for our own specifications, meaning that Infineon – Siemens or Infineon chip specifications were entirely directed towards the -- 100 percent compatibility towards the JEDEC specifications. The reason for that is very simple, because we knew that all the other industry, all the other DRAM vendors and the controller people were working towards the same specification."); CX0167 at 28 (Oh, Dep. Tr. 28 ("Q. Why do you say that [JEDEC-related trip reports are] very important? A. Again, JEDEC is the committee who decides the standards of DRAMs, so the DRAMs we are producing are standard parts, so it's very important.")).

Rambus's Response to Finding No. 658:

The proposed finding is incomplete. In fact, the JEDEC SDRAM and DDR SDRAM standards were insufficient to ensure interoperability forcing other industry participants, primarily Intel, to issue specifications used by the DRAM manufacturers in place of the JEDEC standards. (See RPF 1518-23; Krashinsky, Tr. 2814-15).

659. Paragraphs 659 - 699 are unused.

V. Rambus - Early Company History & Strategy.

A. The Founding of Rambus.

700. Company documents date the founding of Rambus Inc. to March 1990, when the company received venture capital funding from three firms. (CX0545 at 5; RX0081 at 19). By 1992, its headquarters were located in Mountain View, California, in Silicon Valley. (RX0081 at 1, 3).

Rambus's Response to Finding No. 700:

Rambus has no specific response.

701. Rambus is, and at all relevant times has been, a corporation as "corporation" is defined by Section 4 of the Federal Trade Commission Act, 15 U.S.C. § 44; and at all relevant times has been and is now engaged in commerce as "commerce" is defined in that same provision. (Rambus Answer at 5, ¶ 6).

Rambus's Response to Finding No. 701:

Rambus has no specific response.

702. Rambus was founded to solve "the memory bottleneck" – that is, the perception that existing memory designs of the time "ha[d] not kept up with the speeds of today's microprocessors." (CX0545 at 7; see also, e.g., CX0533 at 2 ("the bandwidth of the next generation of processors has far outstripped the capabilities of current memory designs"); CX1282 at 4; RX0081 at 4).

Rambus's Response to Finding No. 702:

This proposed finding is incomplete and misleading. Rambus' founders recognized that, based on then current trends and statistical analysis, computer memory performance would not be able to keep pace with anticipated processor performance advances. (See RPF 28-34). The projected gap in performance between processors and memory was not a perception it was a reality. (See RPF 35-40). Rambus was founded to commercialize a computer memory interface and protocol that would help computer memory keep pace with microprocessors. (Farmwald, Tr. 8112-13).

703. Rambus intended to achieve the goal of fixing the memory bottleneck through an "revolutionary" new memory design. (RX0081 at 2). The trademarked name given by Rambus to this "revolutionary DRAM architecture and high speed chip-to-chip data transfer technology" was Rambus DRAM or "RDRAM." (RX0081 at 3). RDRAM refers to a type of DRAM that is manufactured in accordance with specifications established by Rambus. (CX2112 at 46 (Mooring, Dep.)).

Rambus's Response to Finding No. 703:

This proposed finding is incomplete and misleading. Rambus's founders intended to improve memory performance through multiple inventions based on modifications of standard DRAMs (*see* CX533 at 2), which could be used separately or in combination(s). The greatest performance gains would be realized by using these inventions in combination. RDRAM is the name for a type of DRAM that incorporates several of Rambus' inventions, including its proprietary bus technology. Each of the various generations of RDRAM are manufactured in accordance with specifications established through a collaboration among Rambus and its DRAM partners. (Farmwald, Tr. 8149, 8241).

704. Early on, Rambus realized that it was important to its business strategy to protect the intellectual property rights to its technology. (CX0535 at 1). Part of its early strategy to do this was to pursue an application for "a basic, broad patent filed in all major industrial nations" and thereafter "follow up with additional patents on inventions created during the development of the technology." (CX0535 at 1 (November 1990 Rambus Business Plan)).

Rambus's Response to Finding No. 704:

This proposed finding is incomplete and misleading. CX0535 makes clear that Rambus recognized that, in order to protect its intellectual property rights, it was also important to enter into non-disclosure agreements with companies exposed to its technology. (*Id*. at 1).

705. The only business model that "made any sense" to Rambus co-founder Michael Farmwald "was to patent the technology, convince others to build the device, and charge them royalties." (Farmwald, Tr. 8095; CX2106 at 26 (Farmwald, Dep.) ("When we were first formed, it was my view that we could not possibly raise enough money to build DRAMs. DRAM fabs

cost, even back then they cost, order of a billion dollars. You couldn't really build DRAMs without owning your own fab, and so a business plan which involved actually building and selling DRAMs was hopeless, and so from the very beginning we were a royalty-based company.")).

Rambus's Response to Finding No. 705:

The proposed finding is contradicted by more reliable evidence and is misleading because it leaves out relevant evidence. At the time Rambus was founded Mr. Farmwald estimated that a DRAM fabrication plant would cost half a billion dollars. (Farmwald, Tr. 8095). Mr. Farmwald recognized that is was unlikely that two university professors could acquire the funding necessary to construct a DRAM fabrication plant. (*Id.*)

706. The objective of Rambus, as framed in 1989, was not merely to secure patent rights over widely adopted DRAM industry standards, but to "Make A Lot Of Money At The Same Time." (CX1282 at 5). Rambus intended to achieve this objective, while avoiding the costs of chip fabrication, by charging royalties and license fees for the use of its technology. (*Id.* at 22 ("Nearly All Income in Form of Royalties").

Rambus's Response to Finding No. 706:

This proposed finding is incomplete and misleading. The cited statements in this proposed finding are taken from a very early marketing presentation to potential investors. Rambus' primary objective was to commercialize the revolutionary inventions Drs. Farmwald and Horowitz had created in the form of an open industry *de facto* standard, and to ensure that the standard "didn't go off in incompatible directions." (Farmwald, Tr. 8148). Rambus contemplated that it would earn its income by working with DRAM companies to implement the Rambus interface in their products, and, for that work, get paid consulting fees (for the time its engineers spent working with partners) and royalties for the use of Rambus's intellectual property that would be incorporated into DRAM companies' products. (Farmwald, Tr. 8150). To become

and remain a viable company, Rambus had to make money, but all along it intended to charge low single digit royalties, which it believed to be fair in light of the importance of Rambus's intellectual property contribution to the product and the large size of the DRAM market. (Farmwald, Tr. 8128).

707. Rambus founder Farmwald knew that "companies never like to pay royalties if they can get out of it." (CX2106 at 27 (Farmwald, Dep.) ("Rambus was and has always been a royalty-based company, a company that was going to charge royalties. I knew that people would not lightly pay royalties. The DRAM business is a very big business.")).

Rambus's Response to Finding No. 707:

This proposed finding is incomplete. Mr. Farmwald explained that it was his belief that companies don't like to pay royalties unless "they have to." (Farmwald, Tr. 8249).

708. At the outset, the strategy was to become an industry standard. The founders of Rambus recognized that this plan was not without risks. Two "Risks" in particular identified in the June 1989 Rambus business plan were:

> Need to Establish RamBus as a standard . . .
> Income Depends Mostly on Royalties

(CX1282 at 27). The founders recognized that these two considerations were linked. Thus, its early business planning recognized that "RamBus must be established as a standard to effect large royalty payments." (CX0533 at 19).

Rambus's Response to Finding No. 708:

This proposed finding is incomplete and misleading and leaves out relevant evidence. Rambus's goal was to become an open, *de facto* standard through wide industry acceptance. (Farmwald, Tr. 8110; 8125-26). At the outset, Rambus did not contemplate standardization through a formal standard-setting organization. (*Id*.).

709. The founders also recognized that, once the DRAM industry had adopted a standard, there were strong barriers to change or entry. (RX0015 at 15 ("Once a DRAM or vendor has committed to an architecture unlikely to change."); *id*. at 9 ("The DRAM industry's

penchent for standardization combined with the RamBus marketing strategy of licensing all the major vendors make it extremely unlikely that any potential competitor would be able to gain critical mass enough to challenge an already established and ubiquitous RamBus chip.")).

Rambus's Response to Finding No. 709:

The proposed finding is incomplete and misleading. First, the "adoption of a standard" referred to in the proposed finding is the *de facto* "adoption of a standard" not adoption through a formal standard setting organization. (Farmwald, Tr. 8125-26). Second, the strongest barrier to entry recognized by the Rambus founders was not the mere adoption of its technology, but rather the tremendous advantages its technology offered: "RamBus technology provides several strong barriers to entry for potential competitors, the strongest of which are its patent and the overwhelming 'unfair' advantage its technology enjoys because a RamBus-based DRAM memory is much faster, denser, lower power and cheaper than any other approach." (RX0015 at 9; *see also* Farmwald, Tr. 8121-22).

B. Funding the Start-Up.

710. In an effort to receive funding for the start-up of what would become Rambus Inc., the founders approached various venture capital firms: Kleiner Perkins (KPCB), one of the largest venture capital firms in the world; Merrill Pickard Anderson and Eyre (MPAE); and Mohr Davidow. (Farmwald, Tr. 8099). As part of meetings with the venture capital firms, the founders prepared presentations and showed them documents, such as early business plans. (Farmwald, Tr. 8100). These meetings occurred around the time of a June 1989 RamBus Business Plan (CX0533). (Farmwald, Tr. 8100-8101; CX0533 (also included in record as RX0015 and CX0570)).

Rambus's Response to Finding No. 710:

Rambus has no specific response.

711. The start-up had significant "financial considerations" and according to the June 1989 business plan, "RamBus" founders (Mr. Farmwald, Mark Horowitz, and James Mannos), were only able to invest $75,000 in "seed money" and were seeking an additional $1.5 million in equity investment. (CX0533 at 4). This amount would only fund the company through "the

completion of a prototype and to the development of [its] initial DRAM vendor partnerships." (CX0533 at 4). Until it signed its revenue producing partners, estimated expenses were $100,000 per month. (CX0533 at 5).

Rambus's Response to Finding No. 711:

The proposed finding is not supported by the evidence and is contradicted by other evidence. Jim Mannos was not a founder of Rambus. He was a part-time employee who was at one point being considered as a Vice President. (Farmwald, Tr. 8301, 8131-32). There is no evidence supporting the assertion that he contributed any "seed money" or any other funds to Rambus.

712. In a meeting with one of the venture capital firms, co-founder Michael Farmwald noted that "much depends on getting a standard which depends upon our patents." (CX1702 at 3 (emphasis in original); Farmwald, Tr. 8130-31).

Rambus's Response to Finding No. 712:

This proposed finding is incomplete and misleading. The statement in Mr. Farmwald's notes was not his statement, but rather one made by an Intel attorney. (Farmwald, Tr., 8133-35). Moreover, the Intel attorney's use of the word "standard" did not refer to a formal industry standard. It referred to a *de facto* standard that would become the "most common part" or "default part that people would use." (Farmwald, Tr. 8135-36).

713. In March 1990 Rambus Inc. was born when it finally received venture capital funding of $1.86 million from three firms. (CX0545 at 5; RX0081 at 19).

Rambus's Response to Finding No. 713:

This proposed finding is suggestive of facts not supported by the evidence. The use of the phrase "finally received" suggests some delay in Rambus' ability to acquire funding, which is not supported by the cited evidence nor by any other record evidence.

C. The Basic Rambus Technology.

714. Because from the start the founders believed that "[r]oyalties are the lifeblood of Rambus" (CX2106 at 220 (Farmwald, Dep.)), Rambus placed great importance on promoting and protecting its proprietary technology. The Rambus founders "felt we had a very significant invention. We felt that the only way to protect and to extract value from that invention was to patent it." (CX2106 at 27 (Farmwald, Dep.)).

Rambus's Response to Finding No. 714:

Rambus has no specific response.

715. Rambus saw its proprietary RDRAM technology as offering dramatic improvements over existing memory technology of the time. In 1992 it claimed that RDRAM technology "achieves a ten-fold increase in component throughput" and would result in "dramatically increasing system price/performance." (RX0081 at 3). In addition, Rambus claimed that use of the RDRAM technology "assures a smaller system with fewer components, and provides the user with a modular, scalable solution." (*Id.*).

Rambus's Response to Finding No. 715:

Rambus has no specific response.

716. The high-speed chip-to-chip data transfer RDRAM technology was intended to be used not only in memory chips themselves, but also to be implemented in other chips including memory controllers, processors, graphics/video chips and other high performance components used in virtually every computer system. (RX0081 at 3). The proprietary Rambus technology was targeted at mainstream applications from consumer digital video products through desktop computers and graphics up to massively parallel computers. (*Id.*).

Rambus's Response to Finding No. 716:

Rambus has no specific response.

717. Central to the RDRAM technology was the use of a "narrow, high speed bus" to connect chips and speed the transfer of signals and data between them. (RX0081 at 3, 7). This narrow bus was "a precisely specified, physical and electrical interconnect" between the chips. (*Id.* at 7). The use of a narrow, high-speed bus to carry data between chips is the "basic notion" of the proprietary RDRAM technology (Horowitz, Tr. 8618), and is a characteristic that distinguishes the technology from other memory technologies. (Rhoden, Tr. 400).

Rambus's Response to Finding No. 717:

The proposed finding is inaccurate, misleading and not supported by the evidence. The RDRAM technology in the early 1990s included numerous inventions relating to the bus, the interface between the bus and computer chips, and the DRAM. (RPF 59-71). The 1992 Corporate Backgrounder cited in the proposed findings itself makes clear that the "Rambus solution is comprised of three main elements: the Rambus Channel, the Rambus Interface, and the RDRAM." (RX0081 at 6.) The Rambus Channel refers to the bus, while the Rambus Interface and RDRAM refer to other Rambus innovations separate from the bus. (RX0081 at 7.) Each of these categories themselves contain a number of independent inventions. (RX0081 at 8-11) The quote from Mr. Horowitz's testimony is misleading. The quoted language from Professor Horowitz's Infineon trial testimony referred to the "basic notion" with respect to a particular exhibit from the Infineon trial which Complaint Counsel have not made part of the record here, not the basic notion of Rambus technology. (Horowitz, Tr. 8619 (quoting the question "With respect to Exhibit 911, what was the basic notion?")). Even with respect to this exhibit, Professor Horowitz's answer indicated that many more "basic" notions were involved than just a high speed bus. In response to the question, Mr. Horowitz noted that the "basic idea" was to "change the interface of the DRAMs" and that he had to use various techniques to "make the wires high speed." (Horowitz, Tr. 8619). Because those techniques were expensive, Mr. Horowitz tried to make do with as few wires on the bus as possible. (Horowitz, Tr. 8618-19). Contrary to the proposed finding, Mr. Horowitz made clear that the high speed bus was just one of many Rambus innovations that served to distinguish Rambus technology from other memory technology at the time it was being developed. (RPF 59-71).

718. The typical synchronous DRAM uses a large number of dedicated lines to carry control, address and data signals between the memory controller and the memory chip. (Rhoden, Tr. 401). Control signals specify whether data is being written to or read from the memory; address signals specify the portion of the memory chip that is being accessed; data signals specify the content that is being written to or read from memory. (Rhoden, Tr. 280-82). A typical synchronous DRAM bus contains 100 to 120 parallel lines that are dedicated to carrying control, address and data signals respectively between the memory controller and memory chip. (Rhoden, Tr. 401).

Rambus's Response to Finding No. 718:

The proposed finding is contradicted by more reliable evidence. The first published SDRAM standard showed a pinout for three different configurations of SDRAM. (JX0056 at 106.) The x4 configuration shown had 11 address lines (A0-A11), 4 data lines (DQ0-DQ3), and 5 control lines (W, CE, RE, S, DQM, and CKE, where CE is equivalent to CAS and RE to RAS), for a total of 21 bus lines. (JX0056 at 106; *see* JX0056 at 18-22 (identifying the pin designations)). The remaining pins consist of a clock pin, power pins and "no connect" pins. (*Id*.) The x8 configuration added four data lines, bringing the total of bus lines to 25. (JX0056 at 106.) The x9 configuration added an additional data line, bringing the total number of bus lines to 26. (JX0056 at 106.) No configuration of SDRAM with more than 26 bus lines is shown in the standard as initially published in November 1993. (JX0056).

719. By contrast, the RDRAM technology uses a small number of very high speed signals to carry all address, data and control information. (RX2183 at 5). As originally implemented, the RDRAM technology used a narrow bus of only eight lines to carry control, address and data signals between the memory and controller. (Rhoden, Tr. 400-401). In later implementations of the RDRAM technology, this was widened to a bus of sixteen lines (Farmwald, Tr. 8190).

Rambus's Response to Finding No. 719:

The proposed finding is inaccurate and misleading. The proposed finding purports to "contrast" RDRAM technology with SDRAM based on the number of bus lines. However, as

originally implemented, the RDRAM technology used a total of 10 bus lines. (RX0130 at 13 (noting that the Rambus interface contains 15 signals including 10 bus lines (BusData0 - BusData8 and BusCtrl) in addition to clock, power and reset signals)). A later version of RDRAM, known as "Direct RDRAM" used 24 bus lines – 16 data bus lines and 8 control/address lines. (Rhoden, Tr. 541 (press has reported that Direct RDRAM has a separate, 16-bit wide data bus separate from the address and control bus); RX1030 at 3 (Direct RDRAM has 2 byte (16 bit) data bus and 8 bit control bus)). As noted above in Rambus's response to proposed finding 718, the number of bus lines in the initial configuration of SDRAM ranged from 21 to 26, in the same range as certain RDRAMs.

720. In implementing the narrow bus, RDRAM technology contemplates the use of circuitry on the chips at either end of the bus connection to optimize the signals flowing across the connection. (Horowitz, Tr. 8488-90). This circuitry contains high-level logic which implements a protocol for the chip-to-chip information transfer. (RX0081 at 7; Horowitz, Tr. 8489-90).

Rambus's Response to Finding No. 720:

The proposed finding is misleading in its use of the term "narrow bus." "Narrow bus" is a relative term and, as noted in response to proposed finding 719, some versions of RDRAM have roughly the same number of bus lines as some versions of SDRAM.

721. One of the ways that RDRAM technology achieves a high-speed data transfer over the narrow bus is through "multiplexing," which means that the bus can carry different pieces of information at different points in time. (Horowitz, Tr. 8620). This aspect of the RDRAM interface protocol means that over several clock cycles the bus can carry a combination of address and control and data signals on one or more of the same bus lines. (Horowitz, Tr. 8620-21). (See Rhoden, Tr. 402-03).

Rambus's Response to Finding No. 721:

The proposed finding is inaccurate. As noted above in Rambus's response to proposed

finding 665, certain versions of RDRAM have a separate data bus so that data signals are not carried on the same bus lines as address and control signals.

722. Another aspect of the RDRAM technology is the use of a "packetized" data transfer protocol. (Horowitz, Tr. 8621; Rhoden, Tr. 403-405). This term means that information is bundled and the bundle may be sent over multiple clock cycles rather than transmitted all at once. (Jacob, Tr. 5465; Rhoden, Tr. 404).

Rambus's Response to Finding No. 722:

Rambus has no specific response.

723. The RDRAM technology also contains other distinctive aspects, including a clocking system sometimes referred to as a loop clock to assist in controlling the synchronization of the data transfer between chips (Rhoden, Tr. 404; Horowitz, Tr. 8647), and a method of physically packaging the RDRAM memory chips so that multiple chips could be vertically mounted on one another to occupy a small space (Horowitz, Tr. 8623).

Rambus's Response to Finding No. 723:

The proposed finding is incomplete. When first developed, RDRAM technology contained numerous other distinctive aspects including, but not limited to, the use of registers on the DRAM to store latency values, a variable burst length for data transfers, dual edge clocking in a synchronous memory device, and on-chip DLL or PLL. (RPF 59-71).

724. The RDRAM technology was sufficiently distinctive that it was widely considered "revolutionary" in the industry and was promoted as such by Rambus. (Farmwald, Tr. 8113-14, 8148, 8304-05, 8463-65; Horowitz, Tr. 8571; Gross, Tr. 2291, 2295-96, 2326; Heye, Tr. 3686-87; MacWilliams, Tr. 4822; Bechtelsheim, Tr. 5817, 5845; Tabrizi, Tr. 9138).

Rambus's Response to Finding No. 724:

The proposed finding is vague in it use of the term "revolutionary," which, as Complaint Counsel's economics expert testified, is a relative term. (*See* RRFF 127).

D. The Basic Rambus Patent Application.

725. Rambus filed patent application serial no. 07/510,898 (the '898 application) in the

U.S. Patent and Trademark Office on April 18, 1990. (CX1451 at 001-02; Nusbaum, Tr. 1507). The '898 patent application included a descriptive portion, called the "specification," that was 62 pages long and included 15 original drawings. (CX1451 at 3-63, 140-150; Nusbaum, Tr. 1496-97). The '898 patent application contained 150 original claims. (CX1451 at 64-125).

Rambus's Response to Finding No. 725:

The proposed finding is misleading. The specification and the written description of a patent application are not coextensive. The specification has a written description setting forth a legally sufficient description of the claimed invention. The specification also has claims that define (or will define if issued without revision) the boundaries of the patentee's right to exclude others from making, using, selling, or offering to sell the claimed invention for a limited period of time. (*See* 35 U.S.C. § 112, ¶ 2 ("The specification shall conclude with one or more claims . . . .")).

726. In addition to this basic United States patent application, Rambus pursued foreign applications in a number of countries based on the '898 application. (See CCFF 1115-21, 1669-75).

Rambus's Response to Finding No. 726:

Rambus has no specific response.

727. Despite the stated strategy of seeking "a basic, broad patent" (CX0535 at 1), the specification portion of the United States '898 patent application described the "present invention" as a narrow, multiplexed bus structure. (CX1451 at 9-10, 14; Jacob, Tr. 5461-63; Nusbaum, Tr. 1642-43). (See discussion at CCFF 1283 et seq.). Rambus employee Richard Crisp, its representative to JEDEC from 1992 to 1996, read this original patent application in the early 1990's and believed that it was intended to describe the RDRAM system invention, and that it was limited to the proprietary RDRAM technology. (Crisp, Tr. 2927-28).

Rambus's Response to Finding No. 727:

The proposed finding is misleading in its implication that that the description of the "present invention" in the '898 application is inconsistent with it leading to a "basic, broad

patent." Indeed, the Federal Circuit considered the precise language regarding the "present invention" in Rambus's patent specification that Complaint Counsel cite. *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094 (Fed. Cir. 2003). The Federal Circuit concluded that, when considered in the context of the specification as a whole, that language did *not* serve to limit the scope of the claims that were supported by the specification. (*See* RRFF 1284). The Federal Circuit further held that "a multiplexing bus is only one of many inventions disclosed in the '898 application." (*Infineon*, 318 F.3d at 1095). The proposed finding is also incomplete. While Mr. Crisp initially believed that the application was limited to Rambus technology, his view changed upon further review. (Crisp. Tr. 2927-28.)

728. Rambus recognized the possibility that its pending patents would not issue, or would not issue with claims sufficiently broad in scope to block others. (CX0533 at 19 ("Potential Risks and Problems . . . Will patent be enforceable and broad enough to stop imitators.")). But this risk was of less concern to the Rambus founders, who from very early on – based on input from their attorneys – possessed a high degree of confidence in the likelihood of the patents issuing "largely as filed." (CX0535 at 3 ("The base patent was filed in April of 1990. It has been reviewed by all partners who've signed and several others and found to be a strong, broad patent with high odds of being issued largely as filed."); *see also* CX1702 at 3 (1989 notes of founder Michael Farmwald recording comments of a patent attorney who "says 'he takes adequate patent coverage as a given' & says that if we do the job right it will be very hard to get around")).

Rambus's Response to Finding No. 728:

The evidence does not support the proposed finding regarding the Rambus founders purported "high degree of confidence." Complaint Counsel cites CX0535, a business plan that was not prepared by Rambus founders, Drs. Farmwald and Horowitz. (Farmwald, Tr. 8302-03.) Complaint Counsel also cites Mr. Farmwald's notes of a comment by a patent attorney, not Rambus's attorney at the time, based on a presentation of Rambus technology well before Rambus's first patent application was filed. (Farmwald, Tr. 8131-34). There is no evidence to

support the proposed finding that this comment gave Drs. Farmwald and Horowitz a "high degree of confidence" that, when they eventually did file a patent application, it would issue "largely as filed."

729. In connection with the prosecution of its '898 patent application, Rambus was issued a communication by the patent examiner at the United States Patent Office containing a restriction requirement. (Nusbaum, Tr. 1511). A restriction requirement reflects that the examiner has reviewed the application and determined that the application contains claims describing multiple claimed inventions; the applicant is required to required to elect which of the claimed inventions it wishes to pursue in the application. (Nusbaum, Tr. 1510). The restriction requirement received by Rambus was an 11-way restriction requirement; Rambus responded by restricting its original application and filing ten divisional patent applications on March 5, 1992, all of which claimed priority based on the filing date of the original '898 application, April 18, 1992. (Nusbaum, Tr. 1511-12; First Stipulations, No. 22, Exhibit A; DX14).

Rambus's Response to Finding No. 729:

Rambus agrees with this proposed finding in the most part, except that a restriction requirement reflects not simply that the application contains claims to multiple inventions, but, rather, that the application contains claims to multiple "*independent and distinct* inventions." (35 U.S.C. § 121 (emphasis added)).

730. Over time, Rambus filed numerous additional continuation and divisional patent applications claiming priority based on the filing date of the original '898 application. (First Stipulations, No. 22, Exhibit A). Prior to June 1996, Rambus filed a total of seventeen continuation and divisional patent applications claiming priority based on the filing date of the original '898 application, and had been issued six United States patents on such applications. (*Id.*). As of April 2003, Rambus had filed sixty-three continuation and divisional patent applications claiming priority based on the filing date of the original '898 application, of which ten were still pending. (*Id.*). As of April 2003, at least 43 United States patents had been issued to Rambus from continuation and divisional applications claiming priority to the original '898 application. (First Stipulations, No. 13).

Rambus's Response to Finding No. 730:

Rambus has no specific response.

731. Over time, various of the Rambus continuation and divisional patent applications

claiming priority to the '898 application embodied changes and amendments to the claims made in the original '898 application and came to describe aspects of the original invention in ways that were not limited to the proprietary RDRAM technology. (See, e.g., Crisp, Tr. 2927-28). By 2000, Rambus had secured several patents, issued on the basis of continuation and divisional applications claiming priority to the original '898 application, which it asserted against manufacturers of JEDEC-standard SDRAM and DDR memory chips. (See, e.g., First Stipulations, No. 14-16 (August 2000 infringement suit by Rambus against Infineon was based on 56 claims of 4 patents claiming priority to the '898 application)).

Rambus's Response to Finding No. 731:

The proposed finding is misleading in its implication that Rambus's patent claims were originally limited to "proprietary RDRAM technology" and then later were not so limited. Complaint Counsel is drawing a distinction that does not exist. The claims of the '898 application, as originally filed, claimed certain aspects proprietary Rambus technology many of which were incorporated into RDRAMs. None of the original claims were, however, "limited" to RDRAMs in the sense that none of the claims contained as limitations all of the features that would be found in an actual RDRAM device. Rather each claim involved a certain subset of those features. To the extent that another party later appropriated one of those claimed inventions and used them in a device other than RDRAM, it would be infringing Rambus's intellectual property. Later patents that had claims involving programmable latency, variable burst, dual edge clocking and on-chip DLL (generally in addition to other limitations) similarly claimed proprietary Rambus technology that had been incorporated into RDRAMs. These inventions could also be used, and many have been used, in other devices such as SDRAM and DDR SDRAM memory chips.

E. Promoting Rambus RDRAM Technology as the DRAM Standard.

732. The Rambus founders recognized that the characteristics of the DRAM industry made for the possibility of a lucrative payoff for the company. Early Rambus investors were

informed that "[t]he primary business of the RamBus Company" would be to license proprietary technology "to manufacturers of DRAM chips and microprocessors;" that "[t]he DRAM market is . . . highly sensitized to the concept of standardization;" and that Rambus possessed "the ability to set world wide standards for the next generation of DRAM chips and memory subsystems." (CX0533 at 9).

Rambus's Response to Finding No. 732:

This proposed finding is incomplete and misleading, and unsupported by the evidence. Rambus hoped and expected to be "highly profitable" but neither the phrase "lucrative payoff" nor any negative connotations that may be associated with that phrase is found in the cited text. (CX0533 at 9). Second, the document cited does not state that "Rambus possessed the 'ability to set world wide standards for the next generation of DRAM chips and memory subsystems,'" but rather that the market conditions were such that "there is the ability to set world wide standards for the next generation of DRAM chips and memory systems." (*Id.*). The purpose of this early business plan (which, in addition to being early, was a draft), was to encourage investment by explaining to investors why Rambus' technology would enable it to be successful in the existing and future DRAM market. (*See generally* CX0533 at 9-10). Fundamentally necessary to Rambus's belief that it was indeed worthy of investment was that its technology was far superior and more economical than any other approach. (*Id.*)

733. Investors were told that "the patented RamBus technology . . . has the opportunity to establish a single high performance DRAM standard"; that in part due to "[t]he DRAM industry's penchent [sic] for standardization," once the Rambus technology was licensed to "all major vendors," it would be "extremely unlikely that any potential competitor would be able to gain critical mass enough to challenge" Rambus; and that such considerations, including the existence of "strong barriers to entry" by "potential competitors," made Rambus an "exceptionally attractive investment opportunity." (CX0533 at 9).

Rambus's Response to Finding No. 733:

This proposed finding is incomplete and misleading. As explained in response to

proposed findings 709 and 732, Rambus' business model was not premised solely on the market conditions amenable to the establishment of a standard (a *de facto* standard, that is, in any event). The strength of Rambus's business model depended also on the strength of its technological innovations. Indeed, Rambus's early filed broad patent application and the "unfair" advantage its technology was seen to enjoy by virtue of being "faster, denser, lower power and cheaper than any other approach" were touted to investors as the most significant barriers to entry for potential, follow-on competitors. (CX0533 at 9). It was the "stiff competition" presented by Rambus innovative technology as well as its marketing strategy of licensing all of the major vendors" that it claimed made it less pervious to competitors than other potential investment opportunities. (*Id*.)

734. In its early planning, Rambus executives recognized that the company faced a sort of chicken-and-egg problem – namely, "Most computer companies will want to wait until RamBus DRAMs are easily available," whereas "DRAM and CPU companies need to be convinced that computer builders will use it." (CX1282 at 27). Rambus intended to deal with this in part through the terms upon which it licensed its technology. Rambus recognized that there was a "trade-off of royalty size vs. incentive to develop alternatives" to the Rambus technology (CX0533 at 14), and initially intended to offer licenses at "low enough royalties to discourage 'rolling your own.'"(CX0533 at 15). However, early planning suggests that once Rambus was established as an industry standard, Rambus intended to charge larger royalty payments. (CX0533 at 19 ("RamBus must be established as a standard to effect large royalty payments.")).

Rambus's Response to Finding No. 734:

This proposed finding is contrary to the weight of the evidence. For this proposed finding, Complaint Counsel has done nothing more than selectively quote phrases from various unrelated documents in an attempt to manufacture facts by juxtaposing them in a suggestive manner. This is argument, not a finding of fact. For example, there is no connection in the cited documents or in the record evidence between the risk factors presented at p. 27 of CX1282 and

Rambus' setting of its royalty rates. Moreover, CX0533 at 19 far from evidencing Rambus's intention to increase its royalty rates once the industry had adopted its technology as a standard (again, the use of the term "standard" connotes *de facto* standardization, not standard setting by a formal body), makes clear that the phrase "large royalty payments" referred to obtaining a large share of the market at low royalty rates, which would overall result in large royalty payments. As Dr. Farmwald testified:

> Q: And when you said here "large royalty payments," what did you have in mind in this time frame?
>
> A: All along we wanted to have sort of single-digit – lowish single digit royalties. We thought that was reasonable and fair given sort of our contribution to the thing. But he DRAM market as a whole is very large.
>
> So, that's what we meant. *It's a relatively small number times a fairly large market*.

(Farmwald, Tr. 8128) (emphasis added).

735. Rambus hired its first (and to date only) CEO – Geoffrey Tate – who joined Rambus in May 1990. (CX0545 at 5). Shortly before arriving on the job as the Rambus CEO, Mr. Tate set forth on paper some of his own strategic thinking for the company. (CX2073 at 52 (Tate, Dep.)) Mr. Tate recorded, among others, each of the following thoughts:

> "RAMBUS has a potential for a very strong value-added in a large number of high-volume systems applications combined with a strong barrier-to-entry in the form of a broad patent;"
>
> "There are always ways to get around any patent is the assumption that we should make;"
>
> "If RAMBUS can be seen as a standard . . . it may be very difficult for second solution to develop critical mass in the marketplace;" and

> a "high priority" for RAMBUS should be "to avoid a contending standard from developing."

(CX0569 at 3).

Rambus's Response to Finding No. 735:

This proposed finding is incomplete and misleading in its selective, out-of-context quotation of portions of Mr. Tate's notes. With regard to the second quotation of this proposed finding, Mr. Tate notes that in the case of Rambus, any "ways to get around any patent" are likely to be inferior and/or not successful. (CX0569 at 3). With regard to the third quotation of this proposed finding, the omitted text represented by ellipses is important to put this statement in context, it its entirety, the sentence reads: "If RAMBUS can be seen as a standard and if a large amount of industry momentum is brought onto the RAMBUS bandwagon that can get things to the point where it may be very difficult for a second solution to develop critical mass in the market place." (*Id.*). Clearly, Mr. Tate understood that widespread use as a *de facto* standard would not necessarily be sufficient to hold off competitors, and that Rambus also needed to develop "a large amount of industry momentum." As explained in response to several proposed findings above, Rambus' use of the term "standard" was in reference to a *de facto* standard by virtue of widespread industry use, not a formalized standard. (Farmwald Tr., 8110; 8125-26).

F. Rambus Efforts to License RDRAM Technology.

736. By the time of a November 1990 business plan prepared by Rambus CEO Tate and discussed with the Rambus Board of Directors. (CX2073 at 85, 87 (Tate, Dep.)) Rambus had set out plans for a phased licensing and promotion of the Rambus proprietary RDRAM technology. At an early stage, Rambus would establish "partnerships" with a small number of semiconductor companies to develop new chip products embodying the RDRAM technology, by persuading them that the quality of the RDRAM technology could give them a competitive advantage over other semiconductor companies. (CX0535 at 1). Rambus also would seek to develop relationships with key systems companies to commit to introducing systems using chips

with the RDRAM technology. (*Id.* at 1-2). Later, the RDRAM technology would be announced publicly "in a big way" when a "critical mass" of partnerships was in place and there had been technical demonstration of the RDRAM technology. (*Id.* at 2). Follow-on licenses then would be sought with other semiconductor and systems companies. (*Id.*).

Rambus's Response to Finding No. 736:

This proposed finding is incomplete and misleading. CX0535 makes clear that Rambus' business strategy was concerned, first and foremost, with developing a high bandwidth technology that would be a very high value technology of interest to most semiconductor and systems companies. (CX0535 at 1). Accordingly, insofar as establishing early partnerships was concerned, there is no indication in the cited evidence that Rambus intended to or felt it would need to forge these partnerships "by persuading [semiconductor companies] that the quality of Rambus' technology could give them a competitive advantage." Rather, the cited evidence makes clear that persuasion would not be necessary – the early partnerships would be forged with those semiconductor companies "who see early access to the technology as a means to gain market share against their competitors and so who plan to aggressively implement the technology on their volume products." (*Id.*). The proposed finding omits mention of other aspects of Rambus' strategy related to its licensing efforts, i.e., that Rambus' strategy also involved protecting the intellectual property rights to this technology though patents and non-disclosure agreements and by restricting any licenses to the technology to specific uses of the technology. (*Id.*)

737. The 1990 business plan recognized that if the Rambus royalty demands for its RDRAM technology were perceived as unreasonable, this might motivate potential licensees to "work around" Rambus patents, in order to avoid paying royalties. (CX0535 at 2 (expressing concern that license fees and royalty rates not be set "so high as to create high motivation to work around them").

Rambus's Response to Finding No. 737:

This proposed finding is incomplete and misleading. While desiring to keep its royalties in the low single digits, (Farmwald, Tr. 8128), Rambus also believed that it would be difficult for a competitor to offer a reasonable product that did not infringe its patent(s). (CX0569 at 3).

738. In order to prevent the development of competitive technology, Rambus strategy was among other things to take care in its efforts to promote its proprietary RDRAM technology. In its promotion efforts, Rambus in 1990 resolved to "sign non-disclosures with all parties exposed to the technology" and "only license partners to use the technology in a specific manner specified by Rambus." (CX0535 at 1). The result, it hoped, was to make it "impossible or very difficult for anyone to develop a competitive technology to Rambus." (*Id.*).

Rambus's Response to Finding No. 738:

The proposed finding is incomplete and misleading. Rambus had neither the intentions nor the ability to "prevent" the development of competitive technology; at best, it sought to make it "impossible or very difficult for anyone to develop a competitive technology," by safeguarding its intellectual property. As explained in response to proposed finding no. 737, it sought to protect the intellectual property rights to its technology "through a basic, broad patent filed in all major industrial nations and follow up with additional patents on inventions created during the development of the technology." (CX0535 at 1). Also as explained in response to proposed finding no. 737, the foundation of this strategy was the development of "a very high value technology of interest to most Semiconductor and Systems companies." (*Id.*)

The proposed finding also supports Rambus's position that the DRAM industry was not lulled. By limiting its licensees to very specific uses of its intellectual property, Rambus made clear that there were other potential non-compatible uses of its inventions, i.e., uses of its inventions that did not require the use of Rambus's proprietary bus architecture. (*See* Farmwald,

Tr. 8148 (explaining how it was important to keep control of Rambus' inventions so they did not go off in incompatible directions)).

739. By November 1990, Rambus had already begun its efforts to promote and protect its technology. (CX0535 at 4-5). At that date Rambus had filed for, but not yet obtained, a base patent on its technology (*id.* at 3) and had entered into license contracts that compelled partners to use Rambus technology patents and trade secrets only for use in RDRAM-compatible chips (*id.* at 4).

Rambus's Response to Finding No. 739:

The proposed finding omits relevant information. After stating that the original patent application was filed in April of 1990 the cited document continues: "It has been reviewed by all partners who've signed and several others and found to be a strong, broad patent with high odds of being issued largely as filed." (CX 0535 at 3).

The proposed finding is also unclear and potentially misleading. The original Rambus patent application disclosed numerous inventions. While the originally filed application disclosed all of these inventions, not all of the inventions were adequately protected by the original 150 claims. Therefore, to the extent the use of the language "a base patent on its technology" implies that the original 150 claims adequately described the scope of the disclosure of the inventions set forth in the written description, it is incorrect and misleading.

The proposed finding supports Rambus's position that the DRAM industry was not lulled. By circumscribing the use of its inventions to Rambus-compatible products only, Rambus made it clear that there existed potential non-compatible uses of its inventions, i.e., uses of its inventions that did not require the use of Rambus's proprietary bus architecture.

740. By June 1992, Rambus had signed license agreements with NEC, Toshiba and Fujitsu. (CX0543A at 11). By January 1994, Rambus had signed license agreements with Hitachi, Oki, Lucky Goldstar and Intel. (CX0547 at 12).

Rambus's Response to Finding No. 740:

The proposed finding omits relevant information. The licenses discussed in the cited references were technology license agreements for Rambus-compatible uses of Rambus' inventions. These agreements, as opposed to patent license agreements, were more like joint venture agreements which involved substantial interaction between Rambus and the licensee. (RPF 1401-1402; Farmwald, Tr. 8241).

741. In the course of negotiating with DRAM manufacturers and others, Rambus encountered resistence to its business model, and specifically to the amount of the royalties. (CX0543A at 14 (identifying Sun and Tseng as specific examples); CX0711 at 13 ("Terry Walther of Micron . . . Said they are very nervous about doing a deal. Don't like license type business he says."); CX0711 at 61 ("Farhad [Tabrizi] . . . says their #1 issue with the Rambus business proposal is the royalty rate.")).

Rambus's Response to Finding No. 741:

This proposed finding is incomplete and misleading. The cited evidence reads: "A few systems companies and IC companies have had a very negative reaction to our business model. Some believe that it is not 'fair' that we are wanting to charge a royalty on ICs that incorporate our technology. Others believe our royalty will make ICS incorporating our technology 'too expensive'. Two specific examples are Sun and Tseng." (CX 0543A at 14). This text, as well as the other cited evidence makes clear that it was the imposition of any royalty, as opposed to the amount of Rambus's royalties, that DRAM manufacturers found objectionable.

The cited text goes on to say: "Also we explain, without being specific, that our royalties are in line with IC industry traditional royalty levels of 1-5%." (*Id.*). The evidence shows that licensees were willing to pay royalty rates in this range. Each of the DRAM manufacturers agreed to pay Rambus's RDRAM royalties, which ranged from 2% to 5%. In July 1991, long

before Intel became interested in RDRAM, NEC signed an RDRAM license agreement that specified a 2% royalty rate for Rambus Microprocessors and Microcontrollers, 1% for Rambus Memory Devices, 3% for Rambus Peripherals, and 3% for Customer Specific Rambus Products. (RX 538 at 22). In November 1994, again well before Intel selected RDRAM for the next generation DRAM, Samsung agreed to an RDRAM license that specifies a 2% royalty rate, which declines at certain volume marks. (RX 518 at 23). Hyundai agreed, in December 1995, to an RDRAM license agreement that specifies a 2.5% royalty rate for Rambus DRAMs (which declines to 2% then 1.5% in 2000 and 2002 respectively), 3% for Rambus processors, and 5% for Rambus ASICs and Peripherals. (CX 1600 at 12). Micron agreed to an RDRAM license in March 1997 that specifies a 2% royalty rate. (CX 1646 at 11). Also in 1997, Siemens entered into an RDRAM license that specified a royalty rate of 2.5% for Rambus DRAMs (which reduced to 2% if RDRAMs exceeded 25% of Siemens total DRAM sales) and 5% for Rambus Peripherals. (CX 1617 at 12). Mitsubishi entered into a February 1998 RDRAM license that specifies a 2.5% royalty rate on Rambus DRAMs, 3% for Rambus processors, and 5% for Rambus ASICs and Peripherals. (CX 1609 at 11). AMD {

} (Heye, Tr. 3919-20 (in camera); CX 1420 at 8 (in camera)).

Indeed, the evidence shows that to the extent Rambus encountered resistance, it was due to factors other than royalties – such as losing control of technology development and becoming a "foundry" for Intel, though DRAM manufacturers would most frequently cite royalties as the basis for any resistance. (*See* RPF 1548-1602).

742. Rambus estimated the projected weighted average royalty rate for 1993 to be 1.4%. (CX0547 at 12).

Rambus's Response to Finding No. 742:

The proposed finding is vague and devoid of context. There is no explanation as to the meaning of "weighted average royalty rate" nor how that may relate to the fact that it was apparently computed from a table listing Rambus's "*Lowest* Long-Term Royalty Rate in Contracts." (CX0547 at 12 (emphasis added)).

743. As Rambus continued to negotiate with potential licensees in the mid-1990's, it continued to encounter resistance with respect to the royalty rates it was seeking. (CX0733 ("Big stumbling block is royalties – they [Samsung] want numbers in 1% or less range.")).

Rambus's Response to Finding No. 743:

This proposed finding is not supported by the evidence. The cited email does not refer to license negotiations in the mid-1990s generally, but rather is a discussion that pertains to one specific licensee, Samsung.

The proposed finding is contradicted by the weight of the evidence. Samsung agreed to an RDRAM license that specifies a 2% royalty rate, which declines at certain very high volume marks. (RX 518 at 23). By 1998 nearly all major DRAM manufacturers had signed technology license agreements with Rambus, and in so doing, had agreed to pay royalty rates of 2% to 5% for the use of Rambus technologies in RDRAM and related products. (*See* RRFF 741).

744. Rambus also sought to restrict the field of use of its license agreements to so-called RDRAM compatible uses only. Most companies accepted this term. Samsung, however, insisted on an agreement without field of use restrictions. (CX0767 ("In my view at this point we can either sign the Samsung contract as is or forget them as a licensee. They have made it abundantly clear that without the ability to use Rambus technology in non-Rambus applications there will be no deal.")).

Rambus's Response to Finding No. 744:

This proposed finding supports Rambus' position that the industry was not lulled. In 1994, Samsung clearly recognized that Rambus' inventions, including the PLL, could be used in non-compatible Rambus parts, i.e. in parts without Rambus' proprietary bus technology. (CX0767). Moreover, Rambus made it clear to Samsung that Rambus' intellectual property rights were not limited to the RDRAM product. (CX 2078 at 116 (Karp Depo.)).

745. Rambus was prepared to make compromises during this time period in order to conclude license agreements with DRAM manufacturers. (CX0767; CX0733 ("they [Samsung] want numbers in 1% or less range. We are to try to put together a win/win proposal based on their inputs."); CX0711 at 62 (Crisp proposed to Hyundai a DRAM royalty rate declining with volume to 1.25%)).

Rambus's Response to Finding No. 745:

The proposed finding is vague and potentially misleading. The phrases "make compromises" and "this time period" are vague. With respect to the former, Rambus does not dispute that its negotiations with potential licensees were two-sided negotiations with give and take involved on both sides. (CX0733 ("lowering the royalty isn't impossible, just very undesirable.")).

G. Rambus License Presentations.

746. Continuing for many years, Rambus pursued a strategy of actively promoting its proprietary RDRAM technology to companies that were in a position to manufacture memory chips or related chipsets. (See Crisp, Tr. 2931; CX0543A at 7-8).

Rambus's Response to Finding No. 746:

The proposed finding is incomplete. Rambus also promoted its RDRAM technology to others, including systems companies. (CX0543A at 1, 3).

747. Rambus efforts to promote adoption of its proprietary RDRAM technology included

making presentations concerning the proprietary RDRAM technology to memory chip manufacturers and other firms. (E.g. CX2107 at 63 (Oh, Dep.); Bechtelsheim, Tr. 5818-19; G. Kelley, Tr. 2537; Kellogg, Tr. 5052-53). In connection with such efforts, Rambus commonly entered into non-disclosure agreements ("NDAs") that prohibited the firms from disclosing information concerning the proprietary Rambus technology to others without the consent of Rambus. (E.g. Bechtelsheim, Tr. 5818-19; Rhoden, Tr. 521; Kellogg, Tr. 5052-53).

Rambus's Response to Finding No. 747:

The proposed finding omits relevant evidence. Rambus's presentations often included a discussion of the patent protection Rambus was seeking for its inventions. (CX 2079, Mooring Depo., at 83; CX 2111, Tate Depo., at 314-15, 316-18, 319-20, 320-21, 322-24). Moreover, after Rambus's original patent application was made public through the publication of the corresponding PCT application in October 1991, Rambus did disclose non-detailed descriptions of its inventions in various other public documents. (RPF 638-54).

748. The focus of these presentations was on the advantages Rambus saw of the proprietary RDRAM technology and the unique characteristics of that technology, including its unique bus architecture. (E.g., G. Kelley, Tr. 2538; Sussman, Tr. 1429-31). Rambus' presentations of the RDRAM technology in the 1992-93 time frame involved a DRAM with a multiplexed bus. (CX2114 at 61-62 (Karp, Dep.)). Joel Karp, who was with Samsung at the time, viewed the Rambus RDRAM as "more revolutionary than evolutionary." (CX2114 at 63 (Karp, Dep.)).

Rambus's Response to Finding No. 748:

The proposed finding is vague in its reference to "these presentations." Rambus made numerous presentations to many industry members during the relevant time frame. (Farmwald, Tr. 8166-67). Complaint Counsel's attempt to generalize the subject matter of those presentations is not supported by the evidence and is not a proper factual finding. Notably, the evidence does not support the finding that Rambus's "unique bus architectecture" was a "*focus*" of those presentations. For example, Howard Sussman testified that during a 1991 presentation

by Rambus's Billy Garrett, Mr. Garrett identified three "key features" of the Rambus DRAM. (Id. at 1431). The multiplexed bus was not one of the key features that Mr. Garrett identified. (Id. at 1433). As Dr. Farmwald explained:

> "I don't think I ever thought about it as a narrow bus. We had a set of ideas that implemented a bus. Along the way we would pick implementation choices that made sense at the time. So the first bus we picked was a 9-bit-wide bus because that's what we could fit on the edges of the chips that existed at the time. Later we went to wider buses because we could fit more pins on the chip."

(Farmwald, Tr. 8143-44). Mr. Karp testified that Rambus made it clear to Samsung that its intellectual property rights pertained to more than just RDRAM. (CX 2078 at 116-17 (Karp Depo.)). In addition, the written description of Rambus' original patent, which was provided to Rambus' partners (CX0535 at 3), makes clear that Rambus' inventions were not restricted to a specific bus architecture. (*See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094 (Fed. Cir. 2003) ("a multiplexing bus is only one of many inventions disclosed in the '898 application")).

749. Craig Hampel, Rambus technical director who beginning in 1993 participated in numerous meetings and presentations with DRAM manufacturers and other firms to discuss Rambus technology (Hampel, Tr. 8672, 8729-31), was not aware of any instance in which Rambus representatives told the DRAM manufacturers which aspects of RDRAM were Rambus inventions, or were protected by Rambus patents or patent applications. (Hampel, Tr. 8732-33). Rambus President David Mooring testified that slides used by Rambus in presentations to Rambus customers would "definitely not have put anybody on notice" of the coverage of patents but would only have generic information about aggregate numbers of Rambus patents and/or patent applications. (CX2112 at 180 (Mooring, Dep.)).

Rambus's Response to Finding No. 749:

This proposed finding is against the weight of the evidence and mischaracterizes the evidenced cited.

To the exent that the reference to Mr. Hampel's and Mr. Mooring's testimony is meant to imply that Rambus did not inform DRAM manufacturers that its intellectutal property might cover non-RDRAM devices, the proposed finding is contradicted by the weight of the evidence. The evidence shows that Rambus routinely discussed with DRAM manufacturers, OEMs, and Intel, the breadth of its patent coverage, including the possibility that non-compatible uses (i.e., non-RDRAM uses) of its technology, including SyncLink and SDRAMs, could infringe Rambus patents. (RPF 549-554; see also CX2079 at 83 (Mooring Dep.)). Rambus' presentations often included a discussion of the patent protection Rambus was seeking for its inventions. (CX 2079, Mooring Depo., at 83; CX 2111, Tate Depo., at 314-15, 316-18, 319-20, 320-21, 322-24). Moreover, after Rambus's original patent application was made public through the publication of the corresponding PCT application in October 1991, Rambus also disclosed non-detailed descriptions of its inventions in various other public documents. (RPF 638-54).

Rambus's CEO Geoff Tate and Rambus Vice President Allen Roberts held a series of meetings with DRAM manufacturers in Asia in an effort to convince the manufacturers to become Rambus licensees. Mr. Tate's notes of those meetings reflect that he told DRAM manufacturers LG Semicon, Samsung, NEC, and Oki that Rambus expected to have intellectual property that would read on the SyncLink architecture and on devices manufactured in compliance with the SDRAM standard. (RPF 550-54). Rambus's CFO Gary Harmon testified that he did recall "a couple of cases" during license negotiations where the issue of "whether the

Rambus-issued patents or filed patents would cover SDRAM technologies" was discussed. (CX2070, Harmon Depo., at 43). Rambus also told Intel that it might have intellectual property that covered DDR SDRAMs. (MacWilliams, Tr. 4905). Rambus's actions at JEDEC also indicated that Rambus might have intellectual property that could be related to JEDEC work. Examples include: (1) Rambus declining to comment with respect to its patent position in response to an inquiry in May 1992 (RPF 466-529), (2) Rambus's disclosure in September 1993 of the '703 patent, which contained substantially the same written description as the '898 application and revealed the existence of numerous divisional applications (RPF 714-19), (3) Rambus's letter to JEDEC in September 1995 stating that its silence at meetings should not be interpreted as "mak[ing] any statement regarding potential infringement of Rambus intellectual property (RPF 544-48), and (4) Rambus's June 1996 letter formalizing its separation from JEDEC noting, inter alia, that Rambus had a number of patent applications pending (RPF 560).

Insofar as Mr. Hampel's testimony is concerned, the proposed finding is misleading. Rambus's objections to Complaint Counsel's questions that were not directed specifically to presentations at which Mr. Hampel was present were sustained. Mr. Hampel's testimony reflects only that so far as Rambus presentations at which he was specifically present were concerned, he was not aware of a Rambus representative telling a DRAM manufacturer which features of RDRAM were protected by patents or patent applications. (Hampel, Tr. 8732-33).

Insofar as Mr. Mooring's testimony is concerned, the proposed finding is misleading and omits relevant evidence. While the slides used by Rambus may only have listed aggregate numbers of Rambus patents and/or applications, Mr. Mooring testified that Rambus's RDRAM licensees were explicitly told that Rambus had pending or issued patents that would cover the

use of pieces of the Rambus technology. (CX 2079, Mooring Micron Depo., at 83-84).

750. Gary Harmon, former Rambus Chief Financial Officer, was involved in negotiating RDRAM licenses for Rambus in the 1993-96 time frame. (CX2070 at 42 (Harmon, Dep.)). Mr. Harmon recalled being involved in discussions with Oki, Fujitsu, Toshiba and NEC from Japan; LG, Hyundai and Samsung from Korea; and Intel, LSI Logic, IBM, Texas Instruments, and Cirrus Logic from the United States, among others. (CX2070 at 42-43 (Harmon, Dep.)). Mr. Harmon did not recall any discussions on the scope or extent of Rambus patents during these negotiations. (CX2070 at 42 (Harmon, Dep.)).

Rambus's Response to Finding No. 750:

This proposed finding is contradicted by the evidence. Mr. Harmon testified that he did recall discussing "Rambus-issued patents or filed patents [that] would cover SDRAM technologies." (CX2070, Harmon Depo., at 43). Mr. Harmon further testified such discussions generally arose during the license negotiations when a potential licensee would request a license that covered the full scope of Rambus's technology, in response to Rambus's insistence that the licenses only cover Rambus-compatible products. (*Id.* at 44). Moreover, during this same time period, in the fall of 1995, Rambus CEO Geoff Tate and Vice President Allen Roberts held a series of meetings with DRAM manufacturers in an effort to convince them to become Rambus licensees. Mr. Tate's notes of those meetings reflect that he informed DRAM manufacturers LG Semiconductor, Samsung, NEC, and Oki that Rambus expected to have intellectual property that would read on the SyncLink architecture and on devices manufactured in compliance with the SDRAM standard. (*See* RPF 549-554).

751. Howard Sussman, an employee of NEC and later Sanyo Semiconductor (Sussman, Tr. 1321-22), first learned about Rambus through a presentation made by a Rambus employee in 1991. (Sussman, Tr. 1429). The content of the presentation focused on what were portrayed as the key features of the Rambus RDRAM, which included the use of a low-voltage CMOS driver and packetized input/output (*Id.* at 1430-31). When Mr. Sussman later saw Rambus's European patent application, he did not see anything in it that related to the work going on in JEDEC. (*Id.*

at 1445).

Rambus's Response to Finding No. 751:

This proposed finding is misleading, not supported by the evidence cited, and contradicted by the weight of the evidence.

As an initial matter, Mr. Sussman's testimony that he first learned about Rambus from Billy Garrett at the December 1991 JEDEC meeting (Sussman, Tr. 1429), is contradicted by more reliable evidence. A fax produced from Mr. Sussman's files (with "SUS-FTC" production numbers) indicates that Mr. Sussman already knew about Rambus by October 30, 1991. (RX0181 at 2). The fax is on NEC letterhead and Mr. Sussman's name, while hard to make out, appears to be the third recipient listed. (*Id.*). The fax asks the recipients to provide information regarding, inter alia, "relative cost differences between . . . Synchronous DRAM (Sussman's proposal)/RAMBUS proposed DRAM/and VRAM." (*Id.*). The fax also requested information regarding the size differences between these different kinds of DRAM. (Id.). The fax explained that the information was required because "SUN is inclined to those technologies which will given them faster performance . . . . Thus the interest in the synchronous proposal by Howard Sussman and the Rambus interface . . . ." (*Id.*). Thus, not only had Mr. Sussman heard of Rambus by October 1991, but he was aware that the Rambus technology was a key competitor to the synchronous DRAM technology that he was proposing.

Moreover, review of Mr. Sussman's testimony makes clear that the "presentation" referred to in the proposed finding was a mere 15 minute discussion between Mr. Sussman and Billy Garrett, a Rambus employee, squeezed into a portion of an open afternoon of a JEDEC meeting. (Sussman, Tr. 1430-31). Indeed, Mr. Garrett requested three to four hours of

Mr. Sussman's time, but Mr. Sussman only gave him fifteen minutes. (*Id.* at 1430) Mr. Sussman testified that during those fifteen minutes, Mr. Garrett identified three "key features" of the Rambus DRAM including a clocking scheme, but not including a multiplexed bus. (Id. at 1431, 1433).

In addition, the implications of the proposed finding are contradicted by the weight of the evidence. The evidence makes clear that a patent lawyer or a person of ordinary engineering skill would understand upon review of Rambus's PCT application (which Mr. Sussman referred to as the "European application") that Rambus might seek broad patent claims covering the independent use of the four features at issue here. (RPF 659-706). Mr. Sussman himself testified that the PCT application disclosed independent use of the dual edge clocking feature when he testified that Figure 13 shows "input being sampled on the high and low edge of the clock" and that that is what the DDR SDRAM standard refers to as a "double data rate input." (Sussman, Tr. 1322, 1467-68).

752. In April 1992, Gordon Kelley of IBM attended a presentation by Rambus at IBM comparing the proprietary Rambus RDRAM technology with SDRAM. (G. Kelley, Tr. 2537). Following that presentation, Mr. Kelley believed that the Rambus RDRAM was fundamentally different from the SDRAM technology under discussion at JEDEC that any Rambus patents or patent applications would not apply to SDRAMs. (G. Kelley, Tr. 2537-38 (". . . the Rambus DRAM was so different from the synchronous DRAM being discussed at JEDEC that I just did not believe that anything [patents or patent applications] that Rambus had on the RDRAM might apply to the SDRAM or to JEDEC."); *id*. at 2546 (same); *id*. at 2504 (he only understood Rambus intellectual property as applying to the Rambus DRAM)).

Rambus's Response to Finding No. 752:

The proposed finding is contradicted by more reliable evidence. Contemporaneous documents demonstrate that in June of 1992, Gordon Kelly was concerned about potential Rambus "patent problems" relating to SDRAMs. (RPF 523-526). Mr. Kelley presented these

concerns to a meeting of 30 engineers from Siemens and IBM. (*Id.*).

753. Desi Rhoden was employed at Hewlett Packard when he began to learn about the Rambus technology in the early 90's. (Rhoden, Tr. 396). Rambus came to HP to give a presentation about their new memory that they were developing. (*Id.*). The presentation was made pursuant to a non-disclosure agreement between Rambus and HP. (Rhoden, Tr. 521). Although Rambus did not say anything at that presentation about pending Rambus patent applications, Rhoden assumed that Rambus probably did have patent applications. (Rhoden, Tr. 521). Rambus never suggested to him that its proprietary technology extended outside the RDRAM architecture. (Rhoden, Tr. 521-22).

Rambus's Response to Finding No. 753:

This proposed finding is misleading because it omits relevant evidence. Mr. Rhoden never testified as to the scope of the patents he suspected Rambus to have pending, and he never testified that he believed that scope to be limited to Rambus RDRAM. He also did not testify that Rambus suggested to him in any way that its patent applications were so limited.

Moreover, the implications of this proposed finding are contradicted by the weight of the evidence. In fact, Mr. Rhoden was aware as early as 1992 that Rambus might obtain patent rights with respect to features being considered for incorporation into JEDEC Standards, and Rambus did nothing to dispel those concerns. Mr. Rhoden was in attendance at the May 1992 JEDEC 42.3 meeting when Richard Crisp declined to comment in response to Gordon Kelley's "point blank" question as to whether Rambus had anything to disclose relating to two-bank design of an SDRAM. (RPF 492; *see* RPF 493-515). Mr. Rhoden was also present at a JEDEC 42.3 meeting in September 1995 when Richard Crisp expressly informed the committee that "Rambus elects not to make a specific comment on [Rambus's] intellectual property position relative to the Synclink proposal. Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make

any statement regarding potential infringement of Rambus intellectual property." (JX27 at 26. RPF 536, 544-546). Mr. Rhoden also attended SyncLink meetings, where concerns were raised about Rambus's patent portfolio. (*See, e.g.*, RX 966, 1001; RPF 557). Mr. Rhoden was also present in March 1997 when Terry Lee of Micron, and others, indicated that Rambus "had a patent" on the clocking scheme described in an NEC DDR SDRAM presentation. (JX 36 at 1, 7; *see* RPF 567-569.)

754. Andreas Bechtelsheim, a Vice-President for technology at Sun (Bechtelsheim, Tr. 5752), was involved in presentations and discussions with Rambus and understood that Rambus had patent rights that covered its proprietary RDRAM technology. (Bechtelsheim, Tr. 5828-29; 5841-42).

Rambus's Response to Finding No. 754:

This proposed finding is misleading because it omits relevant evidence. Mr. Bechtolsheim testified not only that he understood Rambus' patent rights to cover its proprietary RDRAM technology, but also that, "[Rambus] made clear is that they were going to protect any patent on their memory technology because that was their business model." (Bechtolsheim, Tr. 5829).

755. Mark Kellogg, an employee of IBM (Kellogg, Tr. 5017), learned about Rambus technology through a presentation by Rambus to IBM in the early 1990's. (Kellogg, Tr. 5052-53). At that time, Mr. Kellogg expected that any Rambus patent activity would be associated with the Rambus proprietary RDRAM product that they were showing to IBM, which was a narrow I/O, high-bandwidth, packetized memory device or card with a loop-back structure and a few other elements. (Kellogg, Tr. 5053).

Rambus's Response to Finding No. 755:

This proposed finding is contradicted by more reliable evidence. Mr. Kellogg's contemporaneous notes of the May 1992 JEDEC meeting clearly indicated that he was concerned about Rambus' patents that may apply to SDRAMs. (Kellogg, Tr. 5319-5324). Mr. Kellogg

explained that concerns about Rambus' intellectual property expressed by other companies raised a “flag” because, "between Siemens and NEC, companies are describing possible intellectual property concerns which may affect our decision process for synchronous DRAM. That is a concern. The lack of response by Rambus is also a concern." (Kellogg, Tr. 5323).

756. Terry Lee, an employee at Micron, learned about Rambus technology in part from a meeting with Rambus held in 1995. (Lee, Tr. 6601-02). Following the meeting, he and a colleague, Mr. Kevin Ryan, reviewed a set of patent abstracts. (*Id*. at 6607-08). Mr. Lee concluded that the patents appeared to apply specifically to the RDRAM bus structure. (*Id*. at 6610-11 (the RDRAM bus is “the narrow bus with the command/address/data multiplexed with this Rambus architecture and Rambus signaling scheme.”)).

Rambus’s Response to Finding No. 756:

The proposed finding is misleading because it omits relevant information. Mr. Lee’s conclusions were unreliable because they were based primarily on a review of selected patent abstracts and not on a review of the entire patent including specifications, drawings and claims. (Lee, Tr. 6608).

The proposed finding is contradicted by more reliable evidence. In March of 1997 Mr. Lee expressed concerns to the JEDEC JC 42.3 committee that a DDR SDRAM presentation “looked like” one of the Rambus patents he had reviewed in 1995. (Lee, Tr. 6956-59). Mr. Lee’s contemporaneous “concerns” that a DDR SDRAM presentation looked like a Rambus patent contradicts the proposed factual finding that Lee had concluded that the Rambus patents applied specifically to the Rambus bus structure.

H. The Rambus Alternative Business Strategy.

757. During 1990 and 1991, Rambus focused on its business model of trying to license its proprietary RDRAM architecture. (CCFF 733-736).

Rambus's Response to Finding No. 757:

The use of "business model" in this context is vague and confusing. Rambus's business model had and has various facets other than licensing, including seeking patent coverage for its inventions, maintaining the secrecy of its inventions through NDAs, etc. In specific response, Rambus incorporates by reference as if restated hereat its responses to CCFF 733-736.

758. December 1991, Rambus attended its first JEDEC meeting "to learn what the competition was working on." (CX0837 at 1).

Rambus's Response to Finding No. 758:

The proposed finding is misleading and not supported by the evidence. It is also contradicted by more reliable evidence. The evidence makes clear that Rambus attended the December 1991 JEDEC meeting as a non-member guest of Toshiba. (JX0010 at 2). Moreover, the cited reference is an email written by Richard Crisp, and makes no reference to the December 1991 JEDEC meeting. Mr. Crisp did not attend the December 1991 meeting and was not involved in Rambus' decision to attend. (Crisp, Tr. 2933; CX 2054 (Mooring Depo. at 42-44)). Moreover, the quotation in the proposed finding is a fragment of a sentence that, in its entirety, makes clear that there were several reasons why Rambus attended JEDEC, not just the one mentioned in the proposed finding. (CX 0837 at 1).

In fact, Rambus decided to joint JEDEC because of the prospect of standardizing the RDRAM device, because it seemed to be a useful place to learn marketplace and competitive information, and because it was a good place for "meeting and greeting" potential customers. (RPF 447).

759. In February 1992, Rambus engineer Billy Garrett reported back to staff at Rambus

concerning events at a JEDEC meeting he was attending: "SDRAMs will happen. They may happen sooner than we want . . ." (CX0672 ("What has happened in the last week borders on the remarkable.")).

Rambus's Response to Finding No. 759:

The proposed finding is misleading because it juxtaposes unrelated sentences from the cited evidence in a way that was not intended by the author. The parenthetical in the proposed finding, "What has happened in the last week borders on the remarkable," follows at least eleven lines after quotation in the text of the proposed finding. There is no indication in the cited evidence that the two thoughts are related. (CX 0672 at 1) Indeed, Mr. Garrett was reporting about several different aspects of the JEDEC meeting; any one of them or the totality could have, in his view, "border[ed] on the remarkable." Moreover, the quotation in the text of the proposed finding is a selected portion of a longer sentence which has a different meaning than the portion cited. (*Id.* at 1).

760. In March 1992, Rambus Vice President Allen Roberts contacted outside patent counsel Lester Vincent to discuss JEDEC. (CX1941 at 1). Mr. Vincent's notes of the meeting reflect the statement, "Said need preplanning before accuse others of infringement." (*Id.*) Two days later, on March 27, 1992, Mr. Roberts and Richard Crisp met with Lester Vincent in person to discuss JEDEC. (CX1942).

Rambus's Response to Finding No. 760:

This proposed finding is misleading. Rambus does not contest that Mr. Vincent's notes reflect these discussions. However, there is no indication that the specific and/or only purpose of the discussions was "to discuss JEDEC." Indeed, the first entry of CX 1941 relates to the filing of a patent application.

The proposed finding is also misleading to the extent it is intended to suggest that the "preplanning" relates to an alleged scheme by Rambus to "lull" JEDEC members. Neither the

notes nor the record evidence supports such a suggestion. In fact, Mr. Vincent's notes of the meeting on March 27, 2002 identified a risk of equitable estoppel should Rambus "mislead JEDEC into thinking that Rambus will not enforce its patents." (CX 1942 at 1). Heeding the advice of its counsel, Rambus took steps to ensure that it did not mislead JEDEC. These steps included: (1) disclosing the '703 patent, (2) expressly declining to comment in response to patent inquiries in May of 1992, (3) informing the SyncLink working group in August 1995 that its work might infringe Rambus's intellectual property; (4) informing JEDEC in September 1995 of the possible patent issues associated with SyncLink and that its "presence or silence at committee meetings does not [ ] make any statement regarding potential infringement of Rambus intellectual property"; and (5) informing DRAM manufacturers that Rambus expected to have intellectual property that would read on the SyncLink architecture and on devices manufactured in compliance with the SDRAM standard; and (6) formally confirming its withdrawal in June 1996 and stating that its withdrawal is consistent with a desire to not "mislead JEDEC into thinking that Rambus will not enforce its patents." (RPF 495-515, 530-560.).

761. In April and May, 1992, Mr. Crisp attended a JEDEC special task group meeting and a regularly scheduled meeting of the JEDEC JC-42.3 Committee respectively. (CCFF 893-99, 902-09). Also in May 1992, Mr. Crisp met with Mr. Vincent to discuss adding claims to Rambus's pending patent applications. (CCFF 900-01, 910).

Rambus's Response to Finding No. 761:

Rambus incorporates by reference as though restated hereat its responses to CCFF 893-99 and 900-910.

762. During this time period, while still pursuing its principal objective of promoting its proprietary RDRAM technology, Rambus was developing an alternative business strategy to deal with the emerging competitive threat posed by the efforts of JEDEC to develop a standard SDRAM technology, as discussed at length below. (CCFF 800 et seq.).

Rambus's Response to Finding No. 762:

This proposed finding is not supported by any evidence. Rambus incorporates by reference as though restated hereat its responses to CCFF 800 et seq.

763. By June 1992, Rambus CEO Geoffrey Tate transmitted to the Rambus Board of Directors a comprehensive five-year business plan, which, he explained, was based on "inputs from all of the executives." (CX0543A at 1). As reflected in the "Executive Summary" of this June 1992 Business Plan, Rambus remained committed to:

> "establish[ing] strong intellectual property barriers";
> "establish[ing] Rambus as the new interface standard"; and
> "establish[ing] a very high profit stream of technology royalties."

(CX0543A at 3).

Rambus's Response to Finding No. 763:

This proposed finding is misleading because it omits relevant evidence. The three quotations contained in the proposed finding are from a lengthy list of bullet points set forth in the Executive Summary portion of the cited document. Not only does the proposed finding omit six of the nine bullet points entirely, it also omits portions of the bullet points from which it does quote. The omitted bullet points include:

"develop a breakthrough technology with high value added in a large percentage of computer, communications, and consumer digital systems products;"

"to license the technology for integration onto high volume ICs of all major IC companies and to have license fees cover the costs of technology and market development;"

"to establish Rambus as the new interface standard for systems requiring high performance at low cost;" (underlined portion omitted in proposed finding);

"to continually improve on Rambus Technology through minor and major enhancements" (CX0543A at 3).

Moreover, Mr. Tate did not describe his June 1992 Business Plan as "comprehensive." Rather, he expressly stated that it was prepared for the limited purpose of acquiring additional funding. (CX 0543A at 1) ("The 'spur' to do this is the Lease Line we are arranging with Phoenix.").

764. With respect to the key goals of establishing Rambus as the new interface standard and establishing a high profit stream of technology royalties (CX0543A at 3), the June 1992 Business Plan acknowledged that Rambus faced two principal impediments: "Resistance to Business Model" and "Competitive Solutions." *(Id.* at 14). Regarding the former, The Plan reported that some firms "have had a very negative reaction to our business model" including resistance to paying royalties to Rambus and fear that the royalties would make chips containing the Rambus technology "too expensive." (*Id.*). The principal competitive threat to RDRAM was JEDEC's emerging standards for "Synchronous DRAMs" which did not suffer from the same "price negative and risk negative associated with Rambus." (CX0543A at 17; see also *id.* at 16 ("many system customers perceive . . . that Sync DRAMs will be sourced more broadly and more quickly," and hence "will be much cheaper," than RDRAMs)).

Rambus's Response to Finding No. 764:

This proposed finding omits relevant evidence and is not supported by the evidence. First, there is no evidence to support that notion that "establishing Rambus as the new interface standard" and "establishing a high profit stream of technology royalties" were Rambus's "key goals." As explained in response to proposed finding 763, these phrases were lifted from the complete list set forth in CX0543A, and given a different meaning in so doing. (CX 0543A at 3). Second, there is no connection drawn in the cited text between the two phrases taken from the Executive Summary list and the other two sections of the document referenced, "Resistance to Business Model" and "Competitive Solutions" headings. *(Id.* at 14). Third, the statement that "some firms 'have had a very negative reaction to our business model, . . ." is incomplete. The following paragraph makes clear that most systems customers agree that If the Rambus-based solution is better than the alternate solution on performance, price and features, the amount of

royalties is irrelevant. (*Id*. at 14). The document also makes clear that Rambus's royalties "are in line with IC industry traditional royalties of 1-5%." (*Id*. at 14). Fourth, the statement that, "the principal competitive threat to RDRAM was JEDEC's emerging standards for 'Synchronous DRAMs.'" is unsupported by the cited evidence. The section that discusses Synchronous DRAMs does not identify SDRAMs in this way, rather, Synchronous DRAM is identified as one of five competitive solutions. Moreover, the document makes clear that Rambus viewed its RDRAM technology as superior to Sync DRAMs, and more likely to succeed as a de facto standard in light of the slow progress of the SDRAM standard at JEDEC. (*See* CX 0543A at 15-17). Fifth, the proposed finding is misleading in creating the false impression that Rambus had concluded that Synchronous DRAMs would not suffer from the same perceived "price negative and risk negative associated with Rambus." A review of the selectively quoted sentence in its entirety shows that the finding is not supported by the evidence: "Finally, many systems customers perceive, because our 4.5Mbits are 25-30% and because they think that Sync DRAMs will be much cheaper at 18Mbit than RDRAMs. *Reality is that 18Mbits, Sync and RDRAMs will have the same die size - and Rambus already has 3 fully-compatible sources, whereas no two Sync DRAMs in development are pin-compatible!"* (*Id*. at 16 (emphasis added)).

765. The June 1992 Business Plan continued to emphasize that the "#1 strategy" of Rambus was "to get our parts proven and in the market." (CX0543A at 16). But the plan also stated a second, alternative patent-based strategy for attacking SDRAMs:

> Finally, we believe that Sync DRAMs infringe on some claims in our filed patents; and that there are additional claims we can file for our patents that cover features of Sync DRAMs. Then we will be in a position to request patent licensing (fees and royalties) from any manufacturer of Sync DRAMs.

(CX0543A at 17).

Rambus's Response to Finding No. 765:

This proposed finding is misleading because it omits relevant evidence and is contradicted by the evidence. The strategy of getting its parts proved and in the market is not referred to as Rambus's "#1 strategy," but rather as its "#1 strategy to counter Sync DRAMs." (CX0543 at 16). The document goes on to discuss three alternative strategies for seeking market acceptance of RDRAM over Sync DRAMs, not just one "alternative patent-based strategy." (Id. At 17). (It is important to note that the Plan uses the term "Sync DRAMs" not SDRAMs. As the document makes clear, the JEDEC Sync DRAM standard was slowly moving through JEDEC at the time the document was drafted. (CX 0543A at 15)). The fourth of the four strategies discussed is only partially block-quoted in the proposed finding. After the section quoted by Complaint Counsel, the document goes on to make clear that preparatory work needs to be done to implement this strategy. (*Id.* at 17). Indeed, Rambus CEO Geoff Tate testified that the statement in the June 1992 draft plan that "we believe that Sync DRAMs infringe on some claims in our filed patents"was based on a "feeling" that "synchronous DRAMs sure looked like they stem[med] from [our] inventions." (CX 2073, Tate *Micron* Depo. at 221-22). Mr. Tate had "assumed" that broad patent applications had been filed to protect all of Rambus's inventions. (CX 2073, Tate *Micron* Depo. at 222; CX 2088, Tate *Infineon* Trial Testimony at 57). At the time that he wrote the 1992 Business Plan, Mr. Tate did not know of any particular claim that might be infringed by SDRAMs. (*Id*.). After the 1992 Business Plan was prepared, a Rambus employee was assigned the task of determining what filed claims would be infringed by SDRAMs. (CX 2073, Tate Micron Depo. at 222-3). The employee subsequently informed Mr. Tate that the filed claims were not as broad as previously thought and did not cover the full

range of what had been invented and disclosed in the '898 application. (CX 2073, Tate Micron Depo. at 222-24; CX 2088, Tate Infineon Trial Testimony at 57-58). (*See* RPF 423-424).

766. The Rambus pursuit of this alternative strategy is the core of the present case, and is discussed at length below. (CCFF 800 et seq.).

Rambus's Response to Finding No. 766:

This proposed finding is not supported by any evidence. Rambus incorporates by reference as though restated hereat its responses to CCFF 800 et seq.

767. Paragraphs 767 - 799 are unused.

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of	)	
	)	Docket No. 9302
RAMBUS INCORPORATED,	)	
a corporation.	)	
	)	

CERTIFICATE OF SERVICE

I, Jacqueline M. Haberer, hereby certify that on October 1, 2003, I caused a true and correct copy of *Rambus Inc.'s Responses to Complaint Counsel's Proposed Findings of Fact, Volume I (Public)* to be served on the following persons by hand delivery:

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