Fraunhofer
ISIT

FRAUNHOFER-INSTITUT FÜR SILIZIUMTECHNOLOGIE ISIT

Achievements and Results Annual Report 2015


Fraunhofer ISIT
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Achievements and Results Annual Report 2015

Test of hermitically sealed laser diode

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Infrastructure in the new cleanroom building

ISIT-presentation at Hospitalar (medtec trade fair) in Sao Paulo: Dr. Eric Nebling, Lars Blohm, Roana Melina de Oliveira Hansen, Prof. Wolfgang Benecke

Dear business partners, dear friends of Fraunhofer ISIT, dear colleagues,

For our institute, the year 2015 was once again characterized by a multitude of key decisions and staffing changes. During the spring, processing equipment was finally moved into the new clean room, bringing our new building project to a successful close. A complete process chain with modernized facilities is now once again available for MEMS technology, Fraunhofer ISIT's key activity, in the enlarged clean room laboratory. Recognizing Fraunhofer ISIT's extensive efforts to completely redevelop its research infrastructure, the Fraunhofer-Gesellschaft's Executive Board has made additional resources available to the institute to overhaul, reinstall and qualify machinery. Meanwhile, in addition to offering planning input and supporting the administrative aspects of the new construction work at Fraunhofer ISIT, the State of Schleswig-Holstein's Ministry for Economic Affairs, Employment, Transport and Technology also successfully campaigned for project cost overruns to be covered by public financing in 2015. We would like to express our thanks here both to the Executive Board and to the relevant decision makers at federal and state level for their commitment. With this modernization completed, Fraunhofer ISIT can once again carry out work on state-of-the-art microtechnology research assignments for external customers. X-FAB is one such contractor and research partner in the new clean room; it successfully pushed through its expansion plans in Itzehoe and Erfurt in the past year. We are optimistic that the many ongoing research projects will serve as a base for X-FAB's steady growth in Itzehoe.

To make it easier for additional research partners to access Fraunhofer ISIT, we are working on a new way to showcase the institute's technological services,

Liebe Geschäftspartner, liebe Freunde des ISIT, liebe Kollegen,

das Jahr 2015 war für unser Institut erneut von zahlreichen Weichenstellungen und personellen Veränderungen geprägt. Im Laufe des Frühjahrs konnte der Umzug von Prozessgeräten in den neuen Reinraum abgeschlossen werden, womit das Neubauprojekt nunmehr seinen erfolgreichen Abschluss gefunden hat. Für den Arbeitsschwerpunkt des ISIT, die MEMS Technologien, steht damit wieder eine komplette Prozesskette im vergrößerten Reinraumlabor mit modernisierten Anlagen zur Verfügung. Vom Vorstand der Fraunhofer-Gesellschaft wurde der umfangreiche Einsatz des ISIT beim Aufbau einer komplett erneuerten Forschungsinfrastruktur anerkannt, indem für das ISIT zusätzliche zentrale Mittel bereitgestellt wurden, um Anlagen zu überholen, neu zu installieren und zu qualifizieren. Auch das Schleswig-Holsteiner Ministerium für Wirtschaft, Arbeit, Verkehr und Technologien hat den ISIT-Neubau inhaltlich begleitet und sich erfolgreich dafür eingesetzt, dass in 2015 noch Projektmehrkosten in die öffentliche Neubaufinanzierung aufgenommen wurden. Dem Vorstand und den zuständigen Entscheidern bei Bund und Land sei an dieser Stelle ausdrücklich für ihren Einsatz gedankt. Nach dieser Modernisierung kann das ISIT für externe Auftraggeber Forschungsaufträge wieder mit hochmodernen State-of-the-Art-Mikrotechnologien bearbeiten. Ein solcher Auftraggeber und Forschungspartner im neuen Reinraum ist auch die Firma X-FAB, die im letzten Jahr ihre Erweiterungspläne in Itzehoe und Erfurt erfolgreich umsetzen konnte.

Mit den zahlreichen, laufenden Forschungsprojekten hoffen wir zuversichtlich, die Grundlagen für ein

Fabian Stoppel: Outstanding poster award at Transducers 2015, Anchorage

ORGANIZATIONAL CHART

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Prof. Dr. Bernd Wagner (deputy director)

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Dr. Chemnitz

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Prof. Dr. Kapels

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Dr. Schwarzelbach

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Mr. Wacker

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Prof. Dr. Dudde
Dr. Schwarzelbach

Quality
Dr. Petzold
Mr. Bertels

Girls information day at ISIT, February 25, 2015

starting with various application areas for the latest microtechnologies.

Fraunhofer ISIT organizes its business into system-oriented fields; business unit heads not only provide access to ISIT technologies but also organize the design of new and more complex application systems in conjunction with customers – enabling Fraunhofer ISIT to open up new areas of activity. This new structure is also expressed in the institute's organizational chart.

Fraunhofer ISIT has already chalked up the first new systems-oriented success. Starting from the core competences power electronics and battery technologies, the institute was able to participate in a competition sponsored by the German Federal Ministry of Economic Affairs and Energy (BMWi) to encourage the adoption of renewable energy. Along with numerous institutions and companies from Hamburg and Schleswig-Holstein Fraunhofer ISIT participated with the NEW 4.0 project as part of the BMWi's "Showcase Smart Energy" funding program, which has a particular focus on wind energy. Approval notices are expected later this year once all of the project proposals are in. I thank the employees in the departments involved for their dedication during the prolonged and complex planning and coordination work.

In the medium term, Fraunhofer ISIT's expansion is expected to create additional development opportunities for our cooperation partner, Vishay. Vishay's plans for multiple investment measures to modernize and increase capacity in Itzehoe are well advanced. Soon it will be possible to perform lithographic processes at Fraunhofer ISIT using a

stetiges Wachstum der X-FAB in Itzehoe zu schaffen. Um den Zugang weiterer Forschungspartner zum ISIT zu erleichtern, wurde an einer neuen Darstellung der technologischen Dienstleistungsangebote des ISIT, ausgehend von verschiedenen Anwendungsbereichen moderner Mikrotechnologien gearbeitet. Das ISIT organisiert systemorientierte Geschäftsfelder, in denen Geschäftsfeldleiter nicht nur den Zugang zu ISIT Technologien vermitteln können, sondern mit Kunden den Aufbau komplexer, neuer Anwendungssysteme organisieren. Für das ISIT erschließen sich so neue Arbeitsgebiete. Diese Neustrukturierung hat auch seinen Niederschlag im ISIT-Organigramm gefunden.

Als einen ersten Erfolg der Systemorientierung hat das ISIT Vorarbeiten durch die Technologiefelder Leistungselektronik und Akkumulatoraufbau nutzen können, um sich erfolgreich in einem Wettbewerb des Bundeswirtschaftsministeriums zum Einsatz erneuerbarer Energien durchsetzen zu können. Mit einer Vielzahl von Einrichtungen und Unternehmen aus Hamburg und Schleswig-Holstein ist das ISIT mit dem Projekt „NEW 4.0" im Rahmen des Programms „Schaufenster Wind" beteiligt. Nach Einreichen aller Projektanträge werden die Bewilligungsbescheide im Laufe dieses Jahres erwartet. Ich danke den beteiligten Mitarbeitern der Abteilungen für ihre Durchführung der langwierigen und aufwändigen Planungs- und Abstimmungsarbeiten.

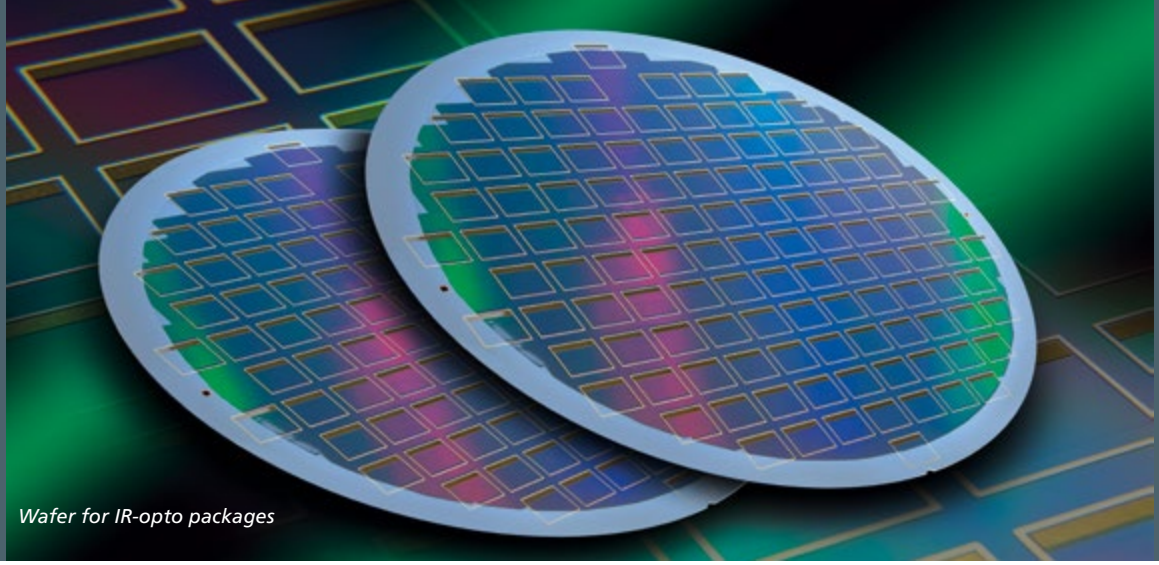
Die vollzogene Erweiterung des ISIT soll mittelfristig auch für den Kooperationspartner Vishay zusätzliche Entwicklungsmöglichkeiten schaffen. Vishay hat bereits

PREFACE

Vishay purchase the red office building next to ISIT

ISIT scientists T. Giese and V. Stenchly at Microsystem Congress in Karlsruhe, 2015

Presented ISIT at Fraunhofer-Tag in Lübeck: Christian Mallas, Vanessa Stenchly, Prof. Holger Kapels and Prof. Bernhard Wagner



Wafer for IR-opto packages

deep-UV scanner that Vishay is currently installing. With the long-term vision of making Itzehoe its production location, a few months ago Vishay purchased the red office building with a clean room basement that was originally built by Philips. Vishay intends to continue its current R&D collaborations with ISIT employees and has begun negotiations with Fraunhofer headquarters in order to extend the existing cooperation agreement.

In November 2015, Fraunhofer ISIT had the opportunity to present its current work results and research projects to the public in Lübeck at Schleswig-Holstein's first Fraunhofer Day – an exhibition sponsored by Fraunhofer headquarters, the Ministry of the Economy in Kiel and the Schleswig-Holstein chamber of commerce and featuring a total of nine Fraunhofer Institutes. Fraunhofer ISIT also took this opportunity to showcase a somewhat unusual project for the institute: a unique cooperation between ISIT and Muthesius University in Kiel.

A competition jointly called to life by the institute and Muthesius University saw nearly 100 students use art and design as a means of representing the social and cultural meaning of microsystems technology and microelectronics. To conclude this competition, we presented a documentation of the best pieces of work at the Lübeck exhibition. The many sketches, models, multimedia animations and films came as a pleasant surprise. The work was imbued with originality and personality, showing humor as well as earnestness, romanticism as well as sarcasm. Whether improvised or professionally presented, every realization provided insight into the visions, fears and hopes of a generation that accepts as a natural part of life what we still sometimes celebrate as innovation.

mit der Planung mehrerer Investitionsmaßnahmen zur Kapazitätserhöhung und Modernisierung in Itzehoe begonnen. Demnächst werden Lithographieprozesse mit einem Deep-UV Scanner im ISIT möglich werden, da Vishay ein entsprechendes Gerät installiert. Vor einigen Monaten hat Vishay das ursprünglich von Philips errichtete, rote Bürogebäude mit Reinraumfundament erworben und sich so längerfristig zum Produktionsstandort Itzehoe bekannt. Vishay beabsichtigt die Fortsetzung der bestehenden F&E-Zusammenarbeit mit Mitarbeitern des ISIT und hat mit der Fraunhofer-Zentrale Verhandlungen begonnen, um den bestehenden Kooperationsvertrag erneut zu verlängern.

Im November 2015, auf dem ersten Fraunhofer-Tag in Schleswig-Holstein in Lübeck – eine von der Fraunhofer-Zentrale, dem Kieler Wirtschaftsministerium und der IHK Schleswig-Holstein veranstalteten Leistungsschau von insgesamt neun Fraunhofer-Instituten – stellte das ISIT neben den aktuellen Arbeitsergebnissen und Forschungsvorhaben auch ein für das Institut eher ungewöhnliches Projekt vor, eine einzigartige Kooperation des ISIT mit der Muthesius Kunsthochschule Kiel.

In einer Ausstellung präsentierte das ISIT in Lübeck eine Dokumentation der besten künstlerischen Arbeiten als Abschluss eines Wettbewerbes, den wir mit der Kieler Kunsthochschule ins Leben gerufen hatten. Die fast 100 beteiligten Studenten der Muthesius Kunsthochschule beschäftigten sich mit der Aufgabe, die gesellschaftliche und kulturelle Bedeutung der Mikrosystemtechnik und Mikroelektronik mit künstlerischen und gestalterischen Mitteln darzustellen.

Es überraschte die Vorstellung der vielen Skizzen, Modelle, multimedialen Animationen und Filme. Die

PREFACE

Karin Pape

Dr. Wolfgang Windbracke

All 22 excellent communicative solutions are showcased in the documentation along with reports about each work from the mentors: Prof. Silke Juchter, Prof. Tom Duscher, Prof. Detlef Rhein and Prof. Wolfgang Sasse. A selection of the work can be viewed on the next two pages.

For nearly two decades, Fraunhofer ISIT has been established in Itzehoe as a leading research institute for power electronics and microsystems engineering technologies. Some of the employees who did much to shape and promote the institute's development are now reaching retirement. In the last year, this included Karin Pape and Dr. Wolfgang Windbracke from the institute's management. When Fraunhofer ISIT was set up in Itzehoe, Ms. Pape integrated her Neumünster-based CEM gGmbH (Centrum für Mikroverbindungstechnik in der Elektronik) into the institute as the Advanced Packaging group and successfully led it with many projects and clients.

Dr. Windbracke planned and carried out the move for his IC Technology department from Berlin to Itzehoe. In subsequent years, he ensured that the right decisions were

Arbeiten waren von Originalität und Persönlichkeit geprägt, zeigten sowohl Humor als auch Ernsthaftigkeit, Romantik oder auch Sarkasmus. Ob improvisiert oder professionell ausgearbeitet, jede Umsetzung vermittelte uns Einblick in die Visionen, Sorgen und Hoffnungen einer Generation, die schon jetzt selbstverständlich angenommen hat, was von uns manchmal noch als Innovation gefeiert wird.

Die vorgestellte Dokumentation zeigt alle 22 ausgezeichneten kommunikativen Lösungen, aufgenommen wurden auch die Werkberichte der betreuenden Professoren Prof.in Silke Juchter, Prof. Tom Duscher, Prof. Detlef Rhein und Prof. Wolfgang Sasse. Eine Auswahl der Arbeiten finden Sie auf den nächsten beiden Seiten.

Das ISIT hat sich in fast zwei Jahrzehnten als führendes Forschungsinstitut für Technologien der Leistungselektronik und Mikrosystemtechnik in Itzehoe etabliert. Einige Mitarbeiterinnen und Mitarbeiter, die den Aufbau maßgeblich mitgestaltet und vorangetrieben haben, erreichen nun ihren Ruhestand. Für die Instituts- und Abteilungsleitung betraf das im letzten Jahr Karin Pape und Dr. Wolfgang Windbracke. Frau Pape hat nach der ISIT Errichtung in Itzehoe ihre Einrichtung aus Neumünster, die CEM gGmbH (Centrum für Mikroverbindungstechnik in der Elektronik), als eigene Abteilung für Aufbau- und Verbindungstechnik ins ISIT integriert und mit vielen Projekten und Auftraggebern erfolgreich geführt.

Herr Dr. Windbracke hatte den Umzug seiner Abteilung für IC-Technologie aus Berlin nach Itzehoe geplant und umgesetzt. In den darauffolgenden Jahren hat er bei allen wichtigen strategischen Entscheidungen zur

Presentation of the ISIT cooperation with the Muthesius Kunsthochschule Kiel. Manuel Reitz, Björn Engholm, Prof. Tom Duscher, Prof. Silke Juchter, Minister of Economic Affairs Reinhard Meyer; Lübeck, November 24, 2015

Bottom:
Mark Helfrich MdB (left) with ISIT employees at AzubIZ, Itzehoe, September 18

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Tronics Microsystems

made in all of the major strategic considerations regarding the institute's orientation. Dr. Windbracke temporarily took on the role of managing director at Fraunhofer ISIT in 2007 and 2008, then continued to guide Fraunhofer ISIT's development as a member of the institute management.

Fraunhofer ISIT owes heartfelt thanks to these two, and many other employees who have already left, for their many successful projects and planning results.

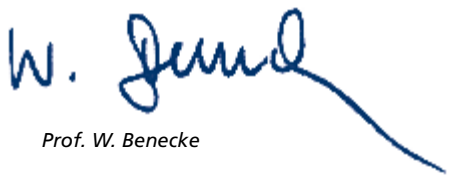
On behalf of my colleagues here at Fraunhofer ISIT, I would also like to say thank you to all of our partners, customers and patrons for your trust and cooperation. I hope you get many interesting new ideas from reading this report.

We look forward to exchanging ideas with you!

Ausrichtung des Instituts für richtige Weichenstellungen gesorgt. In den Jahren 2007 und 2008 wurde das gesamte ISIT von Dr. Windbracke kommissarisch geleitet. Anschließend hat Herr Windbracke als Mitglied der Institutsleitung die Entwicklungen des ISIT weiter mit gelenkt.
Für ihre vielen Projekterfolge und zahlreichen Planungsergebnisse schuldet das ISIT diesen beiden wie auch den weiteren, bereits ausgeschiedenen Mitarbeiterinnen und Mitarbeitern, großen Dank

Auch bedanke ich mich im Namen der Kolleginnen und Kollegen des ISIT bei allen Partnern, Auftraggebern und Förderern für die vertrauensvolle Zusammenarbeit und hoffe, dass Sie beim Lesen des Berichtes viele interessante Anregungen aufnehmen.

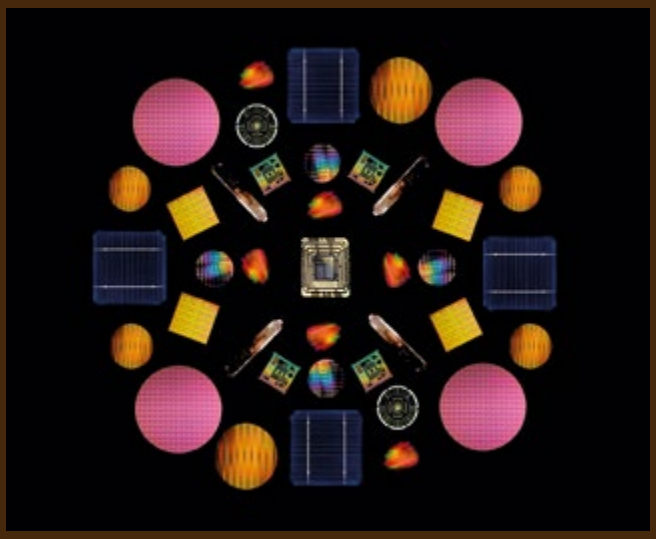
Wir freuen uns auf den Gedankenaustausch mit Ihnen!



Prof. W. Benecke

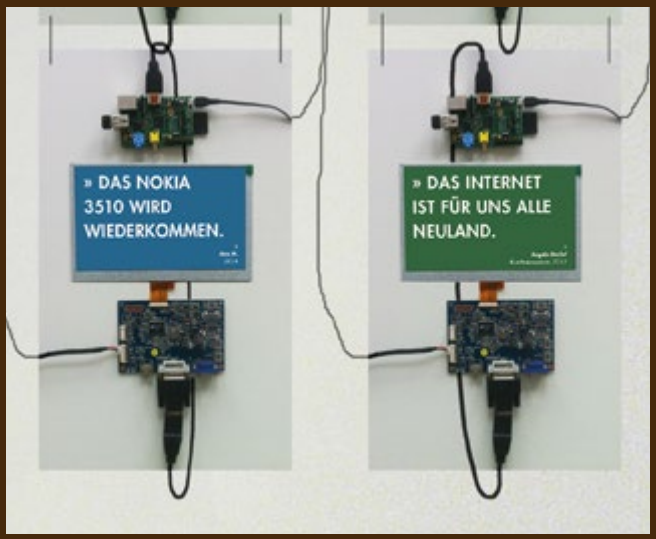

Fraunhofer ISIT

Rhizopoda Radiata, Robin Lison, Fine Arts/Media Art



Am Anfang war Silizium, Celina Golz, Communication Design, Typography

The Internet Is Just A Hype, Manuel Reitz, Interactive Media



MIKROELEKTRONIK AUS DEM BLICKWINKEL DER KUNST

Lässt sich Unsichtbares sichtbar machen? Wie kann die gesellschaftliche und kulturelle Bedeutung der Mikrosystemtechnik und Mikroelektronik mit künstlerischen und gestalterischen Mitteln dargestellt werden? Dieser Frage stellten sich Studierende der Muthesius Kunsthochschule in einem einzigartigen Kooperationsprojekt mit dem Fraunhofer ISIT.
Die Dokumentation zeigt alle ausgezeichneten Wettbewerbsarbeiten.
S. Juchter, W. Sasse, T. Duscher (Hrsg.). **Invisible. Wie die Mikroelektronik unser Leben verändert.** Katalogdokumentation. Muthesius Kunsthochschule, Kiel 2015. ISBN 978-3-943763-41-6. Schutzgebühr:10 €
Zu beziehen über das Pressebüro der Muthesius Kunsthochschule, Legienstraße 35, 24103 Kiel, presse@muthesius.de T +49 (0)431-5198-471

App zum Fraunhofer-Projekt unter http://invisible.muthesius.de/app

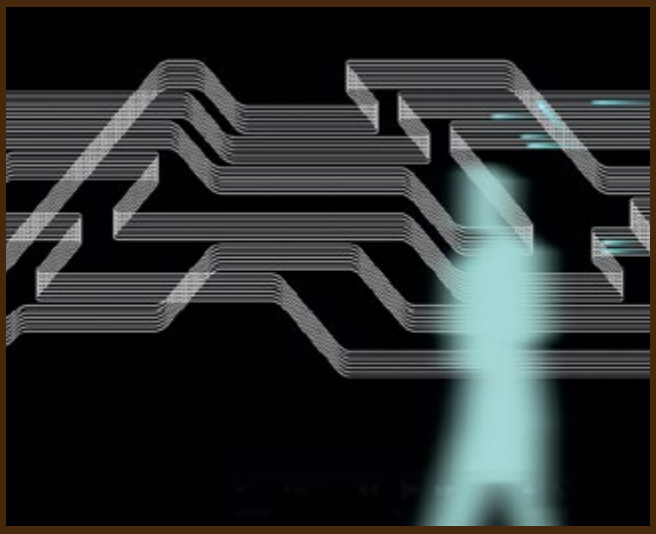
MICROELECTRONICS FROM THE PERSPECTIVE OF ART

Can we make invisible visible? How can the social and cultural significance of microsystems technology and microelectronics be presented with artistic and creative means? Students of the Muthesius University in Kiel presented in an unique cooperation project with Fraunhofer ISIT this question.
The documentation contains all award-winning art works of the contest.

S. Juchter, W. Sasse, T. Duscher (ed.). ***Invisible. Wie die Mikroelektronik unser Leben verändert.*** *Catalogue documentation.Muthesius Kunsthochschule, Kiel 2015. ISBN 978-3-943763-41-6. dt./engl. Nominal charge: 10 €*
To be obtained via the press office of Muthesius Kunsthochschule, Legienstraße 35, 24103 Kiel, presse@muthesius.de T +49 (0)431-5198-471

App of the project with Fraunhofer ISIT: http://invisible.muthesius.de/app

Das Mosaik, Arnulf Lubitz, Communication Design, Typography



Leiterbahnen Netzwerk, Joshua von Hofen, Interactive Media

Cyborgs, Laura Binder, Communication Design, Print Magazine

Mela, Henrike Schrödter, Industrial Design, Medical Design

BRIEF PORTRAIT

The ISIT building complex

FRAUNHOFER-INSTITUT FÜR SILIZIUMTECHNOLOGIE (ISIT)

Research and Production at One Location

The Fraunhofer Institute for Silicon Technology ISIT develops and produces power electronics and microsystems according to customers specifications. Important areas of application include energy technology, automotive and transport engineering, the consumer goods industry, medical technology, communications technology, and automation. Ultra-modern technological equipment based on 200 mm silicon wafer technology and expertise built up over decades put Fraunhofer ISIT and its customers at the forefront of the field worldwide.

Fraunhofer ISIT supports customers right the way from design and system simulation to the production of prototypes, samples, and preparation for series production. The institute currently employs a staff of 160 persons with engineering and natural sciences backgrounds.

Fraunhofer ISIT deals with all the important aspects of system integration, assembly and interconnection technology (packaging), and the reliability and quality of components, modules, and systems. The institute also provides manufacturing support for application-specific integrated circuits (ASICs) to operate sensors and actuators. Activities are rounded off by the development of electrical energy storage devices, with a focus on Li-polymer batteries.

One point that really sets Fraunhofer ISIT apart is the speed with which it can transfer innovative developments into industrial application and production. To this end, Fraunhofer ISIT operates a wafer production line in its cleanrooms in collaboration with the companies Vishay and X-FAB MEMS Foundry Itzehoe. There are longstanding collaborations with a variety of manufacturing companies local to Fraunhofer ISIT.

Fraunhofer ISIT runs an application center at Hamburg University of Applied Sciences, a project group at the University of Applied Sciences in Heide, and a working group at the Christian-Albrechts-Universität in Kiel.

MAIN FIELDS OF ACTIVITY

Customized glass wafer for opto packages on wafer level

MICROSYSTEMS TECHNOLOGY, MEMS AND IC DESIGN

Research in microsystems technology is a major activity of Fraunhofer ISIT in different departments. For 30 years ISIT scientists are working on the development of micro electro mechanical systems (MEMS). This covers the complete development chain starting from simulation and design, technology and component development up to waferlevel probing, process qualification, and reliability tests. One of the core competences of the ISIT service offer is the development of integration technologies, like cost effective assembly of several chips in a common package, MEMS packaging on waferlevel (WLP) with defined cavity pressure or a system-on-chip approach. MEMS devices can be combined with suitable ASICs to miniaturized systems with high functionality. ISIT has also the possibility to offer fabrication of prototypes and low volume pilot production. If high volume MEMS production is requested the on-site operating industrial partner X-FAB MEMS Foundry Itzehoe GmbH is able to meet this demand. All services are offered on a 200 mm wafer technology-platform.

ISIT is focussed on MEMS applications in the following areas: physical sensors and actuators, devices and technologies for high frequency application (RF-MEMS), passive and active optical MEMS as well as piezoelectric MEMS. In the field of sensor systems strong activities are put on multi-axis inertial sensors (accelerometer, gyroscopes), magnetometers and on flow sensors. MEMS for high frequency applications are primarily used in wireless reconfigurable communication networks. In particular developments for RF-MEMS switches, ohmic switches and waferlevel packaging (WLP) are ongoing. In the field of optical MEMS devices ISIT is active in the development of micromirrors for laser projection displays and optical measurement systems based on scanning micromirrors, e.g. LIDAR. Passive optical components based on borosilicate or quartz glass wafer processing are also in the portfolio of ISIT. Examples are glass lens arrays, aperture systems for laser beam forming and waferlevel packaging of optical MEMS. The microsystems department has access to the standard front-end technologies for IC-processing and operates a separate new installed cleanroom with dedicated MEMS specific equipment and processes. The lithographic capabilities include a wide-field stepper, backside mask aligner, spray coating and thick resist processing. CVD, PVD and ALD tools for the deposition of poly-Si, SiGe, SiO_2, SiN, Ge, Au, Pt, Ir, Ag, Al, Cu, Ni, Cr, Mo, Ta, Ti, TiN, TiW, Al_2O_3, AlN, PZT and other thinfilms are available. The wet processing area comprises anisotropic etching of Si, automated tools for metal etching and electroplating of Au, Cu and Sn. In case of dry etching, equipment for DRIE of Si and RIE of oxidic compounds is available. MEMS release etching can be performed using HF and XeF_2 gas phase etching or wet etching followed by critical point drying. A specific focus is given to hermetic waferlevel packaging of MEMS using metallic, anodic or glass frit waferbonding technology. Wafer grinding and temporary

Prototype of a MEMS actuator chip

waferbonding are key process steps for thin wafer and 3D integrated products including through silicon vias. Of high importance for many MEMS, but also electronic products is the capability in chemical-mechanical polishing (CMP). The CMP application lab focusses on the development of polishing processes for Si, silicon oxides, W and Cu (damascene), and also on testing of slurries and polishing pads.

In addition to the single processes, ISIT has established a number of qualified technology platforms. Examples are the thick poly-Si surface micromachining platform for capacitive sensors/actuators and the piezoelectric MEMS platform. In the latter case sputtered thin PZT or AlN layers with suitable bottom and top electrodes are integrated in a complete process flow for piezoelectric MEMS transducers.
Beyond technology the microsystems department offers the design and realization of dedicated electronic circuits for driving/readout of the MEMS components, but also for MEMS testing and system demonstration. Moreover, an experienced ASIC design team is specialized in the design of analog/digital circuits to be integrated in smart systems. The designers also model micromechanical and micro optic elements and test their functionality in advance using FEM and behavorial modeling simulation tools. A final characterization on wafer level or module level allows the verification of the design as well as the used technology.

Microsystems Technology

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IC Design

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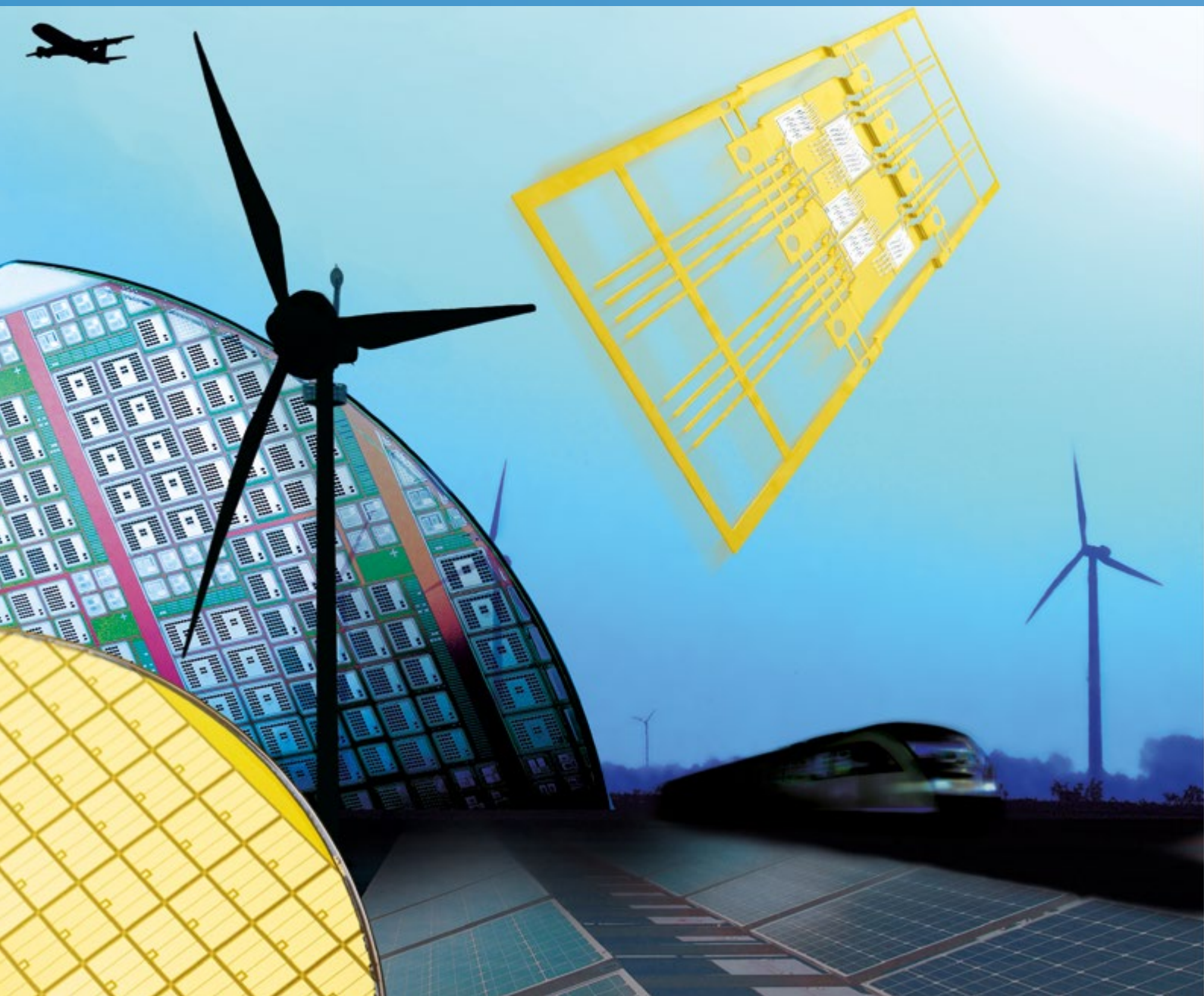
MAIN FIELDS OF ACTIVITY

IC TECHNOLOGY AND POWER ELECTRONICS



The power electronics and IC technology group develops and manufactures active integrated circuits as well as discrete passive components.

Among the active components the emphasis lies on Silicon power devices such as smart power chips, IGBTs, PowerMOS circuits and diodes. In this context application specific power devices and new device architectures are special R&D areas. The development of new processes for advanced power device assembly on wafer level is a further important research topic. Application specific semiconductor devices with non standard metallization layers and adapted layouts for chip geometry and pad configurations are offered for new assembly techniques. Novel techniques for handling and backside processing of ultra thin Silicon substrates based on carrier wafer concepts and laser annealing processes are being used for power device development. Customized trade-off adjustment of static-dynamic losses and robustness are prerequisite for power electronic system optimization and can be developed according to customer requirements.

Additional support is provided by a number of tools for simulation, design and testing. ISIT also benefits from years of experience in the design and manufacturing of CMOS circuits.

Passive components developed and fabricated at ISIT are primarily chip capacitors, precision resistors and inductors. Implementation of new materials and alloys into existing manufacturing processes is an important feature in the development process.

ISIT develops individual processes, process modules and complete process flows for diverse applications. The institute also offers processing of customer specific silicon components in small to medium sized quantities on the basis of a qualified semiconductor process technology.

A special R&D group with focus on power electronic systems works on application specific topics covering the interface to system end users. New circuit topologies based on system specific semiconductor power devices are special R&D topics for system optimization.

In the field of power electronics ISIT coordinates an Innovation Cluster dealing with power electronics for renewable energies. This cluster was founded in close cooperation with companies and universities of the federal state of Schleswig-Holstein.

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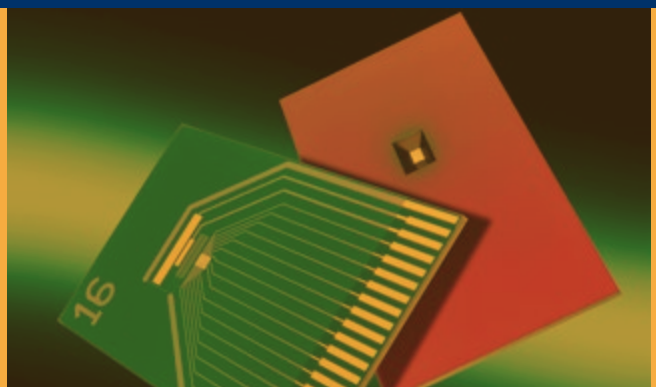

Micropore membrane chip with electrodes for electrochemical analyses

Lactate sensors on flexible substrate

BIOTECHNICAL MICROSYSTEMS

The department BTMS develops and produces silicon based microsystems for high sophisticated biosensors used in miniaturized and mobile analysis platforms. The research focus addresses especially the topic "microsystems for health". Electrical micro-electrode array based tests are a main research field of the department. Position-specific applications are realized by immobilization of biomolecules and highly sensitive, highly selective measurement methods such as the "redox cycling". These very robust sensor systems are useful for the simultaneous detection of a variety of analytes within one sample. In combination with micro-fluidic components and integrated electronics, these electrical microarrays represent the basis of rapid and cost-effective analysis systems. They can be used to identify and quantify DNA, RNA, proteins and haptens.

In a further field of activity biosensors for the continuous monitoring, e.g. of metabolites as glucose or lactate are developed. The monitoring and quantification of these substances is realized by enzymatic conversion and electrochemical detection. These sensors are also used in combination with pH-measurement and -control in bioreactors. In the BMBF-funded project "Cell-free bioproduction" ISIT integrates microelectrodes on pore membranes and also in microreactor systems for example (www.zellfreie-bioproduktion.fraunhofer.de).

For a wider range of mobile analytics, ISIT develops microsystems based on a liquid chromatographic separation process. Various materials, process technologies and system integration technologies are investigated. The aim of this development is an integrated microsystem for detection of contaminants and residues for a sustainable environment, food and health management.

Biotechnical Microsystems
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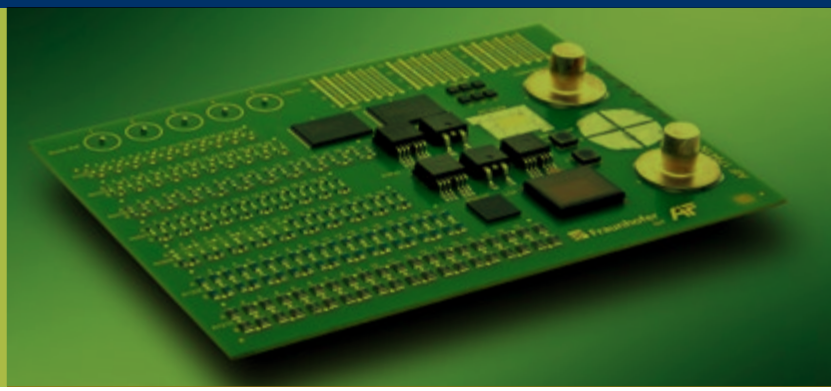

SMD testboard

PACKAGING TECHNOLOGY FOR MICROELECTRONICS AND MICROSYSTEMS

The "Advanced Packaging" group is specialized in the identification and the promotion of new trends and technologies in electronics packaging. The industrial challenges of tomorrow are addressed in direct collaboration with suppliers of materials, components, modules, and equipment. As an example, the automatic pick-and-place assembly of ultra-thin dies on flexible substrates was already developed several years ago. For the encapsulation of MEMS components, the glass frit bonding and metallic bonding was developed. ISIT also participates in the development of organic electronics (functional printing) and RFID technologies.

The Fraunhofer ISIT is equipped with all the basic technologies for automatic or manual handling of microchips and MEMS-devices, as well as electrical interconnect methods like wire bonding and flip chip technologies. Sintered power electronic assemblies with improved power-cycle performance can be developed and connected by thick wire and ribbon bonding technology based on aluminum and copper wire/ribbon up to 200 µm x 2000 µm cross section. Through the close relationship between MEMS technology and packaging under the roof of ISIT, the institute has become a leading R&D service provider in the domain of waferlevel-packaging. A cross-disciplinary technology portfolio is now available that allows to reduce cost and size of a system. Even more, the packaging itself can become a functional part of the microsystem in many cases, e.g. by integrating optical elements or directly interconnecting MEMS and ASIC dies. Outstanding success was achieved in the vacuum encapsulation of micromechanical sensors by eutectic wafer bonding, which paved the way towards the industrialization of an automotive yaw-rate sensor product family.
ISIT continuously expands their assortment of test chips and -substrates that facilitate the ramp up and calibration of production lines for securing quality on a high level.

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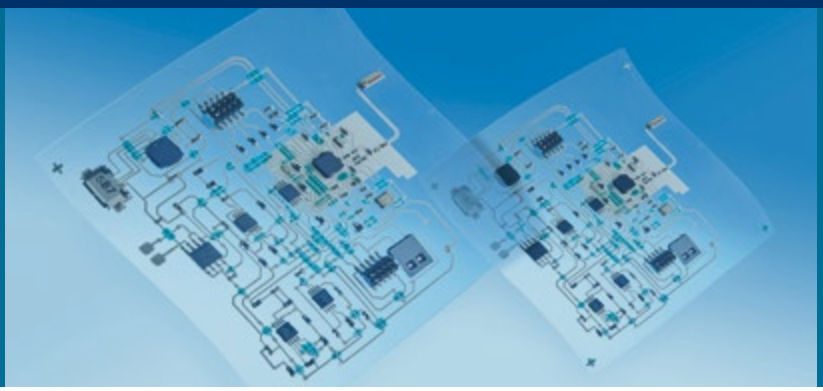

Hybrid sensor system for lactate detection

QUALITY AND RELIABILITY OF ELECTRONIC ASSEMBLIES

Quality evaluation – in particular for the soldering work done in pre-production, pilot and main series lots – represents a continuous challenge for ISIT, as for example whenever new technologies such as lead-free soldering are introduced, or when increased error rates are discovered, or if a customer desires to achieve competitive advantages through continual product improvement.

Important fields of activity are quality assessment, reliability of electronic part, modules and systems. Moreover evaluation and standardization of test methods for quality assessment of printed and hybrid electronics are being developed.

To reveal potential weak points, ISIT employs both destructive and non-destructive analysis methods, such as X-ray transmission radiography, computer tomography, laser profilometry and scanning acoustic microscopy. Working from a requirements matrix, ISIT scientists also evaluate long-term behavior of lead-free and lead-containing assemblies alike. They then formulate prognoses on the basis of model calculations, environmental and time-lapse load tests, and failure analysis.

In anticipation of a conversion to lead-free electronics manufacturing, Fraunhofer ISIT is undertaking design, material selection and process modification projects for industrial partners. To effect a further optimization of manufacturing processes, the institute applies process models and produces samples on industry-compatible equipment. The group also addresses issues related to thermal management and reliability for customer-specific power modules.

In addition to these technological activities, the group regularly holds training sessions, including multi-day classes, at the institute or at company site.

Quality and Reliability of Electronic Assemblies
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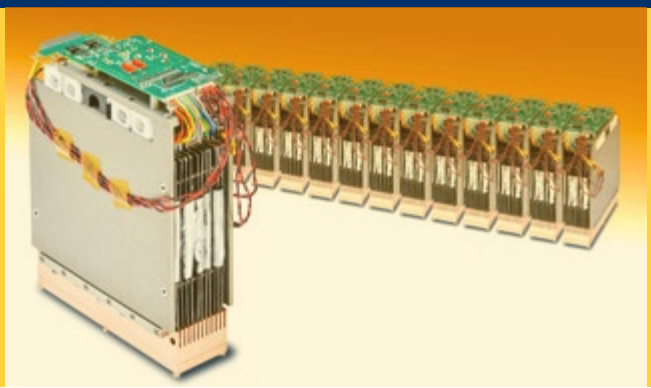
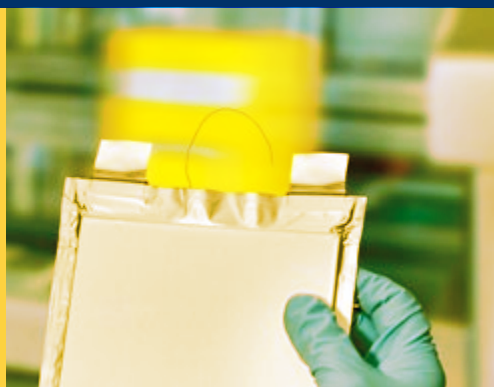


Lithium booster battery module with 12 high performance cells and integrated electronics; backround: complete battery



Lithium polymer cell with integrated temperature sensor

INTEGRATED POWER SYSTEMS

Secondary lithium batteries as a powerful storage medium for electrical energy are rapidly capturing new fields of application outside of the market of portable electronic equipment. These new fields include automobiles, medical devices, stationary electric storage units, aerospace, etc. Therefore, this type of rechargeable batteries has to meet a variety of new requirements. This covers not only electrical performance but also design and safety features. The lithium polymer technology developed at ISIT is characterized by an extensive adaptability to specific application profiles like extended temperature range, high power rating, long shelf and/or cycle life, extended safety requirements, etc (tailor-made, energy storage solutions). Also included is the development of application-specific housings.

In the lithium polymer technology all components of the cell from electrodes to housing are made from tapes. At ISIT the complete process chain starting with the slurry preparation over the tape casting process and the assembly and packaging of complete cells in customized designs is available including also the electrical and thermo-mechanical characterization. This allows access to all relevant parameters necessary for an optimization process. The electrode and the electrolyte composition up to the cell design can be modified.
In addition to the development of prototypes, limited-lot manufacturing of optimized cells on a pilot production line at ISIT with storage capacities of up to several ampere-hours is possible. Specific consideration in process development is addressed to the transferability of development results in a subsequent industrial production.

ISIT offers a wide portfolio of services in the field of secondary lithium batteries:

- Manufacturing and characterization of battery raw materials by half cell as well as full cell testing
- Selection of appropriate combinations of materials and design of cells to fulfill customer requirements
- Application driven housing development
- Test panel
- Prototyping and limited-lot manufacturing of cells

Additional services are:

- Preparation of studies
- Failure analysis
- Testing (electrical, mechanical, reliability etc.)
- Technical consultation

Integrated Power Systems
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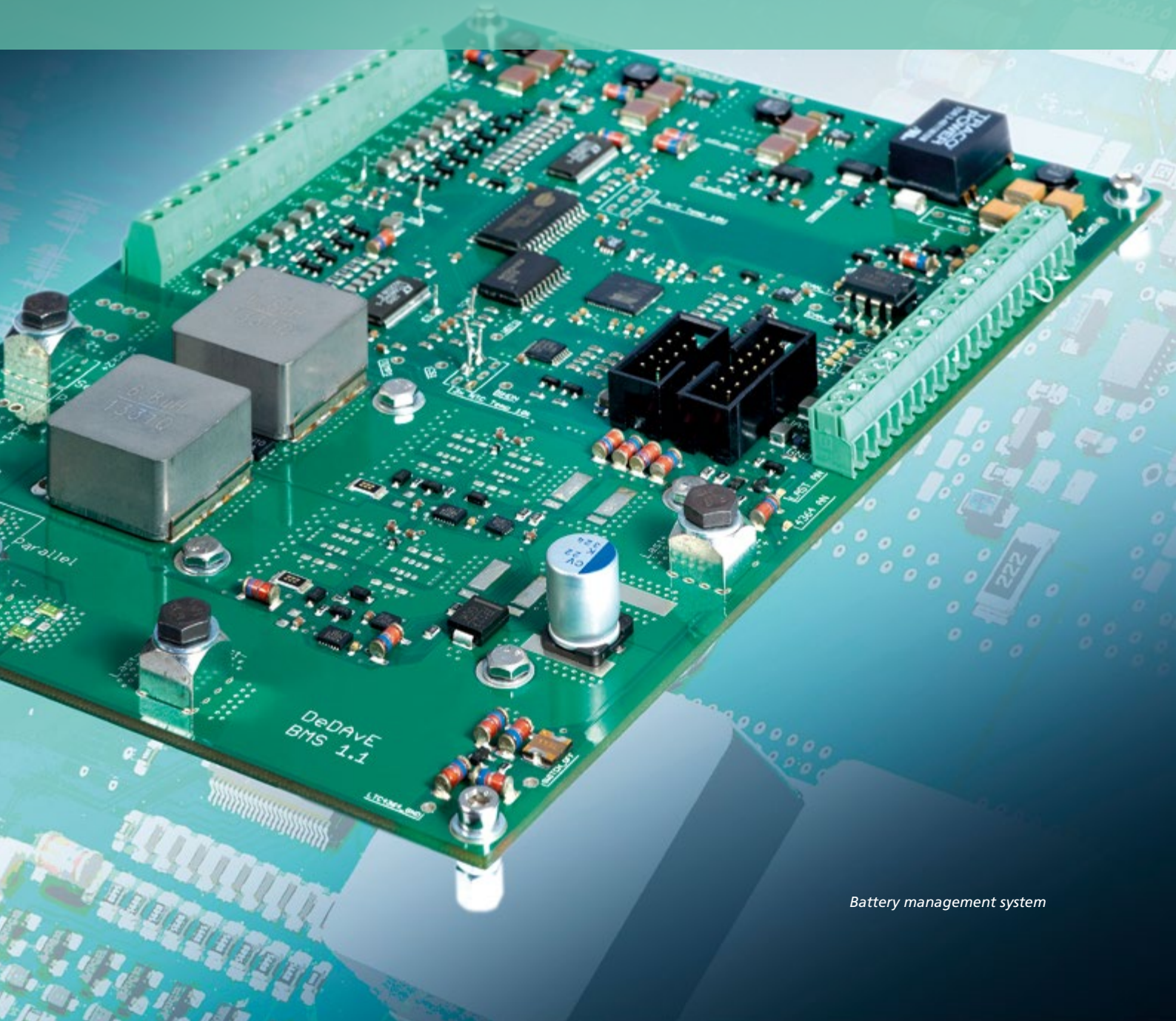
OFFERS FOR RESEARCH AND SERVICE



Battery management system

Infrastructure and production level of the new cleanroom

FACILITIES AND EQUIPMENT

Fraunhofer ISIT has access to a 200 mm silicon technology line (2500 m²) for front-end processes (MOS and PowerMOS). Specific processes for MEMS and NEMS as well as for packaging are implemented in a new cleanroom (1000 m²), dedicated to microsystems technology. This includes wet etching, dry etching, DRIE, deposition of non-IC-compatible materials, lithography with thick-resist layers, gray-scale lithography, electroplating, microshaping, and wafer bonding. Further cleanroom laboratories are set up for chemical-mechanical polishing (CMP) and post-CMP processing.

Extra laboratories covering an area of 1500 m² are dedicated to electrical and mechanical characterization of devices, assembly and interconnection technology, and reliability testing. Fraunhofer ISIT also operates a pilot production line for Li-polymer batteries. The institute's facilities have been certified to ISO 9001:2008 for many years.

RANGE OF SERVICES

The institute's services assist companies and users in a wide range of sectors. Components, systems, and production processes are developed, simulated, and implemented in close collaboration with customers. This process is aided by Fraunhofer ISIT's use of technology platforms – production process flows defined for whole groups of components – meaning they can be used in production unchanged or with simple modifications to the design parameters.

Fraunhofer ISIT's expertise presents particularly exciting possibilities for small and medium-sized enterprises looking for realizing their technological innovations.

CUSTOMERS

ISIT cooperates with companies of different sectors and sizes.
In the following, some companies are presented as a reference:

3-D-Micromag GmbH, *Chemnitz*

ABB AG, *Ladenburg*

Adam Opel AG, *Rüsselsheim*

Advaplan, *Espoo, Finland*

Airbus-Systeme, *Buxtehude*

Airbus Defense and Space, *Ulm*

aixACCT Systems GmbH, *Aachen*

alpha-board GmbH, *Berlin*

Alpha Metals Lötsystem GmbH, *Langenfeld*

Amicra Microtechnologies GmbH, *Regensburg*

Analog Devices, *Ireland*

Analytik Jena AG, *Jena*

Andus electronic GmbH, *Berlin*

Asteelflash Hersfeld GmbH, *Bad Hersfeld*

Atotech Deutschland GmbH, *Berlin*

ams AG, *Unterpremstätten, Austria*

Basler AG, *Ahrensburg*

BesB GmbH, *Berlin*

Besi APac Sdn. Bhd. *Shah Alam, Malaysia*

Besi Austria GmbH, *Radfeld, Austria*

Bioservo Technologies AB, *Stockholm, Schweden*

Bosch Sensortec GmbH, *Reutlingen*

B. Braun Melsungen AG, *Melsungen*

H. Brockstedt GmbH, *Kiel*

Brose Fahrzeugteile GmbH&Co.KG, *Hallstadt*

Brückner Maschinenbau GmbH & Co. KG, *Siegsdorf*

CAPRES A/S, *Kongens Lyngby, Denmark*

CarboFibretec GmbH, *Friedrichshafen*

Cassidian Electronics, *Ulm*

CCI GmbH, *Itzehoe*

Christian Koenen GmbH, *Ottobrunn-Riemerling*

Condias GmbH, *Itzehoe*

Continental Automotive GmbH, *Karben*

Conti Temic microelectronic GmbH, *Nürnberg*

Coronet Electronic GmbH, *Neuhausen*

Danfoss Drives A/S, *Graasten, Denmark*

Danfoss Silicon Power GmbH, *Flensburg*

davengo GmbH, *Berlin*

Diehl Avionik Systeme GmbH, *Überlingen*

Disco Hi-Tec Europe GmbH, *München*

Dräger Safety AG & Co. KG, *Lübeck*

Dräger Systemtechnik, *Lübeck*

EADS Deutschland GmbH, Corporate Research Germany, *München and Ulm*

Endress + Hauser GmbH Co. KG, *Maulburg*

Engineering Center for Power Electronics GmbH, *Nürnberg*

EPCOS AG, *München*

Eppendorf Instrumente GmbH, *Hamburg*

ERSA GmbH, *Wertheim*

ESCD GmbH, *Brunsbüttel*

ESPROS Photonics AG, *Switzerland*

Evonik Litarion GmbH, *Kamenz*

Exceet Security Systems, *Düsseldorf*

Freudenberg Gruppe, *Weinheim*

FMP TECHNOLOGY GMBH, *Erlangen*

FTCAP GmbH, *Husum*

GÖPEL electronic GmbH, *Jena*

Hako GmbH, *Bad Oldesloe*

Hannusch Industrieelektronik, *Laichingen*

Harman Becker Automotive Systems GmbH, *Karlsbad*

Hella KG, *Lippstadt*

Heraeus Materials Technology GmbH Co. KG, *Hanau*

Honeywell Deutschland AG, *Offenbach*

ifm ecomatic GmbH, *Kressbronn*

ifm electronic GmbH, *Essen*

IMS Nanofabrication AG, *Wien, Austria*

Innovavent GmbH, *Göttingen*

Isola GmbH, *Düren*

ISRA Vision AG, *Darmstadt*

Jenoptik Automatisierungstechnik GmbH, *Jena*

Jenoptik ESW GmbH, *Wedel*

Jonas & Redmann Group GmbH, *Berlin*

Jungheinrich AG, *Norderstedt*

Kristronics GmbH, *Harrislee-Flensburg*

Kuhnke GmbH, *Malente*

Lenze Drive Systems GmbH, *Hameln*

Liebherr Elektronik GmbH, *Lindau*

LightStat LCC, *Texas, USA*

Mair Elektronik GmbH, *Neufahrn*

Marum, *Bremen*

Märzhäuser Wetzlar GmbH, *Wetzlar*

Maxim Integrated GmbH, *Lebring, Austria*

Meder eletronic AG, *Engen-Welschingen*

Melexis Ieper N.V., *Belgium*

MicroMountains Applications AG, *Villingen-Schwenningen*

Miele & Cie KG, *Lippstadt*

MKS Instruments Deutschland GmbH, *München*

NXP Semiconductors Germany GmbH, *Hamburg*

Oerlikon AG, *Liechtenstein*

Okmetic Oyj, *Vantaa, Finland*

OSRAM GmbH, *München*

OSRAM Opto Semiconductors GmbH, *Regensburg*

Otto Bock HealthCare GmbH, *Duderstadt*

PAC Tech, Packaging Technologies GmbH, *Nauen*

Panasonic Automotive Systems Europe GmbH, *Lüneburg*

Peter Wolter GmbH, *Rendsburg*

Picosun Oy, *Espoo, Finland*

Plan Optik AG, *Elsoff*

Plath EFT GmbH, *Norderstedt*

PRETTL Elektronik Lübeck GmbH, *Lübeck*

Prodrive Technologies, *Eindhoven, Netherlands*

Raytheon Anschütz GmbH, *Kiel*

Reese + Thies Industrieelektronik GmbH, *Itzehoe*

RefuSol GmbH, *Metzingen*

Rehm Anlagenbau GmbH, *Blaubeuren-Seissen*

Renault SA, *Boulogne, Billancourt, France*

Robert Bosch GmbH, *Reutlingen*

Robert Bosch GmbH, *Salzgitter*

ROHDE & SCHWARZ GmbH & Co. KG, *München*

SAES Getters S.p.A., *Lainate/Milan, Italy*

SAFT SA, *Bagnolet, France*

Sandvik Tooling Supply Germany, *Schmalkalden*

Science&Motion Sports GmbH, *Rüsselsheim*

Sensitec GmbH, *Lahnau*

Senvion SE, *Osterröhnfeld*

Senvion Wind Energy Solutions, *Hamburg*

SGL Carbon GmbH, *Meitingen*

SMA Regelsysteme GmbH, *Niestetal*

Solvionic Site SNPE, *Toulouse, France*

STABILO International GmbH, *Heroldsberg*

Still GmbH, *Hamburg*

Stolle Sanitätshaus GmbH, *Hamburg*

tagitron GmbH, *Salzkotten*

Technolas Perfect Vision GmbH, *München*

TESAT SPACECOM GmbH, *Backnang*

Theon, *Athens, Greece*

Trainalytics GmbH, *Lippstadt*

Trinamic Motion Control GmbH & Co. KG, *Hamburg*

Umicore AG & Co., *Hanau*

Umicore NV, *Olen, Belgium*

USound GmbH, *Graz, Austria*

Vectron International GmbH & Co. KG, *Neckarbischofsheim*

Venneos GmbH, *Stuttgart*

Vishay BCcomponents BEYSCHLAG GmbH, *Heide*

Vishay Siliconix Itzehoe GmbH, *Itzehoe*

Vishay Siliconix, *Santa Clara, USA*

VocalZoom, *Yokneam Ilit, Israel*

Volkswagen AG, *Wolfsburg*

WABCO GmbH, *Hannover*

Würth Elektronik GmbH, *Schopfheim*

X-FAB MEMS Foundry Itzehoe GmbH, *Itzehoe*

X-FAB Semiconductor Foundries AG, *Erfurt*

INNOVATION CATALOGUE

ISIT offers its customers various products and services already developed for market introduction. The following table presents a summary of the essential products and services. Beyond that the utilization of patents and licences is included in the service.

Product / Service	Market	Contact Person
Testing of semiconductor manufacturing equipment	*Semiconductor equipment manufacturers*	*Dr. Gerfried Zwicker + 49 (0) 4821/17 -4309 gerfried.zwicker@isit.fraunhofer.de*
Chemical-mechanical polishing (CMP), planarization	*Semiconductor device manufacturers*	*Dr. Gerfried Zwicker + 49 (0) 4821/17 -4309 gerfried.zwicker@isit.fraunhofer.de*
Wafer polishing	*Si substrates for device manufacturers*	*Dr. Gerfried Zwicker + 49 (0) 4821/17 -4309 gerfried.zwicker@isit.fraunhofer.de*
IC processes and power devices CMOS, PowerMOS, IGBTs Diods	*Semiconductor industry IC-users*	*Detlef Friedrich + 49 (0) 4821/17 -4301 detlef.friedrich@isit.fraunhofer.de*
Single processes and process module development	*Semiconductor industry semiconductor equipment manufacturers*	*Detlef Friedrich + 49 (0) 4821/17 -4301 detlef.friedrich@isit.fraunhofer.de*
Customer specific processing	*Semiconductor industry semiconductor equipment manufacturers*	*Detlef Friedrich + 49 (0) 4821/17 -4301 detlef.friedrich@isit.fraunhofer.de*
Microsystem products	*Electronic industry*	*Prof. Ralf Dudde + 49 (0) 4821/17 -4212 ralf.dudde@isit.fraunhofer.de*
MEMS process development and integration	*Electronic industry*	*Björn Jensen + 49 (0) 4821/17 -1434 bjoern.jensen@isit.fraunhofer.de*
Battery management systems	*Portable devices subsea vehicles automotive*	*Dr. Dirk Kähler + 49 (0) 4821/17 -4604 dirk.kaehler@isit.fraunhofer.de*
Inertial sensors	*Motorvehicle technology, navigation systems, measurements*	*Dr. Klaus Reimer + 49 (0) 4821/17 -4213 klaus.reimer@isit.fraunhofer.de*
Piezoelectric microsystems	*Sensors and actuators*	*Dr. Dirk Kaden + 49 (0) 4821/17-4606 dirk.kaden@isit.fraunhofer.de*
Microoptical scanners and projectors	*Biomedical technology, optical measurement industry, telecommunication*	*Dr. Ulrich Hofmann + 49 (0) 4821/17 -4553 ulrich.hofmann@isit.fraunhofer.de*
Flow sensors	*Automotive, fuel cells*	*Dr. Thomas Lisec +49 (0) 4821/17 -4512 thomas.lisec@isit.fraunhofer.de*
Microoptical components	*Optical measurement*	*Hans-Joachim Quenzer + 49 (0) 4821/17 -4643 hans-joachim.quenzer@isit.fraunhofer.de*
RF-MEMS	*Telecommunication*	*Dr. Thomas Lisec + 49 (0) 4821/17 -4512 thomas.lisec@isit.fraunhofer.de*

Product / Service	Market	Contact Person
Beam deflection components for maskless nanolithography	*Semiconductor equipment manufacturers*	*Dr. Klaus Reimer + 49 (0) 4821/17 -4233 klaus.reimer@isit.fraunhofer.de*
Design and test of analogue and mixed-signal ASICs	*Measurement, automatic control industry*	*Jörg Eichholz + 49 (0) 4821/17 -4253 joerg.eichholz@isit.fraunhofer.de*
Design kits	*MST foundries*	*Jörg Eichholz + 49 (0) 4821/17 -4253 joerg.eichholz@isit.fraunhofer.de*
MST design and behavioural modelling and wafer tests	*Measurement, automatic control industry*	*Jörg Eichholz + 49 (0) 4821/17 -4253 joerg.eichholz@isit.fraunhofer.de*
Electrodeposition of microstructures	*Surface micromachining*	*Martin Witt + 49 (0) 4821/17 -1437 martin.witt@isit.fraunhofer.de*
Electrical biochip technology (proteins, nucleic acids, haptens)	*Biotechnology, related electronics microfluidics, environmental analysis, Si-chipprocessing, packaging, chip loading*	*Dr. Eric Nebling + 49 (0) 4821/17 -4312 eric.nebling@isit.fraunhofer.de*
Secondary lithium batteries	*Mobile electronic equipment, medical applications, stationary storage solutions, automotive, smart cards, labels, tags*	*Dr. Peter Gulde +49 (0) 4821/17 -4219 peter.gulde@isit.fraunhofer.de*
Battery test service, electrical parameters, climate impact, reliability, quality	*Mobile electronic equipment, medical applications, stationary storage solutions, automotive, smart cards labels, tags*	*Dr. Peter Gulde +49 (0) 4821/17 -4219 peter.gulde@isit.fraunhofer.de*
Quality and reliability of microelectronic and electronic assemblies	*power electronic industry*	*Dr. Thomas Knieling + 49 (0) 4821/17 -4605 thomas.knieling@isit.fraunhofer.de*
Material and damage analysis	*Microelectronic and power electronic industry*	*Dr. Thomas Knieling + 49 (0) 4821/17 -4605 thomas.knieling@isit.fraunhofer.de*
Wearable, flexible and hybrid electronics	*Electronic industry, medical and sports applications*	*Dr. Thomas Knieling + 49 (0) 4821/17 -4605 thomas.knieling@isit.fraunhofer.de*
Thermal measurement and simulation	*Microelectronic and power electronic industry*	*Dr. Max H. Poech + 49 (0) 4821/17 -4607 max.poech@isit.fraunhofer.de*
Application center for process technologies in manufacturing electronic assemblies	*Electronic industry*	*Helge Schimanski +49 (0) 4821/17 -4639 helge.schimanski@isit.fraunhofer.de*
Packaging for microsystems, sensors, multichip modules	*Microelectronic, sensoric and medical industry*	*Dr. Wolfgang Reinert + 49 (0) 4821/17 -1440 wolfgang.reinert@isit.fraunhofer.de*
Wafer level packaging, ultra thin Si packaging and direct chip attach techniques	*Microelectronic, sensoric and medical industry, automotive industry*	*Dr. Wolfgang Reinert + 49 (0) 4821/17 -1440 wolfgang.reinert@isit.fraunhofer.de*
Vacuum wafer bonding technology	*Microelectronic, sensoric and medical industry, automotive industry*	*Dr. Wolfgang Reinert + 49 (0) 4821/17 -1440 wolfgang.reinert@isit.fraunhofer.de*

REPRESENTATIVE FIGURES

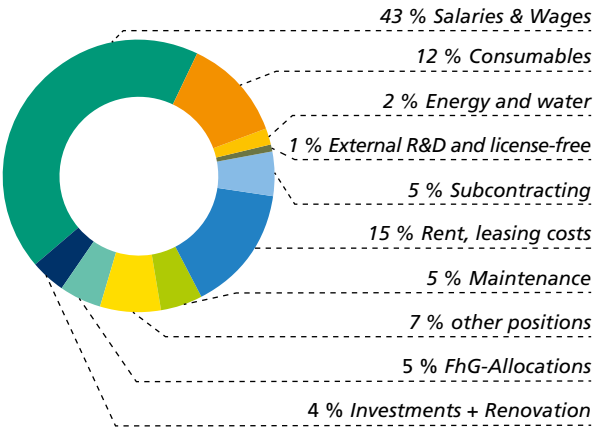
EXPENDITURE

In 2015 the operating expenditure of Fraunhofer ISIT amounted to 25.905,4 T€.
Salaries and wages were 11.178,6 T€, material costs and different other running costs were 13.714,8 T€.
The institutional budget of capital investment and renovation was 1.012,0 T€.

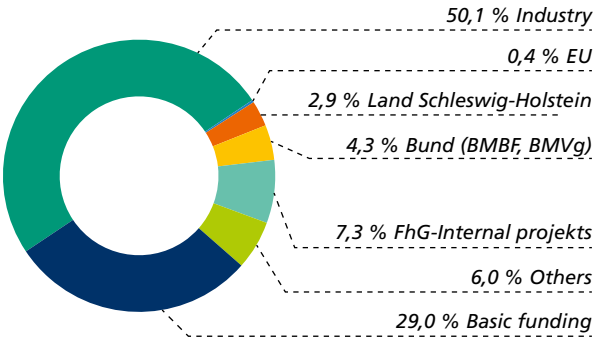
INCOME

The budget was financed by proceeds of projects of industry/industrial federations/small and medium sized companies amounting to 12.970,6 T€, of government/project sponsors/federal states amounting to 1.878,7 T€ and of European Union/others amounting to 1.665,7 T€.
Furthermore there were FhG-projects about 1.879,2 T€ and basic funding with 7.511,2 T€.

Expenditure



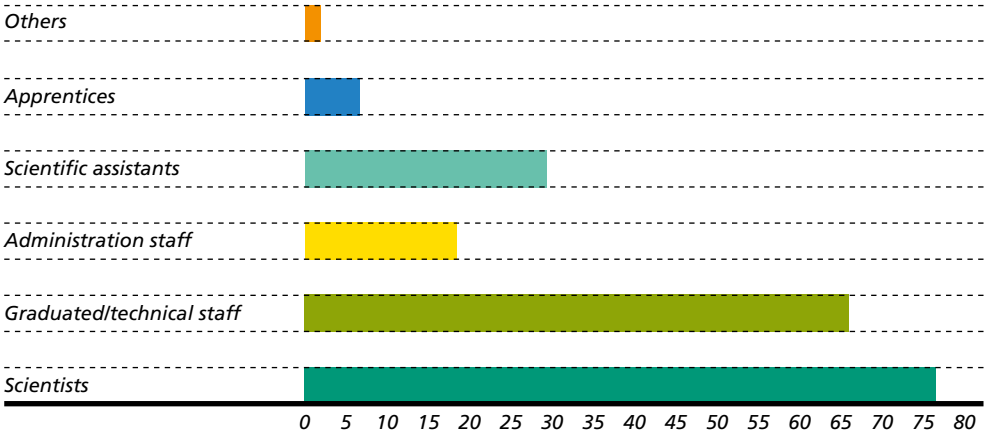
Income



STAFF DEVELOPMENT

At the end of 2015 the staff consisted of 160 employees. 76 were employed as scientific personnel, 66 as graduated/ technical personnel and 18 worked within organisation and administration. The employees were assisted through 29 scientific assistants, 7 apprentices and 2 others.

Staff Development



THE FRAUNHOFER GESELLSCHAFT

Research of practical utility lies at the heart of all activities pursued by the Fraunhofer-Gesellschaft. Founded in 1949, the research organization undertakes applied research that drives economic development and serves the wider benefit of society. Its services are solicited by customers and contractual partners in industry, the service sector and public administration.

At present, the Fraunhofer-Gesellschaft maintains 67 institutes and research units. The majority of the nearly 24,000 staff are qualified scientists and engineers, who work with an annual research budget of more than 2.1 billion euros. Of this sum, more than 1.8 billion euros is generated through contract research. More than 70 percent of the Fraunhofer-Gesellschaft's contract research revenue is derived from contracts with industry and from publicly financed research projects. Almost 30 percent is contributed by the German federal and Länder governments in the form of base funding, enabling the institutes to work ahead on solutions to problems that will not become acutely relevant to industry and society until five or ten years from now.

International collaborations with excellent research partners and innovative companies around the world ensure direct access to regions of the greatest importance to present and future scientific progress and economic development.

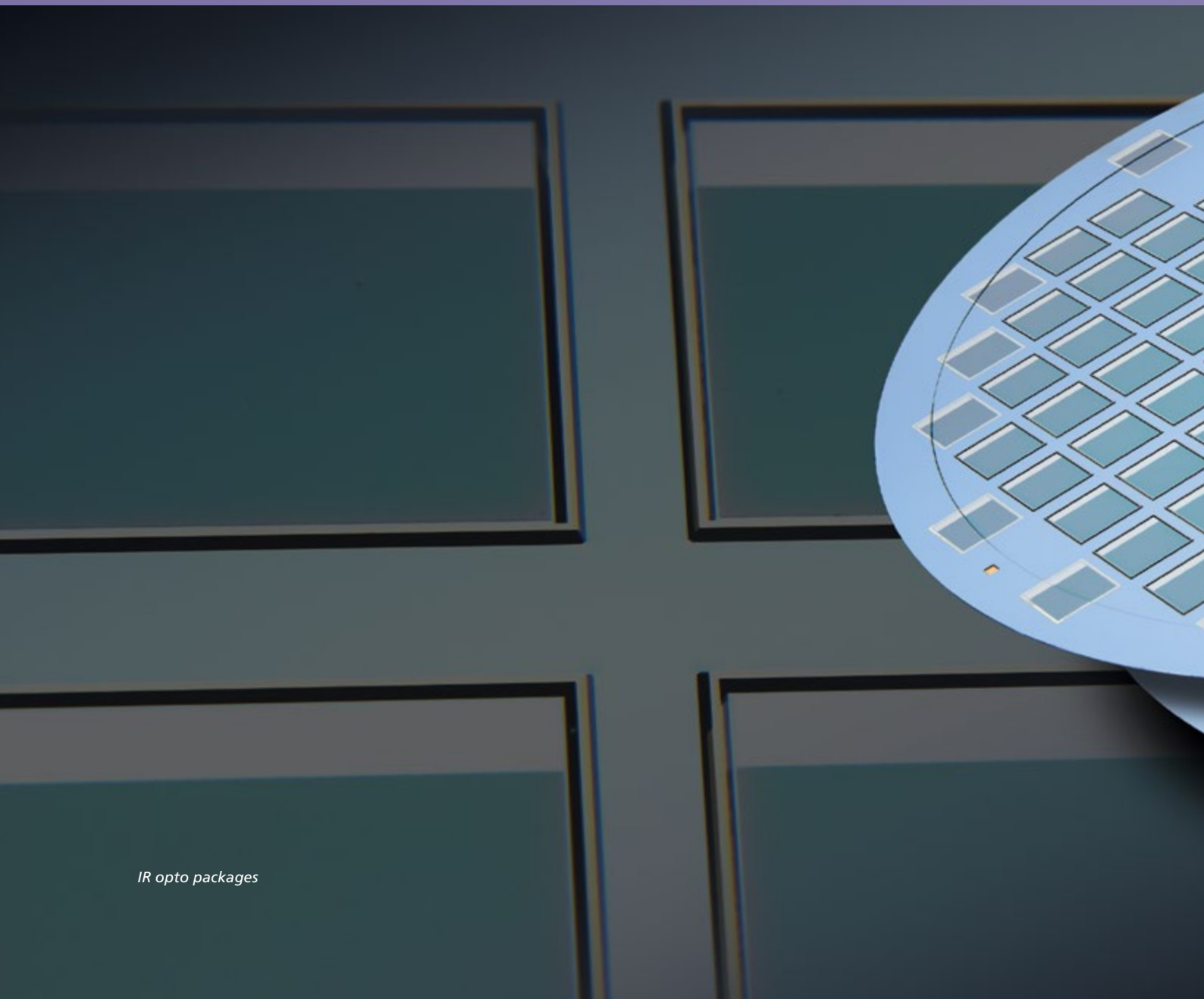
With its clearly defined mission of application-oriented research and its focus on key technologies of relevance to the future, the Fraunhofer-Gesellschaft plays a prominent role in the German and European innovation process. Applied research has a knock-on effect that extends beyond the direct benefits perceived by the customer: Through their research and development work, the Fraunhofer Institutes help to reinforce the competitive strength of the economy in their local region, and throughout Germany and Europe. They do so by promoting innovation, strengthening the technological base, improving the acceptance of new technologies, and helping to train the urgently needed future generation of scientists and engineers.

As an employer, the Fraunhofer-Gesellschaft offers its staff the opportunity to develop the professional and personal skills that will allow them to take up positions of responsibility within their institute, at universities, in industry and in society. Students who choose to work on projects at the Fraunhofer Institutes have excellent prospects of starting and developing a career in industry by virtue of the practical training and experience they have acquired.

The Fraunhofer-Gesellschaft is a recognized non-profit organization that takes its name from Joseph von Fraunhofer (1787–1826), the illustrious Munich researcher, inventor and entrepreneur.

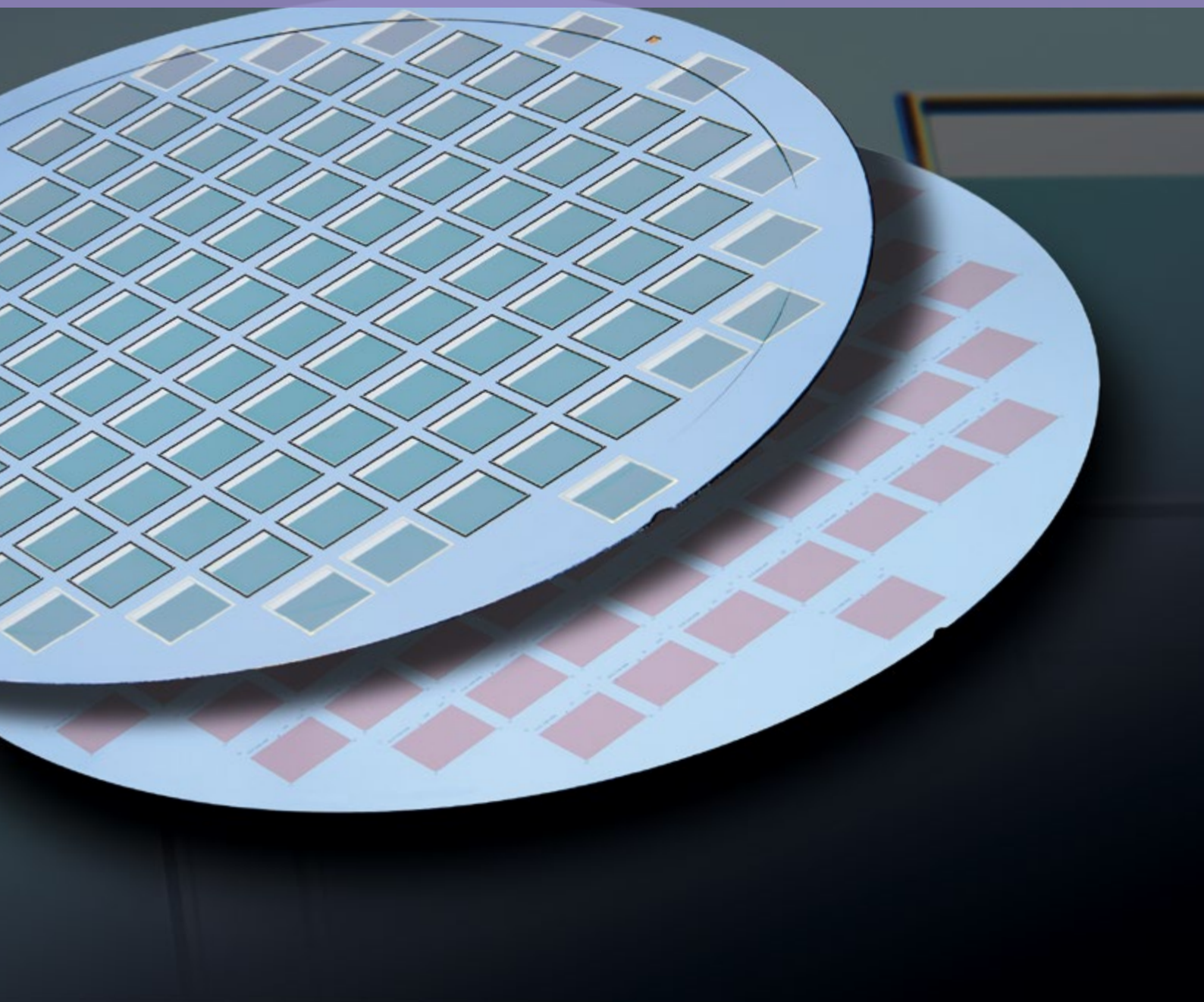
LOCATIONS OF THE RESEARCH FACILITIES

REPRESENTATIVE RESULTS OF WORK



IR opto packages

MICROSYSTEMS TECHNOLOGY, MEMS AND IC DESIGN



LARGE APERTURE MEMS SCANNING MIRRORS FOR LASER MATERIAL PROCESSING (LAMM)

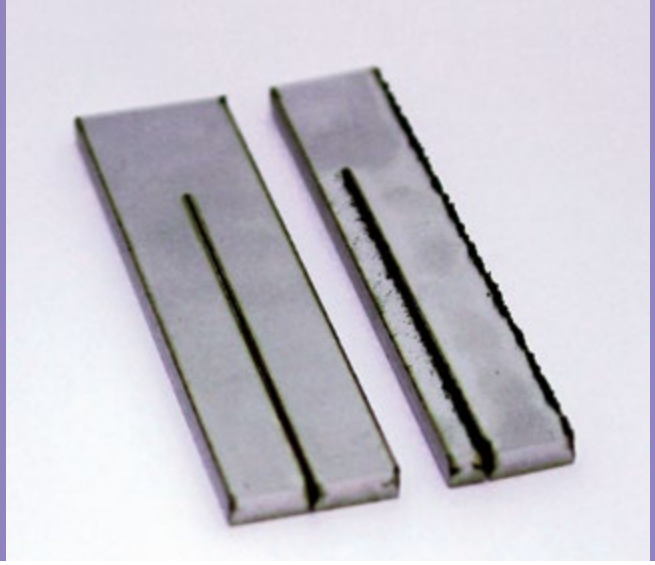
At Fraunhofer ISIT MEMS scanning mirrors have been developed since 1995. Based on electrostatic actuation they serve many different applications, such as endoscopic imaging, confocal laser scanning microscopy and optical coherence tomography. They have been developed for biaxial beamsteering in large matrices of optical cross-connects in optical telecommunication networks, while another class of biaxial scanning mirrors has been developed for high resolution laser video projection purpose to be applied in automotive head-up displays, dashboard displays, smartphones, digital cameras, wearable displays (augmented reality displays) and gesture control.

ISIT was first to develop and successfully apply wafer level vacuum packaging of MEMS scanning mirrors in 2007. Hermetic wafer level packaging is a key factor to enable reliable low-cost mass producible optical MEMS for automotive and consumer industry. Besides protection against contamination by particles and moisture vacuum packaging additionally allows to effectively reduce energy dissipation caused by gas damping. Resonant MEMS scanning mirrors thereby can achieve Q-factors up to 140,000.
This enables to accumulate oscillation energy over a large number of resonant mirror oscillations. Conserving the energy in the vacuum packaged MEMS allowed to largely increase the parameter range in comparison to other MEMS mirror concepts.

In 2013 a further development began, exploiting the advantage of vacuum packaging for biaxial actuation of large aperture MEMS scanning mirrors with diameters up to 20 mm. Such large aperture MEMS mirrors (LAMM) can serve many new applications such as 3D Time-of-Flight cameras and LIDAR systems, but also applications where laser power exceeds the typical milliwatt-range which conventional MEMS-mirrors so far often have been restricted to. In contrast to the fabrication technology used for the typical 1 mm MEMS mirror in which a device layer thickness of 80 µm is used, the new class of LAMM-scanners applies a 10 times greater thickness, which is necessary to minimize dynamic mirror deformation. Appropriate dielectric coatings which provide a high reflectivity of greater than 99.9 % now enable to use such MEMS scanning mirrors in high power laser applications such as laser marking, laser welding and laser cutting.

In 2015 Fraunhofer ISIT was first to demonstrate that a biaxial 20 mm-MEMS scanning mirror can be used for laser cutting of 4 mm thick sheets of stainless steel. CW-laser power loads as high as 4.5 kW have already been applied, causing a temperature rise of the MEMS mirror of only 45 degrees. With a scan frequency of more than 1 kHz, this 20 mm-MEMS mirror produces a circular wobble trajectory that helps to improve quality and speed of the laser cutting process (see picture top right). Comprising two scan axes on a single chip this MEMS mirror enables to replace conventional bulky galvanometric scanning systems.

Author: Dr. Ulrich Hofmann



Laser cutting result of 4 mm thick stainless steel. The picture shows cutting results with use of MEMS mirror based wobble (left) and without wobble (right).

MEMS mirrors can be customized for different applications, e.g. to operate with scan frequencies higher than 100kHz or to achieve optical scan angles larger than 100 degrees.

MONOLITHICALLY INTEGRATED MEMS DEFLECTION ARRAY PLATE SYSTEM WITH DRIVING ELECTRONICS FOR ELECTRON MULTI-BEAM MASK WRITING (MBMW)

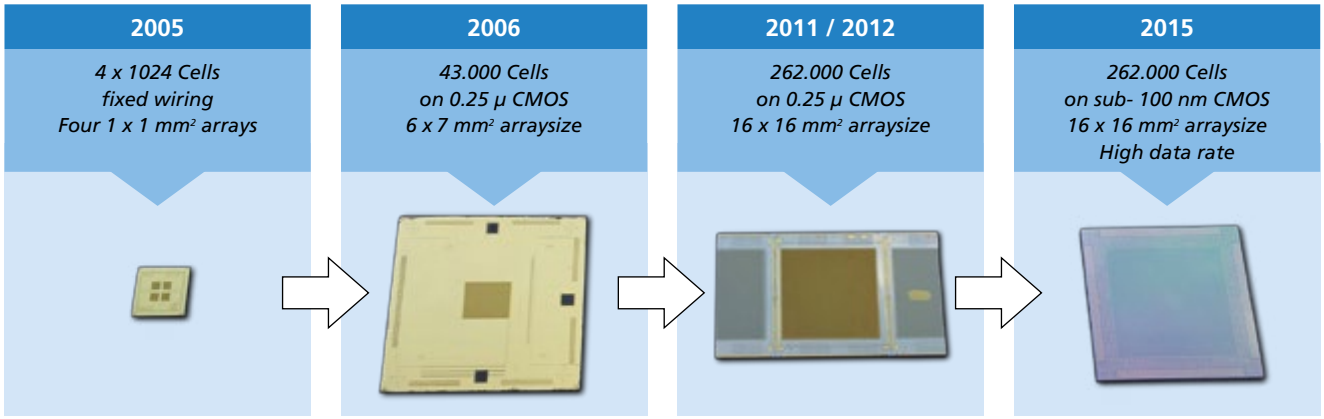
Introduction

Mask writer tools that use electron beams are of key importance in patterning surfaces for semiconductor manufacture. They provide leading-edge masks for 193 nm water-immersion optical scanners and extreme UV lithography, as well as 1:1 templates for imprint lithography. Currently, the most commonly used tools are variable shaped beam (VSB) mask writers. These enable alteration in the shape of the 50 keV beam during writing, achieving considerably higher throughput than Gaussian spot beam tools, which are used for ultra-high-resolution work.

However, water-immersion lithography is now extending to nodes of 20 nm or less, and in achieving these requirements, VSB tools suffer from an explosion in the total number of shots per mask. For example, for the 18 nm node, complex masks need write times of around 30 hours. This 'write time explosion' occurs for three reasons. First, the number of shots grows exponentially from node to node. Second, smaller shapes are needed, leading to decreased average shot sizes. Third, the mask exposure dose must be increased. To address these issues, IMS Nanofabrication AG, Vienna, Austria, developed multi-beam mask writing (MBMW) technology. Instead of using one electron beam, they employ many thousands to write complex mask patterns in parallel (see figure 2)

Electron multi-beam writing is a solution for the 10 nm-node and beyond. It is targeted on using hundreds of thousands of

Figure 1: Evolution of Deflection Array Plates



individually addressable electron-beams working in parallel. MBMW is designed to meet the requirements of several upcoming tool generations.

The operability of electron multi-beam projection could be demonstrated on former European framework projects. Now within MBMW industrial development projects alpha and beta tools were realized by IMS Nanofabrication. These tools contain all necessary components of a full-fledged tool. In the actual MBMW system a programmable aperture plate system (APS) is used to generate more than 262,000 switchable beams of micrometer size which are guided through electro-static- and magnetic-lens optics with 200 x demagnification. Thus, thousands of demagnified electron beams are projected in parallel onto the resist-coated mask blank.

Aperture Plate System (APS) with CMOS addressed Deflection Array Plate (DAP)

One central part of the Multi-Beam Mask Writing tool is the programmable Aperture Plate System (figure 2).

Within the last years Fraunhofer ISIT has developed and refined the MEMS fabrication process for the compact Deflection Array Plate and its monolithic integration starting with CMOS wafer substrates. The total evolution of the DAP's is shown in figure 1. Beginning with fixed wirings to address the deflection electrodes, in 2008 a first monolithic integrated 43 k DAP could be realized. Then in 2012 in a third step the Array size was increased from 43,000 to a 262,000 beam capacity by integration on a 0.25 µm CMOS technology. To achieve higher data rates in 2015 a fourth step was taken by using a sub-100 nm CMOS wafer technology.

The APS constitutes the object in the imaging electron optics. It consists of two silicon plates which exhibit a periodic staggered array of apertures. Individual beamlets are formed by the aperture array plate (AAP) while dynamic structuring is realised by the deflection array plate below. Deflection electrodes at every aperture allow for individual control of each beamlet. The deflected beams are filtered out at a stopping plate further down the electron optical column;

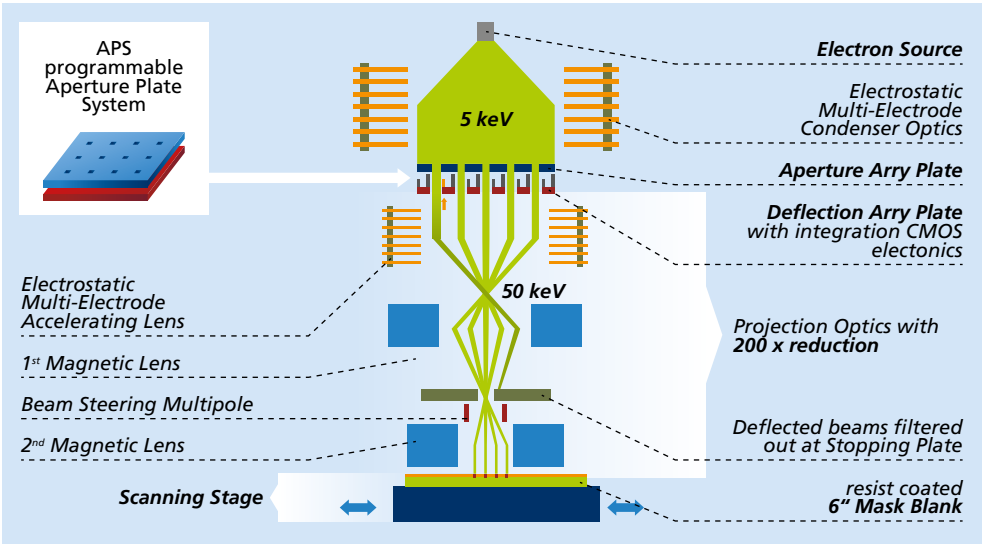


Figure 2: Multi-Beam Mask Writer Tool Principles (Source: IMS Nanofabrication AG)

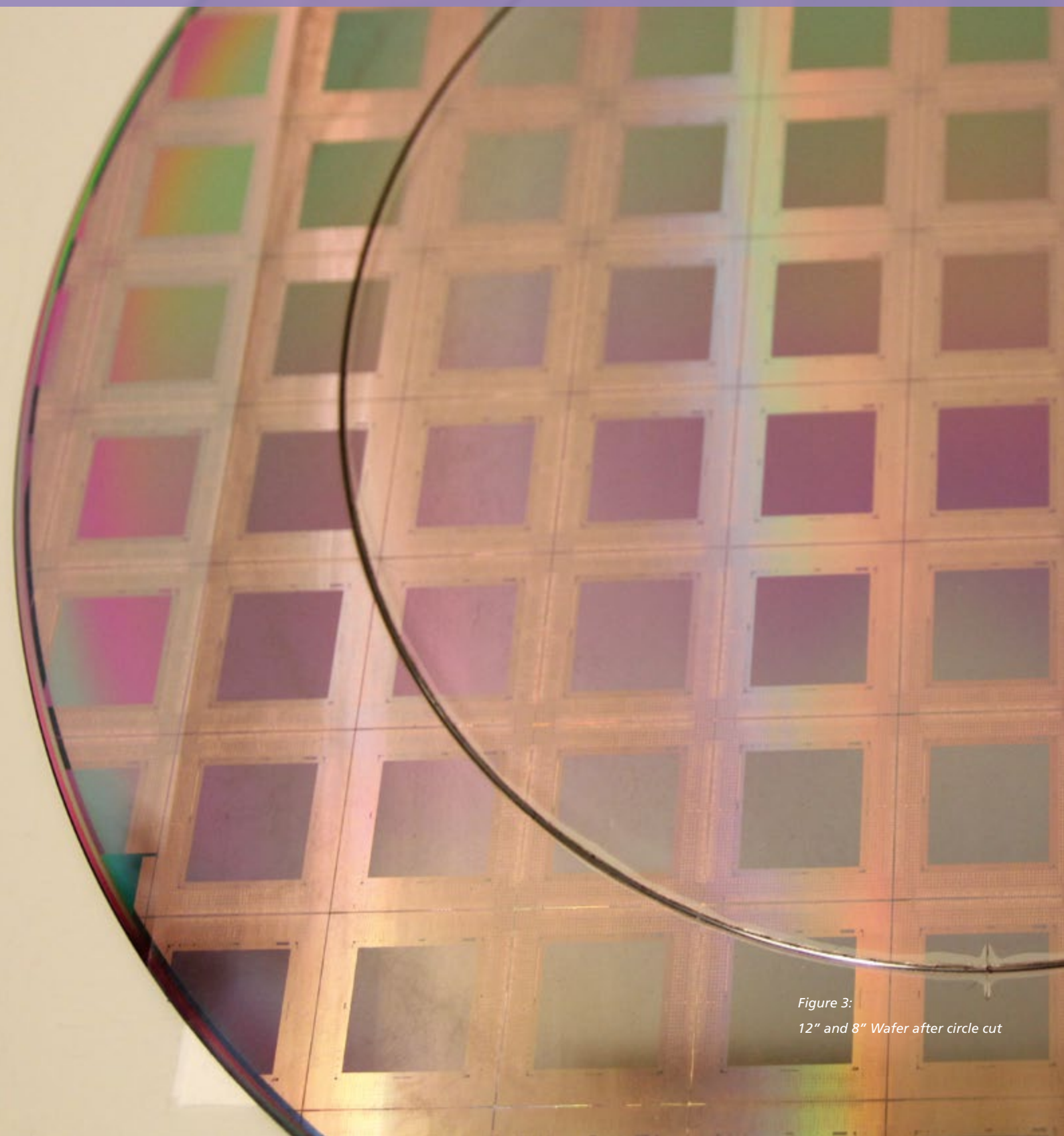


Figure 3:
12″ and 8″ Wafer after circle cut

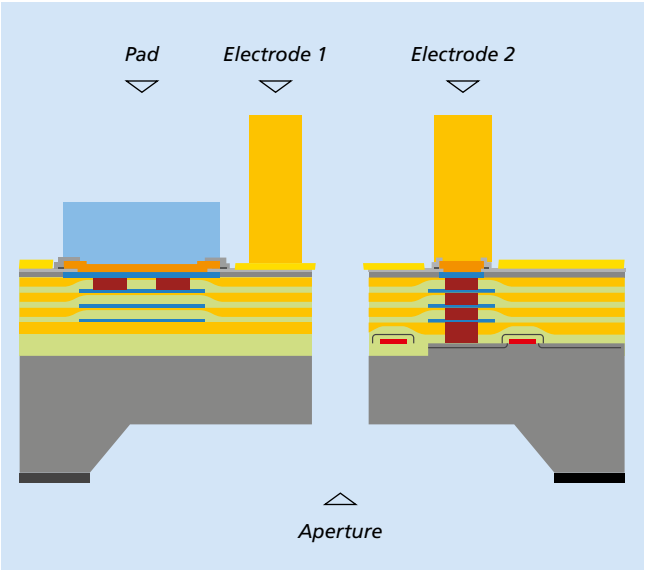


Figure 4: Key MST processes for the blanking plate fabrication

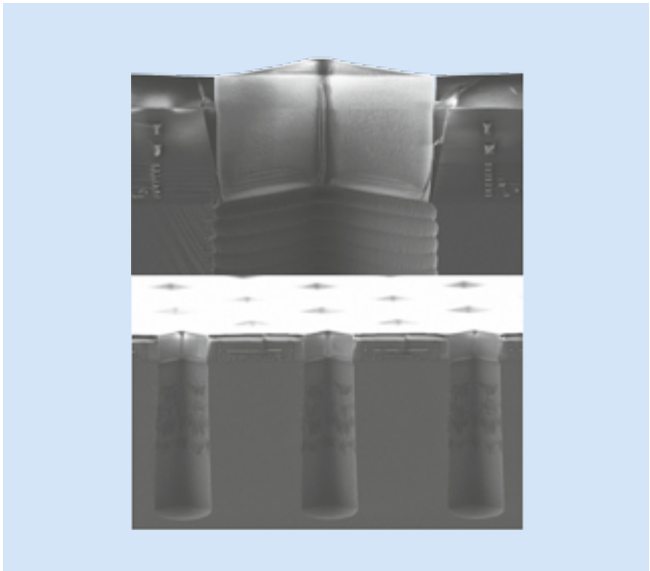


Figure 5: Cross section of the blanking chip with etched apertures close to the CMOS circuit

only undeflected beams reach the 6" mask blank surface. The principle of the Multi-Beam Mask Writer is given in figure 2.

The DAP is driven by a stream of pixel data prepared off-line in advance and transmitted via an optical high speed data path from an outside storage equipment onto the plate. Using a specific driving electronics for each aperture every beam can individually be switched on and off. The exposure concept foresees that the DAP is able to switch 262,000 electron beams in parallel while the exposed mask blank moves continuously. Thus, the amount of data to handle is in the order of many Gbit per second. Therefore only a monolithically integrated driving electronics next to the deflection electrodes is necessary to fulfil this challenge.

The layout of the electronics is based on the geometrical specifications and the electrical requirements of the blanking chip. The area of each aperture cell is 32 x 32 μm^2 and contains the electronics for the blanker activation. For the actual requirements it was elaborated that a sub-100 nm CMOS technology is suitable.

MEMS Process

In order to fit the CMOS wafer and MEMS process technology at ISIT, the design work had to consider the position of the chips on the wafer, the critical dimensions of the patterns, the overlay accuracy of the different exposure tools at the CMOS foundry and at ISIT, a homogeneous distribution of metal layers over the wafer and the implementation of specific alignment marks for the mix and match lithography and test structures.

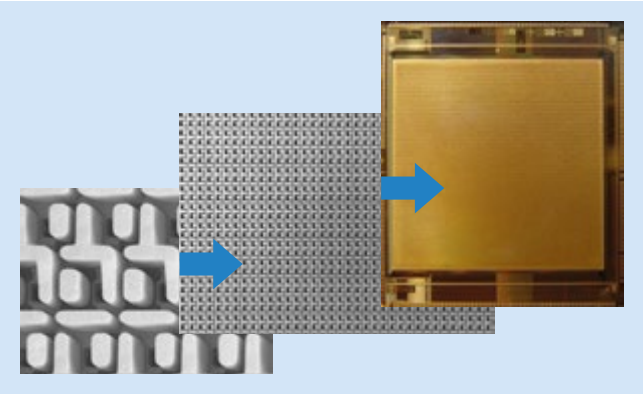


Figure 6: Detail and overview of electrode arrangement and top view of electroplated electrodes close to apertures

The CMOS fabrication has been performed on 12 inch silicon wafers. For MEMS processing the wafers had to be downsized to 8 inch for further processing at ISIT. Figure 3 shows the result after circle cut dicing and the arrangement of the DAP chips on the 300 mm and 200 mm wafer. In principle the MST fabrication of the DAP chip comprises three main processing parts (figure 4): (i) deep reactive ion etching of high aspect ratio apertures, (ii) fabrication of high blanking and shielding electrodes by electroplating and (iii) anisotropic silicon wet etching for the realisation of the membrane with a thickness of 40 µm.

In figure 5 an intermediate cross section of the CMOS blanking chip plate is shown. The upper part depicts the CMOS electronics. Apertures with 9 µm openings and the required retrograde profile have been performed by means of deep reactive ion etching prior to electroplating of the high aspect ratio metal electrodes and prior to membrane etching. The deflection of the pre-formed electron beams is done by electrostatic fields. The available deflection voltage from the monolithically integrated driving electronics is 3.3 V. Together with the required deflection angle of nearly 1 mrad the height of the blanking electrodes has been calculated to be in the range of 30 µm. Based on a thick photoresist process a lithography and electroplating processing sequence has been established which results in a precise fabrication of the metal electrodes fulfilling the high requirements regarding the high aspect ratio, vertical and smooth sidewalls and robustness during further processing the deflection array chip. Figure 6 shows the arrangement of the electrodes after resist removal. The pre-assembled compact programmable aperture plate system is shown in Figure 7. The integration technology for the APS plates covers the assembly and interconnection of (i) the DAP chip on a base plate, (ii) the plug connection and (iii) the precise alignment of the beam forming aperture plate (compare figure 2).

Results

The first characterization of the assembled compact aperture plate systems runs in test benches at IMS Nanofabrication. Tested are several parameters like power consumption, charging, detection of non-functional beam cells and the blanking angle. Figure 8 shows deflected and undeflected beam images from a scintillator detection plate.

A nearly defect-free MST fabrication yielded in a functionality of up to 99.97 % of the Deflection Array Plates (DAP). IMS has performed the writing strategy in a redundant way so that the remaining few failures are far below the tolerable rate of failures. Several writing results on positive (pCAR) and negative (HSQ) resist by IMS Nanofabrication show that all specifications for MBMW can be reached (see figures 9 & 10). Within the last project periods a complex MEMS fabrication process for the Deflection Array Plate has been established on 0.25 µm CMOS. This included the increase of multi-beam capacity from 43-thousand to 262-thousand and the

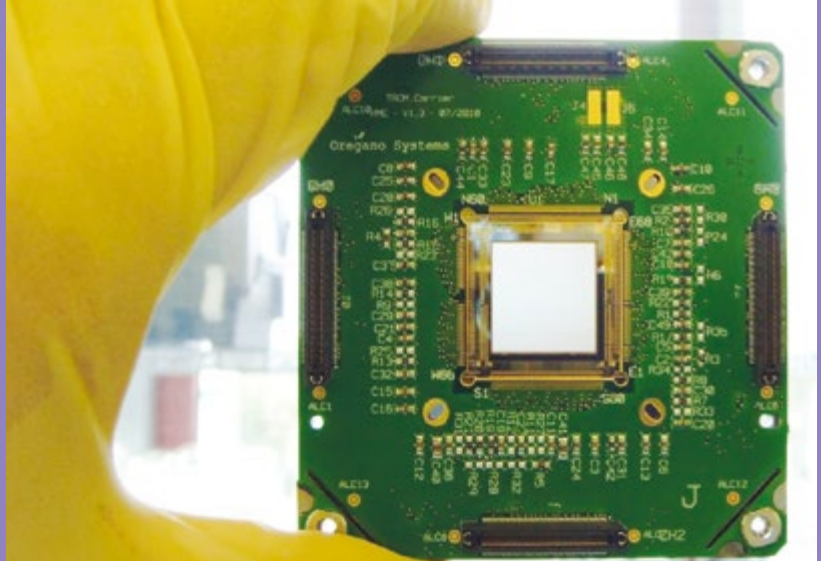


Figure 7: Assembled Deflection Array Plate (DAP)

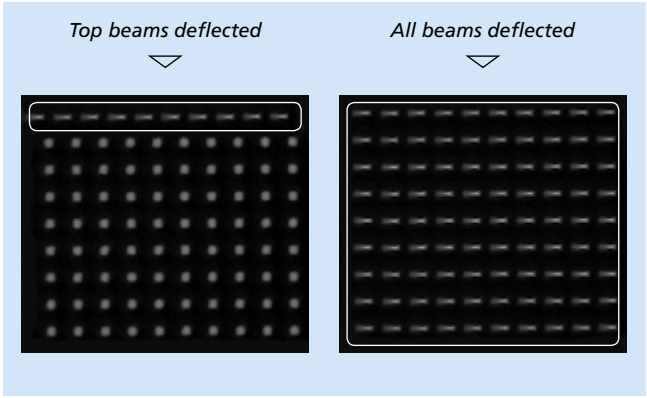


Figure 8: Deflected and undeflected beam images from a scintillator detection plate. (Source: IMS Nanofabrication AG)

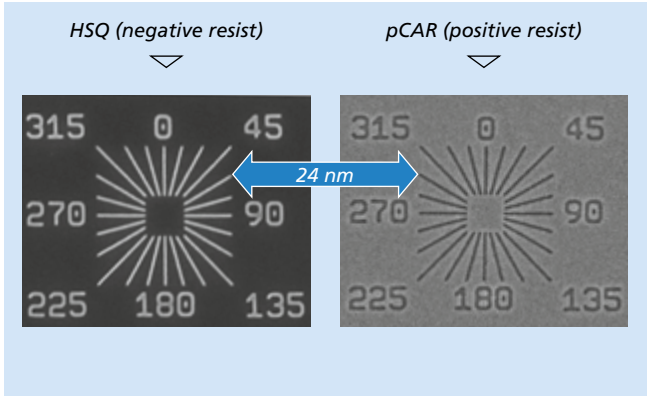


Figure 9: 24 nm lines show any angle capability (Source: IMS Nanofabrication AG)

aperture array field size from 6 x 7 mm² to 16 x 16 mm². Additionally, the monolithic integration on a next generation integrated CMOS electronics type sub-100nm could be realized in a first step.

Outlook

The current industrial project between IMS Nanofabrication AG and Fraunhofer ISIT focuses on optimizations and refinements of the MEMS process to this new sub-100 nm CMOS. First testing results by IMS Nanofabrication show that it will be possible to reduce mask writing times significantly by electron Multi-Beam Mask Writing fulfilling industrial leading-edge mask demands for the 7 nm technology node, and below.

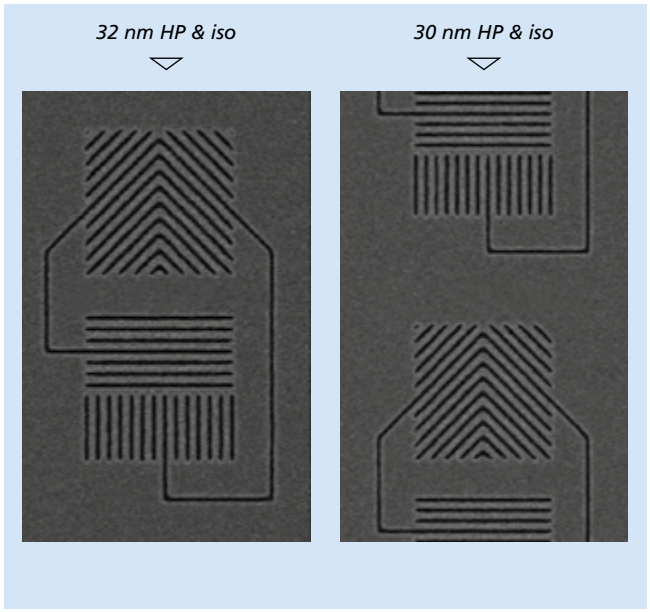


Figure 10: 32/30 nm HP & ISO lines in pCAR (Source: IMS Nanofabrication AG)

Authors:
Martin Witt, Dr. Klaus Reimer

Project duration: 2 years (09/2013-08/2015)
Grant: 350 000 € by
Zentrales Innovationsprogramm Mittelstand (ZIM)
Consortium: Plan Optik AG, Fraunhofer ISIT

TIGLA: A LOW-COST MANUFACTURING PROCESS FOR OPTICAL DEEP-CAVITY CAP WAFERS

A rich portfolio of encapsulation processes is an enabler for many MEMS devices and applications. Cap wafers protect components from ambient atmosphere and particles, and they prevent the fragile structures from mechanical damage. But in many cases, the wafer level package also needs to provide a physical interface to the environment. Specifically, optical MEMS (MOEMS) require packaging solutions that combine hermetic sealing with high-quality optical access.

The high demands related to the optical surface quality yet cannot be achieved with conventional manufacturing processes such as CNC machining. In the project TIGLA, Plan Optik and ISIT developed a process to create several millimeters large and more than 1 mm deep cavities in glass wafers with high optical quality. The project was funded in the frame of the German ZIM research programme for SMEs (ZIM: Zentrales Innovationsprogramm Mittelstand).

The process is based on thermal glass shaping:
A glass wafer is brought to a viscous state and drawn into a silicon mold by the effect of vacuum. While in earlier process implementations the mold wafer used to be lost in the final etching process, the TIGLA project targeted a concept with reusable molds.

High-quality windows at low tooling costs

For economic reasons it is interesting to reuse a mold many times. However, after the viscous flow process, the glass firmly sticks to all touched silicon surfaces. Using Boron Nitride as an anti-stiction coating works well in principle, but creates a rough surface like an orange peel effect that is not suitable for optical applications.

To overcome this problem, additional silicon inserts were placed inside each cavity prior to the molding process. These inserts are sacrificial elements with high surface quality, shaped and aligned underneath the optical window areas (Figure 1). During the high temperature molding, the glass touches the silicon surfaces and spreads across them. As a result, the elements adhere on the glass and, after the glass wafer is separated from the mold, they can easily be removed by wet etching.

However, this approach can only ensure evenness and flatness on one side of the critical glass areas - mostly, surfaces on both sides of the glass wafer are to be protected. The approach is now to firmly mount silicon islands on the other side of the glass wafer, which is routinely made by using bonded glass-silicon wafer stacks and structuring silicon elements with a selective anisotropic etching process. An additional benefit of this approach is that glass areas around the molding cavities are maintained in a flat shape.

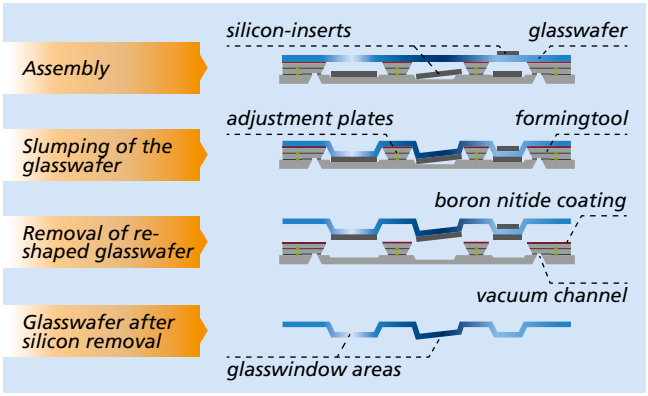


Figure 1: Concept of glass wafer thermoforming process to produce deep cavities with optical windows

Glasswafer with vacuum slumped areas

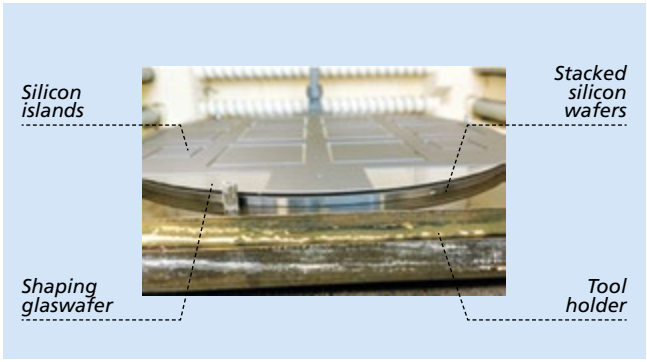


Figure 2: Wafer stack and vacuum tool forming a reusable mold, with glass wafer on top

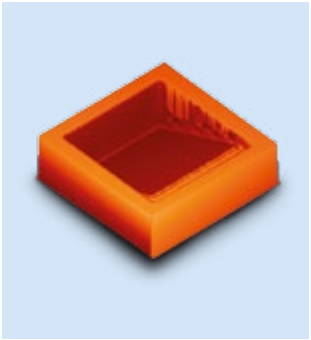


Figure 3: Interferometric 3D-profile of an inclined slumped window (2.5 x 2.5 cm² with an angle of 34°)

Hence, both the loose silicon insert inside and the bonded silicon island outside the cavity contribute to a high surface quality that is suitable to form inclined optical windows in glass caps for MOEMS.

Process and handling

During the TIGLA project, a new production tool has been constructed and built, allowing cost-effective molding.
A simple silicon etching process was used to create an application specific template. An appropriate Inconel tool holder with vacuum connection was prepared and installed in an industrial furnace. The vacuum is generated by an external pump, which is connected to a vacuum port at the bottom of the tool holder. Fine channels in the bottom ensure that the molding vacuum is maintained throughout the process.
The molds are made of stacked silicon wafers and include via holes, vacuum channels and additional alignment structures. The targeted depth of the glass cap cavities is defined by inserting additional silicon wafers in the mold stack.
Their alignment is ensured by using quartz glass plates.
To prevent adhesion of the glass wafer, the top silicon wafer of the mold stack is coated with a Boron Nitride layer, which allows the tool to be used several times. The molding tool can be used very flexibly by changing the silicon template wafers (Figure 2). Different geometries of the window surfaces can be produced, depending on how the silicon inserts are placed in the forming tool – it is equally possible to produce flat or inclined windows (figure 3).

Results

Our first conceptual evaluation of the glass wafer slumping yielded poor surface quality; glass windows and the entire wafer were very uneven. We were able to optimize the process by introducing a mechanical dicing step that localizes the glass bending around the window area. In our final demonstrators, we produced planar and tilted windows with a surface roughness below 1 nm Ra in the optical areas. However, the flatness of the glass window remained an issue, since it is highly dependent on the thickness of the used silicon islands. A flatness of better than 0.5 µm across a 3 mm distance could be achieved. By decoupling the silicon surfaces, the TTV of the glass window is 4-5 %. Glass cavity depths of several millimeters could easily be produced by stacking several silicon wafers. The visual adjustment of the glass wafer on the forming tool generates a misalignment of at least 1 mm, which will be improved by laser marking in the glass. Further optimization is necessary with respect to the flatness of the windows and regarding the overall wafer design in order to cover more application areas.

Authors: Jochen Quenzer, Vanessa Stenchly

Project duration: 3,5 years (05/2012-09/15)
Grant: 750 000 € by Federal Ministry of Education and Research (BMBF)
Consortium: 5 partners

PICOLO: A WAFER-LEVEL PACKAGING CONCEPT FOR LASER-DIODES IN PICO-PROJECTION DEVICES

With the newly developed green-emitting laser diode, it is now possible to produce powerful RGB semiconductor laser light sources. In combination with micro-mirrors the realisation of high efficient and mobile projection systems is feasible. However, a bottleneck for progress in cost-efficiency and miniaturization are the metal packages: TO-cans are still the state of the art in hermetic packaging of laser diodes, but they suffer from size, cost and limited heat spreading capabilities. A challenge in laser diode packaging is thus to create a laterally emitting, hermetically sealed cavity SMD package.

A part of the BMBF (Federal Ministry of Education and Research) supported project "PICOLO" (Pico-projection with RGB laser diodes in mobile terminals and automotive applications) was to develop a novel lateral emission based glass-silicon wafer level assembly and packaging technology for laser diodes that enables the production of small form factor RGB-light engines.

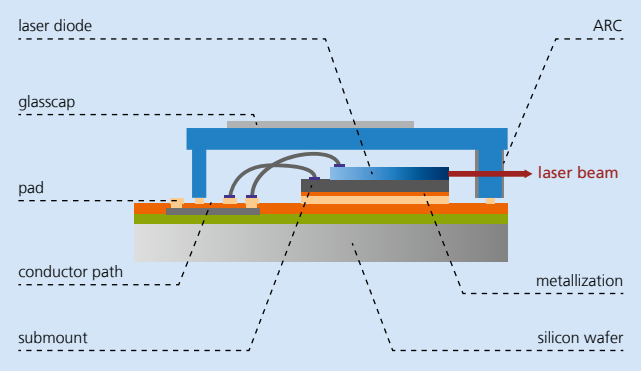


Figure 1: Schematic construction of a miniaturized laser module with lateral emission window

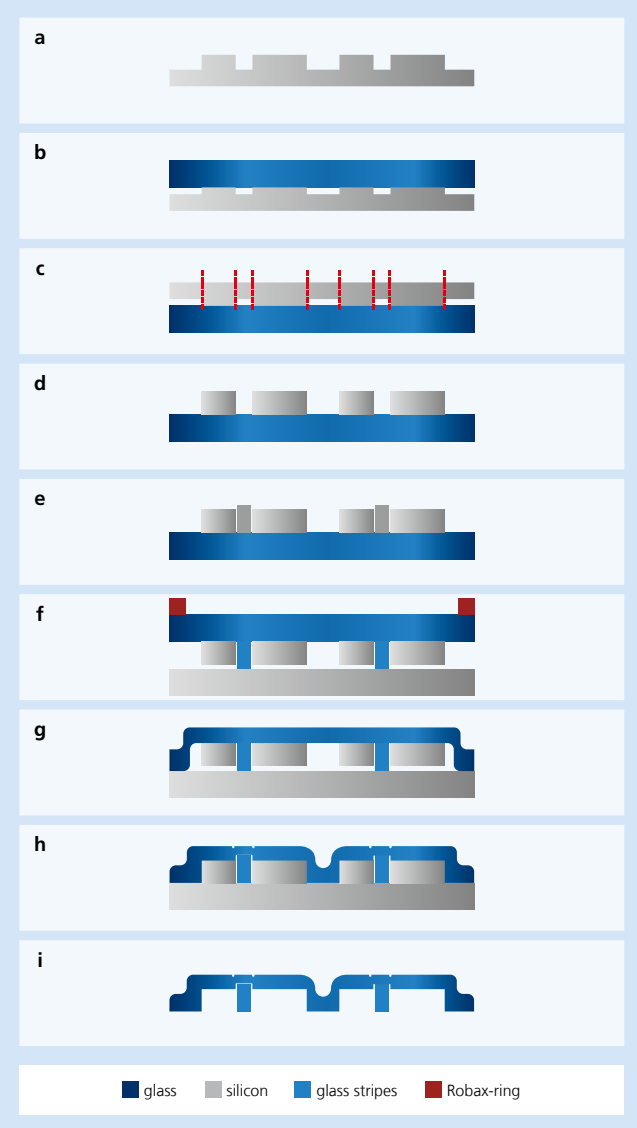
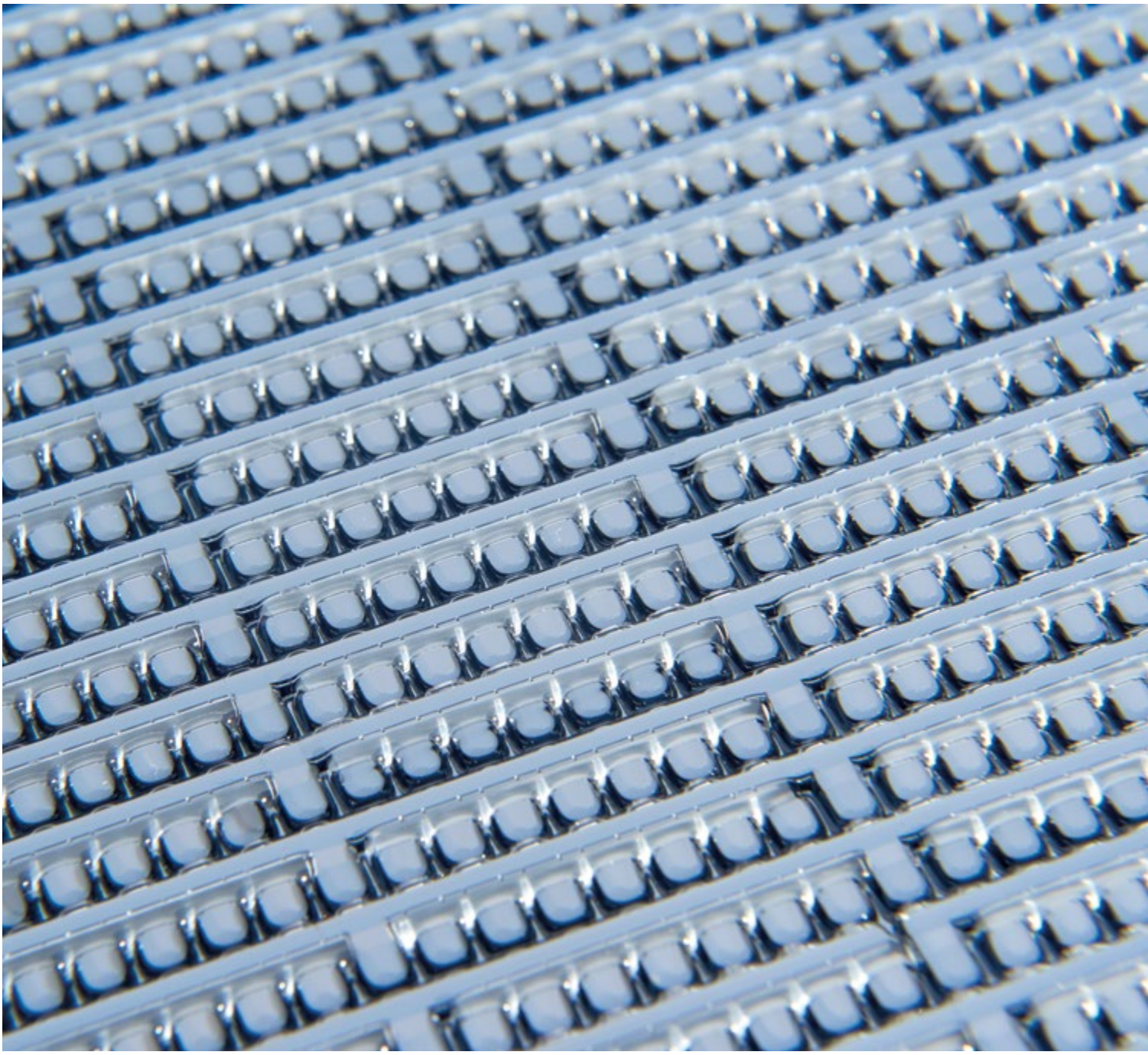


Figure 2: Schematic of the process flow for the glass wafer with vertical windows

Figure 3: Detail view of a separated 8" glass cap wafer with vertical emission windows, multilayer anti-reflective coating and deposited plating base

Figure 4: Siliconwafer with inlaid glassstripes after the second annealing process



Motivation

The requirements for low cost miniaturized hermetic laser diode packages can be fulfilled by a wafer level packaging approach as shown in figure 1. Alternative wafer level housing concepts with a parallel emission window relative to the laser emission are complex and expensive. The lateral emission enables the beam shaping by low cost optics outside of the package while the hermetic sealing in an organics-free gas environment prevents premature laser degradation.

The choice of glass as a capping material is based on its low permeability for water and gases and by the high optical transparency. The good optical quality of the emission window with respect to roughness and flatness is realized by fusing two glasses with different softening points.

Technology

The technology is based on high-temperature viscous glass micromachining with glass and silicon wafers developed at Fraunhofer ISIT. Figure 2 schematically shows the fabrication process flow for the optical cap with vertical emission window: First, cavities are etched into a silicon wafer with a DRIE etching step (a). After anodic bonding of the resulting structured silicon wafer with a borosilicate glass wafer (b), a mechanical dicing step follows from the silicon side along the DRIE etched structures to define the pinboard (c) wherein the high melting glass window can be inserted later (d). The height of silicon islands is predetermined by the wafer thickness of the starting material and also defines the cavity height. After a cleaning step to remove silicon residuals, the high melting glass stripes can be applied (e). Because the stripes were previously separated from a wafer by mechanical sawing, they have to be annealed in a separate step to take out the moisture that accumulates in the sawn edges. When the stripes are inserted in the pinboard, they have to be turned upright, so the polished and smooth surface is arranged perpendicular to the substrate surface. After application of a further silicon wafer, the complete stack is rotated.

In the next step, the glass edge of the peripheral area is to be depressed in vacuum, so the glass is hermetically sealed with the silicon, without any air pockets. A ROBAX®-ring coated with boron nitride is placed on the stack as a downholder (f). Here, it is important that the annealing is performed below the transformation temperature of the higher melting glass (g). In a second step, the stack is annealed under atmospheric

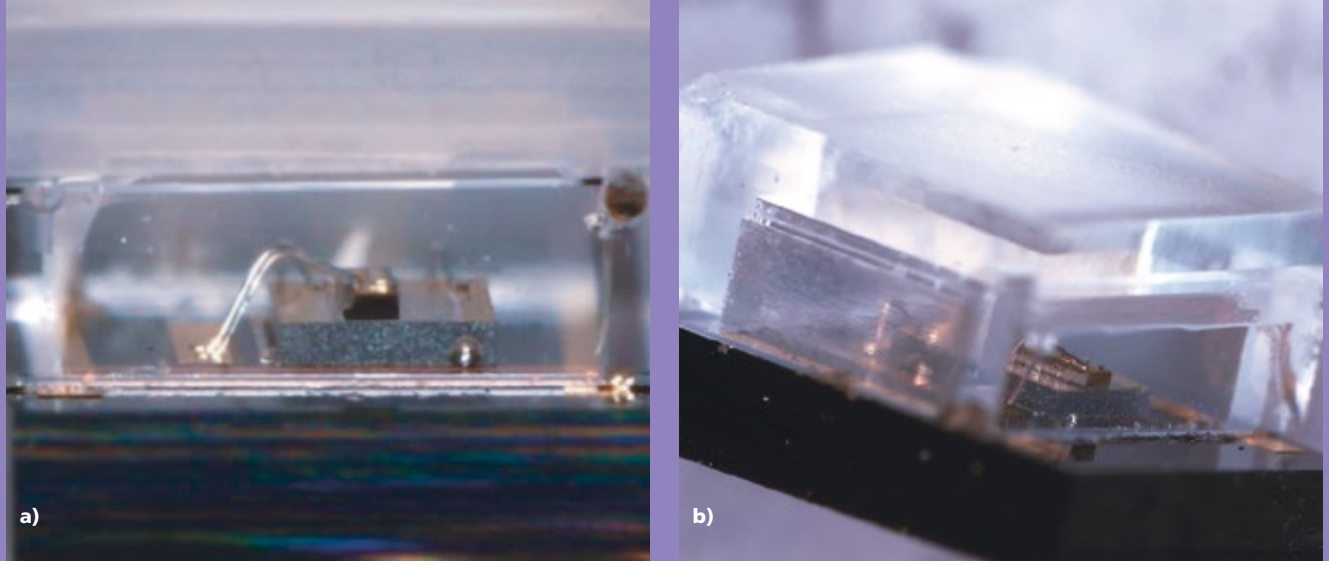


Figure 5: Front view (a) on a mounted laser diode on a submount trough the vertical emission window; b: side view

pressure at the same temperature until the glass is completely flown or pressed down by the pressure difference between the silicon structures and fuses with the high-melting glass window sections (h). The annealing duration is highly dependent on the design and the aspect ratio of the silicon structures. Finally, the silicon is selectively removed in a KOH wet etch step (i). After releasing the complete silicon from the cap wafer, a two-sided grinding step follows.

The front side has to be planarized to enable subsequent processes: A grinding on the lower side must be carried out, because the borosilicate glass does not completely wet the high-melting glass; a resulting gap would prevent subsequent hermetic sealing. After the planarization, an anti-reflective coating is applied. In the next step, a plating base is deposited with a shadow mask on the bond frames of the cap wafer.

Results

First packaged laser diodes with glass cap containing a vertical emission window were built on silicon based wafer substrates. AuSn metallized solder pads and a metal seal frame enable the eutectic laser diode soldering on a sub-mount. An active solder was used for hermetic bonding of the single glass cap.

The first processed glass cap wafer with a vertical emission window for laser diodes demonstrates the capabilities of the new glass forming technology. Recently, the first laser diodes have been successfully packaged with the developed glass caps. The characterization and test of these laser diode devices is still ongoing. The current work is focused on the hermetic bonding technique of the glass cap with the silicon substrate (figure 5).

Authors: Vanessa Stenchly, Dr. Wolfgang Reinert

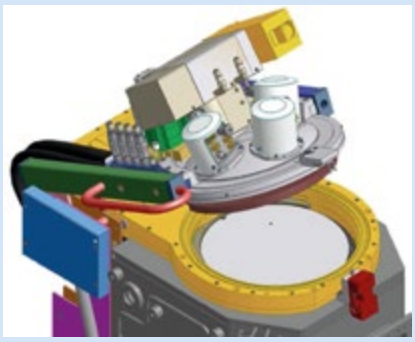
ALScN AS AN IMPROVED PIEZOELECTRIC MATERIAL

Today, the semiconductor Aluminum Nitride (AlN) is the most promising material for numerous piezoelectric MEMS applications. This is due to its good piezoelectric performance and superior dielectric properties, e.g. low permittivity and low dielectric loss. Substituting a fraction of Al with Scandium to form AlScN has been demonstrated to be a viable way to further enhance the material's response. This is of great interest for sensing, actuating and energy harvesting in MEMS applications. Since position sensing of moving parts within MEMS devices is typically carried out by comparably large electrostatic sensors, much more compact piezoelectric sensors help to save space on the device and therefore reduce costs. As it is the same for actuation, piezoelectric materials can introduce significant forces into MEMS, leading to new devices with better actuation performance.

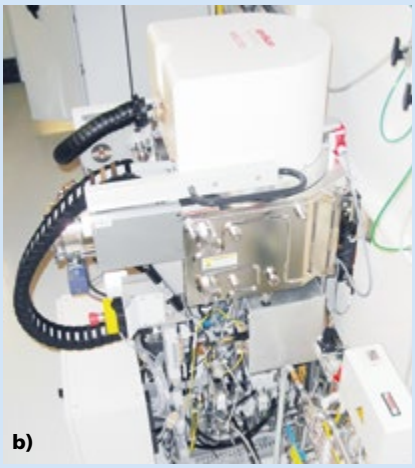
Our work on AlScN is currently focused on energy harvesting applications, where the main goal is an integrated power supply that supports wireless MEMS sensors. Better piezoelectric properties directly lead to an increased output.

We fabricated AlScN on standard 200 mm wafers with Sc content of up to 37 % on top of a platinum bottom electrode in an Evatec MSQ 200 multisource sputtering tool (figure 1).

Precise control of Sc concentration over such a large range was achieved by co-sputtering from two pulsed DC cathodes with varied power. Up to 27 % Sc content, films of constant good quality could be deposited and XRD measurements reveal an exclusively polar texture as well as a narrow rocking curve (figure 3).



a)



b)

c)

Figure 1: (a) sketch of the substrate electrode arrangement and different sources on top; (b) image of the Evatec MSQ 200 single module; (c) view on the upper chamber part with target shutter for single target deposition

Coinciding with these observations, the measured transversal piezoelectric coefficient $e_{31,f}$ peaks at 27 % Sc with 3 C/m², corresponding to a significant increase by a factor of 2.4. At the same time, the permittivity rises moderately by a factor of 1.5 and the loss angle remains constant up to the maximum piezoelectric activity. In our experiments, the favorable behavior of the material's dielectric properties results in a maximum expected performance of AlScN based energy harvesting and sensing MEMS at 27% Sc. Further, control of the AlScN built in stress was achieved over a wide range from strongly tensile to strongly compressive by varying pressure and Ar/N2 ratio during deposition.

In the course of our experiments, we valued the Evatec MSQ 200 sputtering system for its reliability, easy handling and versatility. This enabled a rapid process development for Sc doped AlN with significantly enhanced piezoelectric properties. Deposition and characterization of feasible AlScN layers is only one link in the chain for successful process integration. Issues related to reliability, etching, stress control and compatibility to other processes are equally of great importance and we are working on these topics in order to provide better AlScN based MEMS devices in future.

Author: Dr. Steffen Chemnitz

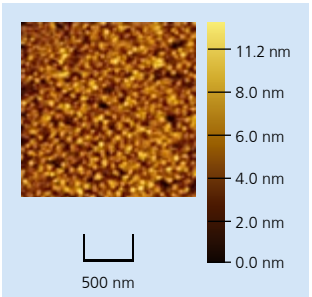


Figure 2: AFM scanned topography of a $Al_{0.73}Sc_{0.27}N$ sample

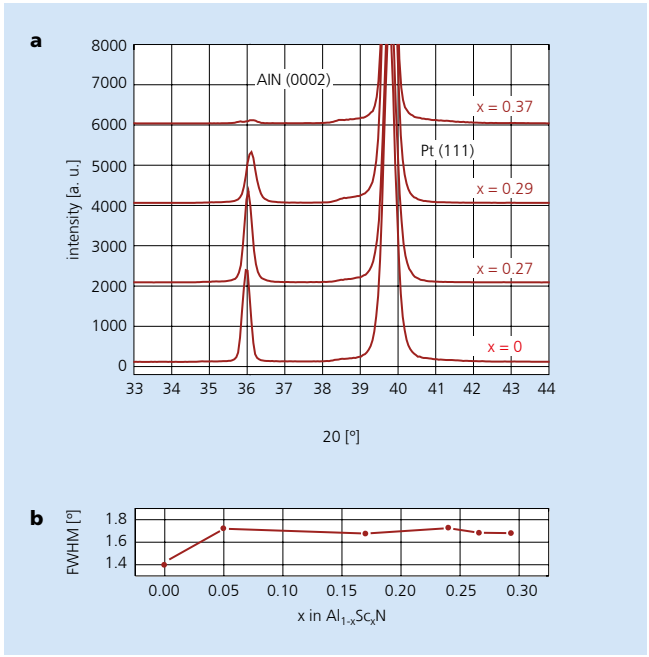


Figure 3: (a) X-ray diffraction patterns for samples with varying Sc content from x=0 to x=0.37 and (b) corresponding rocking curve

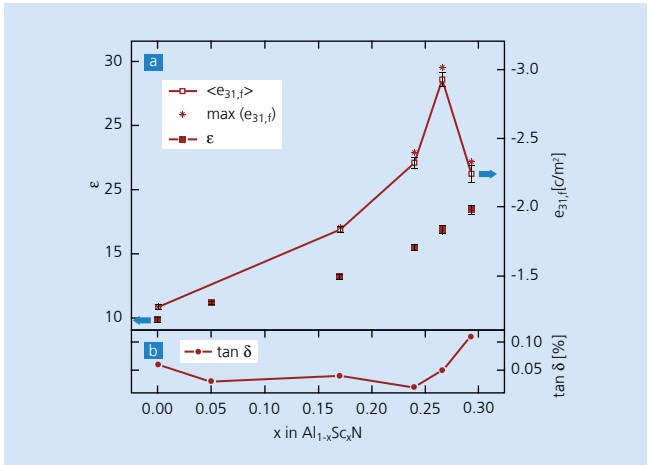
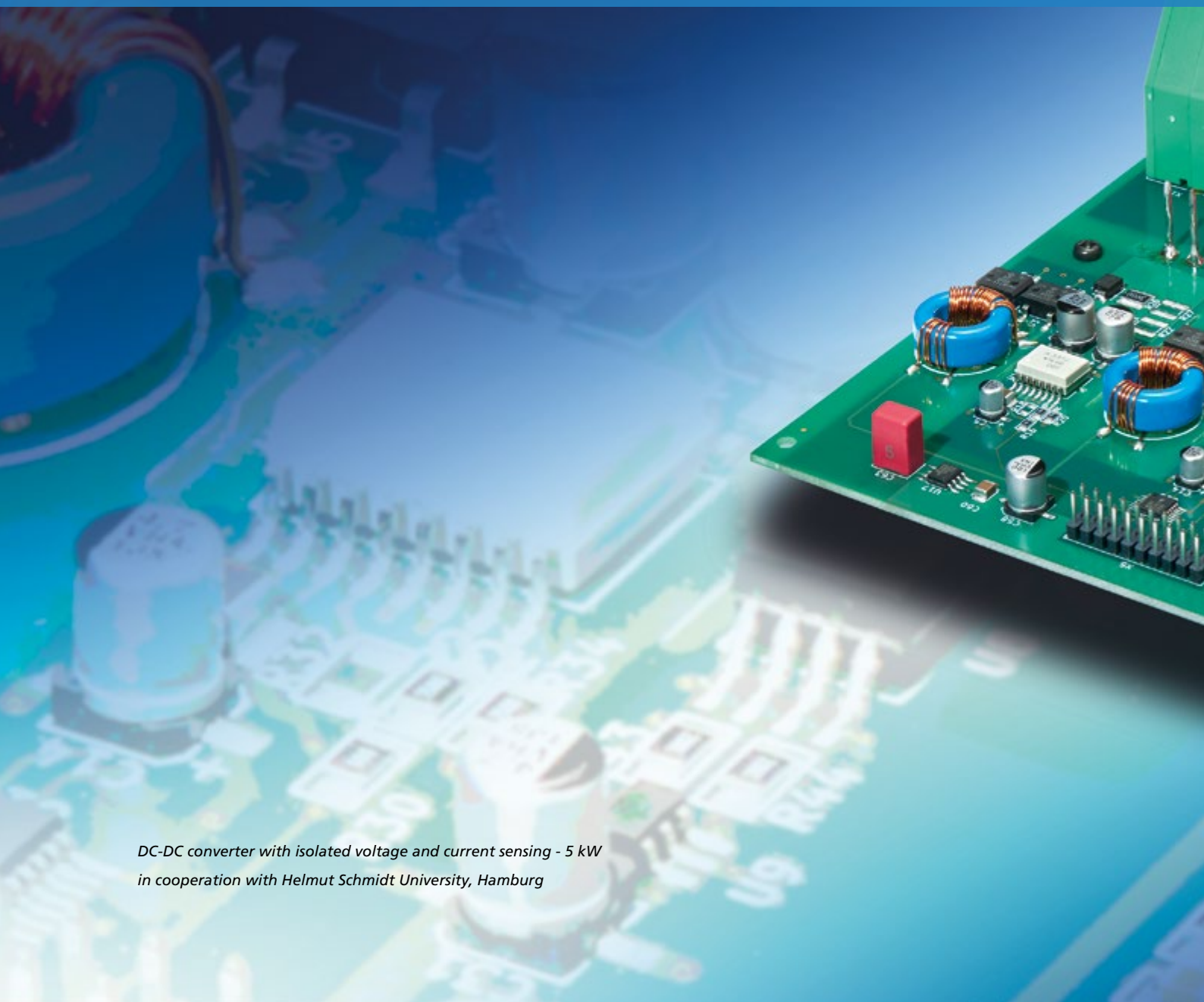


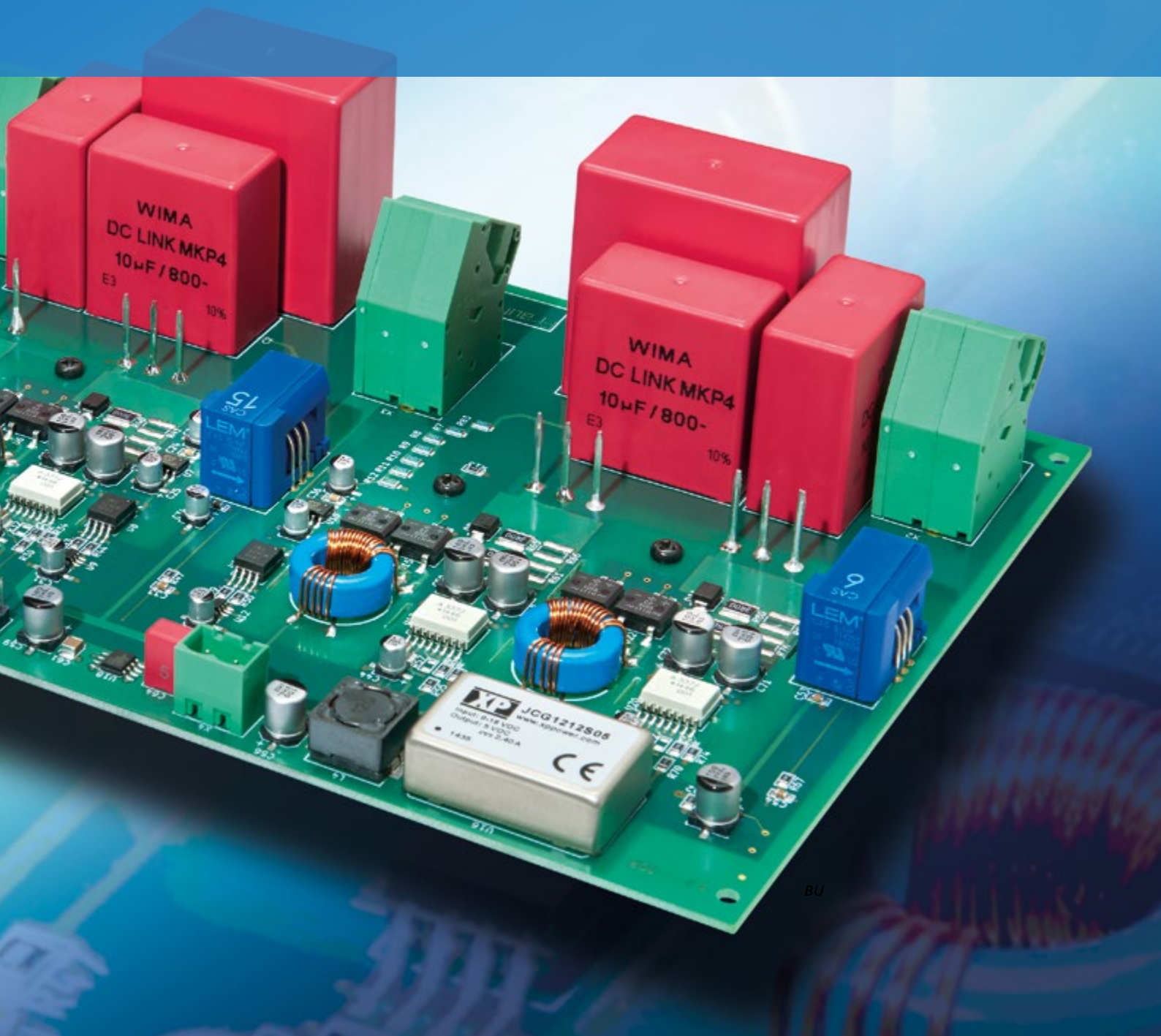
Figure 4: Mean and maximal transversal clamped piezoelectric coefficient $e_{31,f}$ dielectric constant ε and (b) dielectric loss tangent of $Al_{1-x}Sc_xN$ as a function of Sc content

REPRESENTATIVE RESULTS OF WORK



DC-DC converter with isolated voltage and current sensing - 5 kW
in cooperation with Helmut Schmidt University, Hamburg

IC TECHNOLOGY AND POWER ELECTRONICS



Project Name	Zukünftige, effiziente Energiewandlung mit GaN-basierter Leistungselektronik der nächsten Generation (ZuGaNG)
Funding	BMBF (Bundesministerium für Bildung und Forschung) IKT2020 research framework programme
Funding Code	16ES0076K
Organizing institution	VDI / VDE / IT
Partners	Robert Bosch, KACO new energy, Hochschule Reutlingen, TRUMPF Hüttinger, Fraunhofer IAF, Fraunhofer ISIT, EDC Electronic Design Chemnitz, Ferdinand-Braun-Institut, Friedrich-Alexander-Universität Erlangen, LEWICKI microelectronic / First Sensor, Otto-von-Guericke Universität, X-FAB Semiconductor Foundries AG Erfurt
Duration	3 years
Coordinator	Fraunhofer IAF

PROSPECTIVE, EFFICIENT ENERGY CONVERSION WITH GaN BASED POWER ELECTRONICS OF THE NEXT GENERATION (ZuGaNG)

Background

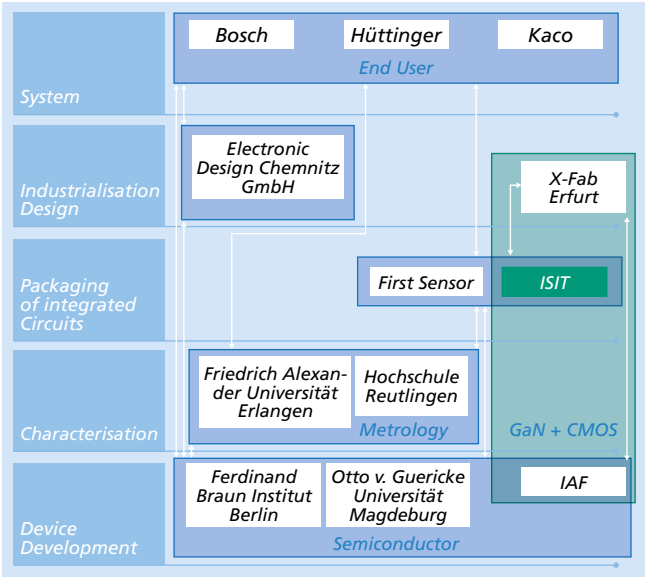
Improving the energy efficiency of silicon-based power electronics systems becomes increasingly challenging. Typical strategies for semiconductor component optimization, namely ultra-thin wafers, gate trench structures instead of planar gates and the CoolMOS technology, are already at the limit of their physical possibilities. By using innovative and future-oriented material technologies, the quest for more efficient, compact, robust and cost-effective power electronic components could be continued. Many of the considered materials are well known III/V or IV/IV semiconductors such as GaN (Gallium Nitride), GaAs (Gallium Arsenide) or SiC (Silicon Carbide). But these kinds of semiconductors have several drawbacks: GaN for wafer substrates ≥ 4" is only available as hetero-epitaxial layer; GaAs requires handling of toxic arsenic chemistry that could exhaust e.g. as arsenic acid during processing, and SiC substrates are 20 times more expensive than silicon substrates.

One solution could be the combination of silicon and other semiconductors to use the advantages of both materials, but almost all semiconductor fabs are exclusively designated for the processing of silicon. Processing non-silicon materials in these fabs is undesirable because this would lead to contamination and failure of the silicon products.

Project description

The project "ZuGaNG" is subdivided into two groups: The main cluster (Figure 1) includes industry manufacturers as well as research institutes, focusing on research, development and optimization of GaN based high voltage transistors. Due to their high operating frequency (100 kHz...1 MHz), these transistors have the capability to further reduce the power loss of voltage transformers by up to 50% and they can operate reliably even at higher temperatures than silicon based transistors. The second group is focused on the technological integration of CMOS and GaN processes. The involved partners are X-FAB Erfurt (CMOS) and Fraunhofer IAF (GaN). ISIT is responsible for standard BEOL (Back-End-of-Line) technologies as well as BEOL process innovation for building functional devices of both semiconductor materials on a Silicon wafer. Along with developing and optimizing the BEOL processes, and depending on previous technology variations, the grade of contamination by GaN is monitored for machines and media. As a consequence of the technical conditions to process on 4" wafers, many tasks are carried out within the "Nanocluster" clean room of the Christian-Albrechts-Universität (CAU) in Kiel.

Figure 1: Project partners and their activities



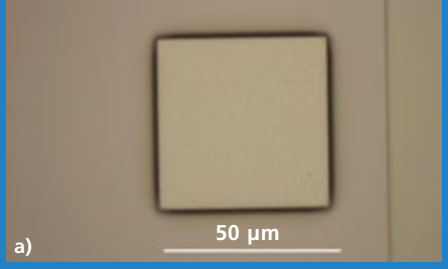


Figure 2: Comparison of the contact hole etch process:
2a) dry etch only, showing damages by plasma etch
2b) dry etch followed by a 100 nm BOE wet etch

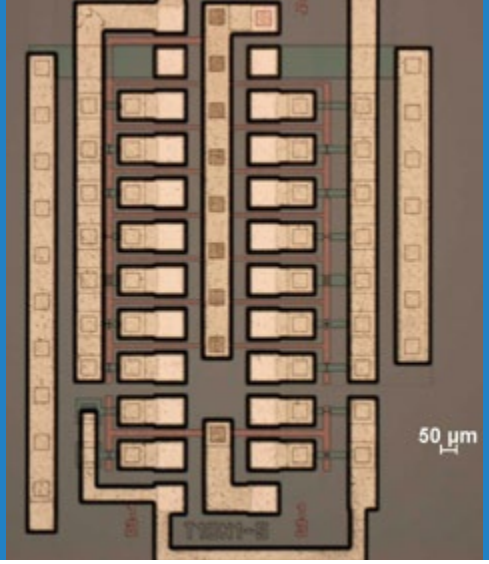


Figure 3: Device after finalization at CAU

Results

In the first phase of the project, ISIT successfully proved that the planned BEOL process is compatible with X-FAB CMOS technology. A batch of CMOS wafers was hence sized down from 6" to 4" and processed according to operation sequences and specifications by X-FAB. While most of the process elements were adopted without difficulty, some steps had to be modified. One of the necessary changes was the contact hole structuring: In a first test, a dry etching process was used to open the 700nm thick SiO (Silicon Oxide) layer. The etching plasma generated a certain roughness of the silicon surface (Figure 2a), therefore the process was split into an initial dry etch for the first 600 nm of SiO, followed by wet etching in BOE (buffered oxide etch) to remove the remaining 100 nm SiO (Figure 2b) until the silicon surface is reached. As a result of the first phase, a finished device is shown in Figure 3.
In the last process step, the wafers were annealed in forming gas. Annealing is a necessary final step in CMOS production to remove crystal defects from the Silicon. The transfer characteristics of transistors (device type "20/20 n-e") before and after annealing are shown in Figure 4. Other electrical measurement results such as characteristics of transistors of other devices and resistant chains show a good accordance to genuine X-FAB fabrication.

Perspectives

In the next steps, the influence of the epitaxial GaN deposition on pre-processed CMOS-wafers will be studied. The goal is to investigate:

- the impact of the GaN deposition temperature on the doping profiles of the CMOS-wafer,
- the growth of GaN on <111> silicon vs <100>,
- suppression of GaN nucleation on the surface of the dielectric layer,
- contamination of tools and process media with GaN after each process step.

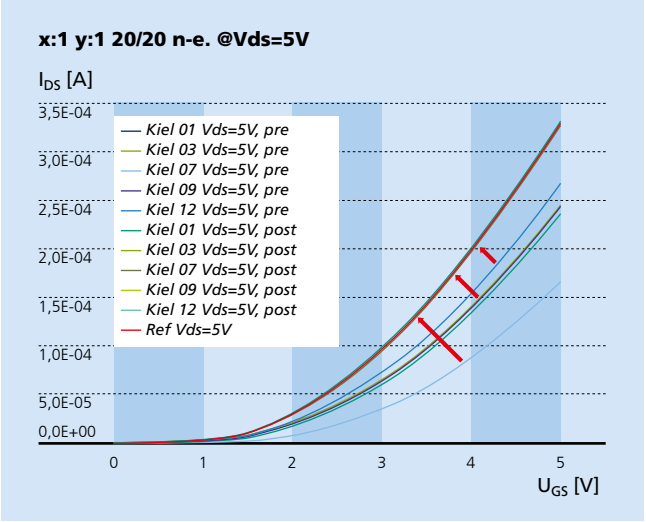
In the second phase of "ZuGaNG", the wafers prepared by X-FAB are sized down from 6" to 4" by ISIT and shipped to Fraunhofer IAF for GaN deposition. The BEOL process flow for this run comprises:

- etching of contact holes into the passivation with silicon and GaN underground,
- metal deposition and structuring for interconnects,
- deposition and structuring of passivation layers,
- annealing of the GaN alloy in forming gas,
- electrical measurement of the transistors.

The first three topics include a monitoring of GaN contamination along the process steps. The goal of the third process run will be to investigate the functionality of monolithic transistors made of Si and GaN, still with the same overall process chain involving X-FAB, IAF, ISIT and CAU.

Authors:
Frank Dietz, Heiko Züge

Figure 4: Relationship between IDS and UGS before and after anneal; reference wafer from X-FAB (device "20/20 n-e", Vds = 5V)



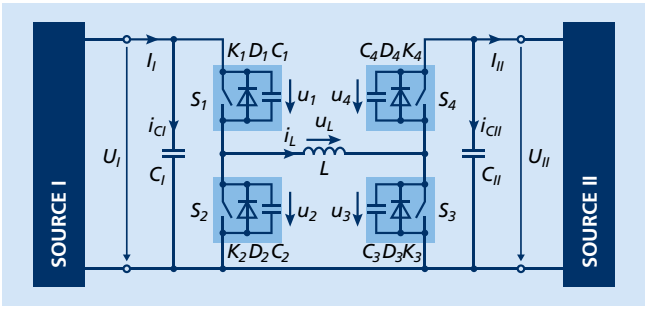
A NOVEL CONTROL SCHEME FOR HIGHLY EFFICIENT POWER CONVERSION WITH NON-INVERTING BUCK-BOOST CONVERTER

Bidirectional DC-DC converters for coupling energy storage with power systems such as hybrid electric vehicles (HEV) and photovoltaic systems have recently attracted a lot of attention. In many of these applications, input and output voltage of the converters have overlapped range.

The bidirectional non-inverting buck-boost converter (NBuBoC), as shown in figure 1, is often employed for these applications due to its wide voltage conversion ratio and simple topology. However, with the conventional control methods, the NBuBoC has a distinct drawback, namely the low power conversion efficiencies, especially during the transition phase between the step-down and step-up modes.

Since the performance of the NBuBoC has a significant impact on the efficiency of the entire power system, there is an urgent demand to minimize the power losses in the NBuBoC. A novel control scheme has therefore been developed at the Application Center "Power Electronics for Renewable Energy Systems" of Fraunhofer ISIT. Using this scheme, the NBuBoC can achieve a highly efficient power conversion at all operating points.

Figure 1: Topology of the bidirectional non-inverting buck-boost converter



Control principle

The main idea of the novel control scheme is to modulate the switching frequencies and the time delays of the Pulse Width Modulation (PWM) signals depending on operating points. In this manner the switches can always be switched under Zero Voltage Switching (ZVS) condition and at the same time the conduction losses in the switches and the power losses in the inductor and capacitors can be minimized. Consequently, the power conversion efficiency of the converter can be optimized for a wide power range. Furthermore, with the novel control, the voltage conversion ratio of NBuBoC can vary from 0 to infinity by changing the duty ratio of the PWM signals, which means no transition of different operating modes due to the change of the voltage levels is needed any more.

ZVS of the switches

A switch used for the NBuBoC is normally a combination of a semiconductor device with an external Schottky diode and a snubber capacitor. Schematically, each switch S_i in the converter consists of a channel K_i, an antiparallel diode D_i and a capacitor C_i, as depicted in figure 1. The diode symbolizes the body diode of the used semiconductor device or the parallel connection of the body diode with an external Schottky diode. Similarly, the capacitor can be the parasitic output capacitance of the semiconductor device or the parallel connection of the parasitic capacitance with a snubber capacitor. For the ZVS of the switches, the inductor current must be positive while turning off the switches S_1 and S_3, and negative while turning off S_2 and S_4. Furthermore, the absolute value of the inductor current must be high enough while turning off the switches so that the capacitors of the switches can be completely charged and discharged within the dead times.

Optimal switching frequencies and time delays

Different combinations of switching frequencies and time delays can stabilize the NBuBoC at one single operating point (U_I, U_{II}, I_I, I_{II}). However, the power conversion efficiency at this operating point can only be maximized by a single combination. One way to find such an optimal configuration is to build the mathematical relationship between the total power losses in the converter and the combination of the switching frequency and the time delay. Then the optimal switching frequency and time delay can be obtained by minimizing the total power losses under ZVS condition of the switches.

Figure 2 and figure 3 show the optimal switching frequencies and the time delay factors for the power range "input voltage 400 V, output voltage range from 150 V to 500 V, output current from 1 A to 5 A" respectively. The switching frequency is first increased with the increase of the differential between the input and output voltages. After reaching a maximum value the switching frequency is reduced. At the operating points where the input voltage U_I is close to the levels of the output voltage U_{II}, the switching frequency approaches its minimum value. Additionally, the switching frequency

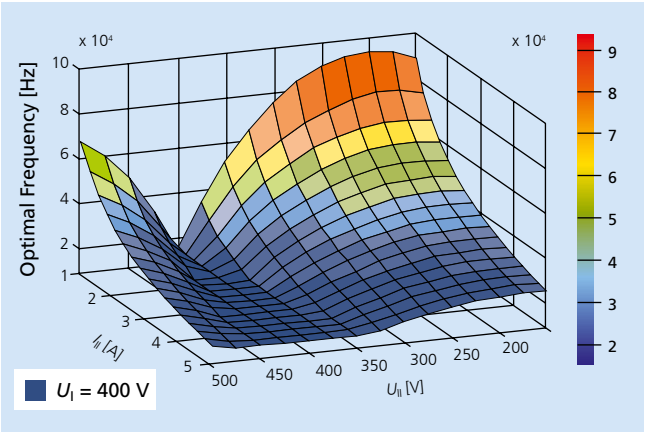


Figure 2: Optimal switching frequency

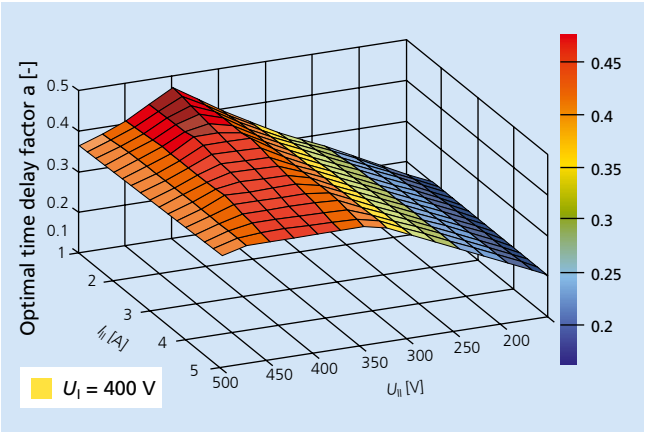


Figure 3: Optimal time delay factor a

Nevertheless, the mathematical model will be very complicated in this way. A simpler strategy is to minimize the RMS value of the inductor current under ZVS condition. The basis for the feasibility of this strategy is that the power losses in the switches, in the inductor and in the capacitors are all dependent on the RMS value of the inductor current when the switches are gated under ZVS condition.

decreases with the increase of the output current I_{II}. Finally, the switching frequency is limited. The lower boundary is utilized to restrict the volume of the system and the ripple of the output voltage as well as to prevent acoustic harassments. The upper limit is determined by the maximum switching frequency of the used semiconductor devices. As shown in figure 3, the time delay factor α decreases with the increase of the differential between U_I and U_{II}.

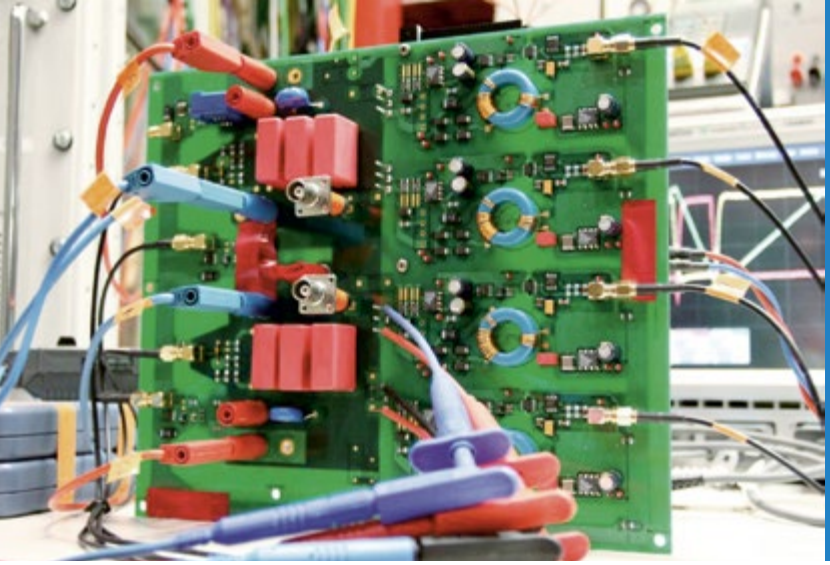


Figure 4: A prototype for verification of the control scheme

Experimental verification

For the verification of the control scheme, a prototype dimensioned for a maximum power of 3 kW and a maximum voltage of 600 V, as shown in figure 4, has been designed and tested in the power electronics laboratory of the Helmut Schmidt University in Hamburg. The gate driver circuits are isolated from the power part, and its voltage levels for the turning-on and turning-off of the switches are adjustable which makes the testing with Si and SiC semiconductor devices more flexible.

The power conversion efficiencies of the prototype are illustrated in figure 5. With the new control scheme, the prototype achieves a minimum efficiency of more than 98 % at 5 % load and a maximum efficiency of more than 99.4 % at the operating points, where the output voltage approaches the levels of the input voltage.

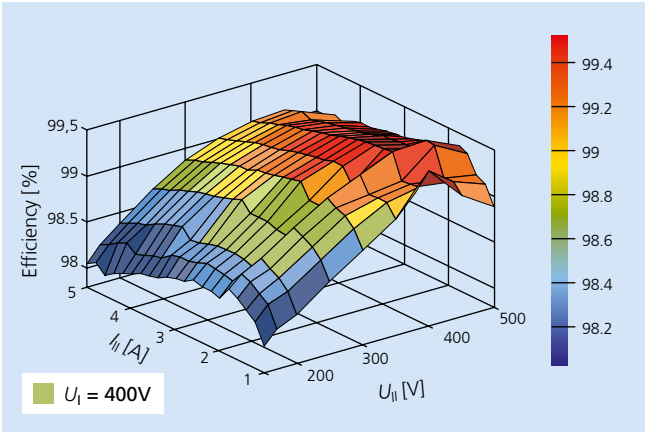


Figure 5: Power conversion efficiencies of the prototype

Acknowledgment

This work was funded by the Free and Hanseatic City of Hamburg (Hamburg City Parliament publication 20/11568).

Authors:
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Prof. Holger Kapels,
Prof. Klaus F. Hoffmann, Helmut-Schmidt-Universität

INNOVATIONSCLUSTER POWER ELECTRONIC FOR RENEWABLE ENERGY

Introduction

Regional network building along the value added chain of a complementary partner consortium is an efficient strategy in strengthening R&D collaboration successfully. A three column model, consisting out of applied research at Fraunhofer Institutes, basic research at universities and R&D transfer for innovative products by industry, is creating economic success, knowledge and employment for regional development. The special instrument therefore are Innovationclusters being funded by Fraunhofer and the federal governments.

One of the natural given highlights of northern Germany is the renewable energy by wind power. More than 14 GW nominal power are currently installed in the german federal states Schleswig-Holstein and Niedersachsen which are providing about one third of the total wind energy exploitation in Germany. Therefore, many companies including SMEs like wind power plant manufacturers, OEM component suppliers up to companies for projecting and operating wind farms are located here. Based on this approach the Fraunhofer society in Germany together with the federal governments in Schleswig-Holstein and Niedersachsen have been funded the Innovationcluster Power Electronics for Renewable Energy.

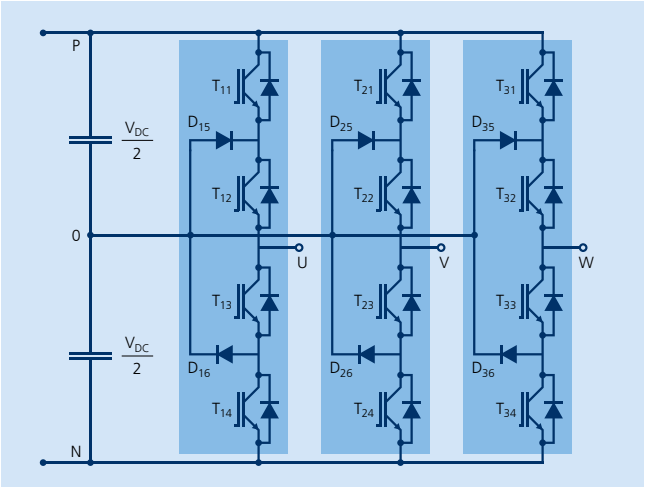
Collaboration

The consortium is consisting of the companies Vishay Siliconix Itzehoe GmbH, Danfoss Silicon Power GmbH, Reese & Thies, FTCAP GmbH and Senvion SE Wind Energy Solutions as well as the academic institutions Christian-Albrechts-University of Kiel, University of Applied Sciences Kiel, University of Applied Sciences Flensburg and the West Coast University of Applied Sciences Heide, all located in the federal state of Schleswig- Holstein. Fraunhofer ISIT in Itzehoe is the coordinator of this Innovation Cluster.

In addition to those activities the Innovationcluster of the german country Niedersachsen is addressing complementary tasks such as analysis of failure causes, conditioning monitoring and life time predictions as well as failure tolerant system concepts for power electronics in wind power plants. This Innovationcluster of Niedersachsen is coordinated by the Fraunhofer Institute for Wind Energy and Energy System Technology IWES.

Both Innovationcluster activities complement one another in terms of expertise, technical cooperation and coordination of joint workshops.

Figure 1: Schematic diagram of neutral point clamped (NPC) 3-level converter



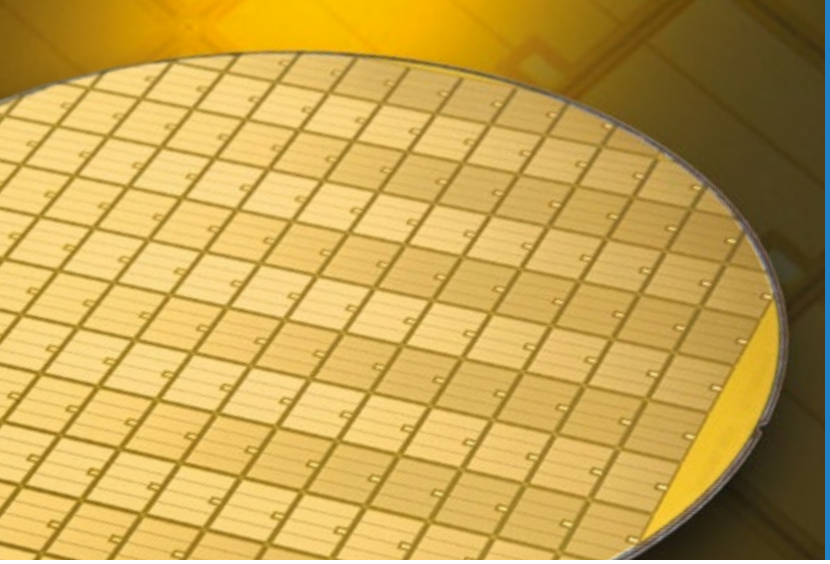


Figure 2: Top view of a 1200 V/200 A IGBT wafer with Ni-Au metallization for DBB assembly technique

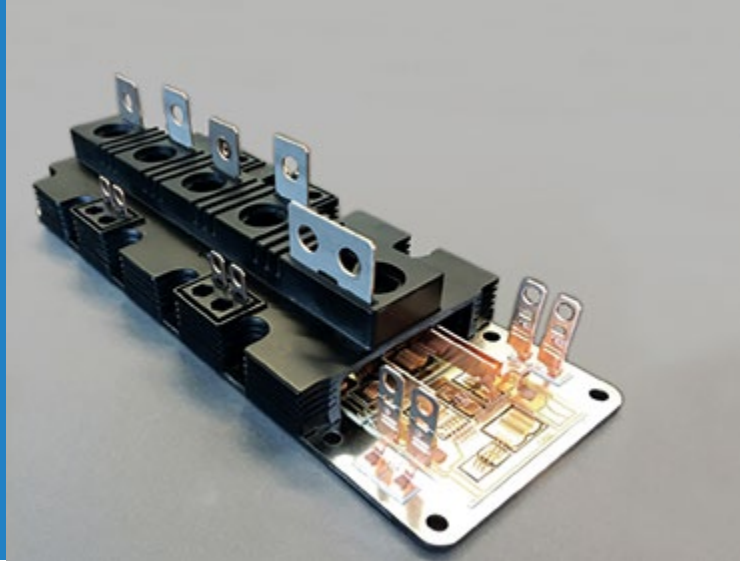


Figure 3: P3L power module with Cu wire bonding in DBB assembly technique (Danfoss Silicon Power)

Objective

The Innovation Cluster Power Electronics for Renewable Energy in Schleswig-Holstein aims at the improvement of power electronic components for wind power plants working in the MW range. With the growing importance of the renewable electrical power generation by wind energy, the requirements on power quality are increasing for electrical current feeding to the grid. Therefore, the project is mainly focusing on the development of innovative system concepts for the power converters of wind power plants.

Special emphasis is put on the considerable enhancement of reliability, efficiency and power density of the components applied which is especially important for offshore wind power plants working under harsh environmental conditions. Most important are failure rates and correlated down times of wind power plants. Statistics show that 15–20 % of loss rate are due to converter failures. Assuming lifetime specifications of 20 years for electronic components, especially for offshore operation under critical maintenance conditions special need for improvement becomes obvious. New components for wind power converters have been developed and tested all along the industrial value added chain.

The objective of this project was the development of highly efficient and reliable 1 MW power stack for a modular back to back full power conversion in a 3-level NPC topology (Neutral Point Clamped) as shown in figure 1. The power stacks are able to be parallelized for a total power up to 6 MW. The advantage of this configuration is an AC output voltage of 950V at a rated current of 600 A. In contrast, the typical AC voltage in a 2-level configuration is 690 V leading to higher currents with increased cable cross sections. The DC-link voltage of +-800 V allows to use 1200 V IGBTs instead of 1700 V IGBTs as being applied for 2-level converters. The reduction of filtering due to the reduced total harmonic distortions is a further advantage of the 3-level topology.

Application specific Silicon power devices (IGBTs) suitable for innovative assembly techniques, power modules with highest reliability based on sintering and Copper wire bonding, efficient converter topologies and driver circuits as well as new mechatronic concepts are the base for an advanced power stack generation.

To comply with special requirements of the Danfoss Bond Buffer (DBB) module assembly technique specific 1200 V/200 A IGBTs were developed by ISIT and Vishay Siliconix Itzehoe GmbH. These requirements included Ni/Au front side metallisation and layout adjustments for optimal fitting of the DBB as illustrated in figure 2. Trade-Off adjustments of static and dynamic losses were carried out with regard to optimal system conditions.

The P3L power module assembled in DBB technique has being developed at the University of Applied Sciences Kiel in close collaboration with Danfoss Silicon Power as shown in figure 3. In the 1 MW power stack 3 modules one for each phase are implemented. To account for a nominal current of 600 A 3 IGBTs have to be used in parallel which results in 12 IGBTs for each phase leg.

In order reach the life time and current density requirements the modules are assembled according to the Danfoss Bond Buffer technique allowing Cu wire bonding without damaging the IGBT and the Diodes mechanically.

Excellent reliability results based on power cycle tests at ISIT have been achieved as illustrated in figure 4. The standard assembly technique refers to Al wire bonding and solder joints

Figure 5: 3-level NPC power stack for 1MW developed by the Innovationcluster Power Electronics for Renewable Energy (Exhibition PCIM 2015)

whereas the new DBB method is based on Cu wire bonding and Ag sintering resulting in a lifetime improvement by a factor 20.

A low inductance Gate Driver has been developed for the NPC converter by the University of Kiel. For increasing the system efficiency an active Gate control was implemented. The transmission of fault and Gate signals is being done by optical fiber connection in order to reduce the impact on possible EMC influence.

The 3-level power stack as shown in figure 5 is based on an industrial 2-level power stack from Danfoss and was mechanically redesigned by the University of Applied Science Kiel, taking into account low inductive design, compactness, reliability and efficiency. The electrical design was carried out by the University of Kiel. The power stack was tested up to 800 kVA in a circulation power test by Danfoss and University of Kiel. The efficiency for grid-side of the overall NPC inverter at 600 V, 600 A is approx. 97,8% and at 1200V, 600 A is approx. 98,3 %.

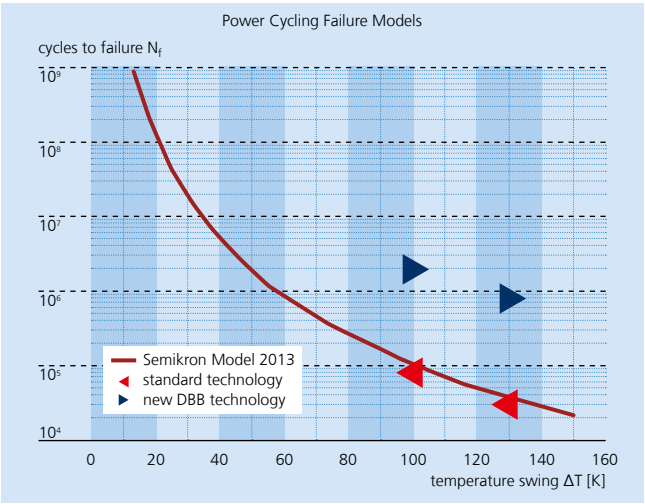


Figure 4: Comparison of reliability results by power cycle tests (blue: DBB Cu wire bonds, red: Al wire bonds)

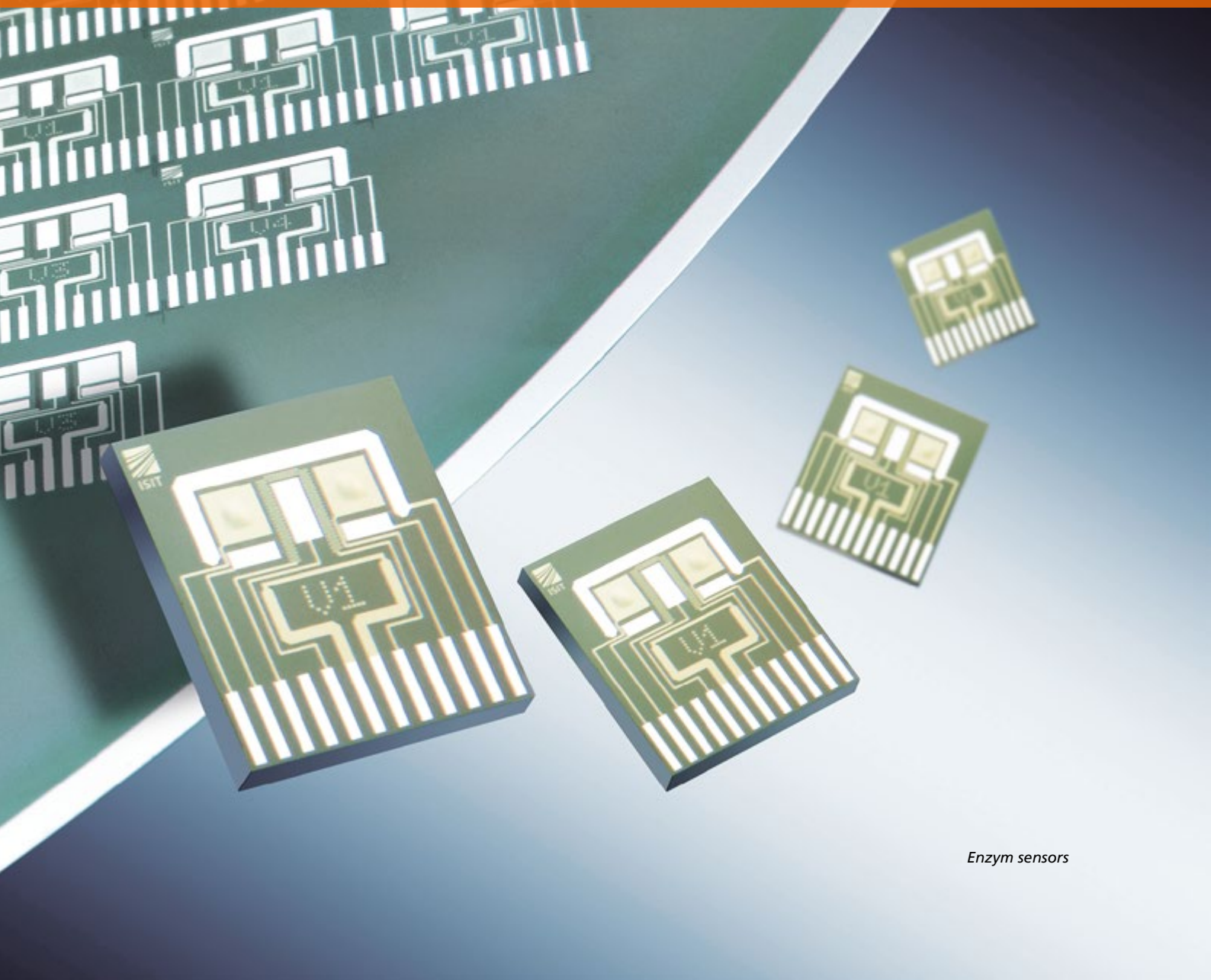
Summary

By the excellent results achieved the innovation cluster is demonstrating successfully the funding concept and the outstanding collaboration of the Schleswig-Holstein consortium. In this context we would like thank the partners, the "Wirtschaftsförderung und Technologietransfer Schleswig-Holstein GmbH", the Ministry of Economy of Schleswig-Holstein and the Fraunhofer Society. The governmental funding is given within the framework of "Zukunftsprogramm Wirtschaft" for European regional development.

Author: Detlef Friedrich

REPRESENTATIVE RESULTS OF WORK

BIOTECHNICAL MICROSYSTEMS



Enzym sensors

Project: MiChroChip (intern)
Internal project of Fraunhofer ISIT
May 2013 – May 2015

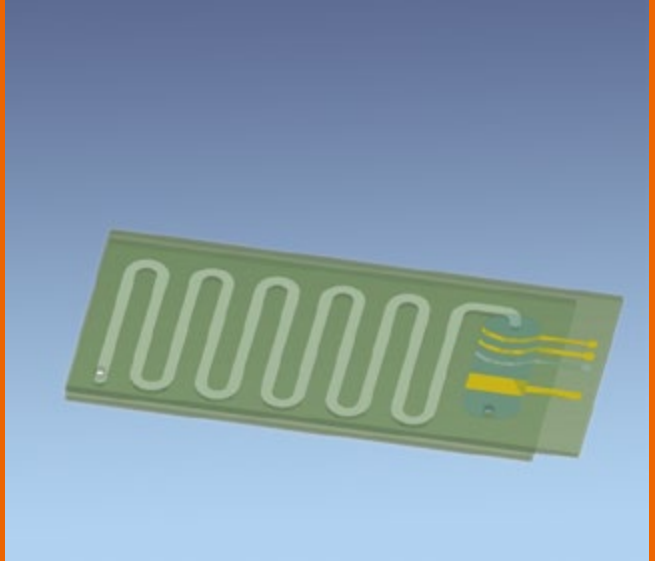


Figure 1: Construction scheme of the chromatography chip

TOWARDS MINIATURIZED LIQUID CHROMATOGRAPHY: ISIT'S INTERNAL "MICHROCHIP" PROJECT

Liquid chromatography techniques and especially the high performance liquid chromatography (HPLC) are well established and commonly used methods in analytical chemistry. The wide field of applications ranges from food chemistry to environmental chemistry, diagnostics and biochemistry. Up to now, HPLC analytics is limited to laboratories, because integrated miniaturized systems do not exist.

To make this technology usable for flexible application scenarios by bringing the system down to handheld size, the internal project "MiChroChip" (Micro-Chromatography-Chip) was carried out for 2 years. The objective was to develop and evaluate basic technologies for manufacturing a chip for miniaturized liquid chromatography. Different departments were involved to bundle inter-disciplinary knowledge available at ISIT: Biotechnical Microsystems (BTMS), Microsystems Technology (MST) and Module Integration (MI) as well as ISIT´s subsidiary at the University of Kiel. Our technological integration was carried out on 200 mm Silicon wafers, using typical MEMS technologies on one hand, and an innovative powder deposition technique on the other.

A fast, flexible and portable liquid chromatography system primarily requires a three-dimensional porous separation "column", which is more of a serpent shape in our case. Under high fluidic pressure up to 50 bar, a carrier liquid containing the analytes is forced through the dense pores. Due to their different specific transition times, a separation of the constituents can be observed and is quantified through a time recording of the analyte detector using amperometry. The deposition of electrode material at the column outlet was not yet part of the project. An external pump from Cetoni, Dresden was used, which will equally be integrated in a later phase using a miniaturized high-pressure pump.

Technological approach

Our technology approach is based on a chromatography chip that is integrated in a cartridge to provide an interface for all fluidic and electric connections. Obviously, both the chip and the cartridge connectors have to withstand high pressure conditions to avoid any leakage. We applied a wafer to wafer bonding process for sealing a two-wafer stack. The bottom wafer contains the porous serpent-shaped separation column ("column wafer"). The upper wafer is used for capping the column wafer ("cap wafer"), but it will also contain the electrodes for the on-line electrochemical detection. A construction scheme of the chromatography chip is shown in Figure 1.

Based on this design, a manufacturing process was established to form cavity structures in the column wafer by dry-etching into the Silicon bulk. In a further step, two different technological approaches for integrating a solid porous material into the cavities were realized, with particular emphasis of the stability under high pressure.

Figure 3: Silicon wafer with "on-chip" porous SiO_2 separation columns

First approach: Al_2O_3/SiO_2 procedure

The first approach was to integrate solid porous columns into the chip cavities using Al_2O_3 and/or SiO_2 material. An innovative micromechanical deposition process was developed that cannot be disclosed further at this time. Porous but very stable structures could be realized, which withstood fluidic pressures up to 50 bar. Figure 2 shows a part of the processed column that was intentionally broken out of the Silicon wafer cavity. The cross-sectional dimensions are 350 x 500 µm.

On the wafer level, the separation columns look like shown in Figure 3 (SiO_2 example).

Second approach: Ceramic material

The second approach was to dispense a porous Silicon-based ceramic paste into the etched wafer cavities, using a specific formulation with defined characteristics that was provided by Fraunhofer IKTS in the framework of a subcontract. This ceramic precursor was sintered into the wafer cavities according to a defined protocol; the result of this process is shown in Figure 3 on a part of the filled cavity.

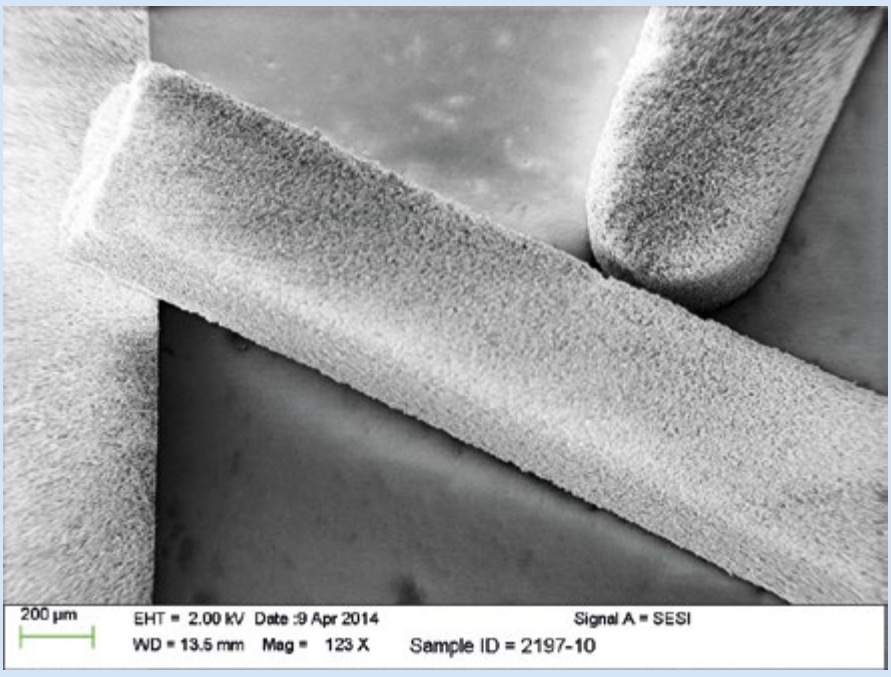


Figure 2: Electron microscopy of a processed porous column (removed from the Silicon carrier)

Figure 5: Chromatography chip

The cap wafer was made of Borofloat® glass. Into this wafer, holes were drilled mechanically for the fluidic connection to the separation column. Both wafers were bonded hermetically tight using a glass frit process, then the wafers were cut into single chips of 10 x 20 mm^2. The complete chromatography chip is shown in Figure 5, with exception of the noble metal electrodes which were not yet included in this project.

A cartridge to take up the chromatography chip was designed (Figure 6), with classical HPLC fittings for fluidic standard high pressure connectors.

For chip evaluation, the amperometric detection was carried out with a second chip placed behind the chromatography chip. As the second detection chip, our array biochip was used, providing 16 Gold working electrodes, a Platinum counter electrode and an Iridium-oxide reference electrode. For our test measurements, only two of the working electrodes were needed. First test separations and measurements show promising results with the SiO_2 approach. Nevertheless, several aspects have to be optimized, e.g. increasing the internal surface of the separation column, close detection and further fluidic integration.

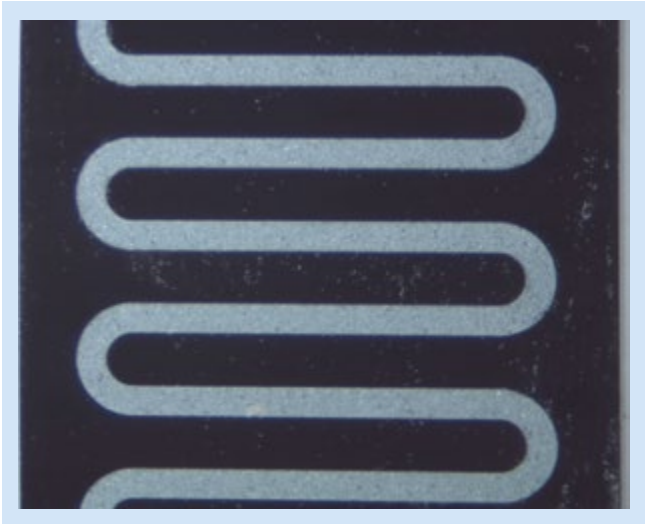
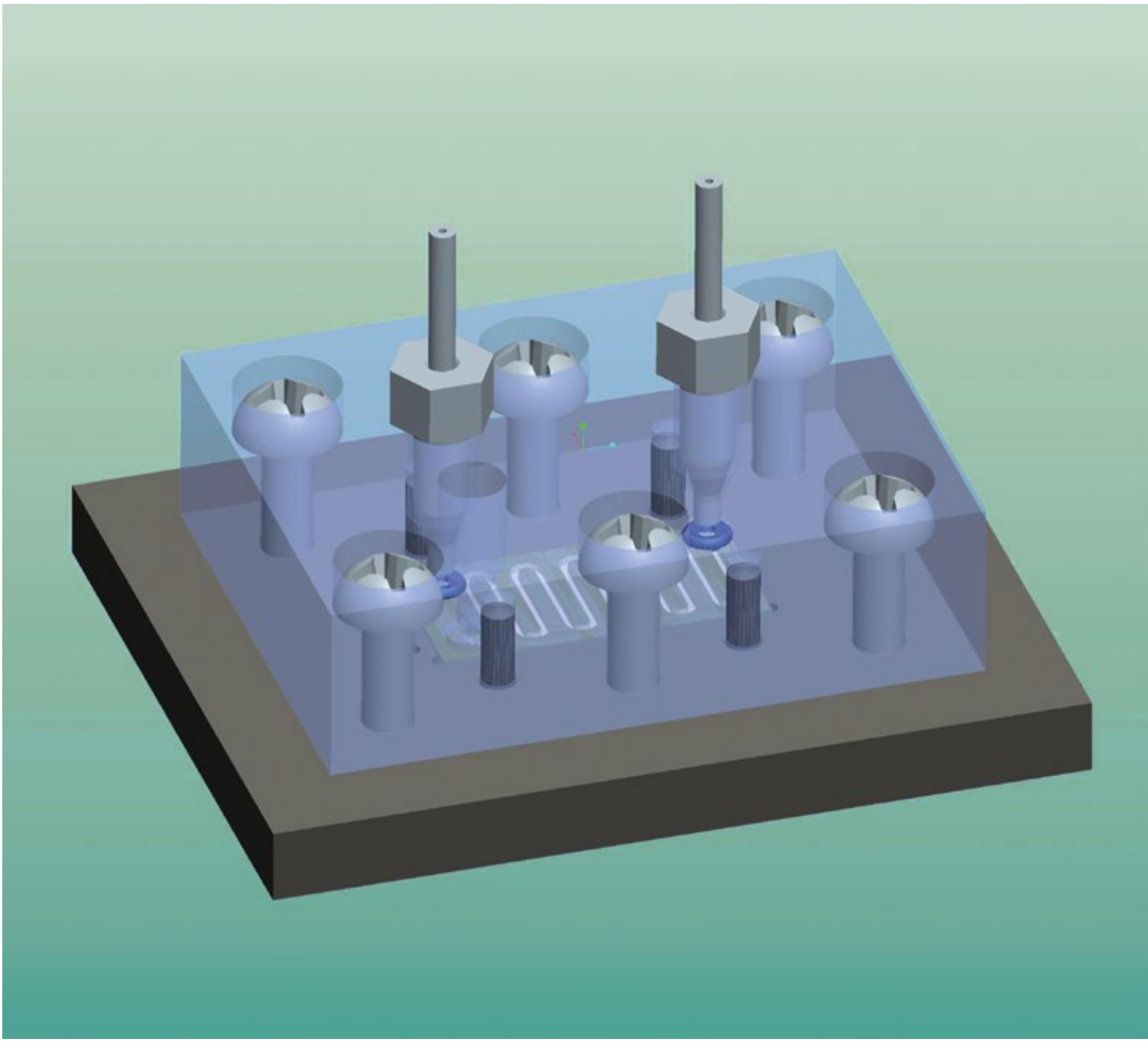


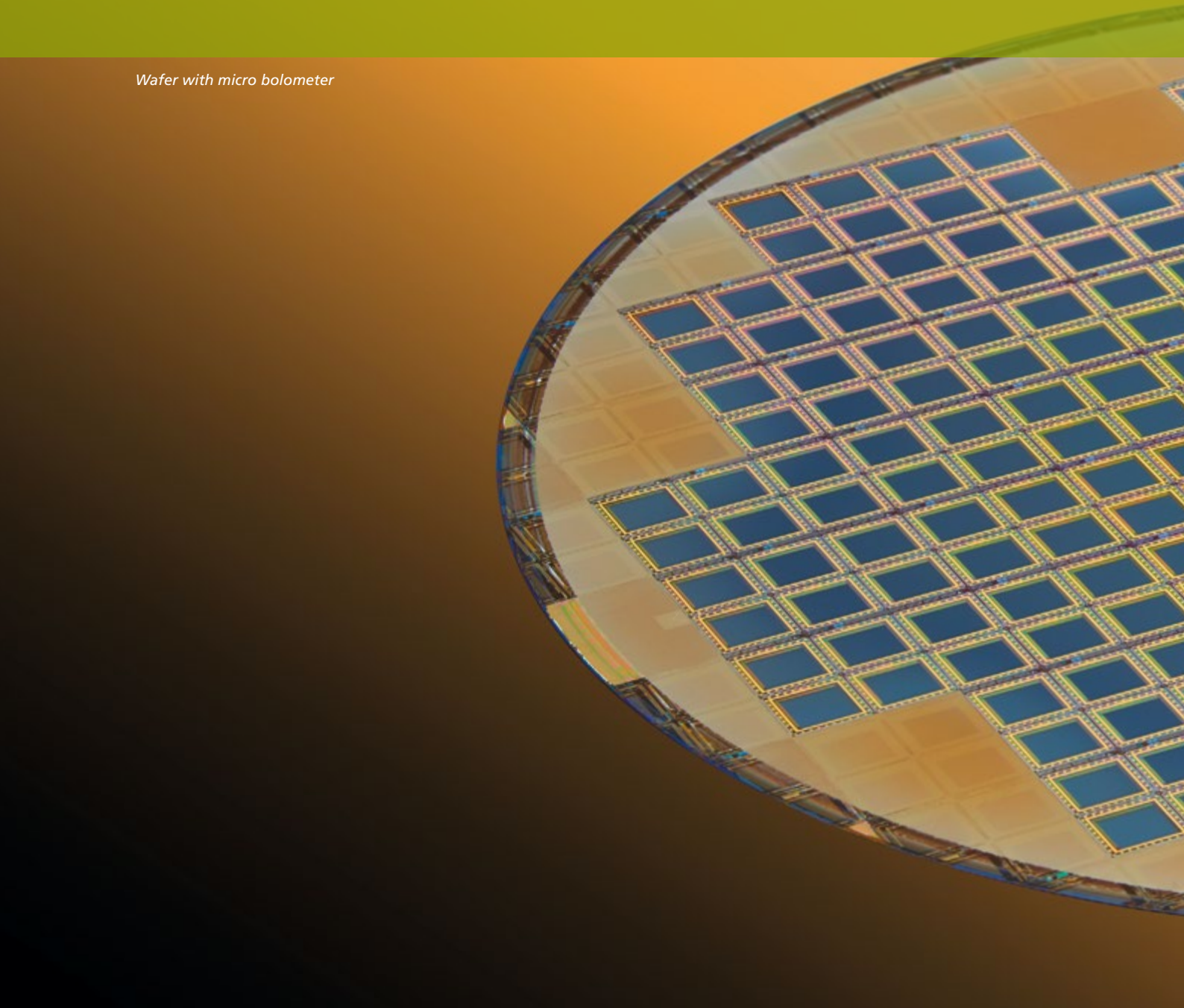
Figure 4: Separator column formed by sintered porous Silicon ceramic

Author:
Dr. Gundula Piechotta

Figure 6: Construction scheme of the cartridge for chromatography chip with fluidic connectors

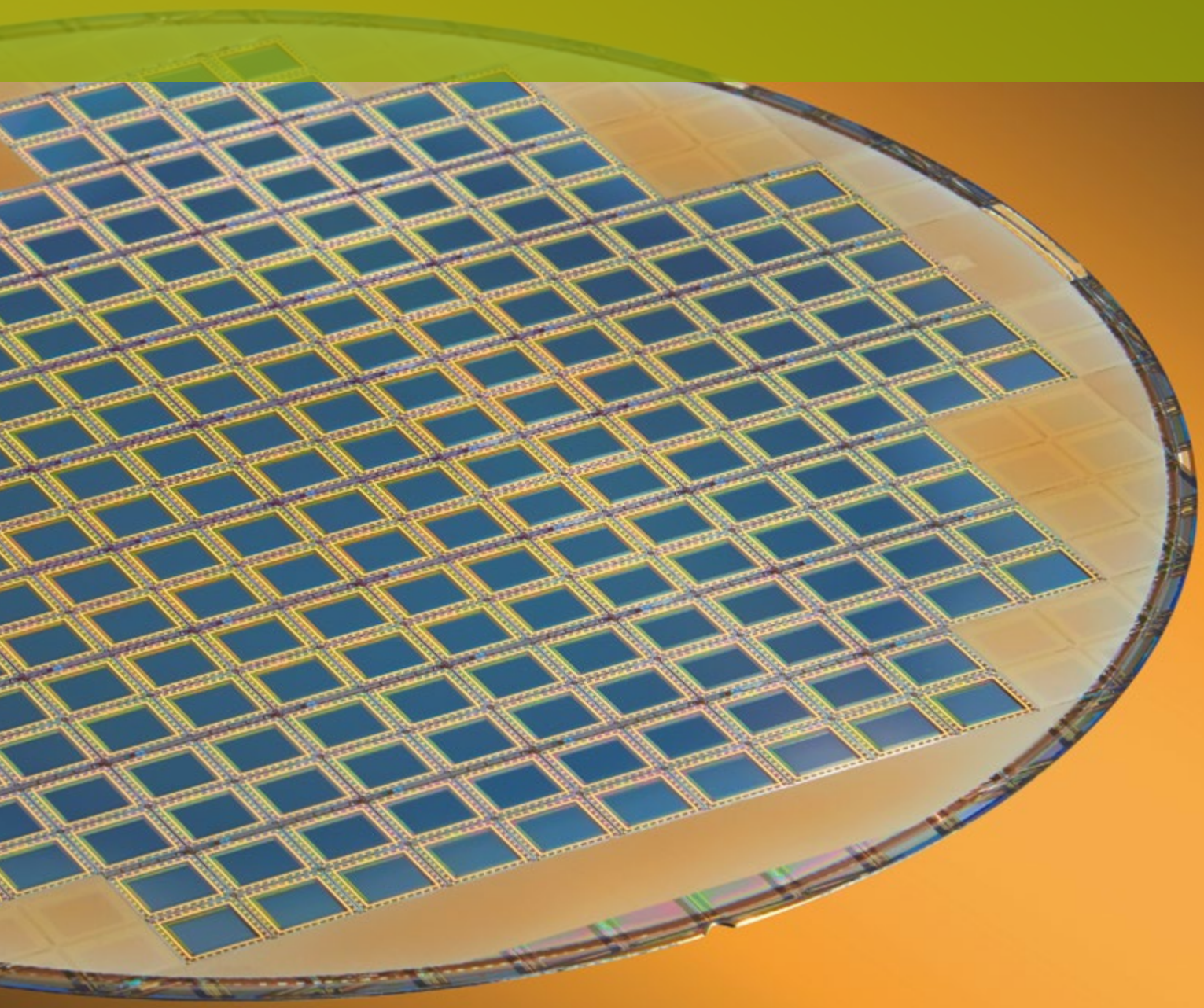


REPRESENTATIVE RESULTS OF WORK



Wafer with micro bolometer

MODULE INTEGRATION



DIGISTIFT: A SYSTEM APPROACH TO AN ENERGY-AUTONOMOUS SMART PEN

Under the lead of STABILO International GmbH, the BMBF funded project "DIGISTIFT" (FKZ 16SV6055) was launched in 2013, targeting the development of a digital pen that would allow writing on paper while transmitting the written content to a tablet PC in real time. Two basic use scenarios for school children were considered:

- In the preferred one, the handwriting would be reconstructed authentically on the display. This would enable a teacher to evaluate the learning progress of a child. It has to be noted that writing efficiency and motoric capability often cannot be judged directly from the graphical appearance of the characters.
- The "simpler" approach would translate written letters into a numeric representation by use of automatic character recognition, which is already a complex task in terms of pattern recognition and requires both a defined set of letter symbols and a limited dictionary for a plausibility check on the word level.

The goal of the BMBF research programme was to provide reliable energy-autonomous mobility to people: Human-Machine Interaction (HMI) and Energy Autonomous Systems (EAS) were thus the two challenges covered in this project.

Approach

Technically, the overall approach was to measure the 3D movement of the pen by using widely available commercial inertial sensors. A force sensor measures the pen tip contact to the paper. Data is transferred through a wireless interface to a tablet PC that allows interacting with some educational software.

After a first concept phase, it became evident that all targets could not reasonably be treated in a single demonstration approach. The primary project path followed by STABILO and other partners was building a pen with sufficient processing performance and memory for writing studies with school

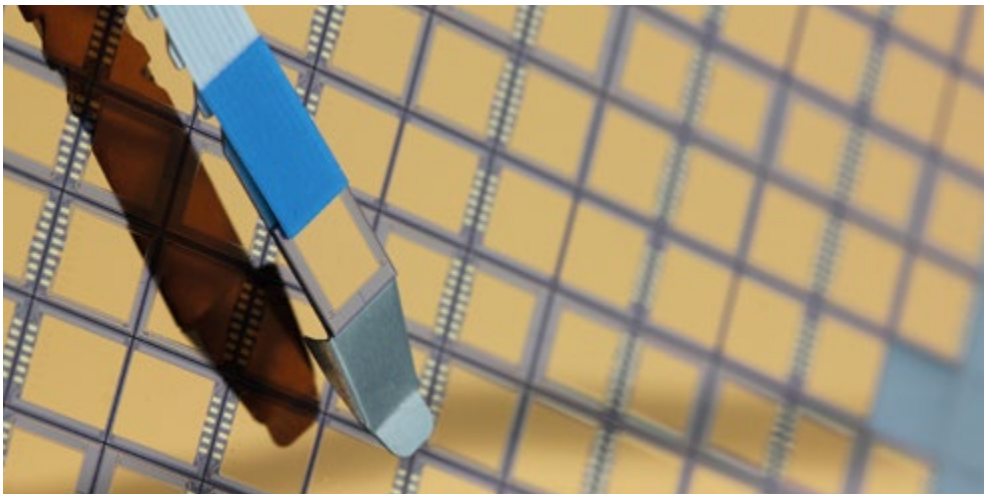


Figure 1:
Mounted on a metal cantilever, ISIT's DISTEL chip combines force measurement with piezoelectric energy harvesting

children, while ISIT focused on energy harvesting and energy-efficient system design.

Due to the complexity of the signal processing task, only a few elementary aspects were included in the project and STABILO performed separate work with third party developers that lead to a first public demonstration of a basic character recognition at the Consumer Electronics Show 2016 in Las Vegas.

Considerations for energy autonomy

Energy autonomy can only be achieved if enough energy is accessible in the surrounding of the system or in relation with its operation. Ambient light and the pen motion belong to the writing process itself and can thus be seen as reliable sources, while temperature gradients or electromagnetic radiation may not be available under all circumstances.

On the consumption side, only a rough estimation can be made since the intensity of writing activity is very different e.g. in basic and higher education schools. Based on a variety of hypothetic use cases, a power consumption of 340 µW in active writing mode was calculated as the acceptable maximum for energy autonomous operation of a pen. The assumptions used for this simulation were a photovoltaic generation of 130 µW from indoor lighting, a piezoelectric generation of 200 µW while writing, a power consumption of 200 µW in standby mode and 3 µW due to leakage currents while switched off. Time profiles were defined for all these operating conditions for a complete one-year cycle. Results from these basic considerations are the following:

- Leakage currents contribute significantly to the average power consumption; the designer should not rely on power-down modes offered by most processors or sensor ICs.
- Transition into standby mode should always be very fast, e.g. 100 ms after lifting the pen tip.
- In average, photovoltaic cells contribute at least 5 times more than piezoelectric harvesting.
- The use of solar cells necessitates a chemical energy storage, e.g. Li-ion accumulators with their low self-discharge.

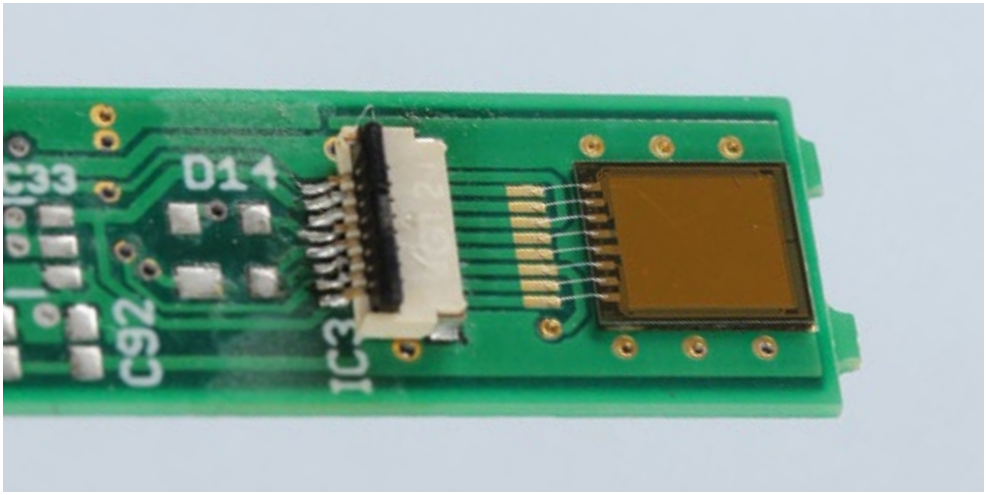


Figure 2:
DISTEL chip assembly on the DIGISTIFT test board

Implementation of a demonstrator

In the past 2 years, significant progress was made regarding power savings in microelectronic products. Current consumption has been reduced by approx. 50 % for micro controllers, Bluetooth Low-Energy (BTLE) transmitters and MEMS gyroscopes. A tiny new Li-ion cell has become available from Panasonic, offering a capacity of 13 mAh in an ideal pen-shape geometry of 3,5 mm diameter and 20 mm length. We selected some of the latest energy-efficient products and built a demonstration platform with the following features:

- Main controller: We use the CC2650 from TI, supporting Bluetooth Low-Energy and an autonomous sensor controller engine.
- Power management: The MAX17710 from Maxim is developed for µW scale energy harvesting, contains full Li-ion accumulator charging and protection and a selectable system supply output voltage.
- Inertial measurement units: Our first design comprises two options, the InvenSense MPU9250 and the more recent Bosch BMI160. With only 1 mA for gyroscope operation, the BMI160 consumes approx. 3 times less than competitor products.

This platform is very versatile for many applications like wearables or other IoT-systems. For our pen application, we developed and manufactured a dedicated chip that combines force measurement and piezoelectric energy harvesting.

The "DISTEL" chip

The DISTEL chip was developed explicitly for the DIGISTIFT project. Three of these chips will form a force direction sensing element mounted in the front part of our pen, and an additional Aluminium nitride layer is able to actively generate a wake-up signal to initialize the system as soon as the pen tip touches the paper. The force sensor is a strain gauge formed by four 10 kOhm Platinum resistors in a compensated Wheatstone bridge arrangement that is read out after a 500x amplification. The chip was dimensioned to 5 x 6 mm² for maximizing the harvesting while still fitting into the pen housing. We measured a pulse of 5V with a simple touch actuation, which is sufficient as a wake-up signal. However, we cannot expect a significant energy gain at the usual writing frequency between 3 and 5 Hz, therefore the electronic circuit is just set up to measure the energy accumulation rather than using it as a power source.

Status and outlook

We developed a first prototype with electronics PCB and a 3D printed housing in the form of a slightly oversized pen. The system is powered by 3 amorphous Silicon solar cells that charge a 13 mAh Li accumulator. A specific software has not been developed yet, but basic functionality and data transfer was realized with TI's source code from the "SensorTag 2.0" application. Force sensor and power monitoring still need to be implemented. A bachelor thesis is running to bring electronics and mechanical integration into a smaller design based on rigid-flex technology.

It is already foreseeable that the energy budget will remain critical. Our assumption on using exclusively acceleration and force sensing will probably not hold; the functionality demonstrated by STABILO could only be realized by including gyroscope and/or magnetometer. Significant savings can be made by reducing the amount of wireless communications; one of the next targets should therefore be the development of a data compression to 3-5 communications per second. A further perspective is using the autonomous sensor controller engine of the CC2650, which will allow data acquisition while the main controller core is in sleep mode with only 50 µA current consumption.

Author: Norman Marenco

Figure 3: The 3 PCBs are folded to a triangular body that is inserted into the pen housing (artist's impression)

INFLUENCE OF FLUX MIXTURES ON THE RELIABILITY OF ELECTRONIC ASSEMBLIES AFTER REWORK

Introduction

A zero defect production is still not fully realized in manufacturing of electronic assemblies, despite all efforts. Necessary rework and repair are often performed with other fluxes than used in inline reflow or wave soldering processes. They can be mixed and react with each other. Especially, if the used flux doesn't reach soldering peak temperature or if excess flux amount remains on the assembly after soldering, a great danger of electrochemical migration (ECM) is given in particular under the influence of moisture.

A rework soldering process is a selective heating of the assembly in general. Only at the solder joint, the assembly must achieve the required solder joint temperature for solder joint formation. Adjacent areas on the assembly remain cold or only reach a maximum temperature notably below the soldering temperature. The introduced soldering heat may not be enough to consume the flux used in a rework process. Undefined, but often harmful residues may remain on the board.

Task

The effect of such flux mixtures on the board reliability has been systematically studied using different materials in inline assembly and rework. The project was funded in the frame of the industrial collaborative research (IGF) research project 17960N "Investigation of the influence of electrochemical migration (ECM) on the reliability of electronic assemblies after rework using lead-free solders and No-clean flux mixtures".

Understanding how a flux works

Depending on the composition, a flux has a defined process window in which the soldering must take place (Figure 1). There is a predetermined temperature time range in which the flux is active. Only above the lower activation temperature the flux unfolds its effect; if the upper active temperature is exceeded, decomposition of the flux begins. If the soldering process is too short, no activation takes place. If the soldering process takes too long, the active ingredients of the flux are consumed before surface wetting has taken place.

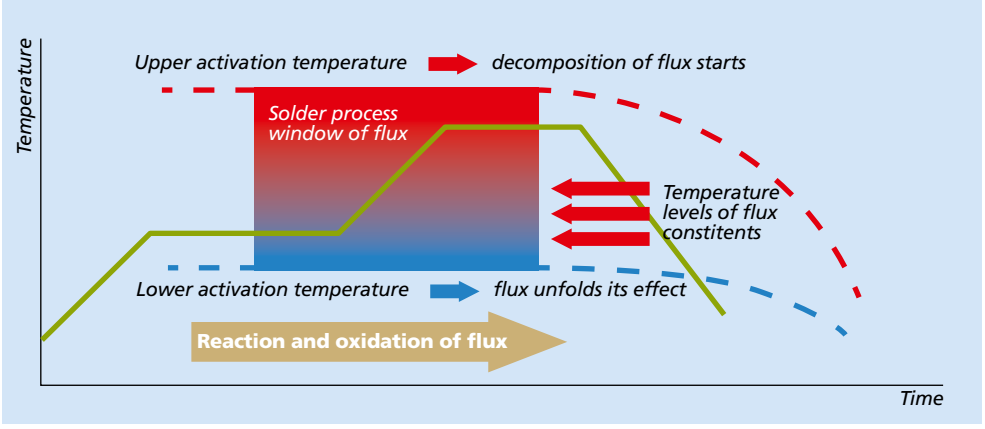


Figure 1: Solder process window of flux

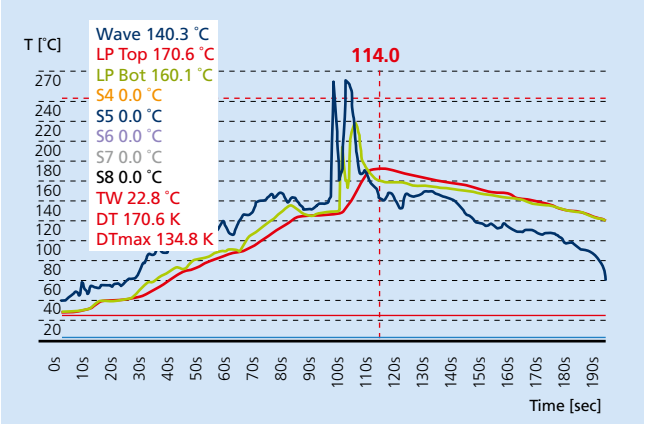


Figure 2: Typical wave soldering profile; max. temperature: PCB Bottom 216°C, PCB Top 171°C

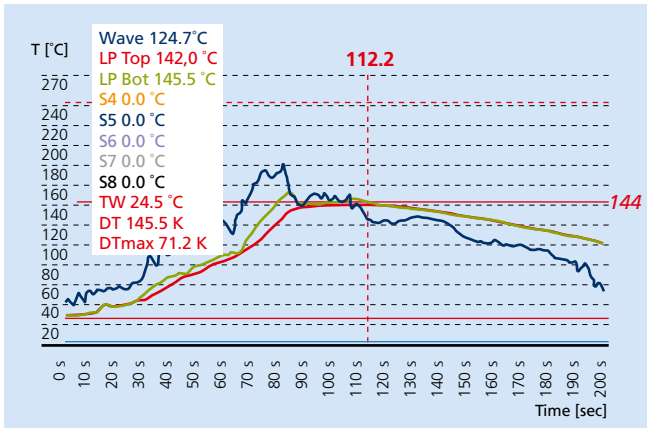


Figure 3: Incomplete wave soldering profile; max. temperature: PCB Bottom 153°C, PCB Top 142°C

Implementation

Using different No-clean flux types (L0, L1 and M1) for lead free application and No-clean SAC-solder pastes with flux type L0, a variation of processing parameters (e.g. time, temperature) was performed. The combination of inline reflow soldering with wave soldering, selective wave soldering, manual iron soldering and rework soldering was studied with Surface Insulation Resistance (SIR) test.

For inline convection soldering, the process profile setting was located in the center of the data sheet settings which corresponds to the typical application in assembling with a maximum soldering temperature of about 245 °C.

With the wave soldering two conditions were studied. First, the usual process, passing through the solder wave with a temperature-time curve as it corresponds to a typical SAC soldering process (Figure 2). The second wave soldering condition corresponds to flux which has flown on top of the board as it occurs possibly during flux application, spraying flux through a hole in the PCB. This flux has no further wave contact and will not be hotter than a maximum temperature of about 150°C (Figure 3).

For the selective wave soldering process, two preheating conditions were studied that represent typical preheating profiles, but also a setting that represents a higher heat transfer. This might happen when soldering large thermal masses by selective wave.

The heat transfer during manual iron soldering should be carried out by the wetted solder. This process can only be simulated with very limited reproducibility when building SIR-Test boards. Variations in the temperature profile were not realized. Instead, the manual iron soldering process was modeled with a rework station using a bonding tool. Temperatures in the range of 100°C to 250°C in 50-degree increments has been applied on the test boards.

During rework, the heat input has been carried out with a 40 x 40 mm² large hot gas nozzle. In order to examine the influence of flux residues that are not exposed to the working temperature, soldering profiles with maximum temperatures of 150°C, 215°C and 230°C have been applied.

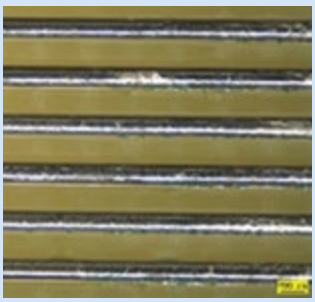
Evaluation and error condition

The SIR Test is a method to characterize fluxes by determining the degradation of electrical insulation resistance of rigid printed wiring board specimens in the presence of moisture. The test is carried out according to IPC J-STD-004 (Surface Insulation Resistance, Fluxes) on standardized comb test patterns according IPC-B-24 (Surface Insulation Resistance Test Board), where an individual comb structure has defined lines and spacing. The samples run through a soldering process as previously described. Experimental conditions are 85% relative humidity and 85°C temperature for 168 hours. A voltage of 100 V is applied to the comb structures and the resistance is measured in 20 minute intervals. Each comb pattern on each test PCB has been evaluated by the insulation resistance values during the climate testing. If the readings at the end of the measurement period are less than 100 megohm (1E8 ohm), the test is evaluated as fail. All specimens have been examined optically within 24 hours of completing the testing. Visible discoloration, corrosion or dendritic growth, which will constitute a failure, have been reported.

Results

The inline convection reflow soldering appears uncritical (for the examined solder pastes) regarding ECM, as shown in Figure 4. The combination of inline convection reflow soldering with nitrogen wave soldering appears uncritical for the investigated fluxes. If not fully implemented in the soldering process (low temperature, lack of wave contact, such as flux on the board top), wave solder fluxes show some corrosion potential (Figure 5) alone and in combination with solder pastes.

If inline convection reflow soldering is combined with selective wave soldering, the examined fluxes for selective wave soldering appear uncritical with respect to ECM, providing they have sufficient preheating. An examination of the residue by SIR test when used in critical (moisture) environment seems nevertheless useful because in individual cases the used process parameters (and flux) may differ from those which have been studied here.



SAC reflow profile

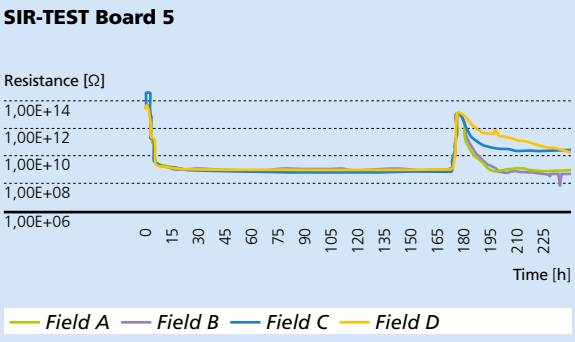


Figure 4:
Inline convection reflow soldering.
Left: Visual inspection of test board, right: SIR measurement

In manual iron soldering process, soldering flux appears to be critical when flux is only exposed to a temperature of 100°C or below. Using process temperatures between approx. 100°C and 250°C, fluxes are still potentially unsafe. Flux for manual soldering application requires a temperature of at least about 250°C to pass the SIR test.

When combining inline convection reflow soldering with a rework process, some fluxes appear critical or at least noticeable when a maximum temperature of less than 230°C is used. After qualified automatic cleaning, all fluxes in all the studied parameters and material variations passed the SIR test.

Summary

- Flux types with activation higher than L0 are critical and the danger of ECM rises.
- Flux mixtures can lead to electrochemical corrosion, especially when the flux does not completely decompose through the soldering process.
- Manual soldering processes are considered as potentially critical regarding ECM, especially again in case of incomplete flux decomposition in the primary soldering process (for example, flux splashes or flux excess that run in gaps).
- The amount of the applied flux should be reduced to the minimum necessary; spreading beyond the soldering area should be prevented.
- The prescribed soldering temperatures (material data sheet) for the process must be respected.
- An individual qualification by SIR test under defined conditions is recommended for use in critical environments. In order to achieve satisfactory results, the material combination should be assessed with realistic production process parameters such as the amount of flux, flux mixture, coating method and soldering profile.
- Qualified cleaning processes can minimize the risk for ECM on electronic components.

Das IGF-Vorhaben Nr. 17960N der Forschungsvereinigung Gesellschaft für Korrosionsschutz e.V. - GfKORR, Theodor-Heuss-Allee 25, 60486 Frankfurt/ Main, wurde über die AiF im Rahmen des Programms zur Förderung der industriellen Gemeinschaftsforschung und –entwicklung (IGF) vom Bundesministerium für Wirtschaft und Energie aufgrund eines Beschlusses des Deutschen Bundestages gefördert.

Author: Helge Schimanski

Visible dendrites

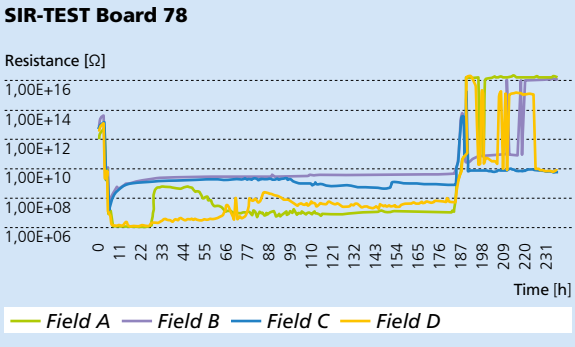


Figure 5:
Inline convection reflow soldering combined with incomplete wave soldering. Left: Visual inspection of test board, right: SIR measurement

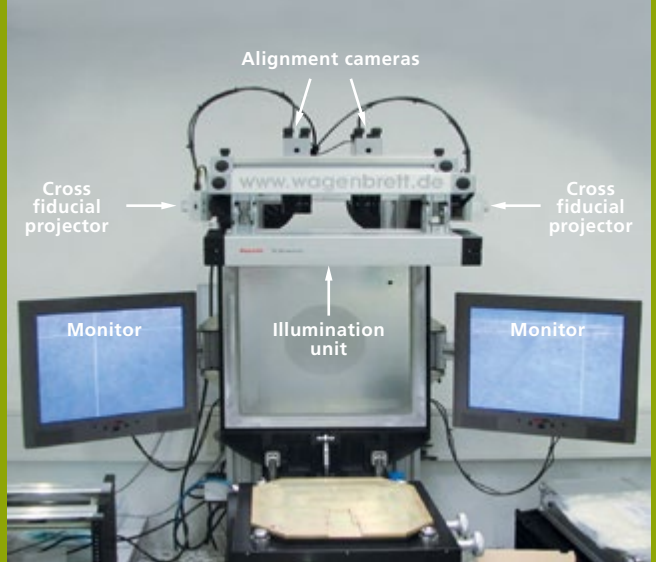


Figure 1: Wafer solder balling machine Wagenbrett WB300

WAFER BALL ATTACH ON TAIKO WAFERS

The TAIKO wafer grinding concept developed by the japanese company DISCO enables the cost effective manufacturing of ultra-thin electronic devices in Europe. The Japanese word "taiko" means "drum": A TAIKO wafer is characterized by a central wafer thinning down to 30 µm. Only a 2-4 mm wide border is maintained that works like a stiffening frame.

Although ISIT had some first experience on TAIKO wafer handling, the customer demand challenged our capabilities in two aspects:

- electroless NiAu plating to obtain solder pads on 50 µm thin fully CMOS processed TAIKO wafers without carrier,
- precise placement and reflow soldering of more than 150.000 solder balls per wafer.

ISIT demonstrated the processing feasibility with ultra-thin short flow CMOS product wafers based on our in-house electroless NiAu deposition line. A slightly modified Wagenbrett WB300 was used for solder balling by gravity feeding (figure 1).

The wafer balling process is based on a first stencil-printed tacky flux deposit that covers the solder pads on the wafer. A second stencil is used to place the solder balls on the flux deposits (figure 2). The process is simple and effective: Millions of balls are manually poured onto the stencil such that each hole contains a single ball. The excess quantity is collected for reuse by inclining the unit of wafer and stencil. An inspection step qualifies the wafers either for solder reflow or for a rework step. The solder reflow is then performed under nitrogen atmosphere in an advanced SMD reflow oven. Wafer carriers are used multiple times to allow safe handling and conveyance through the oven. The process flow for solder-balled TAIKO wafers ends with a wet cleaning procedure to remove flux residues, final inspection and transport packing in coin stack containers.

Our basic solder balling process is qualified with 250 µm solder ball diameter. An excellent uniformity regarding the solder ball

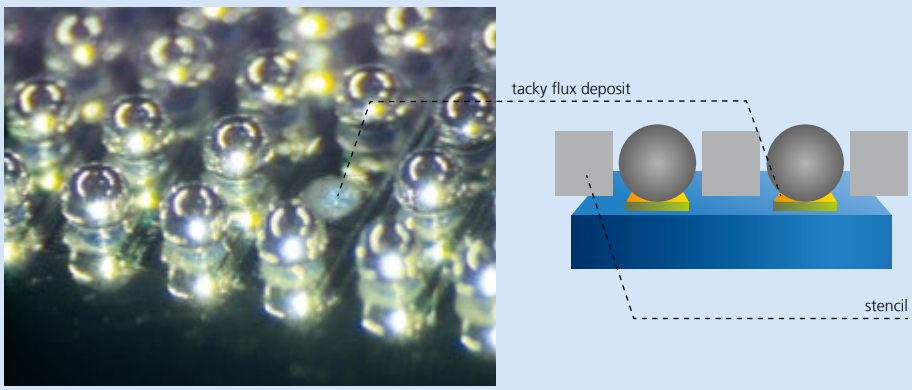


Figure 2: Solder spheres are placed on a wafer via a balling stencil and held in place by tacky flux deposits

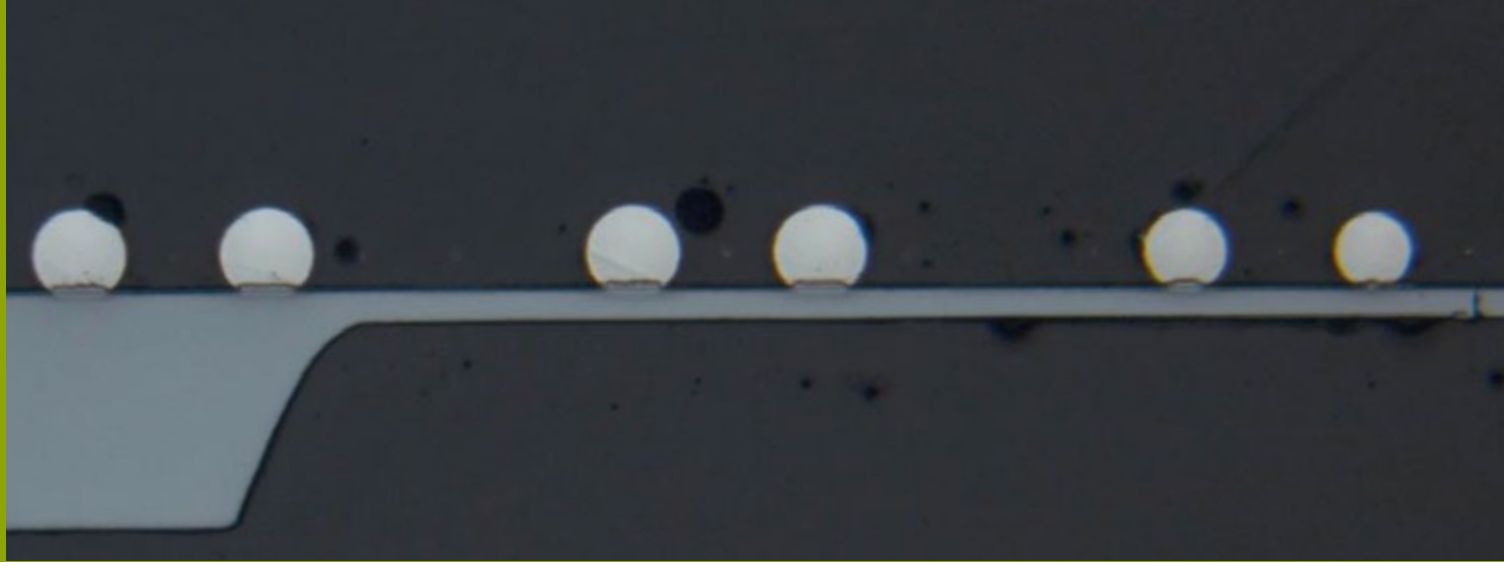


Figure 4: Solder balls applied to 50 µm thin TAIKO wafer. The image shows the thick silicon frame at the wafer periphery

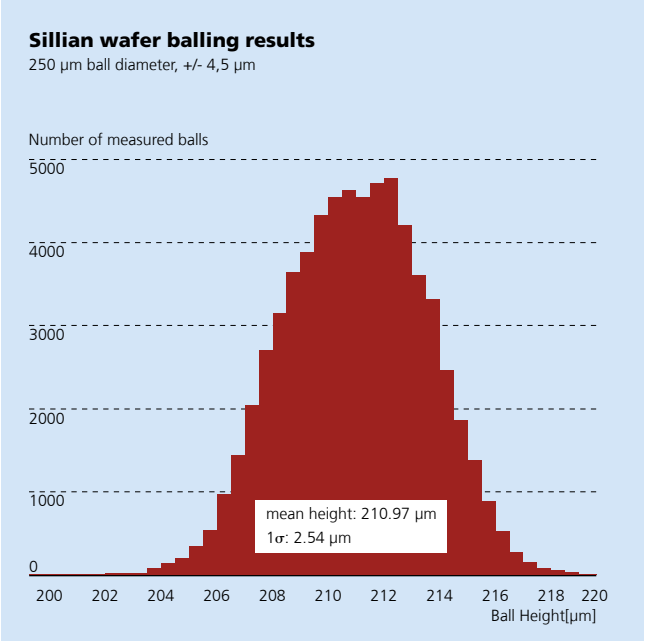


Figure 3. Ball size distribution after reflow using 250 µm balls with 4,5 µm tolerance (3 sigma) on 146 µm UBM pads

height distribution is achieved after reflow, as shown in Figure 3. However, to understand the process limits, a couple of ISIT test wafers (CSP1200-220) were processed at DISCO HI-TEC EUROPE GmbH as TAIKO wafers with thicknesses down to 30 µm. Our test wafers provide 16.768 test chips with daisy chain pattern, leading to a total quantity of 419.200 solder pads per wafer in a 220 µm pitch. The balling yield was found to be quite independent from the residual wafer thickness other than the wafer handling yield.

We can now state a process capability for solder ball pitches down to 220 µm and solder ball sizes ranging from 500 µm to 150 µm. The balling yield with SnAgCu solder spheres is in the range of 99,9% with a minimum number of missing balls or "megaballs" (two neighbouring solder spheres that have flown together). These findings indicate a wide pitch range to cover different requirements in wafer level CSP manufacturing. The process is highly parallel and offers an excellent yield. With some operator training, a wafer handling yield of 99% down to 50 µm wafer thickness (figure 4) is realized and suitable for a pilot production.

Author: Dr. Wolfgang Reinert

Lithium polymer cell with
integrated reference electrode

INTEGRATED POWER SYSTEMS

Projekt: „Temperaturoptimierte Batteriemodule mit instrumentierten Zellen", TopBat
Zuwendungsgeber: BMBF
Laufzeit: 01.05.2013 bis 30.04.2016
Projektpartner: Adam Opel AG, SGL Carbon GmbH
Beteiligte Institute: ISIT, ITWM

BATTERY CELLS WITH INTERNAL REFERENCE ELECTRODES INTRODUCTION

Knowledge of the actual potential of electrodes is desirable for enhancing the safety of Li-ion-batteries. In a 2-electrode system, where only the voltage difference between the anode and the cathode is known, one of the electrode potentials could still be beyond its safety limitation. In this case, a normal voltage difference between the electrodes masks the breach of the safe potential limit of one electrode, as shown in figure 1.

In a system with a reference electrode, the electrode potentials can be monitored directly and the battery management system is able to stop the operation of the battery. By this, common problems of Lithium ion batteries, like Lithium dendrite formation or the onset of oxidation processes on the cathode, can be avoided. Further benefits are:

- longer battery life,
- enhanced energy and/or power density,
- fast charging,
- operation at lower temperatures.

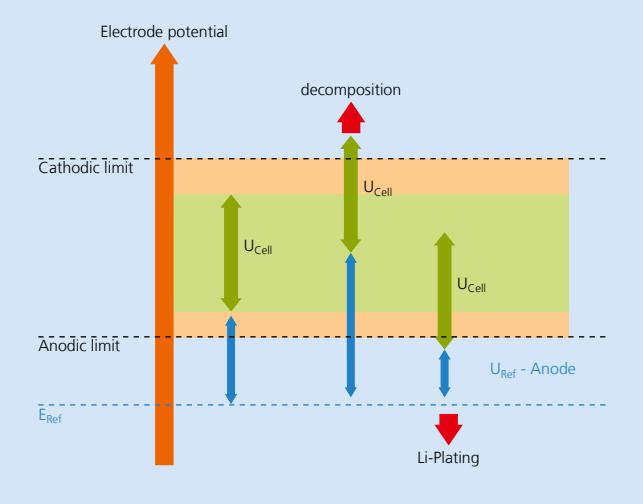


Figure 1: Schematic view of the potential ranges in an electrochemical cell. When the potential of both electrodes is shifted, the potential limits could be exceeded although the cell voltage is inconspicuous

Situation before the project

Despite this, Lithium ion batteries equipped with thermocouples and/or additional reference electrodes are barely described in the literature and even less purchasable. Lithium metal is very common as reference electrode in scientific experiments but not utilizable for commercial cells.

For determining the electrode potentials of the cell independently, the reference electrode has to have a defined stable electrochemical potential, a negligible voltage drift, chemical inertness within the Lithium ion technology and no ageing effects. Furthermore - as a manufacturer's requirement – it has to be compatible to the cell production processes. Materials like $Li_4Ti_5O_{12}$ (LTO) or $LiFePO_4$ (LFP) with a broad two phase equilibrium provide a very stable potential plateau and also meet the requirements mentioned above. These materials can be used as a reference electrode in lithium ion cells, particularly in customized cells.

Methods and Results

The test cells (NMC / Graphite) were produced by ISIT's lamination technology in a bi-cell setup (5,6 x 3,1 cm²), with an internal LTO reference electrode (0,8 x 1,4 cm²) located at the cell bottom between the separators in a sufficient distance from the cell stack. This design was confirmed by computer simulation done by the project partner ITWM.

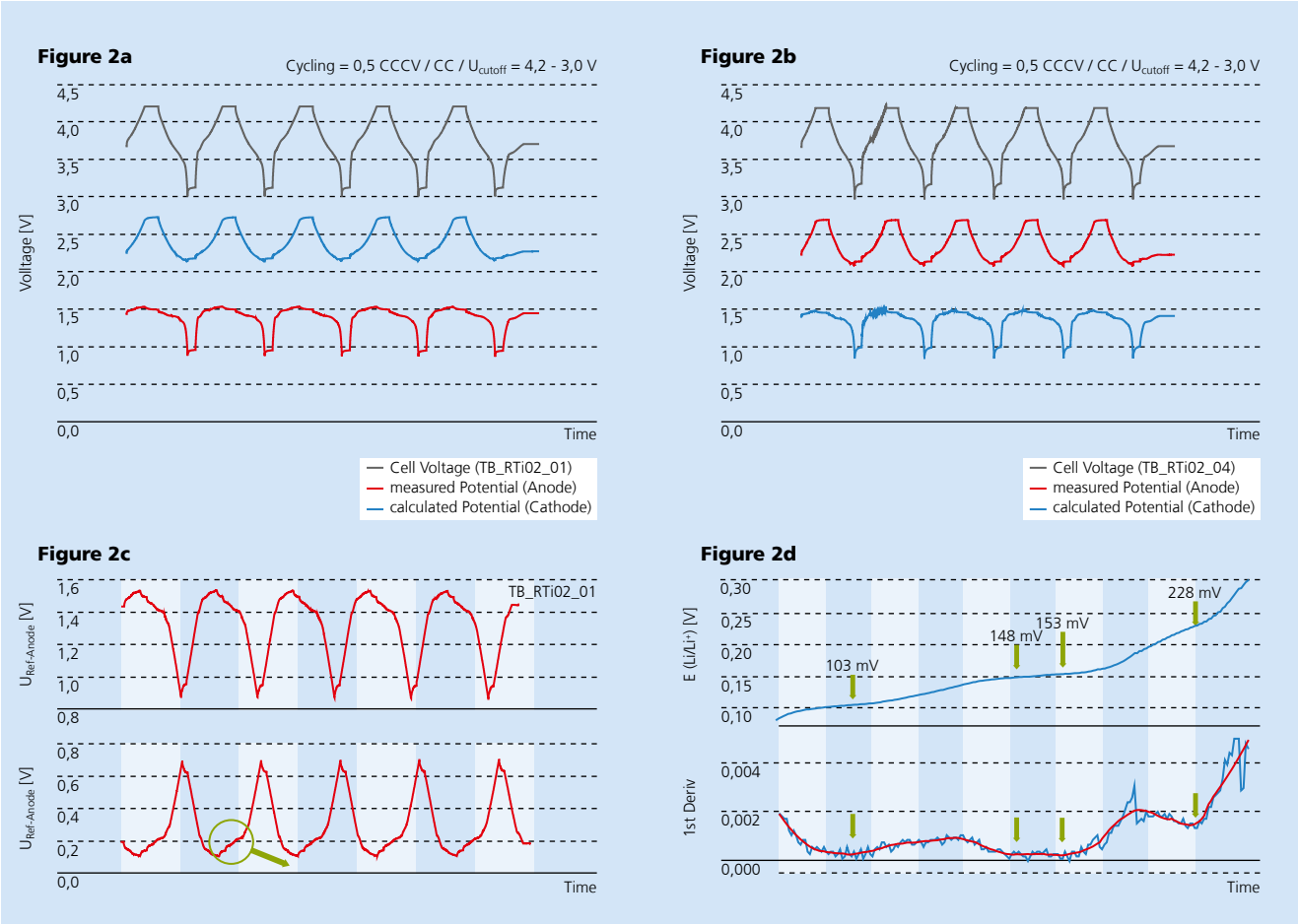


Figure 2: Results of the characterization of a NMC/Graphite cell with an internal reference electrode (LTO)

Figure 2a: Voltage profile of the cell, anode potential monitored against the reference potential

Figure 2b: Voltage profile of the cell, cathode potential monitored against the reference potential

Figure 2c: Recalculated anode (Graphite) potential to a potential against Li/Li+

Figure 2d: Magnification of the green framed part of the potential curve in Figure 2c and its first derivation

The cells were formatted by a usual procedure, then the reference electrodes were charged to a medium state of charge (SOC) of LTO versus the cathode to ensure a constant reference potential.

Afterwards, the cells were cycled at 0,5 C between 4,2 to 3,0 V while the reference voltage was monitored versus the Graphite anode as well as versus the NMC cathode. The corresponding counter electrode voltage was calculated by

$$\mathbf{U_{cell} = U_{C\text{-}Ref} + U_{A\text{-}Ref}}$$

The measurements (figures 2a, 2b) show a highly reproducible voltage profile and the observed voltage ranges (NMC vs. LTO = 2,8 – 1,8 V, LTO vs. Graphite = 1,5 – 0,9 V) correspond to the theoretical values. In addition, the Graphite electrode voltage profile looks similar to the well-known formation stage during Lithium intercalation into Graphite. To confirm this, the Graphite reference voltage profile (vs. LTO) was recalculated to a potential profile against Li/Li^+ (figure 2c; detail magnification of the discharge domain in figure 2d, top and its first derivation in figure 2d, bottom). The minima (figure 2d, arrows) indicate the Lithium stage plateaus and correspond very well with literature values.

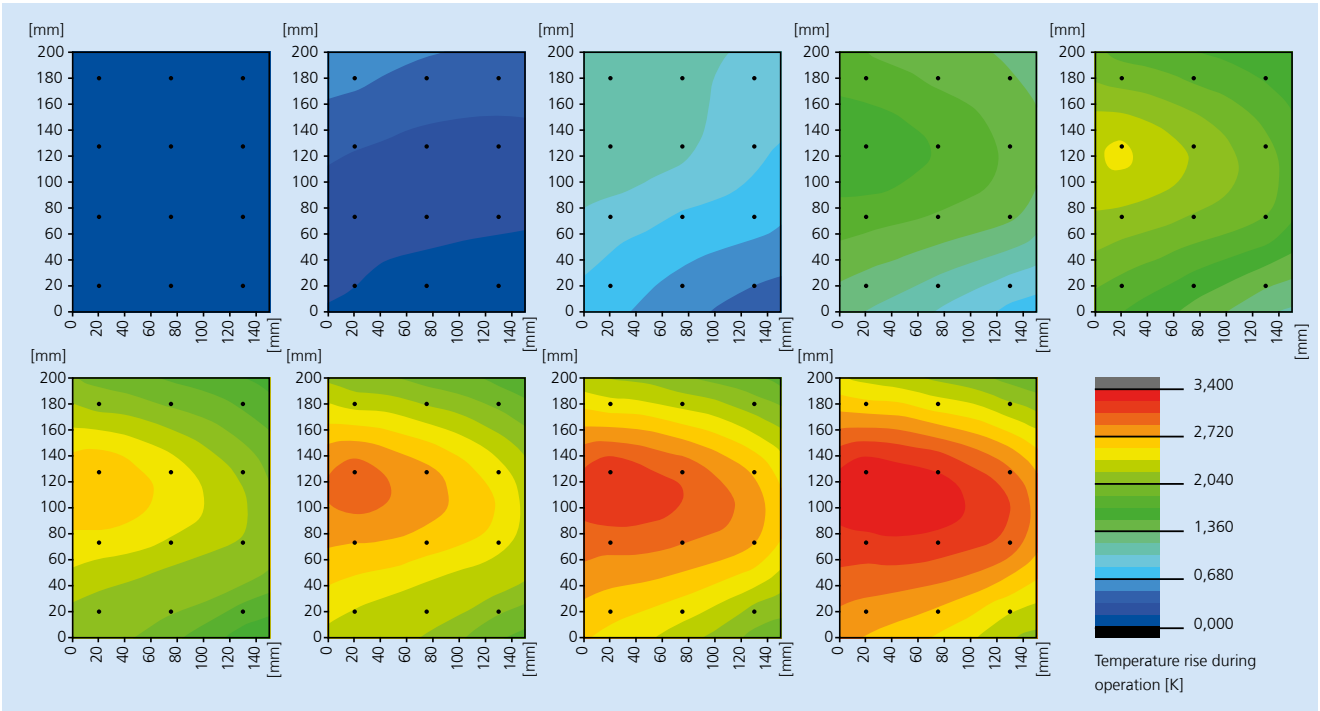


Figure 3: Evolution of the temperature distribution in a rectangular pouch-cell (151 x 200 mm²) during the 2C charge operation, measured with temperature sensors inside the cell. The different graphs show temperatures at SOC = 0%, 15%, 30%, 45%, 60%, 70%, 80%, 90%, 100%

Conclusion

An integrated LTO reference electrode allows an independent and reliable determination of the real anodic as well the cathodic electrode potential. This ensures to avoid undesirable and often safety relevant cell conditions (e.g. Lithium plating). The presented reference electrode is built from typical LIB materials via common coating technology. Hence, the production of LIB cells equipped with reference electrodes within today's well-established production process is possible and allows a rapid commercialization.

Internal temperature measurement

The local temperature inside Lithium ion batteries is also a valuable input parameter for the battery management system to minimize cell ageing and to avoid a safety relevant increase of the cell temperature. As part of the TopBat project, commercially available temperature sensors were tested for their suitability for temperature monitoring inside laminated Lithium-ion batteries. Central criterions were small size, high accuracy and simple installation into the batteries with low failure rate of batteries and sensors. Two types of sensors proved to be suitable, allowing an easy installation at low failure rates (no failures occurred), each with advantages and disadvantages:

1. NTC-thermistor
(Measurement Specialties Micro-BetaCHIP 10K3MCD1)
- acceptable spatial dimensions (cylindrical body Ø 0,5 mm x 3,2 mm)
- high accuracy of ±0,42 K with a high accuracy resistance meter

2. Miniature thermocouple (TC Direct Miniature Thermocouple)
- very small dimensions (Ø 0,25 mm)
- metal sheath may lead to internal shorts (did not occur)
- low accuracy of ±2,0 K with an appropriate temperature transmitter

The NTC-thermistors were selected for installing in different battery cells. This instrumentation of battery cells allows not only the determination of the temperature inside the cells, but also – by installing more sensors inside the cells – the measurement of the temperature distribution at different charging/discharging modes. The temperature distribution in vertical direction, for instance, could be determined by integrating 3 sensors at different places:
- between the bicells ("inside stack")
- between a bicell and the pouch bag ("outside stack")
- on the surface of the battery ("surface")

The lateral temperature evolution during a charge operation with 2C in a cell with dimensions of typical automotive applications is pictured in figure 3. The information was obtained by installing temperature sensors in identical cells at different places (3 sensors per cell).

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Waferlevel Packaging
Fraunhofer
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IMPORTANT NAMES, DATA, EVENTS

LECTURING ASSIGNMENTS AT UNIVERSITIES

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H. Kapels
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O. Schwarzelbach
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B. Wagner
Lehrstuhl Prozesse und Materialien der Nanosystemtechnik, Micro- and Nanosystem Technology, Technische Fakultät, Christian-Albrechts-Universität zu Kiel

MEMBERSHIPS IN COORDINATION BOARDS AND COMMITTEES

W. Benecke
Member of programming committees of:
- IEDM (International Electron Devices Meeting)
- EUROSENSORS
- ESSDERC (European Solid-State Device Conference)
- ESSCIRC (European Solid-State Circuits Conference)
- MST Kongress

W. Benecke
Member of Editorial Boards
- 'Sensors & Acutuators'
- Microsystem Technologies (MST)

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Member of GMM/GI-Fachausschuss EM „Entwurf von Mikrosystemen", VDE / VDI-Gesellschaft für Mikroelektronik, Mikro- und Feinwerktechnik

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D. Kähler
Nanotechnik S-H

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T. Knieling
Technologienetzwerk Körpernahe Systemtechnik (Body Tec)

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Member of Organic and Printed Electronics North (OPEN)

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Member of Verband der Elektrotechnik Elektronik Informationstechnik e.V. (VDE)

T. Knieling
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W. Reinert
Member of FA 10 AVT + Löten

W. Reinert
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W. Reinert
Member of ZVEI Arbeitskreis Packaging

W. Reinert
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K. Reiter
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K. Reiter
Member of Arbeitskreis Präparation

COOPERATION WITH INSTITUTES AND UNIVERSITIES

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Member of Metallographie Nord

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ZVEI Fachverband Arbeitsgruppe „Zuverlässigkeit von Leiterplatten“

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H. Schimanski
ED Arbeitskreis „Zukunftsweisende Baugruppenfertigung“

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G. Zwicker
Member of International Executive Committee of International Conference on Planarization/CMP Technology (ICPT)

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Universität Bremen

Technische Universität Braunschweig

Technische Universität Dresden, Institut für Aufbau- und Verbindungstechnik

Universität Duisburg-Essen

Fachhochschule Flensburg

Hochschule für Angewandte Wissenschaften, *Hamburg*

Helmut-Schmidt-Universität *Hamburg*

TU Hamburg Harburg

Fachhochschule Westküste, *Heide*

FH Kaiserslautern

Christian-Albrechts-Universität, Technische Fakultät, *Kiel*

Fachhochschule Kiel

Fachhochschule Lübeck

University of Naples Frederico II, *Naples, Italy*

Sydansk Universitet, *Sonderburg, Denmark*

Politecnico di Torino, Italy

Fachhochschule Wedel

University of Tohenburg, *Schweden*

Institute of Electron Technology, *Warsaw, Poland*

DISTINCTIONS

F. Stoppel, T. Knieling, B. Wagner
Outstanding Poster Award for: Novel piezoelectric ohmic switches featuring fast switching and high contract forces Transducers 2015, June 21–25, 2015, Anchorage, USA

TRADE FAIRS AND EXHIBITIONS

SPIE 2015
Photonics West Exhibition, February 10 - 12, 2015, San Francisco, USA

6th International Battery Expo 2015
Akkumulatoren als Zwischenspeicher für elektrische Energie, February 25 - 27, 2015, Tokyo, Japan

LOPEC 2015
International Conference and Exhibition for the Organic and Printed Electronics Industry, March 03 - 05, 2015, Munich

MIG – MEMS Executive Congress Europe 2015
New Technology in the Microelectronics, Piezo Drives for Actuators, Technology Transfer in the Production March 07 - 09, 2015, Copenhagen, Denmark

Kongress Elektromobilität 2015
Systematic Innovation, March 10 - 11, 2015, Berlin

Entwicklerforum Akkutechnologien 2015
Accumulator Technologies, March 24 - 26, 2015, Aschaffenburg

Kraftwerk Batterien 2015
Accumulators as an Intermediate Storage for Electrical Energy, April 27 - 29, 2015, Aachen

SMT 2015
Quality and Reliability in the Production of Electronic Modules, Damage analysis, Rework & Repair May 05 - 07, 2015, Nürnberg

PCIM 2015
International Exhibition & Conference, Power Conversion Intelligent Motion, May 19 - 21, 2015, Nürnberg

Hospitalar 2015
Point of Care Diagnostics, Protein Detection, May 19 - 22, 2015, Sao Paulo, Brasil

System Integration 2015
June 09 - 10, 2015, Oulu, Finland

Intersolar 2015
Energy Storage Systems with DC / DC Converter for Storing Solar Energy, June 10 - 12, 2015, Munich

Transducers *2015*
New Technology in Microsystems Technology, June 21 - 25, 2015, Anchorage, USA

Laser 2015
Micro-Actuators for Optical Applications, June 22 - 25, 2015, Munich

Nordjob Unterelbe
Westküste 2015 July 07 - 08, 2015, Elbmarschenhalle, Horst

WindEnergy 2015
International Trade Fair for Wind Industry, September 15 - 18, 2015, Husum

IAA 2015
FSEM, September 17 - 27, 2015, Frankfurt

AzubIZ 2015
September 18, 2015, Regionales Bildungszentrum Itzehoe, Itzehoe

Semicon 2015
October 06 - 08, 2015, Dresden

Battery + Storage 2015
Accumulators as an Intermediate Storage for Electrical Energy, October 12 - 14, 2015, Stuttgart

Mikrosystemtechnik Kongress 2015
MEMS, Mikroelektronik, Systeme, October 26 - 28, 2015, Karlsruhe

Nacht des Wissens 2015
November 07, 2015, Hamburg

Productronica 2015
Development and Manufacture of Electronic November 10 - 13, 2015, Munich

Compamed 2015
High Tech Solutions for Medical Technology International Trade Fair November 16 - 19, 2015, Düsseldorf

MISCELLANEOUS EVENTS

Die beherrschbare Baugruppenfertigung
Herstellungsqualität, Fehleranalyse und Prozessoptimierung
Seminar: February 24 - 26 and September 29–01 October, 2015, Fraunhofer ISIT, Itzehoe

ISIT Presentation in Framework of „Macht mit bei Mint – Zukunftsberufe für Frauen“
February 25, 2015, Fraunhofer ISIT, Itzehoe

Lotpastenapplikation
Technologien, Prozessoptimierung, Fehlervermeidung
Seminar: March 9 - 10, 2015, Fraunhofer ISIT, Itzehoe

Temperaturmesstechnik
Temperaturmessung richtig durchgeführt
Seminar: March 11, 2015, Fraunhofer ISIT, Itzehoe

ISIT Presentation at 9. Deutsches BioSensor Symposium
March 11 - 13, 2015, München

Reflowprofiloptimierung
Vom Wärmefluss in der Lötanlage zum optimierten Lötprofil
Seminar: March 12, 2015, Fraunhofer ISIT, Itzehoe

ISIT Presentation at POC-Biodetection Conference
March 17 - 18, 2015, Berlin

33. CMP Users Meeting and 4. Wet Users Meeting
April 16 - 17, 2015, Berlin

12. Hamburger Studententagung
April 28, 2015, Universität Hamburg, Hamburg

Wellenlöten und Selektivlöten
Technologien, Fehlervermeidung und Prozessoptimierung, Qualitätsbewertung
Seminar: April 29 - 30, 2015, Fraunhofer ISIT, Itzehoe

ISIT Presentation at Biomedizintechnik Konferenz BMT
September 16 - 18, 2015, Lübeck

Microtec Nord 2015
Energieeffiziente Elektronik
September 21, 2015, Fraunhofer ISIT, Itzehoe

ISIT Presentation at GeSiM-Anwenderseminar
September 29 - 30, 2015, Dresden

2. Norddeutsches Luftfahrtforum
Mikroelektronik im Flugzeug
September 30, 2015, Fraunhofer ISIT, Itzehoe

ISIT Presentation at Personalized Medicine Conference
October 07 - 08, 2015, Hannover

34. CMP Users Meeting and 5. Wet Users Meeting
October 29 - 30, 2015, Regensburg

ISIT Presentation at Fraunhofer-Tag Schleswig-Holstein
November 24, 2015, Lübeck

JOURNAL PAPERS, PUBLICATIONS AND CONTRIBUTIONS TO CONFERENCES

B. Benkendorff
Bottom up Research and Development for a Low Voltage Three Level NPC Converter.
PCIM Europe 2015, May 19 - 21, 2015, Nürnberg

N. Budhiman, B. Jensen, S. Chemnitz, B. Wagner
High Temperature Investigation on a Nickel–Tin Transient Liquid-Phaseafer Bonding up to 600 °C.
Springer Link, Microsystem Technologies, Online, December 12, 2015

N. Budhiman, B. Jensen, S. Chemnitz, B. Wagner, U. Schürmann, L. Kienle
Transmission Electron Microscopy Study for Investigating High-Temperature Reliability of Ti10W90-Based and Ta-Based Diffusion Barriers up to 600°C
Phys. Status Solidi A, 1 - 8, Online, December 9, 2015

N.Budhiman, U. Schürmann, B. Jensen, S. Chemnitz, L. Kienle, B. Wagner
High Temperature Reliability of Ta-Based and TiW-Based Diffusion Barriers.
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S. Fichtner, T. Reimer, S. Chemnitz, F. Lofink, B. Wagner
Stress Controlled Pulsed Direct Current Co-Sputtered Al1–xScxN as Piezoelectric Phase for Micromechanical Sensor Applications.
APL Materials 3, 116102, 2015

P. Gulde
Maßgeschneiderte Lithium-Ionen-Akkumulatoren aus Itzehoe für anspruchsvolle Anwendungen.
InnoWATTion Magazin, pp. 10 - 11, February, 2015

S. Gu-Stoppel, H. J. Quenzer, W. Benecke
Design, Fabrication and Characterization of Piezoelectrically Actuated Gimbal-Mounted 2D Micromirrors.
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S. Gu-Stoppel, H. J. Quenzer, W. Benecke
Design, Fabrikation und Charakterisierung piezoelektrisch angetriebener 2D-Mikrospiegel für Rasterscanner.
Mikrosystemtechnik 2015

V. Hrkac, A. Kobler, S. Marauska, A. Petraru, U. Schürmann, V. S. K. Chakravadhanula, V. Duppel, H. Kohlstedt, B. Wagner, B. V. Lotsch, C. Kübel, L. Kienle
Structural Study of Growth, Orientation and Defects Characteristics in the Functional Microelectromechanical System Material Aluminium Nitride, J. Appl. Phys. 117, 014301, 2015

S. Jahns, M. Bräu, B. Meyer, T. Karrock, S. B. Gutekunst, L. Blohm, C. Selbhuber-Unkel, R. Buhmann, V. Nazirizadeh, M. Gerken
Handheld Imaging Photonic Crysteal Biosensor for Multiplexed, Label-Free Protein Detection. Biomed. Opt. Express 6, pp. 3724 - 3726, 2015

D. Kaden, H.-J. Quenzer, B. Wagner, D. Koessler, J. Sichelschmidt, A. Jakob, T. Jung, F. Tiefensee
Herstellung und Integration piezoelektrischer Pb(ZrxTi1-x) O3-Schichten außerordentlicher Schichtdicke für die Erschließung neuer Anwendungsgebiete.
MikroSystemTechnik-Kongress 2015, pp. 322 - 325, October 26 - 28, 2015, Karlsruhe

D. Kähler, W. Reinert, A. Schumacher, U. Gaiß, S. Knappmann, G. Dietrich, S. Braun, E. Pflug, F. Roscher, K. Vogel, S. Hertel
Assembly and Packaging of Micro Systems by using Reactive Bonding Processes.
EMPC-2015, September 14 - 16, 2015, Friedrichshafen

T. Knieling, A. Kurylo, V.S. Sethu-Madhavan, H.-G. Bremes, M. Colsman, B. Schillo, H. Struchhholz, N. Schaffert, I. Goetze, K. Mattes, K.-M. Stephan
Akustische Gang-und Laufanalyse für Sport- und Medizinanwendungen.
8. AAL-Kongress, April 29 - 30, 2015, Frankfurt

T. Knieling, N. Schaffert, I. Goetze, K. Mattes, K.-M. Stephan
Entwicklung eines mobilen akustischen Gang- und Laufanalysesystems.
Konferenzband Hochschultag, 2015, Mainz

T. Knieling, A. Kurylo, F. Beeck, V.-S. Sethu-Madhavan
Verschiedene Kraftsensorprinzipien für flexible Schuheinlagen in der akustischen Ganganalyse.
Konferenzband Mikrosystemtechnik Kongress, 2015, Karlsruhe

T. Lisec, F.Stoppel, B. Wagner
A Novel Type of Small-Size Surface-Micromachined Ohmic Switches with Bidirectional Actuation.
MEMSWAVE 2015: 16th International Symposium on RF-MEMS and RF-MICROSYSTEMS, June, 2015, Barcelona, Spain

F. Lofink, D. Kähler, W. Reinert
Hermeticity Tests. Chapter 40, Handbook of Silicon Based MEMS Materials and Technologies
Elsevier, Second Ed., 2015

F. Lofink, I. Teliban, C. Kirchhoff, E. Quandt, B. Wagner
Highly Sensitive MEMS Magnetic Field Sensor Based on Magnetoelectric Composite.
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J. Paul, H. Knoll, A. Lenkl, R. Tide, M. Theis, M. Saumer, C. Vetter, A. Piorra, D. Meyners, F. Lofink, S. Fichtner, B. Wagner, K. Zoschke
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B. Benkendorff
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L. Blohm
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Sergej Broschko
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FH Westküste, February 2015

Natalia Burchardt
Evaluierung der DNA-Detektion auf Single-Electrode-Arrays in einem integrierten Biochip-Kartuschensystem
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Svenja Dittrich
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Robert Eggersglüß
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Ghandy Ghandy
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Pascal Sebastian Gliesche
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Martin Hanssen
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Jan Labahn
Untersuchung der Laseraktivierung von ionenimplantierten kollektorseitigen Schichten von Feldstopp IGBT's
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Björn Martens
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Henrik Pein
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Vithya Saahar Sethu-Madhavan
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Siri Shastri
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Florian Stern
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Philipp Timm
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Lena Viktoria Vollstedt
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DOCTORAL THESES

S. Gu-Stoppel
Entwicklung, Herstellung und Charakterisierung piezoelektrischer Mikrospiegel
Christian-Albrecht-Universität zu Kiel, January 2016

U. Hofmann
Entwicklung eines mikromechanischen Strahlablenksystems für Laser-Projektions-Displays
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D. Kaden
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OVERVIEW OF PROJECTS

- *Integration von GaN mit CMOS-Technologie*
- *Entwicklung von Fast Recovery Dioden*
- *Innovationscluster Leistungselektronik für regenerative Energieversorgung*
- *Entwicklung neuer Punch-Through-IGBTs und Field-Stop-IGBTs*
- *Advanced Metallization for PowerMOS*
- *CHOS Transfer*
- *Energy-Efficient Piezo-MEMS Tunable RF Front-End Antenna Systems for Mobile Devices (EPAMO)*
- *9 D Sense; Development of Magnetic Field Sensors*
- *High Volume Piezoelectric Thin Film Production Process for Microsystems, Piezo Volume*
- *Magnetoelektronische Sensoren*
- *Development and Fabrication of 256k CMOS Blanking Chips for Maskless Lithography*
- *Development of an ASIC for the control of BLDC-motors*
- *Herstellung eines Multi Deflection Arrays für die hochauflösende Elektronenstrahl-Lithographie*
- *Entwicklung einer Montageplattform für Lasermodule und passive Optiken (PICOLO)*
- *Entwicklung und Herstellung eines MEMS basierten hochgenauen CO_2-Sensors*
- *Silizium basierte Hochtemperatur-Thermogeneratoren auf 8" Wafer-Level (SIEGEN)*
- *Prozessentwicklung MEMS basierter Energie-Harverster*
- *3D-Signage*
- *Hochleistungsmikrospiegel für die Materialbearbeitung*
- *Waferbasierte 3D-Integration von IR Sensor Technologien (WIN-IT)*
- *Tiefziehen von Glaswafern (TIGLA)*
- *AOI Kalibririernormal*
- *Adaptive Lichtlenkung mit Mikrospiegel-Arrays*
- *2D MEMS-Scanning Mirror*
- *Mikro-Auge*
- *PZT Transducer für Ultraschall-Anwendungen*
- *Piezo Stromversorgung on chip*
- *AQUILA: Hochauflösende und hochkompakte energieautarke MR Positionssensorik für smarte Produktionsanlagen und Geräte*
- *SmartSpeaker*
- *Thermoelectric energy harvester*
- *Elektronischer Laktat Nachweis ELaN*
- *Zuverlässige Kontaktierung von Höchstleitungsbauelementen in der Leistungselektronik durch innovative Bändchen- und Litzenverbindungen (MAXIKON)*
- *Produktionsgerechtes reaktives Nanofügen zum hermetischen Versiegeln von Mikrosensoren auf Waferebene (REMTEC)*
- *Glassfritt Vacuum Wafer Bonding*
- *Wafer Level Packaging*
- *Process Development for Hermetic AuSn Vacuum Sealing of IR Sensors on Wafer Level*

- *Wafer Level Balling for 100 µm up to 500 µm Spheres*
- *Neon Ultra Fine Leak Test for Resonant Micro Sensors*
- *Hochzuverlässige Stromrichter für Windenergieanlagen (HiReS)*
- *Qualitätsbewertung an bleifreien Baugruppen*
- *Printed Electronics (Binäruhr, neuer Drucker LP50, Gedruckte Sensoren)*
- *Erhöhung der Lötsicherheit beim Einsatz mikro- und niedrig Ag-legierter Lote in der Fertigung elektronischer Baugruppen (IGF-Vorhaben 17941 N/1)*
- *Untersuchung des Einflusses der elektrochemischen Korrosion auf die Zuverlässigkeit von reparierten elektronischen Baugruppen unter Verwendung bleifreier Lote und No-Clean-Flussmittelmischungen (IGF-Vorhaben 17960 N/1)*
- *Akustische Gang- und Laufanalyse*
- *Digitaler Schreibstift für den Schulunterricht (BMBF-Projekt „DIGISTIFT")*
- *Aufbautechnik für AlGaN-Detektoren zur Emissionsüberwachung von UV-Strahlern (WISA-Projekt „AGNES")*
- *Großflächige Sensorik für die Analyse von Körperbewegungen (Moni Shirt)*
- *European Li-Ion Battery Manufacturing for Electric Vehicles (ELIBAMA)*
- *Hybride Stadtspeicher – Stationäre Energiespeicher für die dezentrale Energieversorgung*
- *Innovatives Elektrofahrrad-KonzeptVelocity*
- *Innovatives Funktionsmaterial für Speichertechnologien „Ormocere"*
- *Entwicklung von Produktionstechnologien für Lithiumakkumulatoren (Protrak)*
- *Entwicklung und Fertigung von Elektroden für Lithium-Schwefel Batterien (Eurolis)*
- *Entwicklung von Hochleistungsakkumulatoren für die Elektromobilität (FSEMII)*
- *Temperaturoptimierte Batterietechnologien TopBat*
- *Neue Konzepte für die Elektroden und Separatorfertigung bei Lithiumakkumulatoren (S-Protrak)*
- *Hellis Entwicklung einer Hochenergie Li-Schwefel-Batterie*
- *Optimus Optimiertes Energiemanagement in Fahrzeugen*
- *FSEM II*

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