JUNE 16, 1981

HAS THE BUBBLE-MEMORY BUBBLE BURST?/93

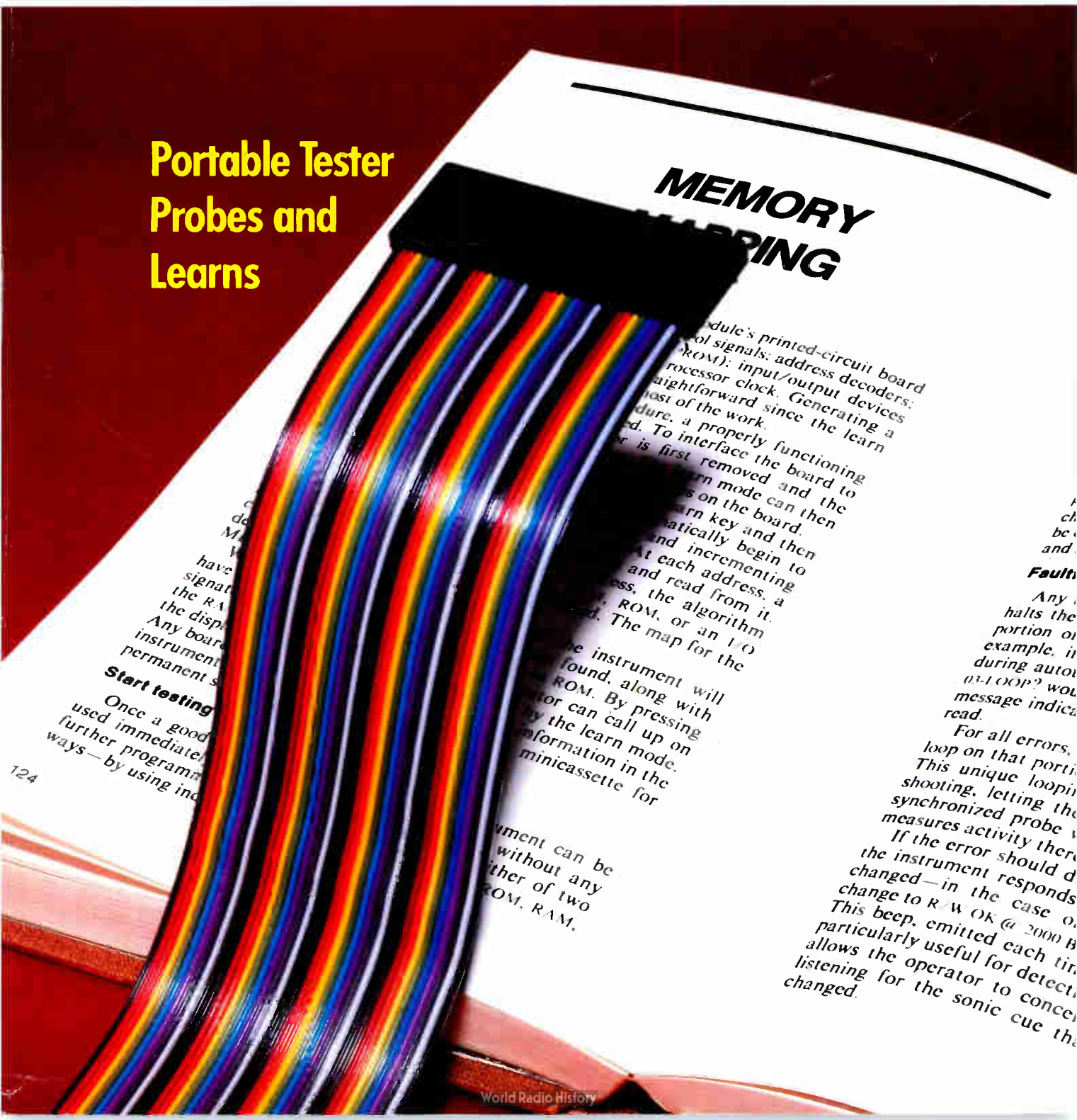
Collision-free local network scheme minimizes delays/176

16-bit C-MOS processor targets small business computer line/182

SIX DOLLARS A Mc GRAW-HILL PUBLICATION

Electronics

Portable Tester Probes and Learns



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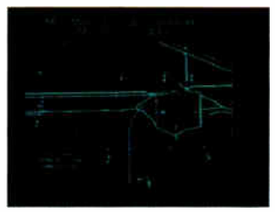

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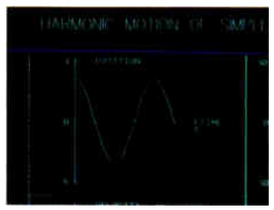

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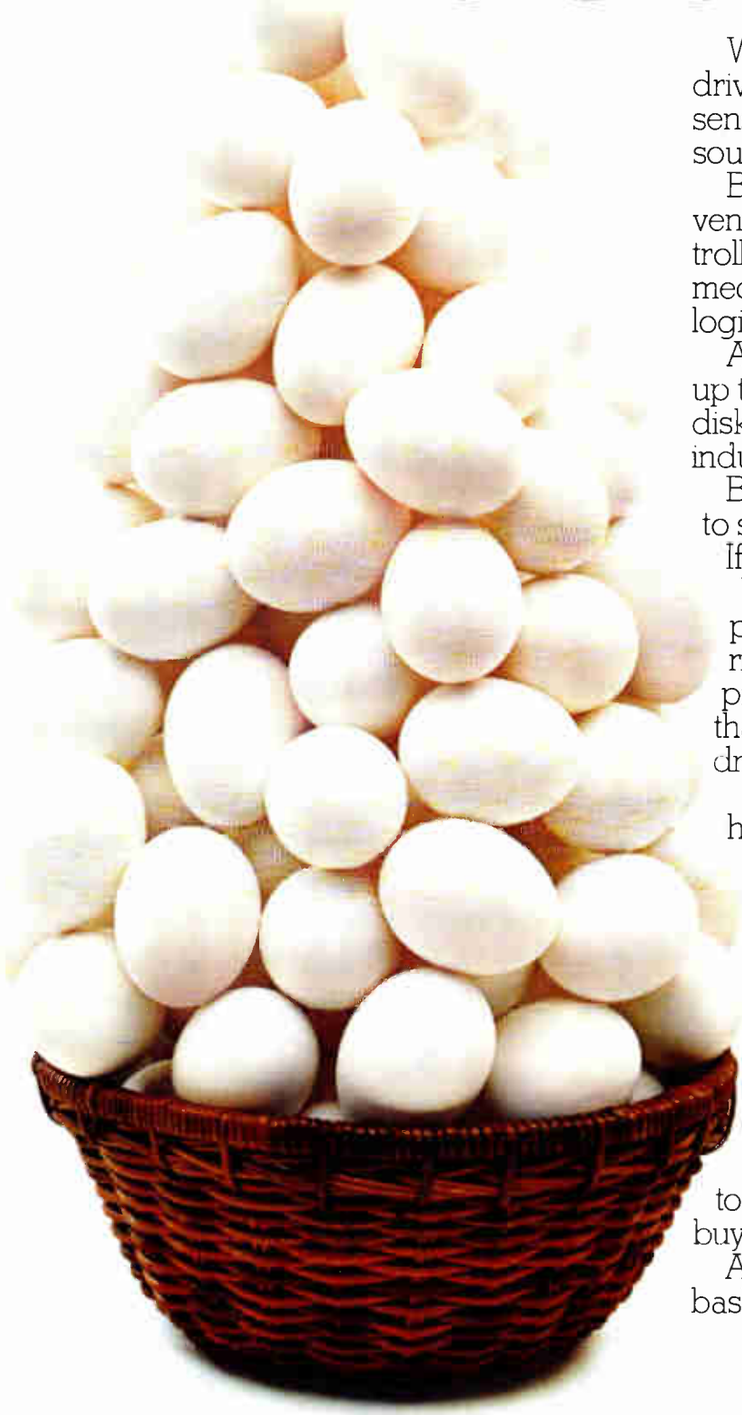

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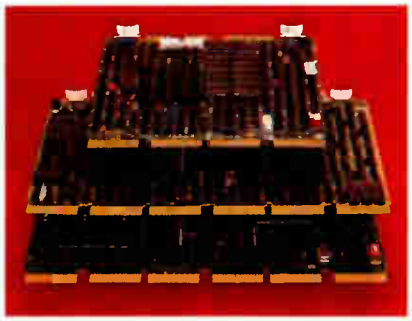

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*Trade name of Digital Equipment Corporation.

Electronics
The International Magazine of Electronic Technology
Vol. 54, No. 12 • June 16, 1981

Electronics

Highlights

Cover: Lightweight tester learns quickly, 153

A portable tester has come along to answer the need of the electronics industries for a troubleshooting tool capable of servicing microprocessor-based products. It is the first such instrument that can map the memory-address locations of a functioning product automatically and use that information to test a malfunctioning one.

The cover photograph is by Joe Ruskin.

Electronics companies remember the past, 96

Having been hurt by their layoff of technical staff in response to economic slowdown, electronics companies are now remembering the past so that they will not have to suffer similar consequences again. Specifically, facing soft markets, strong competition, soaring interest rates, and troubled national economies, many firms are reacting not by laying off employees but by reducing work schedules and closing plants temporarily.

Chip encrypts data on the fly, 161

A single-chip encrypts and decrypts data in conformance with the National Bureau of Standards' data-encryption standard (DES) at 14 megabits a second—fast enough to do the job while data is being read from or written onto disk. It operates under standard microprocessor or bit-slice control.

Local network schemes multiply, 171, 176

Local networks designed to link data-processing gear at a local site are getting a good deal of attention of late. The recently announced Cluster/One is aimed at the personal-computer level, in particular, the Apple II (p. 171). It uses flat cable with 16 wires to keep costs down. In another development, a new method of distributed control for such networks has been implemented for experimental purposes (p. 176). Having the data-processing terminals sound off in a fixed sequence, whether or not they have any message to send, keeps delays to a guaranteed minimum while preventing collisions.

16-bit processor wants small-business work, 182

A 16-bit microprocessor is crammed with hardware like error-detection circuitry, supports virtual memory, and divides its operations into four levels to make it highly suited for multiuser applications. It can emulate any existing processor through microprogramming.

And in the next issue . . .

What the Reagan military buildup means to electronics . . . a new linear process . . . a 64-K random-access memory design using epitaxy for noise immunity . . . designing a super-mainframe computer . . . a 16-bit processor with virtual memory hardware.

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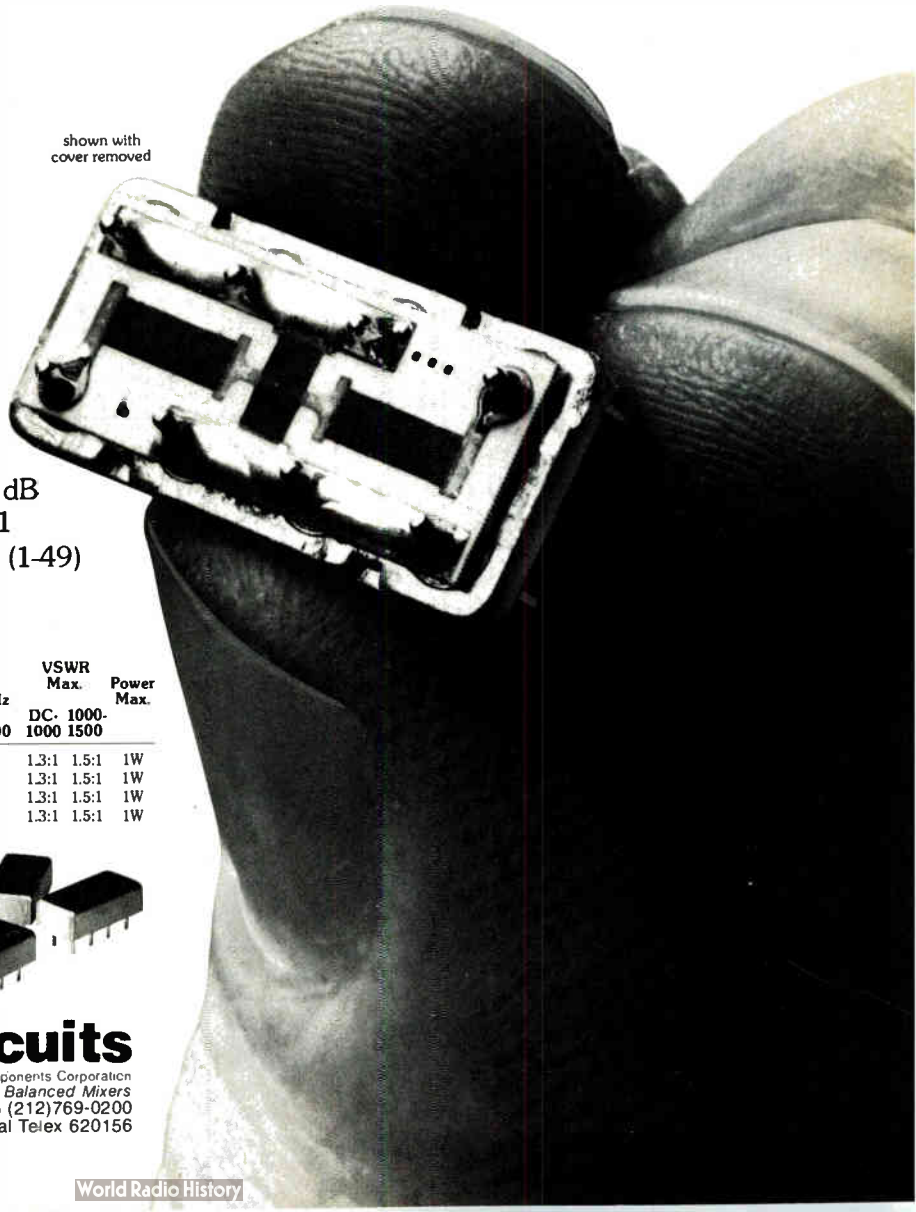

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AT-10	10	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1	1W
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67-2 REV. ORIG.

Publisher's letter

Our cover story this issue describes a major new fault-finding tool for microprocessor-based systems. Author of the article and product manager Don Cassas (below, working with the 9010A) explains that his firm, John Fluke Manufacturing Co., arrived at the project in a rather indirect way.

"In 1978, John Fluke wondered whether the company should be in the oscilloscope business. So we looked at the market to see if there was a need for a digital scope or something similar to service microprocessor-based systems," Cassas says. But "after a year of asking customers what tools they would need, we realized that a scope was not the answer," he says.

From the research, a pattern began to appear. "In most cases, the problems were on the bus," Cassas explains. "The microprocessor rarely failed, but RAM, ROM, and I/O often did." So Fluke set out to build a bus-oriented tester, a prototype of the 9010A. "We took it on the road for a year," Cassas adds, "to try out the concepts."

One concept that proved to be a winner, he says, was the learn mode. As the article beginning on page 153 describes, the 9010A Micro System Troubleshooter inspects the memory locations of the unit under test and studies the buses—in effect, it learns the operation of a functioning system and puts that information to use in fixing a faulty one.

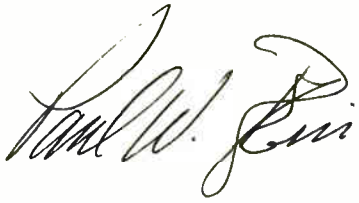
The advantage of this approach is that once a piece of equipment has been learned by the 9010A, a guided-probe–type test routine can be prepared by the manufacturer and stored on cassettes using the 9010A's built-in cassette drive. The unit then becomes suitable for field service, as a relatively unskilled technician can follow the test routine through prompts by the 9010A's display.

In fact, Cassas adds, future members in the 9000 family will include nonprogrammable models aimed specifically for field-service use. "The 9005A will be a stripped-down version that, for example, will be minus some programming keys but will accept cassette tapes programmed by the manufacturer on the 9010A," he explains.

The second entry in our newly formed Computer Notes section of the Engineer's Notebook (p. 189) applies to the newest breed of personal computer—the hand-held computer. Although it could be argued that all calculators are computers, we're distinguishing the latter from the former by merit of their high-level language—they are programmed in Basic.

The program solves the relatively simple but useful equations for coil-capacitor (LC) resonance. Submitted by Cass R. Lewart of System Development Corp. in Eatontown, N. J., it was spun off from an earlier routine for the HP-67 calculator.

We asked Lewart to compare the feel of the two machines: "The Radio Shack hand-held computer has almost twice the program capacity and gives you more flexibility when it comes to changing variables," he says. "The program for LC resonance took less than an hour to write, compared with several hours for the calculator." Lewart adds that the tiny computer has its limitations, "but its battery-backed memory keeps the program and data alive even when the unit is off, and that's a real plus."



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Circle 7 on reader service card 7

Readers' comments

Nothing new under the sun

To the Editor: Your Feb. 24 report on solar-cell developments at Bell Laboratories ["Liquid-junction cells move in on silicon," p. 46] discussed a technology that is far more than six years old. Robert Sabine published a short paper on the subject entitled "Action of Light on a Selenium (Galvanic) Element" more than a century ago that described a liquid-junction cell consisting of a platinum strip and a selenium plate immersed in water.

Incidentally, there is reason to believe Sabine's paper was read by Alexander Graham Bell while on his honeymoon in England. Soon after the paper appeared, Bell made plans to design his Photophone, the sunlight-based device that on Feb. 19, 1880, became the first mechanism for transmitting human speech over a beam of electromagnetic radiation by employing various kinds of selenium detectors.

As it is written in Ecclesiastes: ". . . there is no new thing under the sun. Is there any thing whereof it may be said, 'See, this is new?' It hath been already of old time, which was before us."

Forrest M. Mims III
San Marcos, Texas

Corrections

In "Thermal recorder makes its own grid" (May 19, p. 216), the name of the thermal strip-chart recorder made by Gulton Industries Inc. was incorrectly given. The printer is properly called the Supertrak 60.

In "Removable cartridges inch up on disks" (May 19, p. 106) the unit in the photo identified as the model 899 floppy-disk drive manufactured by PerSci Inc. of West Los Angeles, Calif., is actually the model 2000 tape-cartridge drive made by Pragma Data Systems Inc. of Sunnyvale, Calif.

Finally, in an Electronics Newsletter item (June 2, p. 33), Standard Microsystems Corp.'s process for lowering the sheet resistance of polysilicon interconnections in n-MOS circuits was described as incorporating tantalum disilicide ($TaSi_2$). The correct compound is titanium disilicide ($TiSi_2$).

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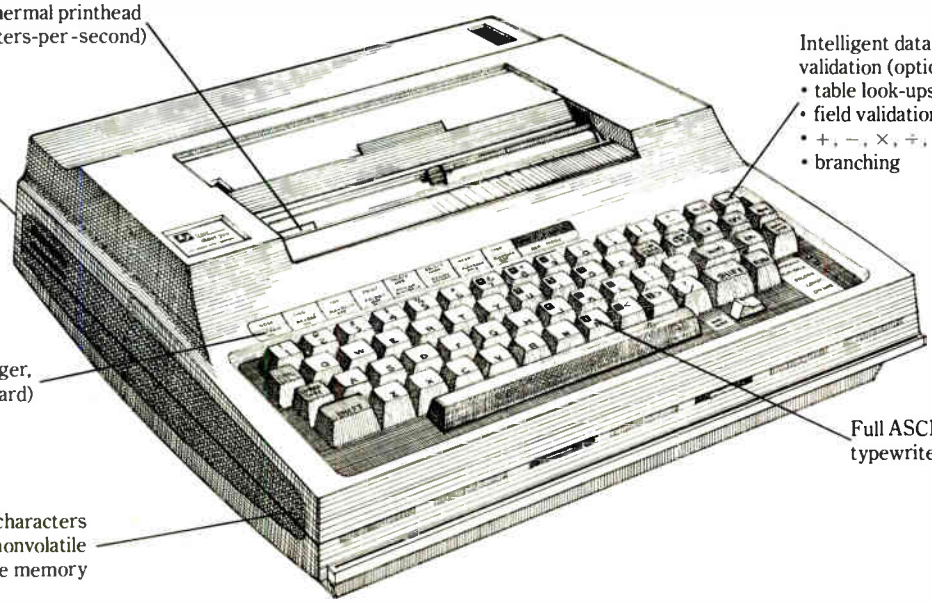

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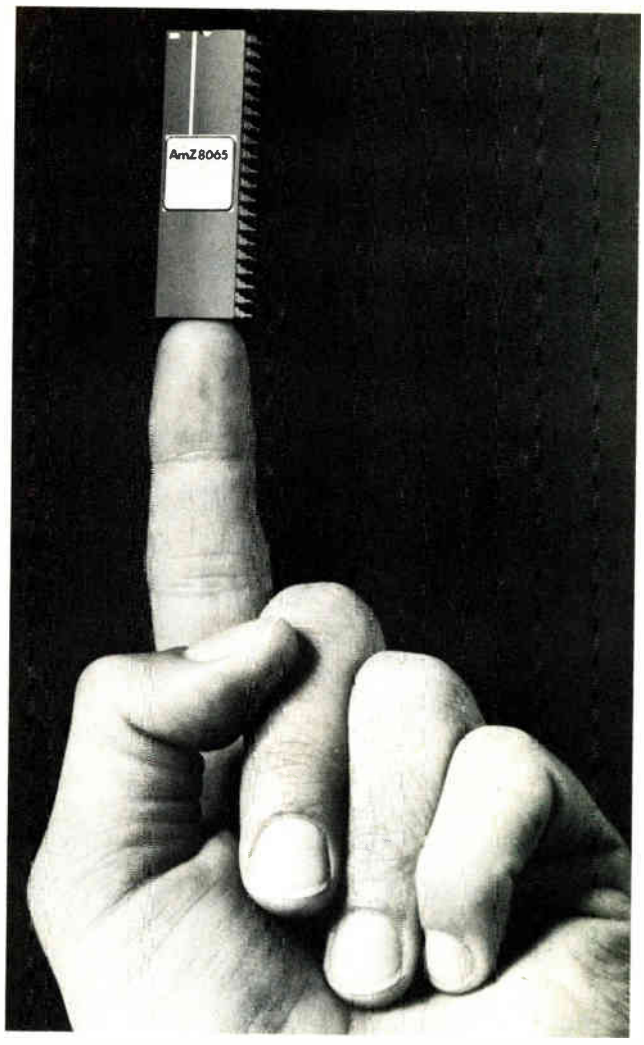

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News update

■ A mainframe computer is sometimes needed to develop programs for 16-bit microprocessors. That means the initial software from the mainframe must be compiled to retarget the program for the microprocessor instruction set.

For those who use Pascal and Intel Corp.'s 8086, Language Resources Inc. is offering retargeting software packages that will run on a Digital Equipment Corp. VAX system or on an IBM System 370 mainframe. The PAS-86 series from this Boulder, Colo., company is the first follow-on of the surprisingly successful Pascal language system packages that the fledgling firm put on the market last year [*Electronics*, March 27, 1980, p. 185]. They were designed to run on smaller host computers like DEC's PDP-11 series, Intel's MDS/ISIS-II, and CP/M-based systems.

Originally, Language Resources had planned to start shipping object-language versions of its Pascal packages in the form of protected diskettes by May 1980. However, the shipments were delayed until February of this year. Geoffrey Archibald, the company's director of operations, says, "When the first article [about the packages] hit the streets last year, we were flooded with so many requests that we decided to hold off deliveries until we could develop a larger service organization. We were a much smaller company then."

Since then, the company staff has grown from 4 to 12 programmers, and Archibald maintains that it can now adhere to delivery dates that have been set for the products it currently has in the works.

Other new products include a symbolic debugger, several central-processing-unit simulators, and programs allowing the host processor to directly run in-circuit emulation hardware that is connected to a microprocessor-based system under development. In addition, the company intends to reach beyond its actual Intel-oriented base with a Pascal compiler for Motorola's 16-bit 68000. The package should be ready for release early next year, Archibald notes. **-Martin Marshall**

Super High Speed 64K Dynamic RAMs

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(industry standard)

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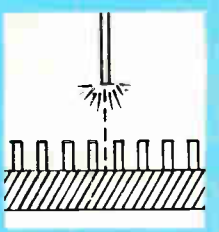
64K bits of dynamic RAM on a single chip! Confirms again OKI's strong on-stream capabilities in VLSI memory technology. Based on OKI's solid 3-year headstart in Electron Beam lithography. Begun in 1977, now fully on-line, OKI application of E-Beam defect-free masks is now producing high density chips: working products with close geometries that yield 6x or more functions than standard masking procedures.



ALPHA PARTICLE PROTECTION

The destructive bombardment of line data by alpha particles is eliminated by OKI's state-of-art 64K DRAM fabrication process. To assure total data protection, a key error prohibitor is built into every MSM3764 — through silicon doping, and unique design and manufacturing techniques.

In extensive life-cycle testing, the Double-Poly doped 64K device has experienced zero failures from alpha particle exposure.

Ceramic
OKI MSM 3764 AS, packaged for high-rel applications.

TWO PACKAGING OPTIONS

Plastic
OKI MSM3764 RS, for cost-efficient commercial/industrial applications, available May 1.

VOLUME AVAILABILITY

OKI is now filling qualification, preproduction and production orders for MSM3764 from stock. OKI's Hachioji facilities and the new $72,000,000 Kyushu fabrication plant are both now producing this device.

OKI MSM3764. The fastest 64K RAMs shipping from any memory source today. OKI is now delivering the ultimate in work-horse VLSI. 65,536 bits of dynamic NMOS RAM on a single 16-pin chip: optimized for MCU system applications requiring high speed, high density and high performance.

Volume production of the 3764 in three very fast access-time configurations—resistant to soft errors through advanced circuit design; resistant to alpha particle damage through unique processing steps—gives OKI 64K DRAM users an important edge. For main-frame memories, buffer memory, peripheral storage systems—virtually any microprocessor-related environment where high quality, strict reliability and compact layout are critical design criteria.

Availability of a more workable, more usable, faster 64K RAM underscores OKI's significant lead in VLSI memory product design and production. Today's ability to supply results from our early commitment of time, manpower and capital resources to the mastery of E-Beam lithography—at least three years before most memory suppliers began E-Beam machine experimentation and trial runs.

For full technical data and specs on MSM3764, send the coupon below. For qualification orders of the OKI 64K RAM—at 120, 150 or 200ns—contact Mary Briganti, Inside Sales Manager, OKI Semiconductor, 1333 Lawrence Expressway, Santa Clara, CA 95051. (408) 984-4842.

OKI MSM3764 — 64K NMOS dynamic RAM

( ) Please send data sheet and volume pricing.
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Title _____

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People

Motorola's Silva plans to divide and conquer

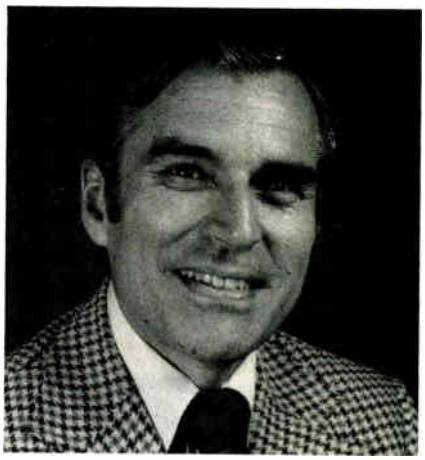
With the reorganization of its MOS memory operation in Austin, Texas, complete, Motorola Inc. is poised to step up its static random-access memory efforts. In fact, that underscores a new aggressiveness on all fronts, says Charles C. Silva, who continues as Semiconductor Group vice president and director of MOS memory operations.

That's why the operation was split into four separate product centers: 64-K RAMs, read-only memories and special products, static and dynamic RAMs (other than 64-K devices), and erasable programmable ROMs and electrically erasable PROMs. "In three years, we expect each of these product groups to grow to the same size of our total MOS memory business," says Silva, who has headed the operation since January 1979.

On top of that, Motorola has created a 256-K RAM product development group, which Silva says will eventually turn into a fifth product center. "We have set an aggressive goal of having early test parts on the 256-K RAM next year," states the graduate of Northeastern University in Boston, where he earned BS and MS degrees.

The memory operation's reorganization marks the second time this year that Motorola has divided an MOS product group into separate profit-and-loss centers. Last February, the microprocessor business was split into three centers. And under the same divide-and-conquer strategy, Silva believes each memory-product center will be able to concentrate more heavily on specific customers and technologies.

One memory sector already targeted for "a little extra attention" is the static RAM field. "We are going to try to do more in this area," vows Silva, who joined Motorola in 1965. "That is where we have a little bit of catching up to do." But the 51-year-old Silva also intends to keep pressure on other memory markets where Motorola is a volume leader—like the developing 64-K dynamic RAM arena, where it leads.



Growth. Charles Silva says Motorola will have test parts of a 256-K RAM next year.

Silva, who was in charge of Motorola's first offshore plant in Seoul, South Korea, in 1967, expects to see a peak in 16-K dynamic RAM business this year as customers finally begin to cross over to 64-K devices. He says that Motorola believes the 64-K will peak in 1985 or 1986—and that is when the firm hopes to begin showing samples of a 1-megabit RAM.

Dumas builds industrial base in Europe for Fairchild

Fairchild Camera & Instrument Corp. has not fared well in West European semiconductor markets. But the Mountain View, Calif., company, backed by its money-churning parent, Schlumberger Ltd., has started to position itself to move out of the pack to join the front runners—Philips Gloeilampenfabrieken, Texas Instruments, Motorola Semiconductor Products, and Siemens.

"We have the means and the motivation to bring Fairchild in Europe up to the same competitive level it is at in the U. S.," says Guy Dumas, general manager of Fairchild Europe, the organization set up this spring at Schlumberger's Paris headquarters to manage the move.

The 52-year-old Dumas maintains that Fairchild lags behind the European leaders largely because it

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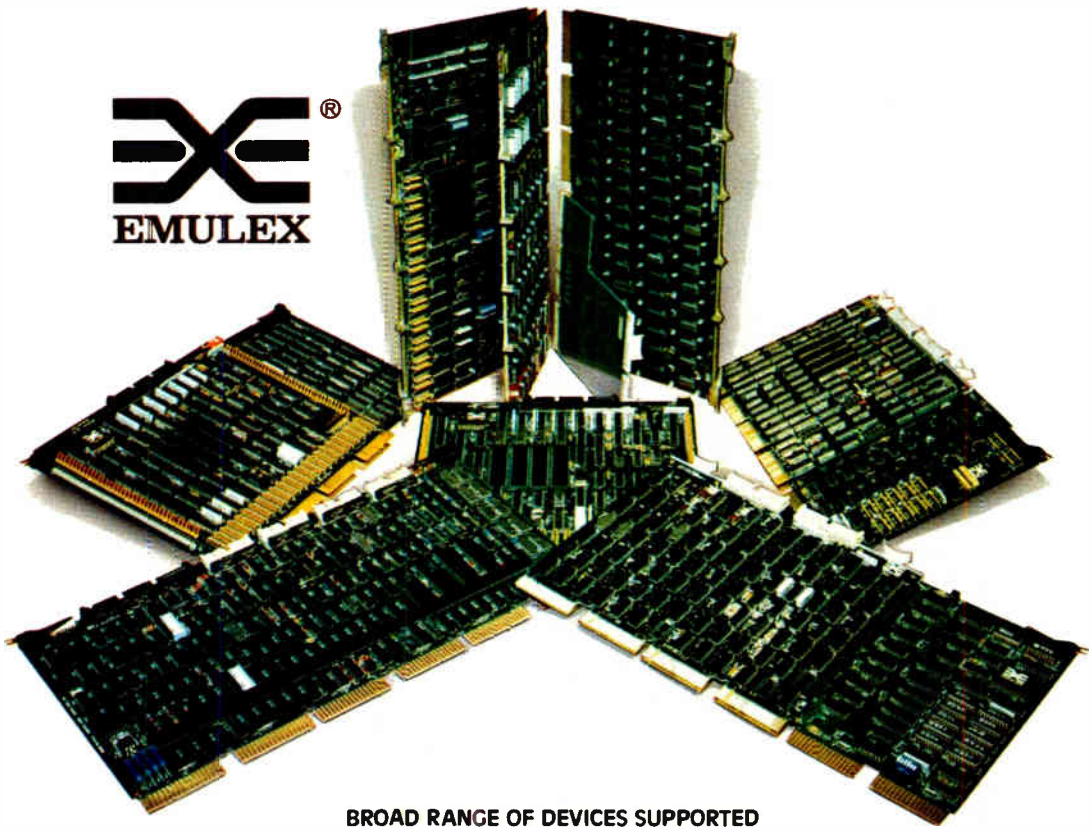

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It makes no difference which of the DEC PDP-11 or LSI-11 family you are using or which type of storage device is required for your application. We can support 59 different drives from 13 different manufacturers.

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You can be assured of the quality and reliability of these Tape and Disk Controllers because First Computer Corporation specializes in PDP-11 and LSI-11 computer systems, components, and peripherials. Over the years our reputation was built on the quality and reliability of the products we sell. We continue to protect this reputation by selling only the very best.

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Your satisfaction is fully guaranteed by First Computer Corporation. We believe in every product we sell. If for any reason these Tape and Disk Controllers do not meet your expectations, simply return them freight prepaid and insured, within 10 days of receipt and we will refund your money in full. First Computer Corporation backs each of these products with a full one year warranty.

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Circle 15 on reader service card

Builder. Guy Dumas plans plant and design centers for Fairchild in Western Europe.

has no industrial base there. So the first move he has in mind is to build an ambitious full-fledged production plant in West Germany, the dominant West European market. "We'll make the announcement about the plant in September or October and should have assembly operations started in about a year. Wafer processing will start about another year after that," he says.

Although he has not set firm dates yet, Dumas has roughed out plans to give Fairchild an industrial presence in Britain and in France, the other two major markets in the region. "We'll have our European research and development center in the UK, where there already is a design center at Bristol. After that will come a design center in France."

If Dumas can manage a replay of his track record, Fairchild will become a strong contender in European semiconductor markets. Before taking the top job at Fairchild Europe, he headed Thomson-CSF's semiconductor division, the French firm's linear-circuits operation. While there, Dumas reorganized the linear business after meshing with it a small power-semiconductor producer (Silec Semiconductor) that he was running when Thomson-CSF acquired it. Dumas, who holds an engineer's diploma from the prestigious Ecole Supérieure d'Electricité and a doctorate in physics from the University of Paris, had the division in the black until semiconductor markets in Europe soured last year. □

MIL-SSR UPDATE

We married SSR technology to military needs... and the family keeps growing

It all started with our M640 series – miniature SSRs in hermetically sealed TO-5 packages. These were the first solid state relays ever to receive QPL approval to MIL-R-28750.

Teledyne is still the first and only SSR manufacturer with a family of products designed specifically for military and aerospace applications. We have AC and DC models with outputs ranging from milliamps to 25 amps, featuring optical as well as transformer isolation. All utilize military grade components and hybrid microcircuit techniques to reduce parts count and increase reliability. Our latest is a 3-phase AC SSR designed for 220 volt, 400 Hz operation.

If you need a solid state relay for military or aerospace applications, come to the recognized leader in military SSR technology – Teledyne Relays.

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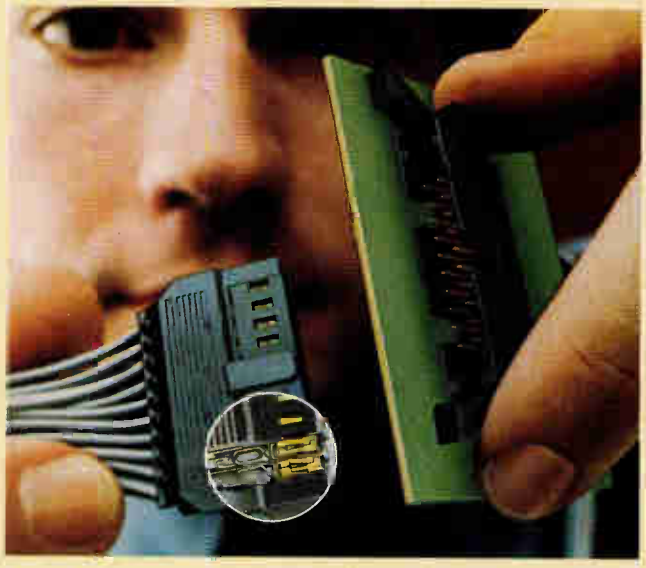


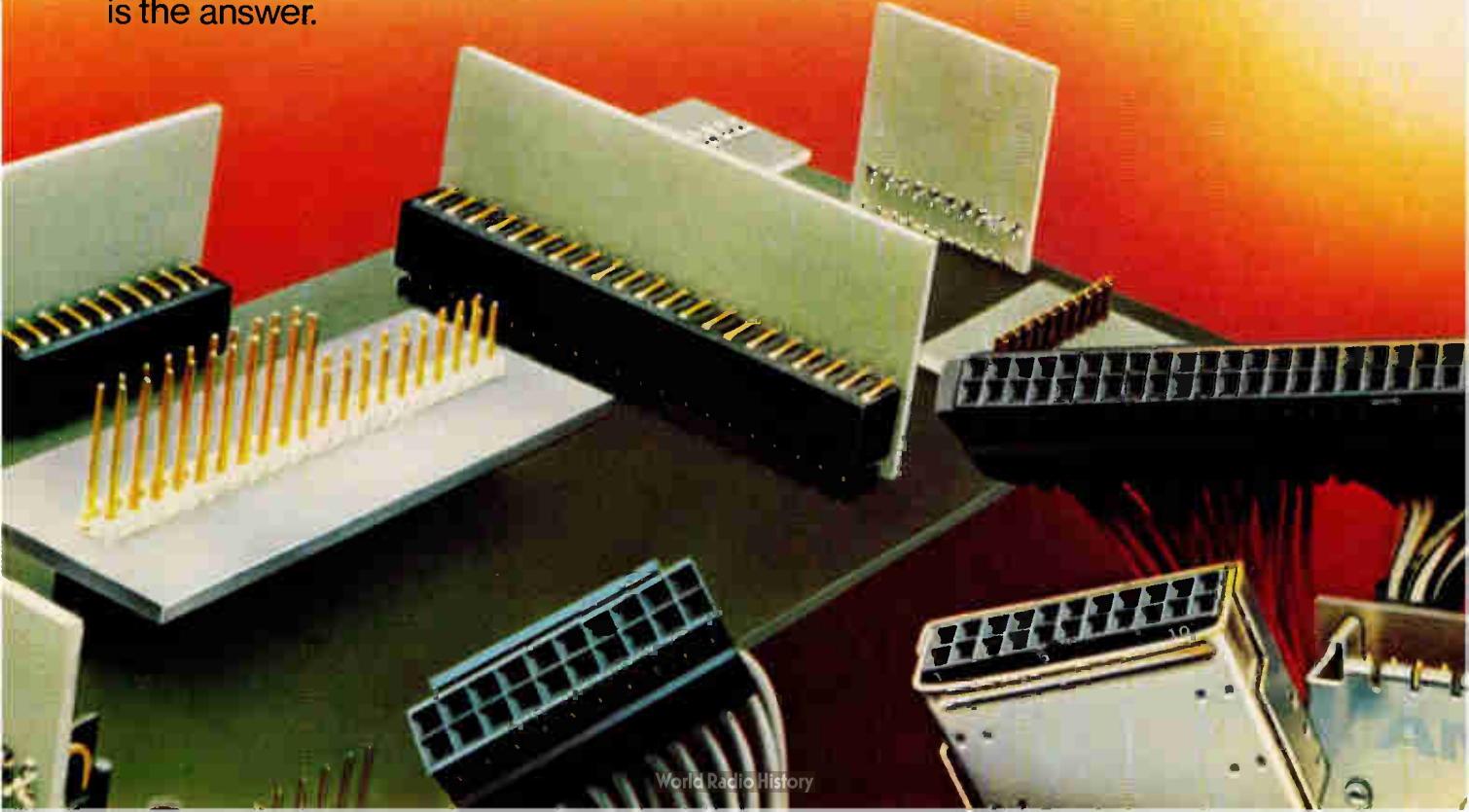
Now you can have the money-saving benefits of mass termination with the design advantages of our universal board-to-board, wire-to-board and wire-to-wire AMPMODU interconnection system.

The AMPMODU MT connector.

Its insulation displacing contact works with discrete wire, or jacketed and ribbon cable. And housings gang together with one low-profile cover assembly for multiple cable style applications. If you need EMI shielding, our inexpensive hardware kit is the answer.

We've advanced mother/daughter board packaging, too. Our newly-designed two-piece connector gives you higher density and greater performance than one-piece designs. At comparable cost.

These are just two of the latest innovations in our AMPMODU receptacle design—proved reliable for fifteen years, and even more cost-effective now with Accu-plate precision plating. So keep updating your product for the better with the AMPMODU system.

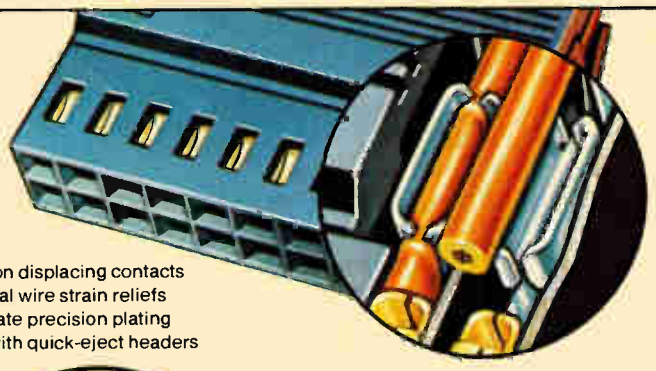


AMP Facts

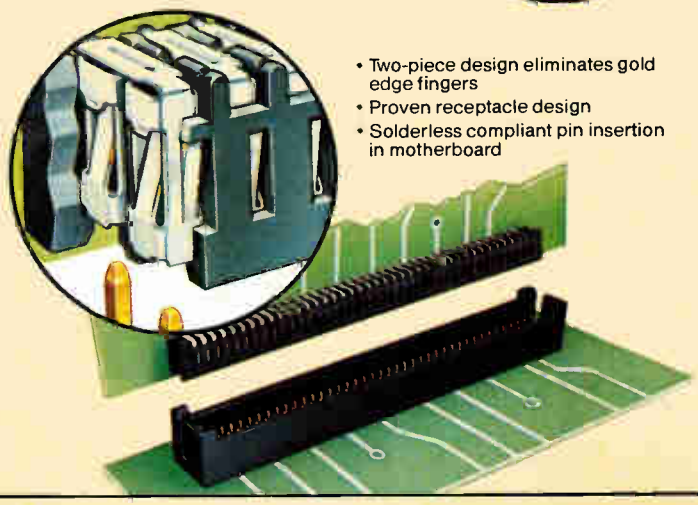
General classifications of AMPMODU posts and mating receptacles:
.031" x .062" and .025" x .025" incorporating standard, intermediate, and high-pressure design.

Housings:
A wide variety of sizes, styles and centerlines, including .100", .125" and .150". Single or double row.

AMPMODU MT Connectors:
Range from 6 through 72 positions and can be terminated to discrete wire, jacketed cable, twisted pair cable, and ribbon cable.



- Insulation displacing contacts
- Individual wire strain reliefs
- Accu-plate precision plating
- Mates with quick-eject headers



- Two-piece design eliminates gold edge fingers
- Proven receptacle design
- Solderless compliant pin insertion in motherboard

For more information, call the AMPMODU System Desk at (717) 780-8400.
AMP Incorporated, Harrisburg, PA 17105.

AMP means productivity.

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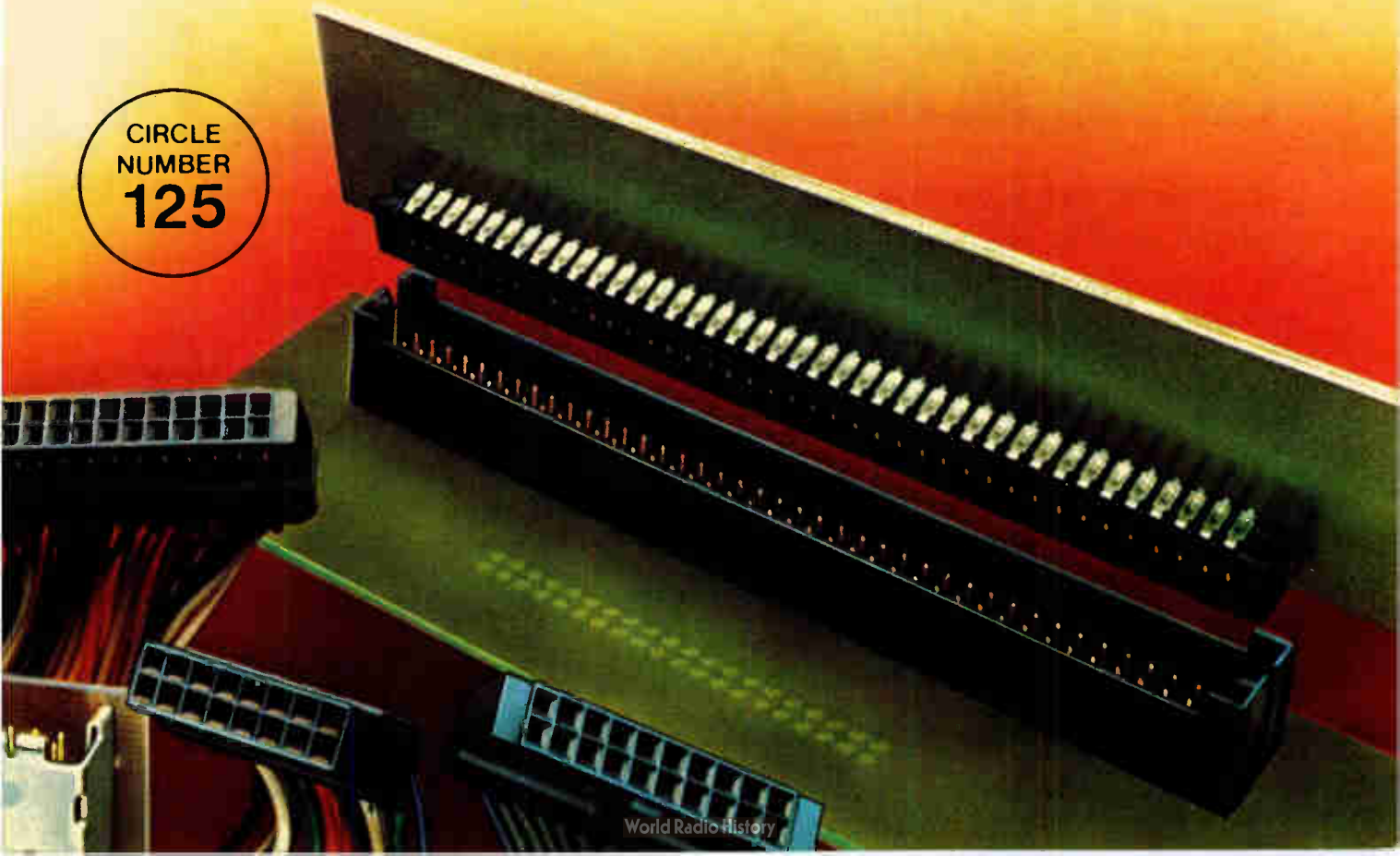
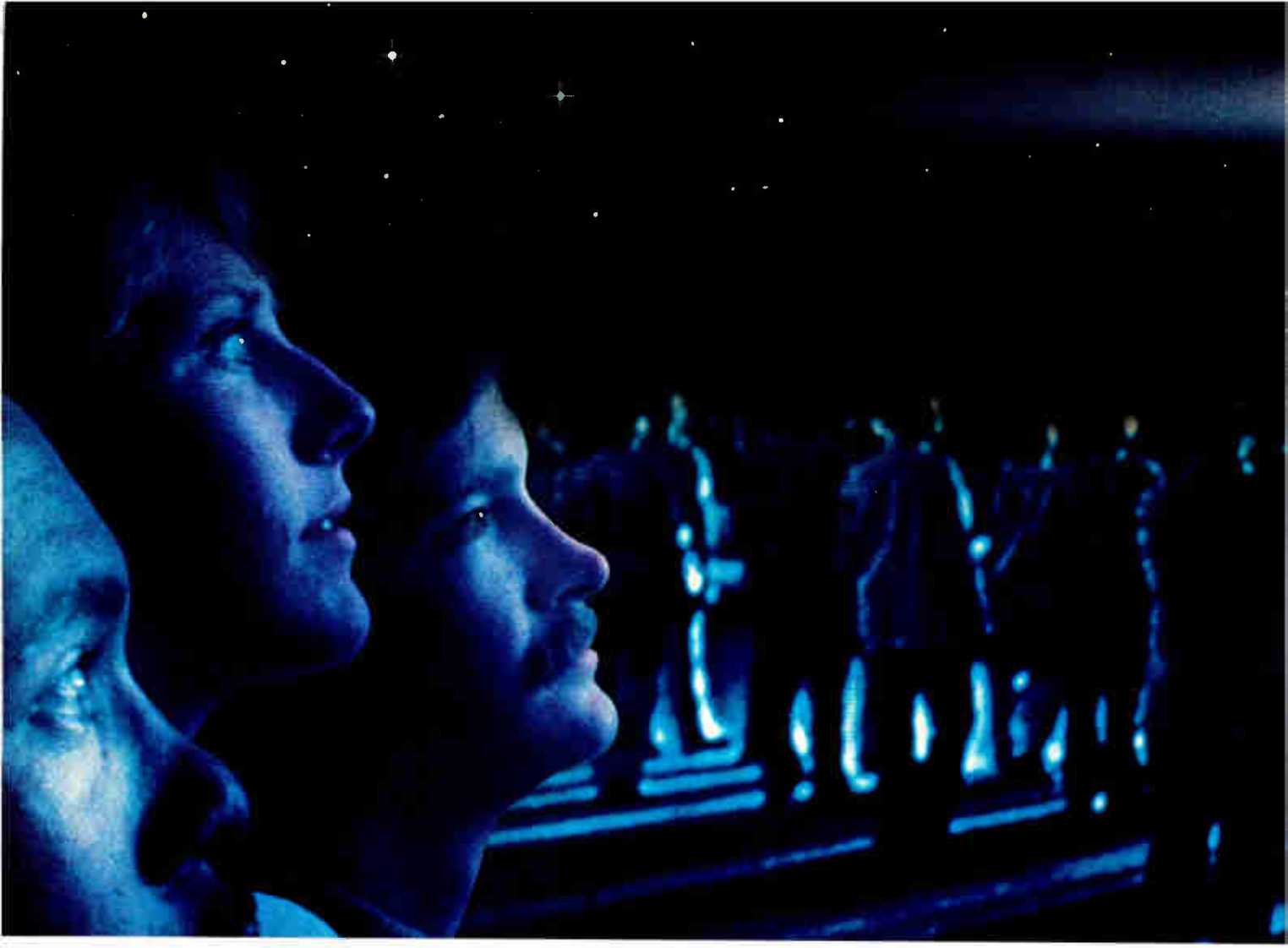




Blinding speed in

Intel introduces the world's fastest 16K bipolar PROM, the 3636B.

At a blinding 35ns, our new 3636B offers the fastest access time ever in a 16K bipolar.

The newest member of our complete family of 8K and 16K bipolar PROMs, the 3636B is now being produced in volume. Which means you not only get speed in access times, you get it in delivery times too.

Breaking speed barriers to performance

Exceptional speed...density... reliability. Super-high-performance applications demand them all.

Take microcode or program store in bit-slice microprocessors, for example. Or high-speed data-comm, telecom and military applications.

That's where the 3636B really shines. It's got what it takes to increase throughput in today's high-performance microprocessors. Plus it's got plenty of features to help simplify design cycles. Features like three chip-select inputs and three-state outputs. A 10% power supply tolerance. And an industry-standard 24-pin package.

Boosting yields and reliability too

How do we achieve the 3636B's remarkable speed, while reducing its die size, boosting yields and improving reliability figures? Simple. With our exclusive Stacked Fuse Bipolar* technology.

This is the same technology that's proven itself in millions of device hours over the past four years,

*Stacked Fuse Bipolar is patented by Intel Corporation.

Intel Bipolar PROMs		MAX.
3636B-1	2K x 8	35ns
3636B-2	2K x 8	45ns
3636-1	2K x 8	55ns
3636	2K x 8	80ns
3628A-1	1K x 8	50ns
3628A-3	1K x 8	70ns
3628A-4	1K x 8	90ns
M3636 (Military)	2K x 8	80ns

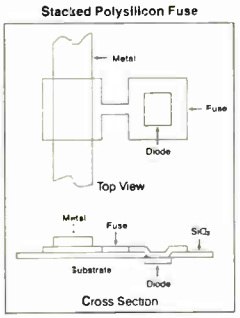
bipolar PROMs.

in our existing line of bipolar PROMs. And in millions of devices delivered—including military versions for hi-rel applications.

This dual layer metalization and polysilicon fuse process makes possible the inherently high reliability of our bipolar PROM family. And the higher yields you get from programmed parts.

Coming on strong with a full line

No matter what you need in high-density bipolar PROMs, Intel's got it. For hi-rel applications, there's our military-qualified 16K. Or if you're designing in 8K increments, you can put our bipolar technology to use with parts as fast as 50ns.



Intel's new Stacked Fuse Bipolar process allows a 30% reduction in the 16K cell size. This dramatic density improvement yields faster access speeds than ever before possible. The illustration shows the "stacking" of our polysilicon fuse over the diode, instead of placing them side by side as in older designs.

In fact, we've got a high-speed 8K or 16K bipolar PROM to upgrade virtually any other part you may now be using.

Dazzling delivery times

Bipolar PROMs from Intel are now available off the shelf. So whether it's the world's fastest 16K part or any other part of our complete bipolar line, you'll be dazzled by our delivery times.

To order, or get complete specifications, reliability information, and our convenient Bipolar PROM Reference Guide, contact your local distributor or Intel sales office. Or write to Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

Europe: Intel International Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors. Alliance, Arrow/Stroum, Arrow Electronics, Avnet Electronics, Component Specialties, Hamilton/Avnet, Hamilton/Electro Sales, Harvey, Industrial Components, Pioneer, L.A. Varah, Wyle Distribution Group, Zentronics

intel® delivers solutions

Circle 21 on reader service card

NEC SYSTEM350 WORKS FOR U.N. COMMISSION

An NEC computer system is in operation at the Economic and Social Commission for Asia and the Pacific (ESCAP), a subagency of the Economic and Social Council (ESC) of the United Nations.

Headquartered in Bangkok, Thailand, ESCAP was established in 1947 as one of ESC's regional commissions. Its activities include the collection of statistical economic data, research and investigation, and the promotion of economic development and cooperation.

The NEC SYSTEM350 is used to collect and analyse data and to simulate various economic conditions. The system consists of a central processor unit, two line printers, three 600M byte magnetic disk units, and nine on/off-line terminals.

NEC SYSTEM350 is a medium-size computer that incorporates the latest hardware technology, such as a high speed bipolar CML LSI having a capacity of 1,200 gates/chip and a high density MOS LSI with 6,000 gates/chip.

NEC's computer series now has a full line of models, provided with all types of peripherals and terminals, and comprehensive software. It ranges from the small business computer, NEC SYSTEM100* to the world's largest computer, NEC SYSTEM1000.

* *"Astro" in the U.S.A.*

NUMBER 118

DIGITAL DISPLAY PAGER DEVELOPED

Better and more versatile paging is offered by a new NEC radio pager with a liquid crystal display unit.

The R3D3-1A display pager with an incorporated microprocessor can display a calling party's telephone number up to 10 numerals. Moreover, if another call comes in while a paging call is being received, the second call can be stored and later retrieved by pressing a readout switch.

Incoming calls can be signalled by a beep tone, LED, or vibration, with the user able to select the mode. In this way, the user can make sure that an important meeting—for example—will not be disturbed by a beeping noise.

Since the display pager can respond quickly to signals from the base station, 20,000 to 40,000 pagers can be operated on a single frequency within the service area—a much more efficient use of radio frequency than conventional "tone and voice" pagers.

The completely solid state R3D3-1A is extremely compact (89mm height × 51mm width × 20mm thickness) and weighs approximately 130 grams. It operates on the 138—174MHz VHF band and runs for about five months on one standard 'AA' size 1.5V penlight battery.

As soon as the new pager was unveiled, three Hong Kong paging companies placed orders for a total of 16,000 sets. And soon, some American companies will also make the R3D3-1A available to their subscribers.

NEAX 22SA SIMPLIFIES OFFICE COMMUNICATIONS

Up to 1,600 extensions can be accommodated by the NEAX 22SA, a medium-to-large capacity PCM digital electronic private automatic branch exchange (EPABX).

This addition to NEC's NEAX 22/12 family of EPABX systems interweaves new functions that simplify office communications to save time and money.

A remote line system lets outlying offices share one NEAX 22SA.

Another remote system with a self-diagnostic function permits centralized administration and maintenance of the main NEAX 22SA through trunk lines.

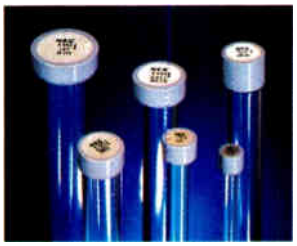
Three different recording systems for station message details enable the user to quickly obtain information most frequently sought, such as billing and traffic.

And PCM switching technology gives the NEAX 22SA the highest possible speech quality, plus compatibility with CCITT specified PCM 24 or 32-channel digital networks and various data terminals. It can also be interconnected with analog telephone lines.

Since it is a multiprocessor EPABX, the NEAX 22SA can be started with any number of lines up to 1,600 and extended to full capacity as the need arises. Compact design and modular construction also contribute greatly to its cost-effectiveness.

SUPERCAPS PROTECT CIRCUITS FROM POWER SHUTDOWNS

NEC has developed farad range capacitors, dubbed "Supercaps", which can be used in lieu of NiCd batteries to protect programmable timers and control circuits against momentary power shutdowns, or to retain the contents of volatile memories for several weeks.



Five-volt Supercaps (0.047 to 1.0 farad) and ten-volt Supercaps (0.10 to 0.47 farad) are available in sizes between 15.5mm (height) × 16mm (diameter) and 28.5mm (h) × 44.5mm (d).

Their extremely high capacitance in extremely small packages results from a practical use of the "electronic double layer" phenomenon.

(Supercaps may not be suitable for filtering circuits because of high ESR.)

NEC
Nippon Electric Co.,Ltd.
P.O. Box 1, Takanawa, Tokyo, Japan.

Editorial

Learning to postpone the pleasure

Maturity has been defined as the ability to postpone immediate gratification in return for a longer-term advantage. If that's the case, then the electronics industries are earning the sobriquet of "mature" the hard way—but they are earning it. Certainly immediate gratification has been denied many companies by the current economic slowdown, as witnessed by such recent announcements as a profit squeeze at Intel Corp. and others and product line curtailment and layoffs at Texas Instruments Inc. But despite these reverses, the general picture throughout the industry is still one of cautious optimism.

The universal feeling seems to be that the turnaround will come in late 1981 or early 1982, and companies are wisely using this lull to get ready for the good times. Having learned the hard way in 1974–75 that laying off workers and cutting back on additions to production capacity in response to a slowdown is a big mistake, the semiconductor manufacturers are not resorting to wholesale layoffs and cutbacks. They are still plowing full speed ahead on research and development and holding on to people through temporary plant shutdowns and forced vacations (see p. 96).

There may be months of crunch still ahead, but the industry seems ready and willing to cope with it without panic. The long-term payoff for this newfound maturity will be readiness for the coming big boom.

Keeping secrets in the family

The presidents of five of the United States' most prestigious schools—Stanford, Cornell, and Berkeley universities and the California and Massachusetts institutes of technology—say that the Government's attempts to restrict the export of technology could harm university-based research. At the root of their complaint is the Department of Defense's Very High Speed Integrated Circuits program and the contracting of certain Phase 3 VHSIC work to universities, where foreign nationals routinely do research work.

Complicating the situation is the fact that there are actually two sets of regulations that sometimes conflict in their restrictions on the mixing of Government-sponsored research and foreign researchers. Those of the Defense Department are the International Traffic in Arms Regulations. The Commerce Department's, labeled by one university official "the most bewildering set of regulations I've ever had to deal with," are called Export Administration Regulations.

The universities are right to be concerned over the possible loss of academic freedom, as well as the need to comply with complex and bewildering rules. The rest of the U. S. engineering community should also be concerned by what the outflow of any advanced information might mean to the continued prosperity of their enterprises. But perhaps the VHSIC program is not the issue on which to make a stand. As Larry Sumney, the Pentagon's VHSIC program director, says, the parties involved are making much ado about little. The story on page 39 points out that the regulations apply only to process steps, not to such other classifications as stress analysis, statistical inference, and device physics. In other words, the U. S. does not want to tell how to make devices, but it has no objection to disclosing the basis of their behavior.

TEK 8500 SERIES MDL

FLEXIBLE SOLUTIONS
FOR A FUTURE OF CHANGE

Some revealing facts about real-time emulation.

Real-time and not-so-real time explained.

Suppose you had a prototype designed to run at 1 MHz. If your emulation system drove it at one clock cycle per second, would you call this real-time?

Of course not.

But others would. "Real-time" emulation often refers to any speed that executes the proper logic sequence on the prototype. No matter how long it takes.

So why the muddy terminology? Because running an emulator at specified processor speeds is a tricky business. There's very little time left to extract debugging information.

It's much easier to refer to any time as "real" time by adding "wait states" or clock stretching techniques. Even if it has nothing to do with the true operating speed of your prototype.

Tek emulators like our new 6809 give you the real thing.

At Tektronix, real-time emulation means exactly what it should.

Take our new 6809 emulator for instance. The 68B09 version of this processor is the fastest. It allows prototype bus cycles up to 2 MHz. And this is the true speed at which our 6809 emulator can fully function. With all debugging information still perfectly intact.

And the 6809 is just a single example. Tek's entire line of emulators run in true real time.

And that's really just the start.

In addition to real-time, Tektronix gives you an outstanding lineup of debugging features.

Like our new terminated low-profile probes, using special hybrid circuitry that permits smaller size for easy access to crowded prototype locations.

And symbolic debug for rapid entry of trace commands. Symbolic disassembly, too.

Also service calls that let you simulate I/O by using development system resources, such as keyboard, display, printer and mass storage.

The broadest chip support anywhere.

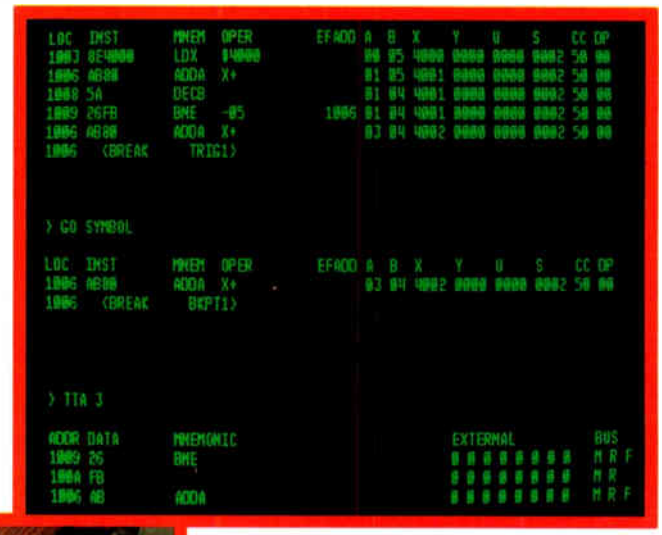
Nobody offers the breadth and depth of chip support you get from Tektronix:

6809	**8048**	**8049**
6800	**8039**	**3870**
6808	**8039-6**	**3872**
6802	**8035**	**3874**
Z80A	**8021**	**3876**
8080A	**8022**	**F8**
8085A	**8041A**	**1802**

Assembler support is available now for the 16-bit chips listed below. Emulation support for the 9900 is available now. Real-time emulation and Pascal support will be available in stages for the 68000, Z8001, Z8002 and 8086 beginning the third quarter of 1981.

68000	**Z8001**
8086	**Z8002**
SBP 9900	**TMS 9900**

6809 Prototype Control Probe tip fits easily in hard to reach locations. Probe status lights monitor key processor signals.



(top) Trace All display gives disassembled prototype code plus the status of all key processor registers on a step-by-step basis.

(middle) Symbolic debugging allows all major address locations to be defined as easily read mnemonics. Breakpoint information includes full display of processor status.

(bottom) Trigger Trace display shows real-time bus activity on a cycle-by-cycle basis plus eight channels of hardware logic defined by the user.

Find out more today.

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Meetings

ICALP **81—Eighth International Colloquium on Automata, Languages, and Programming,** European Association for Theoretical Computer Science (S. Even [ICALP 81], Computer Science Department, The Technion, Haifa, Israel), The Technion, Haifa, July 13–17.

Fifth International Conference on Vapor Growth and Epitaxy and Fifth American Conference on Crystal Growth, American Association for Crystal Growth (Conference Secretariat, Anthony L. Gentile, Hughes Research Laboratories, 3011 Malibu Canyon Rd., Malibu, Calif. 90265), Hotel del Coronado, Coronado, Calif., July 19–24.

Fourth International Conference on Software Engineering for Telecommunications Switching Systems, Institution of Electrical Engineers (Savoy Place, London WC2R 0BL, England), University of Warwick, Warwick, England, July 20–24.

WCCE **81—Third World Conference on Computers in Education,** International Federation for Information Processing (WCCE 81 Organization Committee, Pierre Immer, 33, av. de Cour, CH-1007 Lausanne, Switzerland), Palais de Beaulieu, Lausanne, July 27–31.

Siggraph '81, Association for Computing Machinery, (Siggraph '81 Conference Office, 1 Illinois Center, 111 E. Wacker Dr., Chicago, Ill. 60601), Dallas Convention Center, Dallas, Aug. 3–7.

16th Intersociety Energy Conversion Engineering Conference, IEEE, American Society of Mechanical Engineers, American Institute of Aeronautics and Astronautics, *et al.*, Hyatt Regency Hotel, Atlanta, Ga., Aug. 9–14.

20th General Assembly of the International Union of Radio Science, (c/o R. Dow, National Academy of Sciences, 2101 Constitution Ave. N. W., Washington, D. C. 20418), Hyatt Regency Hotel, Washington, D. C., Aug. 10–19.

Optical Information Processing For Aerospace Application, (H. Hendricks, Langley Research Center, Hampton, Va. 23665), Hampton, Va., Aug. 18–19.

VLSI **81—International Conference on Very Large-Scale Integration,** (Secretariat, VLSI 81, 26 Albany St., Edinburgh EH1 3QH, UK), University of Edinburgh, Edinburgh, Scotland, Aug. 18–21.

1981 International Conference on Cybernetics and Society, IEEE, Atlanta Hilton Hotel, Atlanta, Ga., Aug. 24–27.

SPIE **International Symposium and Instrument Display,** Society of Photo-Optical Instrumentation Engineers (P. O. Box 10, Bellingham, Wash. 98227), Town and Country Hotel, San Diego, Calif., Aug. 24–28.

Seventh International Joint Conference on Artifical Intelligence, (Pat Hayes, General Chairman, IJCAI-81 University of Rochester, Department of Computer Science, Rochester, N. Y. 14627), University of British Columbia, Vancouver, B. C., Canada, Aug. 24–28.

1981 International Conference on Parallel Processing, IEEE Computer Society, Shanty Creek Lodge, Bellaire, Mich., Aug. 25–28.

Fifth Annual National Small Computer Show, (110 Charlotte Pl., Englewood Cliffs, N. J. 07632), New York Coliseum, New York, Aug. 26–29.

Seminars

1981 International Symposium on Electromagnetic Compatibility, IEEE, University of Colorado, Boulder, Aug. 18–20.

Office Automation and Integration of Word Processing and Data Processing, (Frost & Sullivan Inc., 106 Fulton St., New York, N. Y.), Holiday Inn, Fisherman's Wharf, San Francisco, Aug. 19–21.

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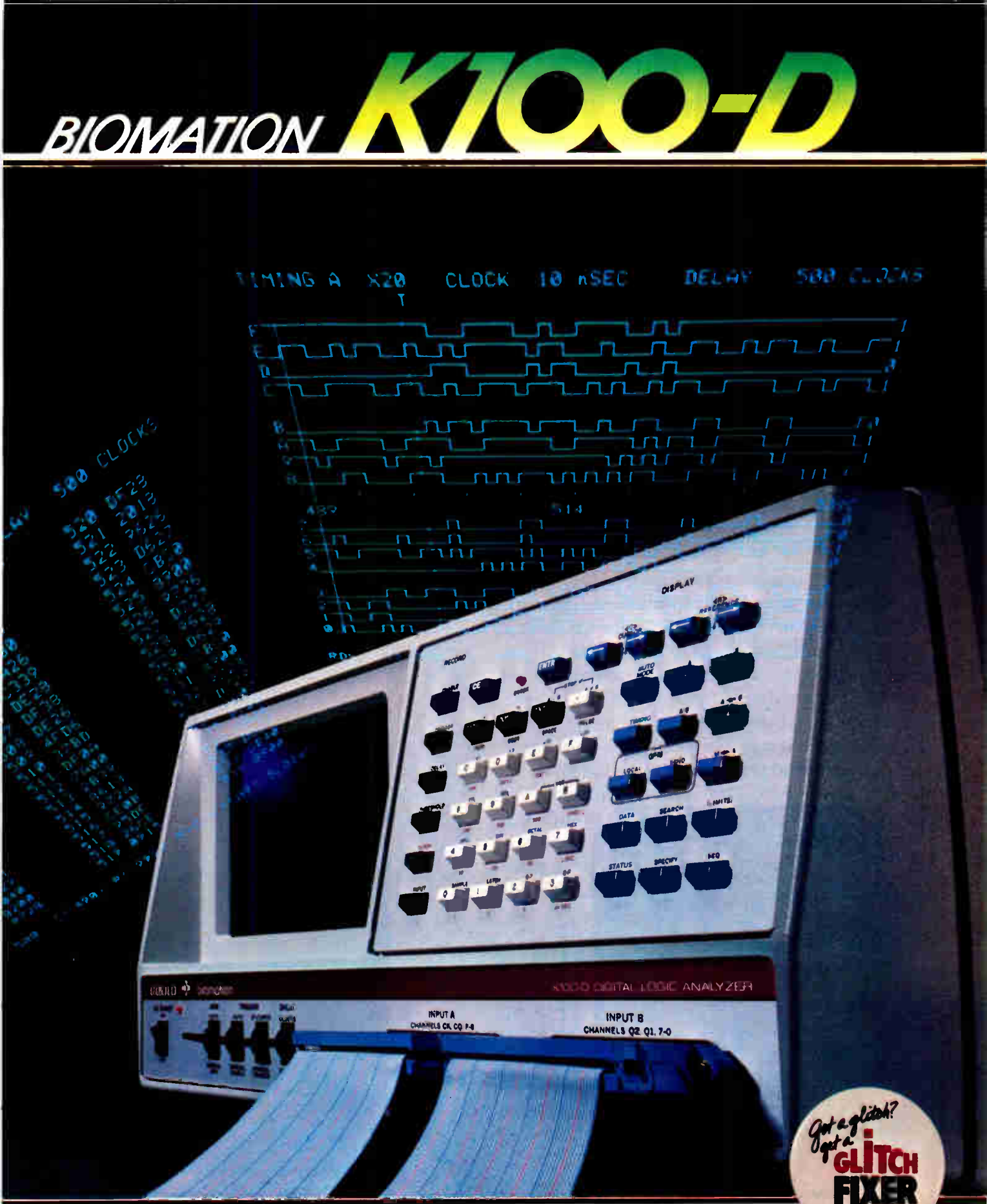

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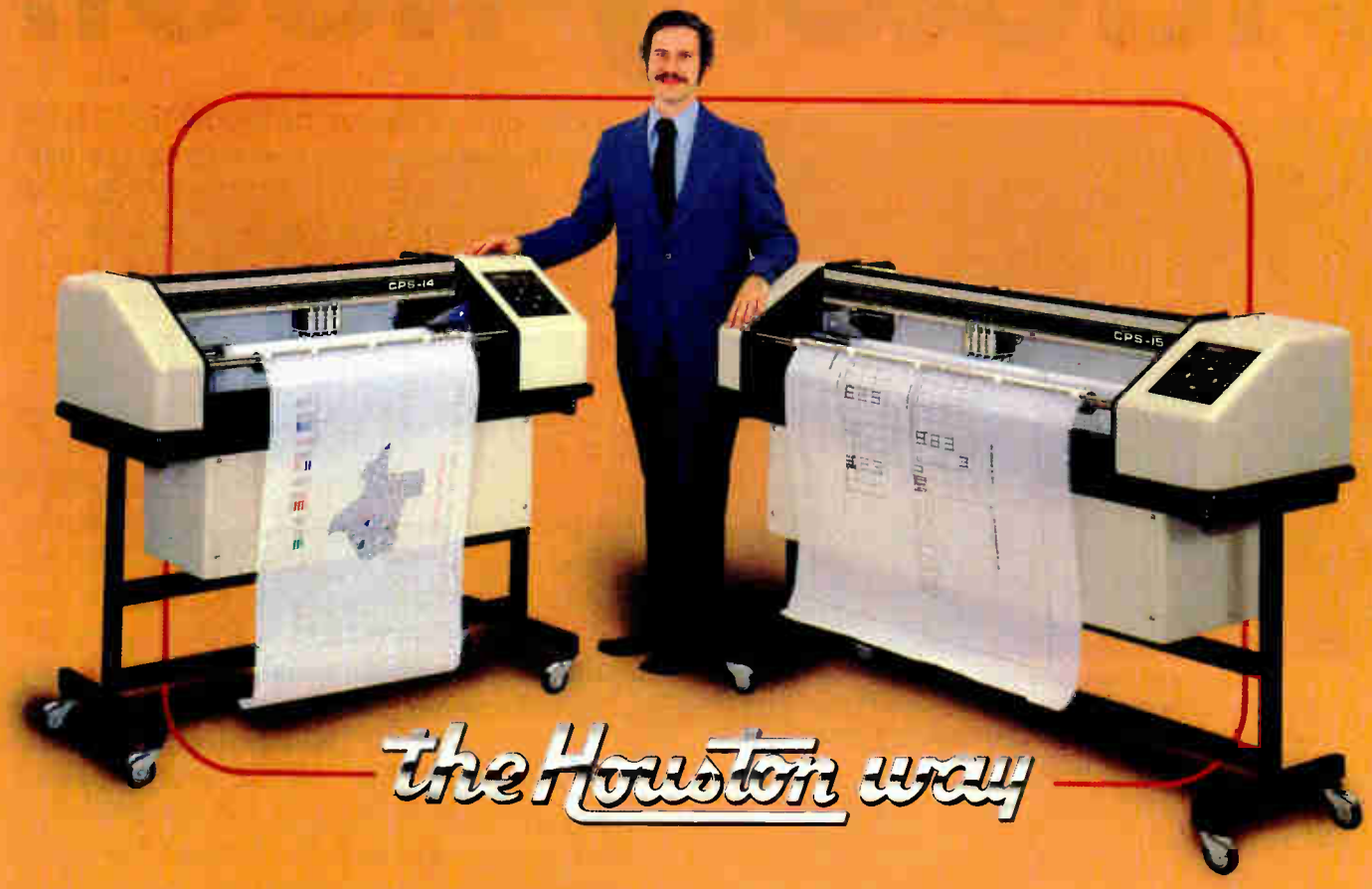

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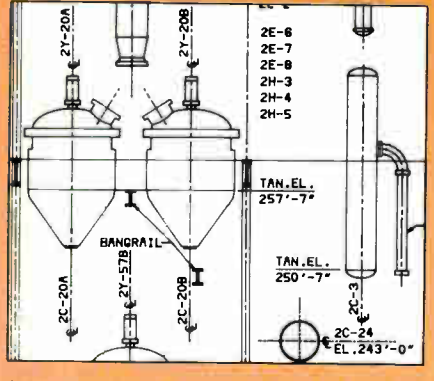

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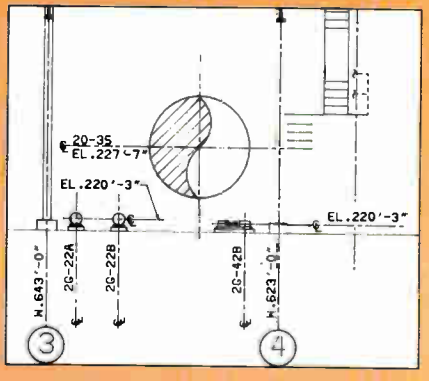

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Electronics newsletter

Synertek to build National's 16000 microprocessor . . .

The second-source derby in the 16-bit microprocessor contest shows no signs of slowing down. The latest addition to the field is the Synertek division of Honeywell Inc. in Santa Clara, Calif., which will second-source National Semiconductor Corp.'s 16000. **Synertek is the second alternative source for the 16000,** joining Fairchild Camera & Instrument Corp. The latest lineup, in addition to National's two teammates, shows Motorola leading with five other sources, Zilog with Advanced Micro Devices, and Intel with Harris (see below). As for Synertek, it will also turn out all six of the 16000 family's support circuits. In return for masks from National, also in Santa Clara, Synertek will design and produce as yet unspecified peripherals in its own process, similar to National's X-MOS.

. . . as Harris signs to make 8086

Having lost Mostek Corp. as the only domestic second source for its 16-bit 8086 microprocessor [*Electronics*, April 21, p. 41], Intel Corp. has signed a technology swap with Harris Corp. Intel will provide the Melbourne, Fla.–based company with hardware know-how, documentation, and software tools for the 8086 and its 8-bit-bus counterpart, the 8088, plus associated peripheral chips. In return, **Harris will develop complementary-MOS versions of these devices** and provide the Santa Clara, Calif., chip maker with tooling so that both companies can manufacture and market the C-MOS versions in the U. S. In addition, Harris has garnered the right to license the production of these products to Matra-Harris Semiconducteurs SA, which recently signed a wide-ranging pact with Intel [*Electronics*, April 7, p. 71].

VLSI test system coming from Teradyne

Look for Teradyne Inc.'s semiconductor test group in Woodland Hills, Calif., to introduce a test system for very large-scale integrated circuits by year-end. To be called the J900, the system should cost between $500,000 and $1.5 million depending on the configuration. **It will be able to test microprocessors, memory, and custom logic.** The unit is aimed at the market now served by systems from GenRad STI of Milpitas, Calif., and Takeda Riken Industries Co. of Japan.

Xerox to market personal computer . . .

Xerox Corp. has become the first major U. S. office products company to enter the personal computer market. The Xerox 820 information processor from the corporation's Office Products division in Dallas is a Z80-based system for use as a personal business computer and word processor. **The 820 is aggressively priced at $2,995 for the basic system,** which includes the processor, 64-K bytes of memory, a standard typewriter keyboard; a 24-line, 80-character display; and dual 5¼-in. floppy-disk drives. A Diablo letter-quality printer is available for $2,900. Connection to Ethernet is through the Xerox 8000 series communications servers.

. . . with IBM to follow suit

Look for International Business Machines Corp. to follow Xerox next month with its long-awaited personal computer. It will be produced in IBM's General Systems division, Boca Raton, Fla., **and has won out over a similar computer developed by Matsushita Electric Industrial Co.** that IBM would have second-sourced. Chess is built around Intel's 8088 microprocessor, which has an 8-bit data bus and the instruction set of the 16-bit Intel 8086. Priced at $3,000 to $4,000, the system will include two

double-sided double-density 5¼-in. floppy drives from Tandon Magnetics Corp. in Chatsworth, Calif. It will also have a detachable keyboard and will be in a configuration similar to the IBM 3101 terminal's. Its disk operating system, developed by Microsoft Inc. of Bellevue, Wash., is similar to CP/M and will be called IBM Personal Computer DOS. The system will have from 64 to 256 K of random-access memory and a 600-by-400-line display in black and white. It will also be able to handle eight colors with a resolution of 400 by 200 picture elements or four colors with twice that resolution. IBM will market its computer nationally through Sears and Computerland stores, and is negotiating with J. C. Penney.

Fairchild wins suit on use of Nova's software

Data General Corp.'s appeal of a court ruling that its computer architecture and operating systems were separate products has resulted in another ruling **that places the software essentially in the public domain.** The decisions came in a suit filed against the Westboro, Mass., computer maker by Fairchild Camera & Instrument Corp., Mountain View, Calif., over its 9440 line of microcomputer products that execute the instruction set of Data General's Nova minicomputer [*Electronics*, June 23, 1977, p. 113]. Fairchild charged, along with Digidyne Corp. of San Diego, Calif., that Data General had hindered its sales by refusing to permit use of the Nova's operating system. As a result of the latest ruling—that Data General's policies violated U. S. antitrust laws—Fairchild and Digidyne could receive as much as $300 million in damages, with the exact amount to be set by a Federal court jury.

FCC to weigh North American videotex standard

The text of a North American standard for broadcast and telephone-line videotex will be submitted to the Federal Communications Commission "in the near future," says Telidon Videotex Systems Inc., the U. S. subsidiary of Canada's government-developed system. The proposed standard has been developed by **Canada's Department of Communications, the Columbia Broadcasting System, the developers of the French Antiope system, and American Telephone & Telegraph Co.** The Canadians say that their system will be compatible with it, as will Antiope, with minor adaptations.

Board tester talks for Fairchild

At the Ninth Semiannual Automatic Test Equipment Seminar and Exhibit in Boston last week, the Fairchild Test Systems Group of Billerica, Mass., demonstrated a prototype of a voice-output module for use with the series 70 model 60 functional and in-circuit test system. The module's audible instructions on where to place the system's probe for guided-fault routines **reduces the diagnostic time by up to 30%,** according to the company, by eliminating the need to refer to displayed instructions.

Faggin leaves Exxon post

Federico Faggin, cofounder of Zilog Inc. and more recently vice president of Exxon Enterprises Inc.'s Computer Systems Group, has left Exxon **to pursue personal interests.** Faggin was promoted to the position late last year, after being chief executive officer of Zilog, in Cupertino, Calif., since 1974, but the day-to-day operation of the company had been in the hands of Zilog's current president, Manny Fernandez.

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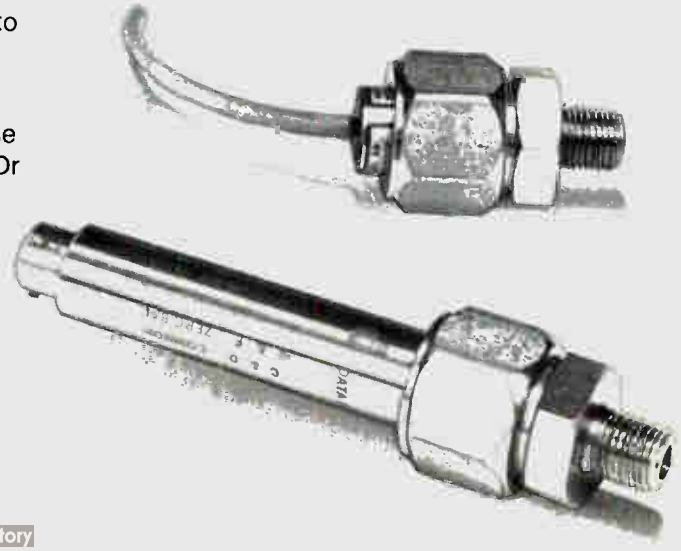

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E-beam machines paired with optics pare wafer costs

by J. Robert Lineback, Dallas bureau

Electron beams scribe layers with fine-featured motifs; photolithography takes care of less-demanding layers

Even though many semiconductor houses are counting on direct-writing electron-beam technology to carry them into the submicrometer era, most will likely end up working with the combination of electron-beam and the photolithography that prevails today. The reason: such double-teaming affords significant savings in production costs.

International Business Machines Corp., for one, has been double-teaming wafers with the two technologies ever since it started using a direct-write-on-wafer electron-beam machine at its quick-turnaround facility at East Fishkill, N. Y., in 1974 and plans to stick with it. Texas Instruments Inc., for another, expects to shift to a combination of the two later this year for one of its most advanced products, the SBP-9989E 16-bit military-grade integrated-injection-logic microprocessor, used internally in the Dallas firm's equipment group.

Picking patterns. Both companies discussed the combination late last month at the 16th Symposium of Electron, Ion, and Photon Beam Technology in Dallas. Crucial to the mix is determining which integrated-circuit patterns should be directly written by electron-beam and which should be put down with optical masks, notes G. L. "Gil" Varnell, manager of lithography for TI's Semiconductor Research and Development Laboratory in Dallas and chairman of the symposium.

Actually, TI did not mix the two technologies for its initial production run on the SBP-9989E. "We just went with 100% direct-write electron-beam because it was easier to get into quick production, since we had the system ready to go. We also wanted to develop an entire E-beam process first so that we would have the option to go back and do any levels with it," Varnell explains.

TI maintains that its 16-bit military microprocessor is the first production IC fully fabricated by direct-writing techniques. But the distinction will become history reasonably soon. To pare production costs, Varnell reports that the company will change the processing of the 16-bit part within the next six months or thereabouts to use optics for certain levels.

Good mixer. Richard D. Moore, manager for electron-beam systems development at IBM's General Technology division, sees several more years ahead for combined electron-beam and optical wafer fabrication.

TI, he says, is working on resists and etching processes that will be compatible with both technologies. "Also, once you have chip-by-chip alignment and automatic distribution control, then you've done the tricky part of combining the two," he adds. The change will not force any trade off in pattern-feature size to win the cost advantage. In fact, the firm plans to shrink the minimum line width—currently 1.25 μm—to the 1-μm level next year and will do it with the combined technique.

Still mixing. IBM unveiled its third-generation, EL-3 system at the symposium, a fast-stepping machine that can write lines as fine as 1 μm on as many as 20 wafers an hour. Although IBM now has an EL-3 at its quick-turnaround facility and three older electron-beam machines as well, the company will hew to the combined approach for several years more because of its cost advantages, says Richard D. Moore, manager of electron-beam system development at East Fishkill.

"Let's say that you have a 1-micron product," Moore suggests. "It may take 15 masking levels to make the product, and it may have only five levels that actually use 1-micron features. The rest may have much coarser edges. So even with 1-micron products you can get by with more than half of the levels written by optical techniques."

"I think as you go beyond the 1-micron level," he continues, "a

higher percentage of the levels will be done with direct-write E-beam. In the immediate future, we are looking at about 30% to 40% of the patterns being scribed with E-beams and the rest being done optically."

Production

Fast E-beam machine writes 0.5-μm lines

For the moment, executives at companies whose bread-and-butter business is production lithography equipment for integrated-circuit makers needn't stock up on worry beads. Hewlett-Packard's new electron-beam machine, which can write patterns with sub-micrometer line widths at speeds fast enough for production, won't explode into the market for a long time to come, if ever.

But if and when it does, it will make possible a quantum step ahead in complexities for ICs compared to what can be done with commercially available equipment. Using a modified raster scan, the new instrument [*Electronics*, June 2, p. 33] from the Palo Alto, Calif., company obtains registration accuracies between 0.1 and 0.2 μm, all the while controlling the 600-nanoampere writing beam at data rates up to 300 megahertz.

That works out to a throughput fast enough to process five wafers an hour containing chips that could have as many as 1,350,000 transistors each. Optical aligners cannot work on geometries this fine, nor can they match the throughput in functions per hour, HP maintains.

For the modified raster scan, HP uses a mechanical X-Y table to shift from one 5-by-5-millimeter field to the next. Each field is split up into blocks, each consisting of 128 by 128 picture elements exposed by raster scan. The size of the pixel is determined by the pattern-grid spacing, but in half-micrometer geometry, up to 10^8 pixels may be placed in one field of view.

The machine can be used for the production of 10-up reticle masks, which need about 10^{10} bits of pattern memory, as well as for scribing lines on wafers. Since the time needed to load the memory is long, compared to the exposure time for one field of view, HP turned to data-compression techniques to fit in all the data for a reticle mask without increasing the memory size.

Much memory. The major components of the electron-beam system consist of an electron column, a target area with a semiautomatic cassette-loading system and the X-Y stage, a computer control system, and a special-purpose beam drive. The main system computer is an HP 1000, but the pattern memory is controlled by a much faster special computer called HAL. Based on emitter-coupled logic, it draws upon 20 megabytes of random-access memory in the system pattern memory.

In the electron beam column itself, both quadrupole and octopole deflectors are used. Beyond the first beam-focusing lens is a stigmating system that corrects beam astigmatism electronically, since the tolerances required are beyond the machining tolerances of the column.

Below the astigmatic system is the crucial beam blanker stage, which intensity-modulates the beam during the raster scan. To do so, the beam is focused within a few micrometers of a metallic knife edge. When a small potential is applied to the blanker, the beam is deflected a few micrometers into the metallic edge. Because of the small deflection required, only 3 volts is required to provide the necessary blanking.

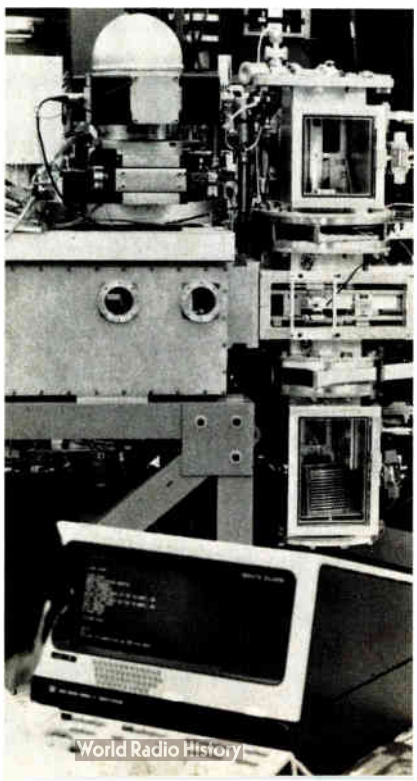
Following the final lens is the deflector system, in which a quadrupole deflector is used to raster-scan the beam over a 128-by-128-pixel area. A second deflector, an octopole, is used to position the beam at the center of the 128-pixel-squared subfield.

The system also has a novel way of coping with a major obstacle for electron-beam systems, the proximity effect. It results in unwanted exposure of the resist because of electron scattering in the resist layer and from the substrate underneath.

Previous electron-beam systems have tried to correct for the effect by preprocessing the input data and modifying the dose at exposure time. HP chooses instead to use chemical techniques that involve special processing of multilayer resists as well as a small beam.

HP described the new machine in four papers presented at the 16th Symposium on Electron, Ion, and Photon Beam Technology. The conference was held late last month in Dallas. **-Martin Marshall**

Fast and fine. Hewlett-Packard's prototype electron-beam machine can scribe five wafers an hour with lines for chips having over a million transistors.



Military

Academics fret over VHSIC controls

A twinge of anxiety about academic freedoms is coursing through the universities participating in the Defense Department's Very High-Speed Integrated Circuit (VHSIC) program. DOD has expressed a preference that foreign nationals not work on the program and insists it be notified when they do. Academic leaders say the restrictions could be unfair both to students and schools.

Larry W. Sumney, the Defense Department VHSIC project director, admits there is concern in academe about the restrictions. But at the Institute of Electrical and Electronics Engineers' Fourth Biennial University/Government/Industry Microelectronics Symposium held late in May at Mississippi State University, Starkville, Miss., Sumney insisted the concern "has been blown out of proportion."

His office, he explained, makes a distinction between basic research and specific technologies for VHSIC in applying the restrictions mandated by Congress in the International Traffic in Arms Regulations (ITAR).

Under control. Aimed at controlling the flow of export technology to all foreign countries except Canada, the technical data governed by ITAR does not include information related to materials properties, physical and chemical reactions, fundamental physical limitations, stress analysis, device physics, and similar results of basic research, he pointed out.

But information not generally made public—control parameters of processes, temperature and gas-flow profiles, and the like—is controlled; it cannot be freely published or transmitted to foreign nationals. Potential conflicts in the gray area between basic science and technological process data, he says, will be reviewed case by case.

In phase. Meanwhile, Sumney's office has geared up for the first annual VHSIC contractors' meeting, scheduled for mid-June in Washington, D. C. All the Phase 3 contracts, which focus on support technologies rather than the development of actual devices and brassboards (as do the Phase 1 contracts and the Phase 2 work that will follow) come up for renewal this summer. The upcoming meeting will review the half-dozen contracts awarded last month as well [*Electronics*, May 19, p. 40].

Large companies dominate the Phase 3 lineup of 50 contracts worth $30.6 million, but there are six universities and two university-affiliated research institutes involved as well. Sumney indicates that "for the most part, we've decided to go ahead with all of the existing contracts." He states that an additional 15 or so unsolicited proposals are currently under review but that at present no decision can be made on them "until we have straightened out congressional funding." **-J. Robert Lineback**

Assessing the impact of VHSIC on industry

The Defense Department's very high-speed integrated-circuit (VHSIC) program will accelerate technological advances in military electronics by two to three years, reports a nine-month study by the Analytic Science Corp., Arlington, Va. The study, which involved 11 firms, 17 individuals, 2 industry associations, and 6 outside experts, forecasts the likelihood of much less impact on nonmilitary electronics by the program "because it does not generate large transfers of resources from other markets to the military market, nor are the probabilities high that it will generate independent process, product or organizational outputs likely to have a major effect on other markets."

David H. Moore, an ASC economist and coauthor of the report, says merchant semiconductor houses, where commercial research is already under way on many of the VHSIC goals to shrink integrated-circuit feature sizes and develop new processing technologies, generally expect little impact. But that is not to say that the program is being viewed as missing its mark, says Moore. He notes that VHSIC is aimed at only the military segment and is not intended to be industrial policy or to aid firms competing with foreign manufacturers.

"The general consensus is at VHSIC will indeed accelerate military electronics development—such as advanced integrated circuits, software and systems—so that it will be on the same level or even ahead of the commercial segment of the industry," Moore states. Only if VHSIC were to come up with a revolutionary design in architecture, software, or testing would it bring about a significant change in the pace of commercial innovation, he adds. And he concludes, "the limited industry impact of VHSIC will also result in the program's success." ASC released results of its report at the Institute of Electrical and Electronics Engineers' University/Government/Industry Microelectronics Symposium held at Mississippi State University, Starkville, Miss., last month. **-J. Robert Lineback**

Photovoltaics

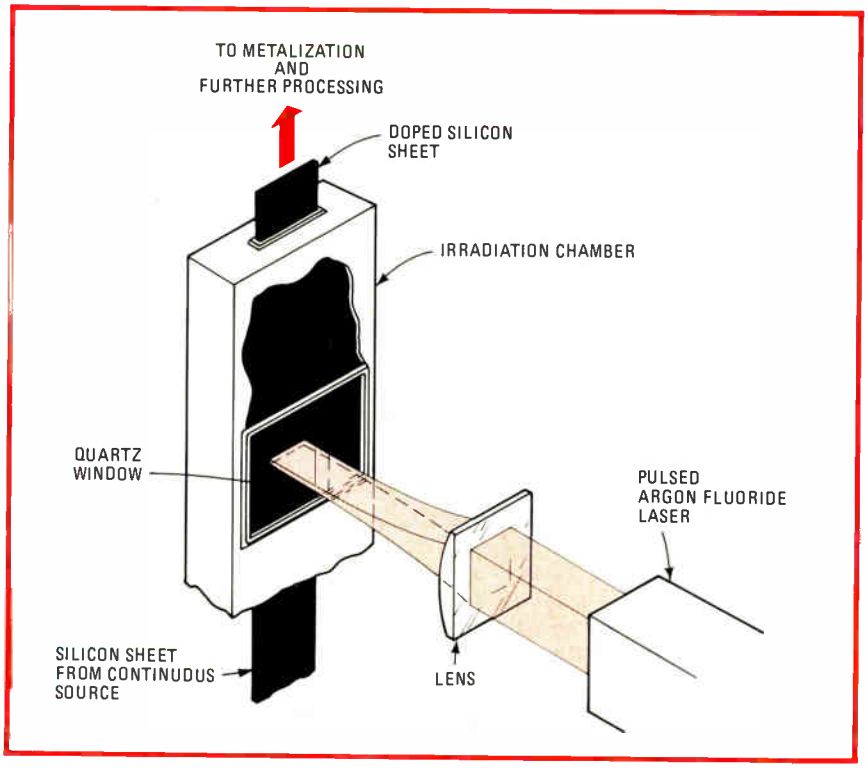
Laser pulses create junctions in silicon-ribbon solar cells

Zapping silicon substrates with pulsed beams from an ultraviolet laser may light the way to low-cost solar cells. Researchers at the Massachusetts Institute of Technology's Lincoln Laboratory have proved out the basic technique, which creates pn junctions in a single pass instead of the two or more steps needed for conventional doping processes.

What's more, the technique seems admirably suited to continuous processing of silicon ribbons or sheets, themselves potential low-cost substrates for solar cells. The prospects are so promising that already the technique has evoked industrial interest, even though it must undergo the pangs of development before anyone could put it into production.

At the Lexington, Mass., laboratory, boron-doped solar cells measuring 0.5 by 1.0 centimeter have been fabricated using a pulsed argon fluoride excimer (excited dimer) laser. In such a laser, each gas molecule has two atoms, only one of which is in a higher-energy state.

The experimental cells show efficiencies of up to 10.3% without an antireflective coating, reports Thomas F. Deutsch, a member of the Lin-



Light touch. Photovoltaic pn junctions form in silicon ribbons when they are irradiated inside a gas-filled chamber by laser pulses. The one-step process comes from MIT.

coln Lab team. He estimates that such a coating would boost the efficiency to a more respectable 13% or thereabouts.

Doing the one-step. The processing concept is straightforward. Light pulses at a 193-nanometer wavelength from the excimer laser are focused on a substrate inside an irradiation chamber filled with boron trichloride gas, breaking the molecular bonds of the gas and freeing dopant atoms. At the same time, the laser beam melts the substrate surface locally and the free atoms diffuse into it, forming a pn junction between 0.3 and 0.4 micrometer below the surface.

Because the silicon absorbs the ultraviolet light only to a depth of some 100 angstroms and because the pulse duration is only 7 nanoseconds, melting takes place only to a depth of about 1 μm, explains Deutsch. Thus there is no need to encapsulate the rear surface of the substrate to protect it against unwanted diffusion, a processing step needed for conventional diffusion methods. And because the process is one of diffusion rather than ion implantation, there is no crystal-lattice damage that would necessitate a thermal annealing step.

Getting to the floor. At least one solar-cell maker is getting ready to pursue the initial work done at Lincoln Lab. "There's a big gap between the laboratory and the production floor, but if this approach can make the leap, it will be a beautiful technology—probably even better than ion implantation," asserts K. V. Ravi, general manager of production and development at Mobil-Tyco Solar Energy Corp. His Waltham, Mass., firm, whose work on silicon-ribbon technology is part of the Department of Energy's Low-Cost Solar Array (LSA) project [*Electronics*, July 19, 1979, p. 108] plans to devote "substantial research and development money" for in-house exploration of the technique.

Lincoln Lab's Deutsch believes the technique can easily scale up to large production operations by shifting to a more powerful laser that permits very fast pulse-repetition rates and by increasing the area of the focused laser beam on the substrate. He projects that, for continuous doping, a 100-watt argon fluoride laser operating at a pulse-repetition rate of about 150 hertz would be able to process a 7.5-cm-wide sheet of silicon at about 20 cm per minute (see figure). As part of the process, Deutsch adds, individual cells could be delineated by periodically interrupting the laser beams.

One drawback for production-scale use of the technique is the cost of the laser source itself, Deutsch admits. A 100-watt argon fluoride laser today remains a research tool, since it costs several hundred thousand dollars—about the same as commercially available ion-implantation systems cost. Lower-cost production versions of high-power lasers would make the process more attractive. Deutsch adds that other costs—notably for the energy to operate the excimer laser and for the doping gas—will be negligible compared to the overall cost of solar cell fabrication. **-Linda Lowe**

Software

DEC promotes cable TV packages

Digital Equipment Corp. has registered the messages from the media and, having done so, has positioned itself to become a major supplier of distributed processing systems to the booming cable-television industry.

The Maynard, Mass., minicomputer pioneer decided to tune in to CATV last year, when it began to see saturation in the slow-growing newspaper business, an important vertical market segment for DEC. The decision followed a nine-month study aimed at finding a fast-growing medium where it could exploit its newspaper-management expertise. CATV, the firm is convinced, will in the future provide newspaper and other information services as well as entertainment and, what's more, appears to be ripe for computerization. "Cable management has focused on the outside, and now it

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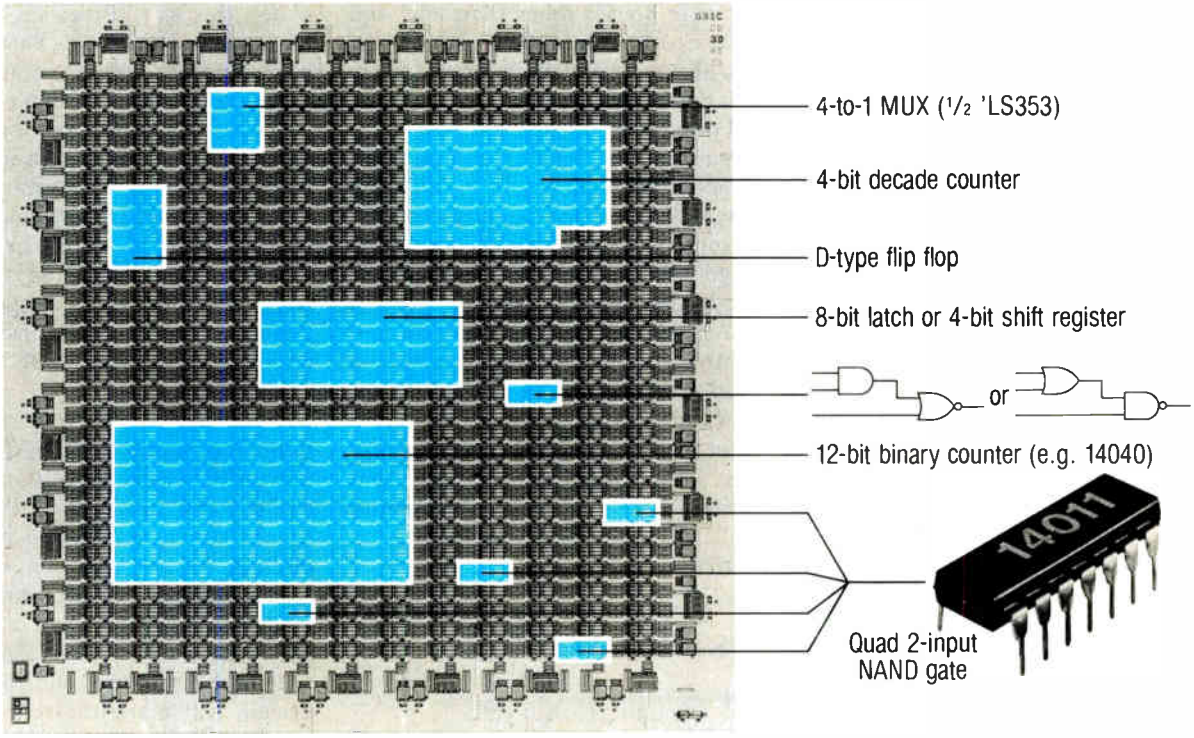

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must look inside," says Joseph W. Ford, the company's graphic arts product line manager.

Software first. DEC is not coming out with any hardware as it begins its CATV thrust, but it has made a strong start on the software. At the National Cable-Television Association's annual convention held in Los Angeles late last month, where 14,000 cable operators and their equipment suppliers showed up, DEC announced that it will market software packages developed for cable-TV operators by Business Controls Corp. (BCC) of Elmwood Park, N. J., and Applied Data Research Inc., (ADR) of Princeton, N. J.

BCC's new package, CABS-1, is an $85,000 turnkey Cobol system that offers as an option a Cobol program generator for cable-TV operators who need to customize the basic software. Fees for ADR's Basic-language package, Cadre, start at $150,000 and can go as high as $500,000. The software from both firms utilizes interactive file handling to manage such tasks as work-order processing and complaint calls. Program segments for billing and accounts receivable are designed to handle complicated charges for customers who subscribe to the many different services offered.

DEC itself has not yet written any software for the cable-TV industry, but Ford says that some of the firm's newspaper subscription packages could be adapted to the cable environment. Along with in-house developments, packages from independent software houses other than BCC and ADR are possible, Ford adds. DEC has also started talks with multisystem cable operators.

Ford hopes the preliminary conversations will lead to a multiyear project that will result in software that will make for ready communications between cable-TV operators, large and small. As an executive at one of the big cable networks puts it, "In trying to run your business and control the cable environment, you need tremendous support from the [data-processing system] manufacturer. DEC is the only company that has moved aggressively into that area." **-Terry Costlow**

Instruments

Tektronix counters Far East competitors with a new line of low-cost oscilloscopes

Many companies want Washington to protect them, so they badger Congress and the Administration for protective barriers like import quotas, higher tariffs, and Orderly Marketing Agreements. But for Tektronix Inc., the defense against market raids by instrument makers from the Far East has been marshaled at Beaverton, Ore., the company's headquarters. Convinced that oscilloscope makers from the Far East will threaten the high-end markets where Tektronix dominates once they gain a beachhead in the United States with low-cost hardware, Tektronix has started to lay down its own interdiction barrage.

This month, the company will introduce its 2200 series of 60-megahertz scopes, with price tags starting at $1,100 for the 2213, which has a single time base with a delay-time accuracy of within 3%. The 2215, with a dual time base and twice the delay-time accuracy, sells for $1,400.

The introduction of the two comes a mere month after that of the 100-MHz 2300 series, the first shot Tektronix fired at foreign low-end competition [*Electronics*, May 5, p. 42]. Along with low-cost hardware, the firm will take a new marketing tack this fall to make it a tougher competitor in low-end markets like television and small-business computer servicing.

The new scopes will make a good part of Tektronix' current low-end products obsolete, forcing the company to drop five models (the T922, T922A, T935, 422, and 455), a painful procedure. But, explains John Gragg, product marketing manager for the firm's Instruments division, the move had to come. He notes that the latest scopes will serve the same world market as the older T921, which was dropped by the company last November.

"It's natural for companies such as Matsushita and Trio-Kenwood [whose scopes are sold in the U. S. under the B&K Precision label] to move in and then up. They already have the high-volume, mass-market experience, and if we don't compete, we'll be in a weak position to hold onto the high end," he observes.

Single board. "Designing a 60-MHz scope that can be sold for just over $1,000 was one of the toughest jobs we've ever done," says the division's engineering manager, Gary Neher. The 13.5-pound instrument's circuitry is packed onto a single 11.5-by-17.3-inch board.

To hold down parts costs, Neher built the scope around Tektronix' most widely used 8-by-10-centimeter cathode-ray tube. With the exception of six custom hybrid integrated circuits, all the parts on the board are standard, mostly small- and medium-scale ICs. That, along with the nearly empty chassis interior that results from the one-board design, will make the scope easy to service, Tektronix asserts. Even more important, the design makes it cheap to manufacture.

The 2200 series models will be among the first produced at the company's new Vancouver, Wash., facility. The assembly will be almost entirely automated.

Added outlets. Tektronix plans to pare sales costs as well. About 85% of 2200 series will be Tektronix' traditional industrial and government customers the first year, Gragg figures. But he also plans to widely penetrate the more disperse market of service operations and will adopt a new marketing approach this fall to do so.

"Based on the results of a blind study conducted last summer," Gragg explains, "we believe we can reach a broad range of potential cus-

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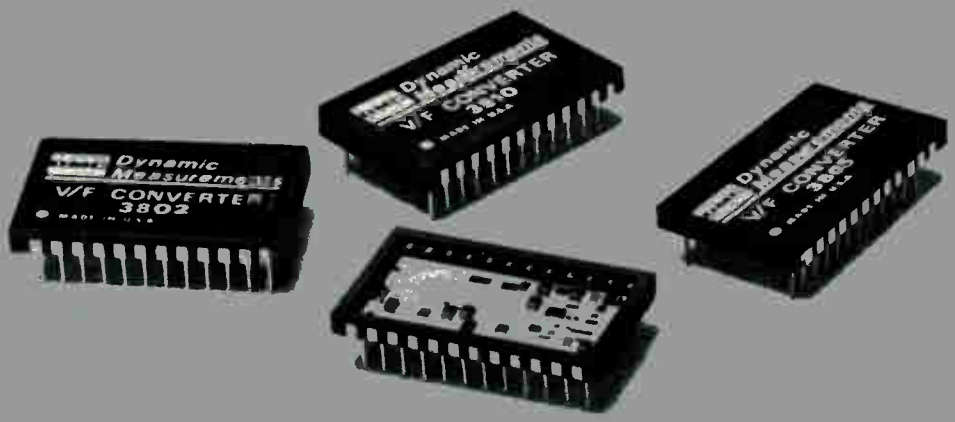

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tomers through direct orders." The study showed that less than 30% of the people contacted actually needed face-to-face contact with a salesman. About 46% of the respondents indicated that they could make a decision to buy based only on literature and ordering information. Another 9% replied that they could decide after only telephone contact.

These approaches to customers, Gragg notes, will cut sales overhead and thus help keep the cost of the new units low. **-Richard W. Comerford**

Consumer

Video peripherals buoy set sales

In a land where 83.5 million color-television sets already glow in 76.3 million households, a surge in set sales would seem well-nigh impossible. Yet set makers active in the U. S. market say a surge is in sight this year. They now expect to sell 11 million units, which would make 1981 the best color TV year ever.

Replacement sales, obviously, count heavily in a saturated market. But as they sized up the merchandise at the early-June Consumer Electronics Show in Chicago's massive McCormick Place, set makers discovered to their delight that what amounts to a new market for them has started to emerge. Instead of just color sets, they now can count on a range of video peripherals—video cassette recorders, video disk players, monitors for home computers, video games, and projection TV—to keep the market growing. As a result, modular TV, the video analog of component audio high-fidelity equipment, is on the rise. What's more, a market for home satellite receivers has started to take shape among people who cannot get regular TV service.

Projections. Even more impressive than the expected 10% rise for color sets is the one projected for video cassette recorders. They will bound up better than 60% to reach 1,316,000 units this year, in the view of Zenith Radio Corp., Glenview, Ill., a major U. S. marketer of them.

Sales of VCRs, in fact, have outpaced even the most optimistic predictions of a few years ago. And there is no sign that that will taper off. Portable VCRs figure to keep the market heading upward in the short term; after them it will be the turn of video cameras with VCRs incorporated. Three Japanese setmakers—Hitachi Ltd., Matsushita Electric Industrial Co., and Sony Corp.—have already demonstrated them [*Electronics*, Feb. 24, p. 80].

Roll 'em. Micro video cameras with built-in VCRs seem sure to supplant 8-mm home movie equipment. Matsushita's entry records for two hours.

The prospects for projection TV are glowing, too. Sales will more than double this year to reach something like 100,000 units, figures Henry Kloss, a U. S. pioneer in projection TV. There will be another bound, to perhaps 140,000 units, in 1981, he thinks.

Kloss, who launched the consumer market for projection TV in 1967 when he formed Advent Corp., Cambridge, Mass. to produce and sell the new hardware, now heads Kloss Video Corp., also in Cambridge. KVC turned up at the show with a $2,495 wide-screen projection monitor. Since there is a tuner built into every video cassette recorder, Kloss explains, VCR owners can plug in the monitor and save some $600 to $1,500.

That projects Kloss into modular TV, where tuner, monitor, and sound are split up much as they are in hi-fi audio, bringing to video the same add-on capability that exists in audio. Kloss is not the first, though, to exploit the concept. At the show, Japan's Sony Corp. showed its Profeel component-TV hardware for the first time in the U. S. The line includes a separate monitor, tuner, and speaker system. Anticipating the advent of stereo sound on TV, there are two audio amplifiers in the monitor unit. Sony reports that a full 25% of its sales in Japan comes from Profeel hardware (there is a choice of either 25-inch or 19-in. Trinitron monitors, with multiple video and audio inputs and output). Sales in the U. S. will start this fall; Sony has yet to set prices.

Looking up. The ultimate in modular TV at the moment, though, is a parabolic dish antenna for pirate reception of unscrambled satellite-transmission feeds to cable-TV operators. Fourteen such dishes from 10 to 16 feet in diameter were lined up outside the Chicago exhibit hall. There are "more than 10,000 in the U. S." says Larry W. James, director of marketing for SatFinder Systems, a Tulsa, Okla., earth-station manufacturer.

The owners, he explains are "everyone from dirt farmers to millionaires," especially people who cannot

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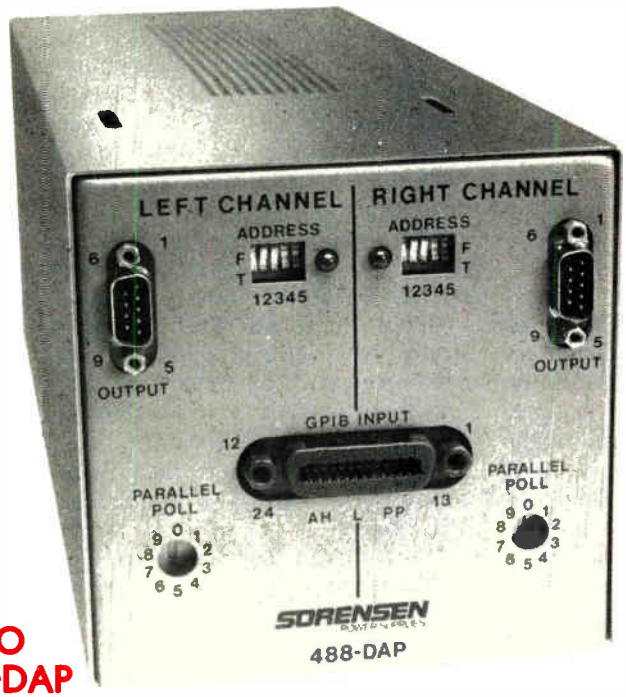

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get regular broadcasts or a commercial cable feed. Since they are picked off the air, there is no charge for the programs—first-run movies, live sports events, and even Russian TV. But to get them, it is necessary to spend some $10,000 for the dish and the associated electronics for 3.7-to-4.2-gigahertz reception. (See related story, p. 100). **-Gil Bassak**

Packaging

Copper plus Invar suits chip-carriers

Leadless chip-carriers hold high promise as a way to mount very large-scale integrated circuits on printed-circuit boards. But they present a problem. The ceramic of the carrier has a lower coefficient of thermal expansion than commonly used pc substrate materials, and as the boards heat up and cool down, the differing expansions tend to fracture the solder joints between carrier and board, especially on big boards.

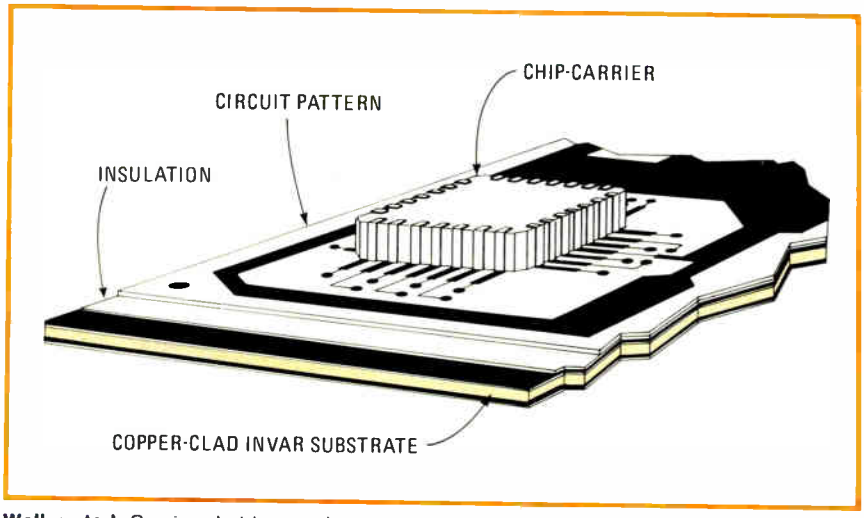
An obvious solution is a substrate sandwich having an expansion coefficient that matches that of the chip-carrier ceramic. The latest such sandwich comes from Texas Instruments Inc.'s Metallurgical Materials division in Attleboro, Mass. It has a core of Invar, a low-expansion alloy based on nickel, clad on both sides with copper (see figure). The thermal expansion coefficient is 6×10^{-6} inch/inch per °C, which just about matches that of alumina and thus makes a pc-board material suitable for large arrays of chip-carriers.

First out. TI has started supplying samples of its sandwich material, making it the first actually available on the market. However, the company faces competition from the PCK Technology division of Kollmorgen Corp., Melville, N. Y., which has a metal-backed Multiwire board under development [*Electronics*, Feb. 10, p. 44]. Also, in Denver, Bell Laboratories is investigating metal-backed boards [Electronics, Jan. 13, p. 48].

TI can fabricate the new substrates, which are produced by roll bonding, anywhere from 4 to 100 mils thick, in sheets as wide as 24 in., with no practical limitation on length. The most-used thicknesses will run between 25 and 50 mils, the firm expects.

Worth it. As for cost, TI has not set firm prices but admits that the metal substrate material will cost twice as much as glass-epoxy or more. However, the premium should not seem prohibitive to designers of densely packed chip-carrier arrays when the dimensional stability and high heat dissipation of the new substrate are essential.

To turn the substrates into finished boards, users can coat them with an insulating layer of epoxy, bond on a flexible circuit, or bond on a thin sheet of epoxy-glass. The insulation layer also serves as a medium for printed wiring. Ground planes, obviously, are already there. The material can be drilled, punched, or bent. **-Jerry Lyman**



Well mated. Copper-clad Invar substrates match the thermal expansion of alumina so well that dense arrays of ceramic leadless chip-carriers can be mounted on large pc boards.

Electro-optics

Pyroelectric array images by night

Manufacturers of thermal imaging equipment for the armed forces, with good reason, traditionally have striven for high performance more than anything else. For their martial customers, the ability to "see" farther and sharper in the dark than the enemy overrides considerations of costs.

As a result, what might be a significant market has been left largely untapped. In the view of Shigesato Iwasa, supervisor of the charge-coupled-device laboratory at the Electro-Optics Center of Honeywell Inc. in Lexington, Mass., a sizable base of potential applications has been ignored, "the ones in which performance requirements are modest but low cost and reliability are essential." Not surprising, Iwasa's group has been working on a pyroelectric infrared imager that would be suitable for such applications.

"We have demonstrated the nation's first experimental pyroelectric imager in a 10-by-32-element mosaic," he maintains. The all-solid-state device pairs a lithium tantalate pyroelectric sensor array and a silicon CCD multiplexer that takes parallel picture elements and converts them into a serial video data stream. The two are bonded together with indium bump interconnects for minimum heat loss and mounted under a window in a 40-pin dual in-line ceramic package (see photo, p. 48). This makes for a rugged assembly, immune to microphonics.

Unlike the mechanically delicate mercury cadmium telluride detectors used for high-performance military infrared imagers, which need

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Electronics review

cryogenic cooling, Iwasa's pyro imager operates at ambient temperature. Another plus: the response is panchromatic—flat over the spectrum of wavelengths from 1 to 40 micrometers—so little amplitude compensation is needed over the infrared band. The field of view is wide-angle (imager makers thus would call it a "staring" sensor), so that no scanning mirrors and drive motors for them need be incorporated in cameras built around the imager. As a result, cameras are lightweight and reliable, as well as relatively inexpensive.

Above all, Iwasa figures that if funds are made available, commercial versions of a working camera could come by 1983. Such a device would sell for something like a couple of thousand dollars, a far cry from the tens or even hundreds of thousands of dollars that cooled mercury-cadmium-telluride detectors/cameras cost.

On the lookout. Iwasa reports that thermal imaging of people at 20 meters and cars at 200 m with the experimental device showed good minimum resolvable temperature differences that, as expected, depend on what is being looked at. Specific numbers cannot be quoted because of potential security classification, but sharp definition is possible and human figures are clearly resolved.

In the window. A pyroelectric array bonded to a charge-coupled-device multiplexer promises to lower costs of infrared imagers enough to open new kinds of applications.

Perimeter security systems is a possible class of commercial and military applications. "What is needed," Iwasa says, "is a surveillance sensor that produces good infrared imagery on a TV monitor of objects within, say, 200 yards. And it is absolutely essential that the reliability of the camera be high."

Still another class of applications might be in "smart" munitions. Here, the sensor would be the "eye" that guides the munition in the last hundred meters or so before impact. Cost becomes a factor in this case since munitions are expendable and used in quantity. **-Harvey Hindin**

News briefs

Motorola's Stein goes to Arrow

Ending a lengthy search, Arrow Electronics Inc., Greenwich, Conn., has named Alfred J. Stein, 48, as its president and chief executive officer. Stein has been a vice president and assistant general manager for Motorola Inc.'s Semiconductor Group in Phoenix, Ariz. He succeeds the late B. Duke Glenn Jr., who died along with 12 other Arrow executives in a fire at the Stouffer's Inn in White Plains, N. Y., on Dec. 4, 1980. Motorola says no one has been named to replace Stein.

IBM will support plug-compatible mainframes

International Business Machines Corp. has issued a directive to its field service organization that tells it to support plug-compatible mainframe equipment. The company will offer System Installation Productivity Options (SIPOs) and Program Update Tapes (PUTs) to IBM-licensed software customers, regardless of whether that customer is using IBM or plug-compatible hardware. The SIPOs aid in the installation and service of current operating systems and associated program products, and the PUTs are used for periodic updating of software. IBM's previous refusal to make SIPOs and PUTs available has caused a number of companies to file a complaint with the Commission of European Communities in Brussels. One of the firms, National Advanced Systems, Santa Clara, Calif., has dropped its participation in the complaint as a result of this directive.

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National creates the bubble memory system nobody else could.

The industry's biggest news in bubble memory is its smallest subsystem, the 1/4Mbit BLX-9252. It's an ultra small, low power module that is positioned to be the industry standard.

The BLX-9252 is a member of National's new line of BLX (board level expansion) modules.

As a low power (under 5 watts operating) expansion module, it plugs directly into any BLX bus compatible host board to add 32K bytes of non-volatile fast access storage capacity (under 7ms typical).

As a low cost (under $1000* in volume), ultra dense bubble memory subsystem, it's the new cost-effective standard for the industry.

1/4Mbit in eleven square inches. Built onto a 2.8" x 3.7" BLX module, the BLX-9252's 32K bytes can be configured into either 64 byte pages or 256 byte sectors.

The BLX-9252 is designed for use on any of National's BLX bus compatible boards, such as the BLC-86 12B, BLC-80 11A/12A/14A and BLC-80 116.

But for non-BLX bus compatible systems its signals are duplicated into a standard 50-pin PC card edge connector. This offers maximum on-board performance and frees the host's bus traffic for other resources.

The subsystem's subsystems. The BLX-9252 incorporates an NBM2256 bubble memory, timed and driven by the NBC82851 bubble memory controller.

The system software communicates with the BLX-9252 across the BLX interface with I/O read/write commands to the controller's eight user accessable registers.

Additionally, data transfer can take place in polled or interrupt driven modes. Alternately, the BLX-9252 can act as a channel to a DMA controller on the host board.

Reliable error detection and correction. Its data reliability is reinforced with a 12 bit Fire Code that will detect up to three random errors or an error burst up to 12 bits in length.

In turn, it will correct any error burst up to three bits in length.

The bottom line however, is that the BLX-9252 is the most dense and cost-effective bubble memory subsystem available today.

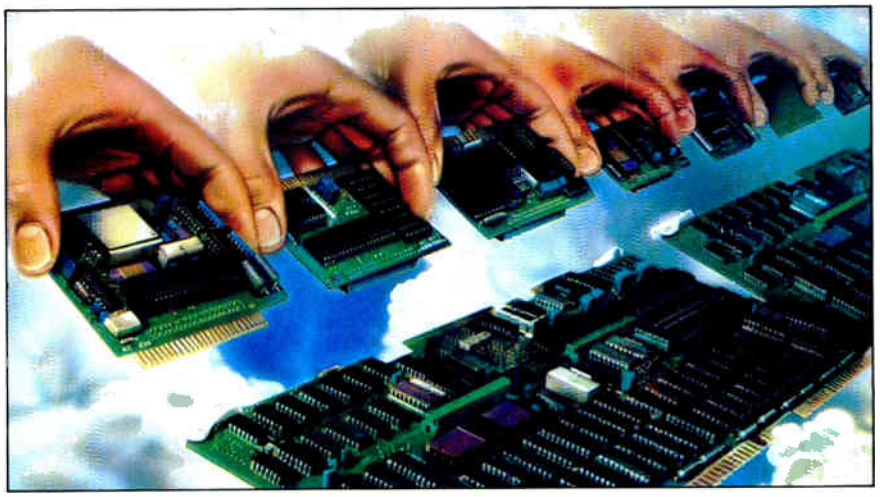
For data sheets and application notes on the BLX-9252, check box number 086 on the National Anthem coupon.

And start saving space, power and money on memories from National.

*U.S. prices only

BLX modules create expanding board level versatility.

National puts the industry's broadest line of semiconductors on modules for Multibus™ board level expansion.



It's the BLX solution—National's low cost board level expansion for BLC users that the competition can't even begin to match. And it brings total versatility to SuperChips™ board system designs. Cost-and space-saving configurations are now just a matter of choosing which modules provide the best approach.

On-board expansion is accomplished by plugging any of National's BLX modules directly into sockets on their BLX-compatible host boards. Each of the BLC-80/11A, BLC-86/12B and BLC-80/116 host boards can accept any two expansion modules.

At present, modules are available to expand board level capabilities with speech synthesis, analog output, fixed or floating point math, parallel I/O, serial I/O, bubble memory and prototyping.

Soon, however, the growing BLX line will expand to cover National's entire line of semiconductors—the industry's broadest.

National's established manufacturing capabilities and technical innovation make them the logical choice for board level leadership from the chip up—with a full 12-month warranty.

For example, everyone has boards that compute and remember. There's no trick to that. But National has boards that translate (BLC-8488 Intelligent GPIB Controller), talk (BLX-281 Speech Synthesis Module) and measure (BLC-8737 & BLC-8715 Analog I/O Boards). The fact is, no one else can touch them in board technology.

Modules and SuperChips. Because man cannot live by chips alone.

For more information, just check box 088 on this Anthem's coupon.

SuperChip is a trademark of National Semiconductor Corporation.
Multibus is a trademark of Intel Corporation.

High performance PCM filter gets digital telecom systems off hold.

The TP3040 is pin and function interchangeable with the 2912 and 2912A with significant performance advantages.

National's new TP3040 PCM filter is a lot more than just a pin-for-pin, function-for-function replacement for the industry standard 2912.

The TP3040 surpasses both the 2912 and the 2912A filters with low power, noise, crosstalk and better low frequency rejection. So it brings new levels of cost-efficiency and performance to telecom applications.

Plus its unique monolithic design incorporates pre- and post-filtering in both the transmit and receive sides.

The TP3040 offers clear performance advantages over its pin-compatible counterparts, particularly in terms of power consumption. The TP3040 uses up to 85% less power than the competition.

This kind of performance is a direct result of NSC's innovative double-poly silicon gate P²CMOS technology. National brought together the most advanced fabrication techniques to perfect P²CMOS. It will allow them to create an entire line of problem-solving devices for the telecom marketplace.

The Practical Wizards are already turning TP3040s out in high volume. So now telecom design engineers can get their switching systems off hold with a truly superior 2912 and 2912A replacement filter from National Semiconductor.

For complete details on the TP3040, check box number 089 on this issue's National Archives coupon.

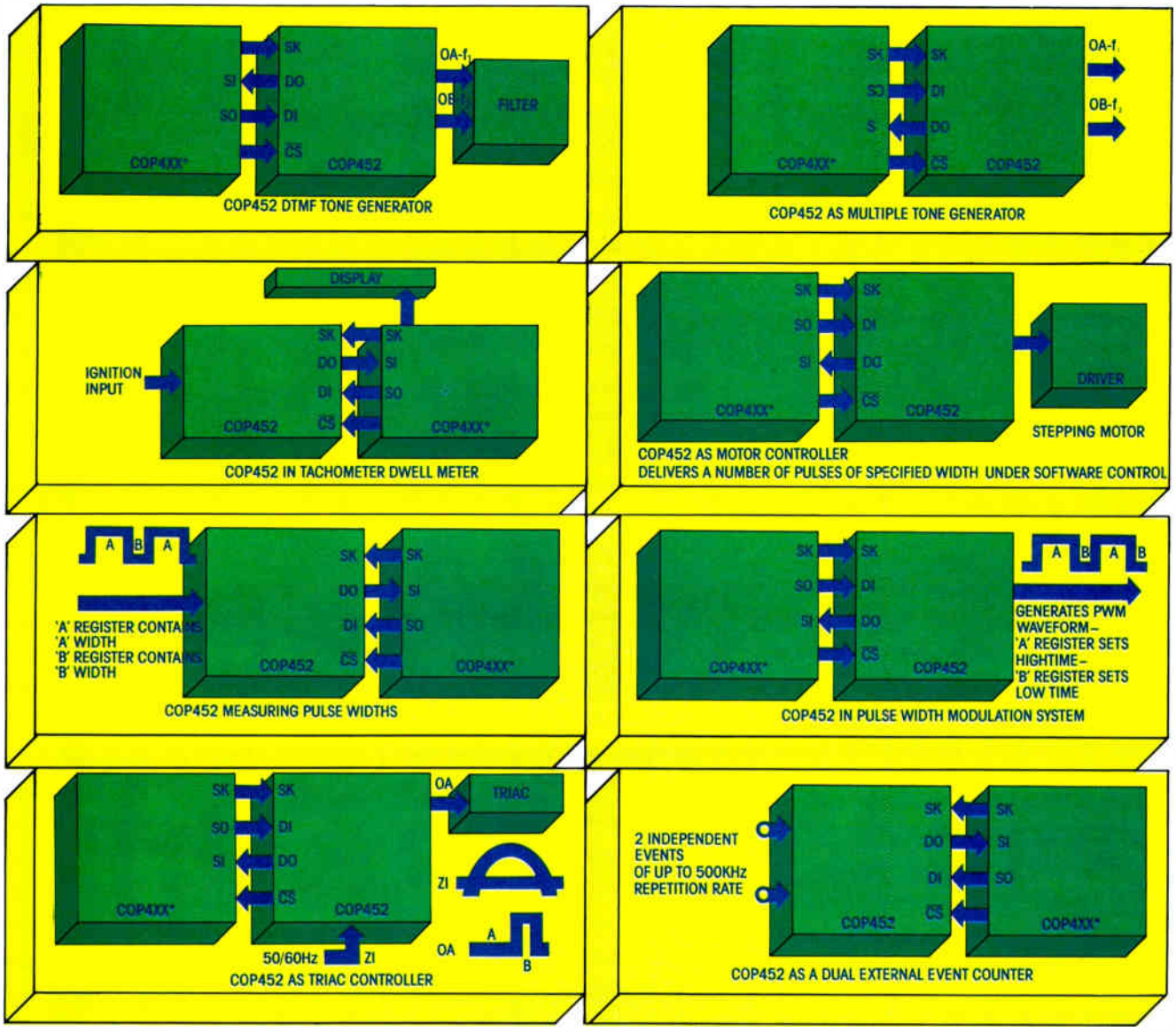
PCM FILTER COMPARISON TABLE

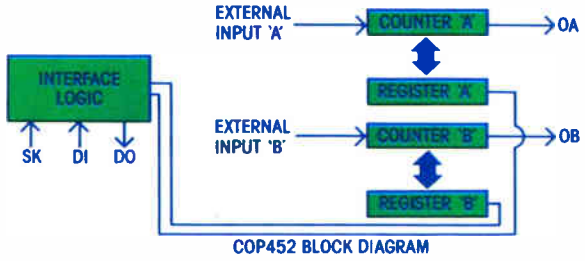
	2912		2912A		TP3040	
	Typ	Max	Typ	Max	Typ	Max
Power Consumption						
With power amps (mW)	280	440	80	N/A*	46	64
Without power amps (mW)	210	340	50	N/A*	30	40
Power down mode (mW)	55	90	0.4	N/A*	0.5	1.0
Idle Channel Noise						
Receive (dBrnC0)	9	12	3	N/A*	2.5	5
Transmit (dBrnC0)	10	13	9	N/A*	2.5	6
Crosstalk						
(dB; over 200-3400 Hz range)	N/A*	N/A*	N/A*	N/A*	−80	−70

*Data Unavailable

Eight more ways to use a COPS™ peripheral that a microcontroller can count on.

The COP452 time machine frees processors of most time-dependent tasks. With multiple tones, precise duty cycles, event counting, waveform measurement, "white noise" generation, and A/D–D/A conversions, it produces a wide variety of well-timed events.





COP452 BLOCK DIAGRAM

*Any COPS Microcontroller

For additional information on the COP452 check box 087 on this Anthem's coupon.

The low cost, easy-to-use development system for COPS™ microcontrollers.

It's the COP400-PDS, with a host of features for microcontroller software and hardware development.

The COP400-PDS product development system is the most cost-effective way to edit, assemble and debug hardware and software for COPS microcontrollers.

The COP (Controller Oriented Processor) family is National's complete line of single-chip microcontrollers. Each contains all the necessary system timing, internal logic, ROM, RAM and I/O to implement dedicated control functions in a variety of applications.

Disk storage eases the effort. The user interacts with the COP400 via a front panel keypad or an optional CRT and printer. Programs are edited and stored on the COP400's floppy disk.

Disk storage allows users to perform edit-assemble-test cycles much easier than on paper tape systems. And it's the most convenient means of providing National with the program data necessary for the mask-making process.

An important feature of the COP400-PDS is its debugging capability. It enables users to single step through a program, breakpoint to an address, trace program execution and dump out internal COP400 registers. The ability to execute these types of commands significantly reduces development time.

An emulator card attachment allows the execution of object code under the system's control. And an additional QUIKLOOK™ test module provides GO, NO GO inspection testing of incoming COPS devices.

This is, after all, National's way of providing an integrated concept support for their line of COPS microcontrollers.

For more information on the COP400-PDS and QUIKLOOK tester check box number 070 on the National Archives coupon.

COPS and QUIKLOOK are trademarks of the National Semiconductor Corporation.

STARPLEX II™ is fluent in PASCAL, PL/M, BASIC, FORTRAN and ordinary English.

National's highly interactive, easy to use development system now supports high level languages and speeds the overall development effort.

STARPLEX II is the perfect system for designers developing systems using high level languages. It incorporates full compilers for both PL/M and PASCAL with code generators for the 8080/8085 and NSC800/Z80.

BASIC and FORTRAN also come standard on STARPLEX II.

New features speed development. The new STARPLEX II has enhanced features designed in for high throughput and vast performance improvements. With its high level language support and 128K bytes of RAM, STARPLEX II offers an increase of performance up to three times that of STARPLEX.

The man/machine interface is greatly simplified by using menus to access desired software modules. Plus, a complete on-line library of the system's operating commands and procedures is maintained for instantaneous referencing. And it's all in plain, ordinary English.

STARPLEX II features two Z-80A processors in a master/slave configuration. Its operating system and user programs are segregated to offer system integrity not offered in any other development system.

Its slave processor has its own 64K bytes of RAM dedicated to user programs while the system incorporates 128K bytes of total RAM.

With its easy to use, time saving features, STARPLEX II becomes the logical choice for system developers of all of National's programmable devices, including processors, boards, PROMs, PALs and bubble memory.

STARPLEX II offers support for National's own BLMX real-time operating systems and the industry standard CP/M operating systems.

Also, a spooled printer capability allows a decrease in development time by allowing users to print out on-screen information, from file listing to compiler output.

User definable function keys (16 total) allow new versatility in both command mode and application runs on the system.

ISE™ has microprocessor emulation down cold. With ISE, engineers can now develop, test, analyze and debug prototype software/hardware for 8080, INS8048, INS8049, INS8050, INS8070 family μPs, Z-80, COPS™ microcontrollers, NSC800 and 8085 microprocessors plus National's Series/80 board level computers.

ISE's powerful debugging capability allows simultaneous software and hardware debugging of single or multiple processors for faster, more efficient system integration.

And since the symbol table is available during emulation, the same symbols are used in debugging that are used in writing the program being examined.

STARPLEX's symbolic debugging capability provides not only the usual breakpoint conditions, but also a "coast" command which allows you to continue executing a program after the breakpoint combination has been satisfied.

Also, with ISE's in-line assembler and disassembler, programmers can modify object code and display it in assembly language without having to leave the debug and emulation environment. And without editing and re-assembly of the entire source program, thus eliminating many tedious manual steps.

National's easy-to-learn ISE software comes completely integrated into the STARPLEX II system, including the unique Automatic Testing mode called "In File." In-File implements a predefined sequence of tests based on user-selected system and emulation commands. ISE can also record those results to show exactly how each part of the system performs during the tests.

STARPLEX II means a more powerful STARPLEX. Since STARPLEX II support packages are upward compatible with those of STARPLEX, it's a simple procedure to upgrade the original version.

For this purpose, National offers a special kit consisting of two master/slave CPU boards, the new keyboard with user definable keys, and the new STARPLEX II operating system.

All STARPLEX peripherals and options—including ISE modules—also remain compatible with STARPLEX II.

To get the full story on STARPLEX II and its fully developed capabilities, check box 037 on this Anthem's coupon. And hear about a major development in efficiency.

STARPLEX, STARPLEX II and ISE are trademarks of National Semiconductor Corporation

National conquers space with Megarad CMOS logic.

Presenting the industry's broadest line of metal gate CMOS devices capable of withstanding radiation levels in excess of 10^6 rads (Si).

Military and aerospace design engineers have long needed a dependable source of low power radiation-hardened logic devices. Bipolar components were radiation resistant, but required current supplies of several milliamps per gate. And although traditional CMOS operated at microamps per gate, they began to degrade at radiation levels well below 10^4 rads (Si).

But the Practical Wizards solved these problems with a full line of megarad hardened CMOS logic and memory circuits. In fact, National's intensive two-year research and development program has resulted in the industry's broadest line of metal gate CMOS products hardened to 10^6 rads (Si).*

So they're ideal for use in satellites and similarly demanding Mil/Aero applications.

The CMOS megarad line consists of devices ranging in complexity from simple gates to flip-flops to RAMs, all available with 883S/RETS™ or 883B/RETS™ processing.

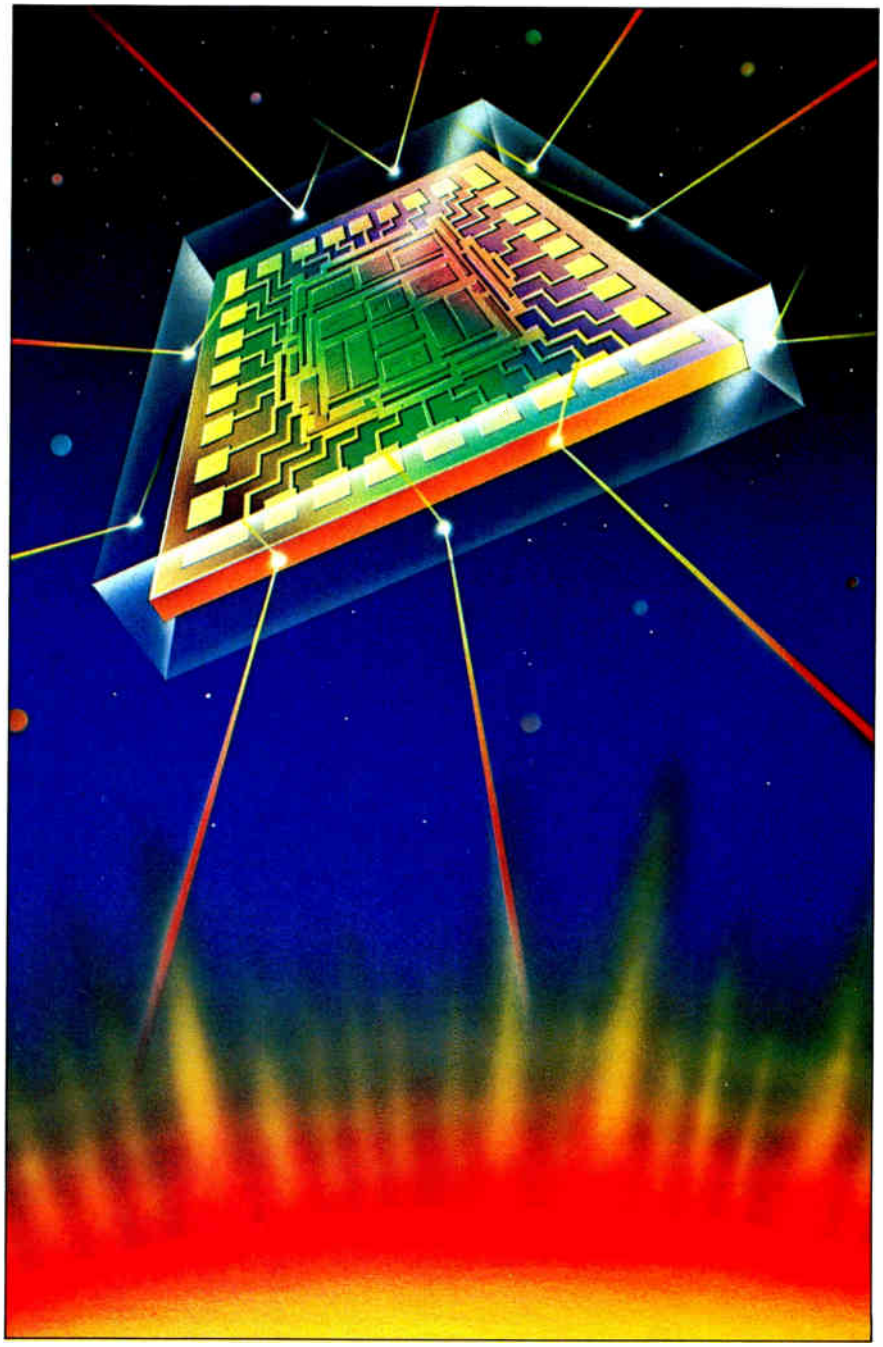
What does rad hard really mean? National has insured the radiation tolerance of their rad hard devices through several methods.

The radiation-induced oxide charge and the formation of $Si\text{-}SiO_2$ interface states were minimized by converting from a wet to a dry oxidation process, with the gate oxide thermally grown in a pure oxygen atmosphere rather than in steam.

This gate oxidation is processed through a nitrogen annealling cycle, thus producing oxides highly resistant to ionizing radiation effects as well as having excellent pre-radiation MOS characteristics.

Since the E-beam aluminum evaporation process normally used on commercial CMOS ICs emits a soft X-radiation—which produces positive charge threshold shifts in the gate oxide and interface states similar to those seen during radiation—National uses induction heated evaporation of the aluminum rather than E-beam aluminum evaporation.

To minimize the effect of threshold voltage shifts, the Practical Wizards significantly raised the negative threshold voltage and brought the positive threshold voltage closer to zero. This was accomplished with absolutely no sacrifice in performance, even on such complex components as the MM54C200 256-bit RAM.



Megarad for maxisystems. The result of all this Practical Wizardry is the industry's broadest line of reliable and readily available CMOS logic and memory devices capable of withstanding the rigors of a radiation-filled environment.

For more on National's rad hardened line of CMOS devices, check boxes 062 and 079 in this Anthem's coupon.

*One rad (Si) is the quantity of any type of ionizing radiation which imparts 100 ergs of energy per gram of silicon.

Six tricks with low-cost 8-bit A/Ds.

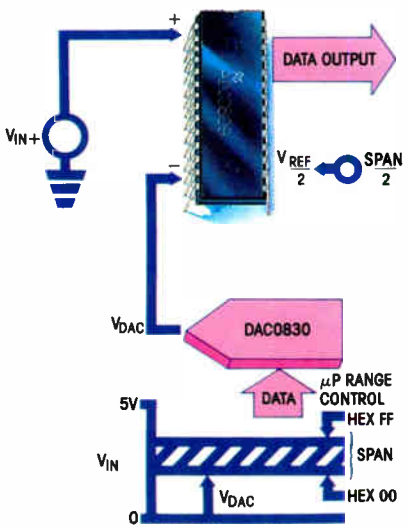
National Semiconductor's line of 8-bit A/D converters with differential input and span adjust—the ADC0801/02/03/04—are finding their way into all sorts of interesting applications. Here are just a few to stimulate the imagination.

1. Analog Self-Testing. More and more digital systems perform a self-test. To take this concept one step further, NSC's low-cost 8-bit A/Ds can be used to encode the analog voltages in a system—power supply voltages, comparator set points, reference voltages, etc.

This way, the microprocessor can ensure that all of the components are operating properly.

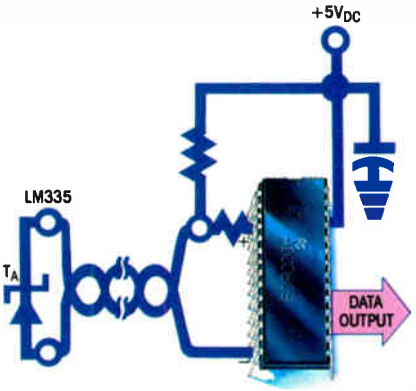
2. A μP-Compatible Comparator. Need a comparator that interfaces directly with the data bus? The differential input on the A/Ds allows the comparison of the input signal to a reference voltage.

3. High Resolution μP Ranging A/D



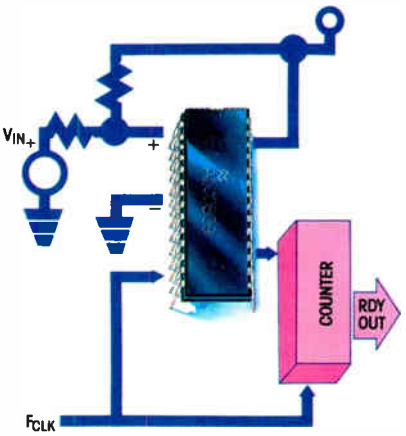
By increasing the apparent sensitivity of the 8-bit A/D, the effective resolution can be increased to give the same performance as more expensive 10- and 12-bit A/Ds.

4. Temperature Sensing



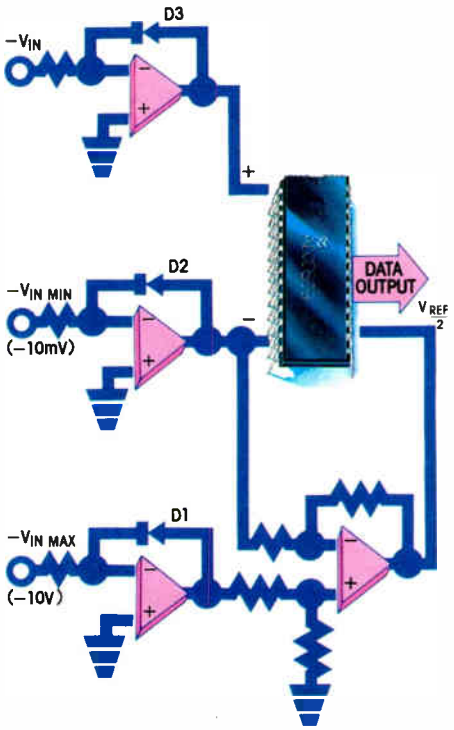
Since μPs are now used to control environmental and system temperatures, the combination of the LM335 and the A/D digitizes temperatures accurately and easily.

5. High-Speed A/D with Bipolar Input



To reduce the apparent conversion time to only a few μsecs, the A/D is operated in free-running mode. Two resistors are added enabling conversion of bipolar input signals (±5V, ±10V).

6. Three Decade Logarithmic A/D



When conversion of a wide dynamic signal range is required, this log A/D converts a three decade range.

ADC0801/02/03/04

- Total error ± ¼ LSB, ± ½ LSB, ± 1 LSB
- 100 μsec conversion time
- μP compatible
- Prices start at $2.95* @ 100 pieces

For more ideas and information on ways to use these versatile A/Ds, be sure to check boxes 023 and 051 on this issue's coupon.

*Prices shown are U.S. prices only.

National Semiconductor-the best reference for references.

2.5V micropower and low cost 5.0V references join the industry's broadest line of high performance IC voltage references.

The Practical Wizards at National have a linear IC voltage reference for every application. No one else can offer it all:

- Broadest line—over 35 references to choose from
- Lowest power—12μW (LM385-1.2V)
- Lowest drift—.5ppM/°C (LM199AH)
- Lowest prices—$.45* @ 100 pcs. (LM329DZ)
- Widest range of voltages—1.2V to 10.24V
- Tight tolerance—±0.01% (LH0070)

That's why National is the industry's best reference for references.

The LM385-2.5V micropower reference. The LM385-2.5's low power drain (50μW) enables battery life to actually approach shelf life.

And with an operating range from 20μA to 20mA, older references can now be replaced by this tight tolerance part. Because the LM385 Family's 1.5% to 3% initial tolerance and its low drift with temperature means high performance operation in almost any reference application.

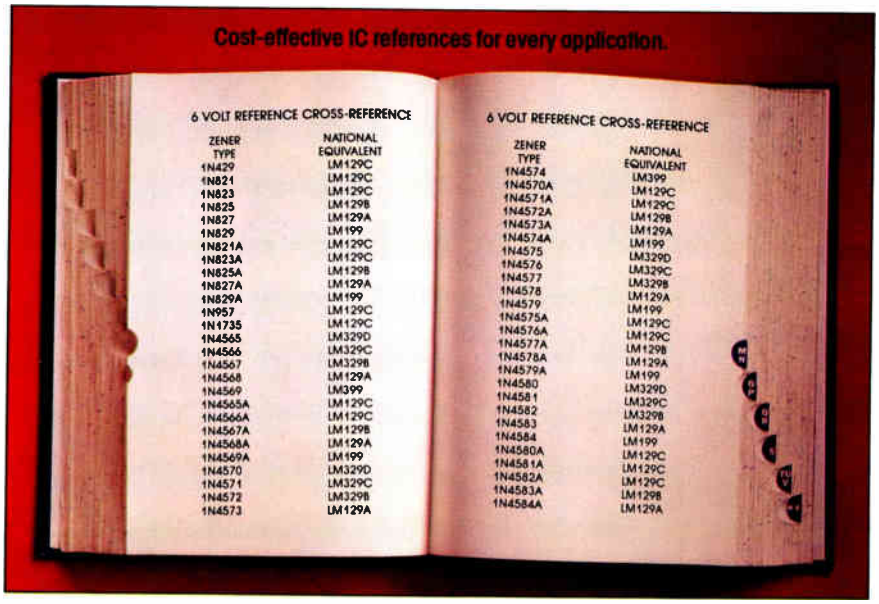
The LM336-5.0V precision reference. With guaranteed temperature stability and ± 1% initial tolerance available, the LM336 Family is a very practical reference for digital voltmeters, power supplies and op amp circuitry.

The addition of a third terminal allows the output voltage to be easily set from 4V to 6V. It can also be used for easy trimming to minimize temperature drift.

The LM336-5.0 is available in the low-cost TO-92 package with prices starting at $.75* @ 100 pcs. And since it operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

Be sure to check boxes 053 and 058 on this issue's National Archives coupon for complete details on the new LM385-2.5, LM336-5.0 and all the rest of the superior linear references.

*Prices shown ore U.S. prices only.



What's new from the National Archives?

023 ☐ ADC0801-4/ ADC0808-9/ ADC0816-17 A/D Converter Data Sheets
037 ☐ STARPLEX™ and ISE™ Information
051 ☐ Data Conversion/ Acquisition Data Book ($7.00)
052 ☐ Free Subscription to the Data Update
053 ☐ Linear Data Book ($9.00)
058 ☐ Voltage Reference Data Packet
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070 ☐ COP400-PDS and QUIKLOOK™ Data Sheets
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087 ☐ COP452 Data Sheet
088 ☐ BLX Expansion Module Information
089 ☐ TP3040 Filter Data Sheet

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The Practical Wizards of Silicon Valley

NA 29

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Printed in USA

Washington newsletter

Patent Office seeks advice on automation

The Commerce Department's Patent and Trademark Office—long a subject of industry and government criticism for its antiquated operations and error-prone file searches—is soliciting industry views as it gets ready to automate. The office has set July 23 for its first hearing on the automation study ordered late last year by Congress. The legislature wants the study, due by Dec. 12, 1982, to contain a plan, including costs and a timetable, that identifies "computerized data and retrieval systems equivalent to the latest state of the art which can be applied to all aspects" of the office's operation, **"particularly the patent search file, the patent classification system, and the trademark search file."** Written testimony must be received by the office before the hearings, and oral testimony requests must be filed by July 16 with Bradford R. Huther at the agency's offices in Crystal Plaza Building 3, 2021 Jefferson Davis Highway, Arlington, Va.

NBS sees need to measure radiation from 0 Hz to 300 GHz

New instrumentation, measurement standards, techniques, and calibration services for measuring nonionizing radiation in the spectrum from 0 Hz to 300 GHz are badly needed, says a National Bureau of Standards study for Congress. The need far exceeds that for U. S. regional calibration laboratories that the Senate Committee on Commerce, Science and Transportation initially asked the NBS to examine. The most important problem to be solved, says the report, **is the simultaneous measurement of both the electrical and magnetic fields from a nearby source.**

Pentagon challenged on waivers . . .

Waivers of competition requirements in the fiscal 1982 House and Senate defense-budget authorization bills are being challenged on Capitol Hill, particularly by Rep. Jack Brooks (D., Texas), chairman of the Government Operations Committee and its subcommittee on legislation and national security. The 1965 Brooks act (P. L. 89-306) mandates competition wherever possible, but the Defense Department's new management team wants authority to waive that requirement where necessary as part of its plan to speed up the procurement process and hold down overhead costs [*Electronics*, May 19, p. 66]. **Despite earlier approval by the House Armed Service Committee, the Brooks subcommittee rejected the Pentagon's plan** of waiving competition rules at its option, contracting for up to five years for major weapons, and raising the Government's termination liability $100 million from today's $5 million. The Brooks substitution permits multiyear buys only on a pilot basis and leaves the $5 million ceiling unchanged.

. . . CCIA says buyers cause delays

Also under fire is the Senate military authorization (S. 815) that would raise the Pentagon's contract cancellation liability to $50 million, and which the Computer and Communications Industry Association says removes numerous Pentagon computer purchases from requirements of the Brooks act. The CCIA's president, A. G. W. Jack Biddle, told the Brooks subcommittee that the General Services Administration, which must authorize all Federal data-processing purchases except weapons computers, "is not an obstacle to expeditious procurement," as its Defense Department critics argue. **"The real cause of procurement delays," says Biddle, "is the procuring agencies themselves,** particularly the Defense Department, with their numerous levels of review and clearance."

Washington commentary

Deregulating telecommunications: new arguments, new problems

Foreign competition and its increasing inroads into the U. S. telecommunications equipment market is American Telephone & Telegraph Co.'s latest argument to Congress against the company's dismemberment. It is an argument that is getting increasing attention and sympathy from a legislative body that is far more conservative in its views than any of its recent predecessors. Legislators are listening as they tackle once more the issue of telecommunications competition and deregulation and the roles that AT&T and a revamped Federal Communications Commission will play.

According to AT&T's William P. Stritzler, an assistant vice president for business marketing, "artifically constraining the Bell System, or any other competitor, substantially weakens the U. S. information industry's ability to withstand competition from large, often government-supported foreign firms. As we have seen in the automotive industry, such an effect can be measured in the number of jobs available to American workers."

"Foreign competitors operating unencumbered in the U. S. are an incredibly large market force that should give concern to the entire industry," says the AT&T executive. In 1979–80, for example, he says that "in Bell territory, foreign competitors won nearly one fourth of PBX [private branch exchange] sales against domestic competitors. In the same period, they won about 35% of the key systems sales against domestic competitors." Direct foreign investment in the U. S. telecommunications business "almost doubled from 1979 to 1980 to $1.6 billion," he says, compared with the five years it took total foreign investment of all types to achieve the same result.

Realities versus principles

"It sounds like a scare tactic to me," observes one hunkered-down House Democrat, adding quickly that "I doubt that I'll fight it right now. When AT&T says, in effect, 'Leave us alone and we'll put an umbrella over the rest of the domestic market,' I don't believe it. Yet Congress has a bigger concern for the shorter term—saving the national economy and its jobs. Bell might help there."

Another element in the congressional formula for telecommunications deregulation is that the Republican-controlled Senate, rather than the Democratic-dominated House, has taken the lead on legislation. And despite the fact that new telecommunications legislation has been considered in each of the last six years, Senate Republicans are having just as much trouble with it as the Democrats did.

The immediate problem for Robert Packwood (R., Ore.), chairman of the Commerce, Science and Transportation Committee, is that the Reagan Administration is unable to get its act together on the telecommunications bill. Meanwhile, Packwood's S. 898, which would permit AT&T to set up subsidiaries to compete freely in deregulated new markets for communications and data-processing equipment and services, waits while the Administration decides.

Justice versus Commerce

The Administration's uncharacteristic failure to state its position stems from a dispute between the Departments of Justice and Commerce, whose National Telecommunications and Information Administration is reputedly responsible for the relevant policy. The Justice Antitrust division continues to oppose new legislation before its ongoing suit in Washington's Federal district court is decided—which could take years if the judgment expected by year's end is appealed by either side, as is probable. Moreover, Justice officials say privately that Packwood's S. 898 would not prevent AT&T from, in effect, controlling competition. That position is strongly supported by AT&T's competitors, who are lobbying hard against the bill.

Generally in favor of the legislation, on the other hand, are Commerce Secretary Malcolm Baldridge, U. S. Trade Representative William Brock, new FCC chairman Mark S. Fowler, and AT&T. Yet Baldridge and Brock enraged Packwood when they canceled on less than 24 hours notice their long-awaited Senate testimony to detail Administration policy. "This is not a bill we sprung on them," notes the angry chairman.

Packwood rejects the Antitrust division's argument on the premise that no telecommunications deregulation bill will ever pass if that view prevails. Other Republicans believe that resolution of the dispute can be achieved only by White House intervention—a tricky business as long as the antitrust suit is still in the courts.

Nevertheless, the Reagan Administration must take some action and make its position known, even if it conflicts with the Justice Department, for telecommunications business growth is not waiting and neither are AT&T and the rest of its competitors, foreign and domestic. As one telecommunications industry witness put it in early June to the Packwood committee, "the worst course of action now is no action at all."

-Ray Connolly

OCTOPLUS

The Sprague Monolithic Arrays That Provide the Muscle of 8 SCRs in a Single DIP.

Sprague UTN-2886B and UTN-2888A SCR arrays are expressly made for use with microprocessors which are strobing power loads. Compatible with TTL, LSTTL and CMOS, they will interface to high-current loads including lamps, relays, and solenoids.

Each array contains eight SCRs with integral current limiting and gate-to-cathode resistors.

The combining of SCRs in one DIP reduces component count, assembly time, and circuit space while improving overall circuit reliability. Each of the isolated devices within the array is capable of continuous and simultaneous operation at 200 mA or 250 mA, at ambient temperatures to +50°C. The arrays operate from an unfiltered half-wave (50 or 60 Hz) or full-wave (100 or 120 Hz) rectified source.

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For application engineering assistance, write or call Mark Heisig, Don Bird, or Paul Emerald, Semiconductor Division, Sprague Electric Co., 115 Northeast Cutoff, Worcester, Mass. 01606. Telephone 617/853-5000.

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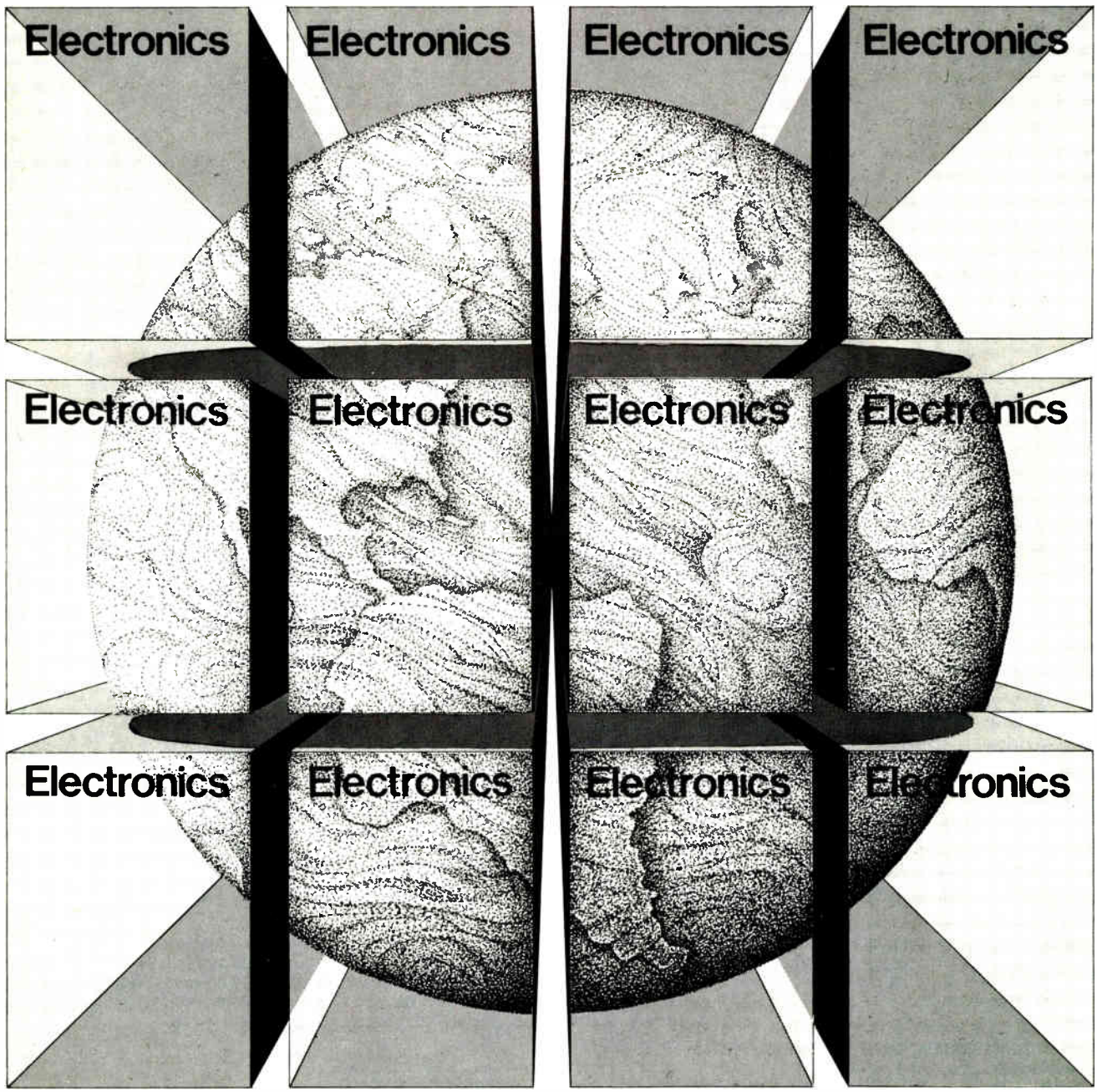
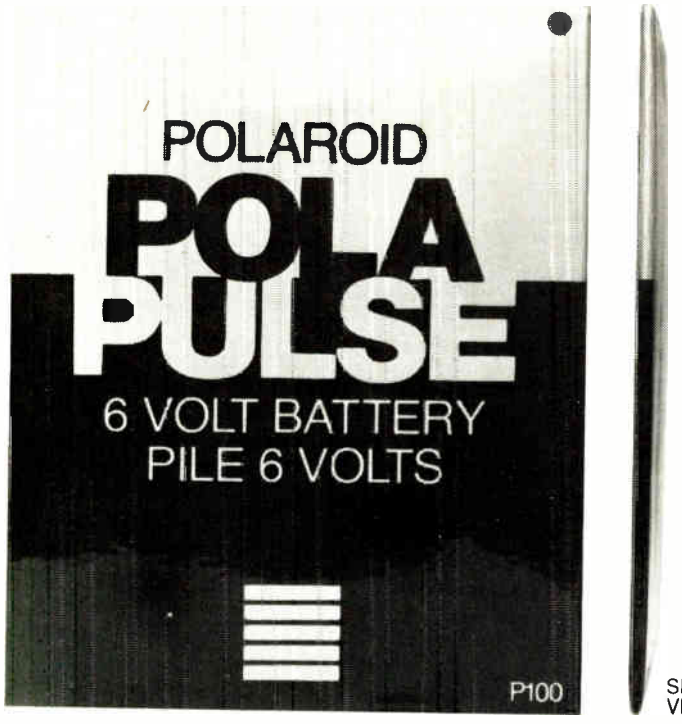




ACTUAL SIZE

SIDE VIEW

The 6-volt wafer-thin battery that can change the shape of things to come.

We've developed a battery at Polaroid called the Polapulse P100. It's thinner and lighter than any conventional battery we've ever seen.

It can make products thinner, lighter and more compact than if they used conventional batteries. In some cases it can make a product easier to use. It can even help, in some instances, to increase profits.

Less cost, more profit.

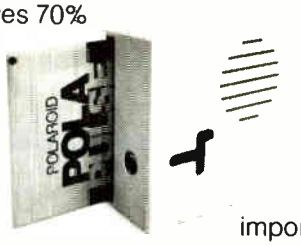
For example, take the prototype for a printing calculator.

The Polapulse battery's unique card-in-slot replacement feature requires a one-piece, rather than a three-piece mold, saving 33% of a manufacturer's plastic costs.

With less plastic the calculator is a sleek 6½ x 3⅜ x 1½", weighs only 11.2 ounces, and saves 38% of packaging and shipping costs.

And since Polapulse needs fewer contacts, a manufacturer saves 70% of contact costs.

Equally notable is the particular ability of the Polapulse battery to power a printing calculator's motor with a surge of high current at the beginning of each print. It can then satisfy the high surge demand with low internal resistance and fast voltage recovery.



Heavy duty lightweight.

Design engineers at D.E.I. Teleproducts, a West Coast manufacturer of line drivers, developed test equipment with the Polapulse P100 battery. D.E.I.'s new interface monitor and tester is less bulky and more portable because Polapulse is four times lighter than the conventional power source.

Polapulse has 6 volts of power packed into a one-ounce 3.73 x 3.04" parcel only .18" thick and offers high surge at short pulse. This provides D.E.I.'s new equipment with brighter, easier-to-see LED's.

The interface monitor and tester, only 5¾ x 4⅜ x 1", has a larger face than comparable testers which permits bigger turrets spaced farther apart for easier connections.

Thin battery, wide appeal.

A new slide bolt, door-mounted burglar alarm owes its streamlined 4 x 3¼ x 1⅝", 8-ounce design to the Polapulse battery.

Again, the card-in-slot replacement feature makes an important contribution. The burglar alarm can remain in place at all times. Even when changing batteries.

It is also virtually impossible to short out the battery by accidentally reversing polarity of the contacts. The user does not experience perceived product failure. And, therefore, does not send the product back to the manufacturer for a repair that simply entails proper battery replacement.

Security is a Polapulse battery.

Every Polapulse receives 100% inspection, the sort of inspection reserved for major manufacturers' top-of-the-line power cells. Each Polapulse receives electrical and visual inspection at assembly and again after 60 days of controlled aging.

It also features a unique seal modeled on the Polapulse SX-70 film pack battery which boasts an infallible leakage record—no known leak damage in over 400 million SX-70 film packs.

Your chance to wield power.

Experiment with our Designer's Kit. It contains five Polapulse P100 batteries and a molded battery holder.

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Polaroid

Our inventions can be your components.

Circle 62 on reader service card

International newsletter

Japan's optoelectronics lab to open in the fall

Japan's Optoelectronics Laboratory, at which researchers from many firms will cooperate in the same way as they did at the now-defunct VLSI Cooperative Laboratories [*Electronics*, Aug. 28, 1980, p. 76], is scheduled to go into operation in October for a six-year period in a 1,600-m² area of Fujitsu Ltd.'s Kawasaki works. **During the first year, the research staff will total about 30,** with an increase to 50 expected during the second year.

Managing the project will be the Engineering Research Association of Optoelectronics Applied Systems, which was established to manage this research in January and includes among its 10 members NEC, Oki Electric, Toshiba, Hitachi, Fujitsu, Matsushita Electric, Mitsubishi Electric, and the Electrotechnical Laboratory of the Agency of Industrial Science (part of the Ministry of International Trade and Industry). Funds for equipment and operation will come from the $9.7 million appropriated for contract research during the 1981 fiscal year that began on April 1.

British Telecom weighs laser link for London

A 2-Mb/s line-of-sight laser link from Modular Technology Ltd. of Watford is to be evaluated by British Telecom, which is considering its use alongside cable and microwave links **to provide the City of London with a sorely needed digital overlay network.** The $34 million modernization program is intended to supply high-speed data, facsimile, teleconferencing, word-processing, and satellite business service before System X becomes available in 1983. The laser link from Modular Technology is aligned with telescope eye pieces and can operate over distances of 15 km. A full-duplex 50-kb/s link costing $10,000 is already in operation.

Italy developing 100-W photovoltaic unit

Scientists in sunny Italy expect to have ready by year-end a 100-W photovoltaic power module that will work at record solar levels—720 suns at an air mass of 1.5. All the photovoltaic elements of the module, which uses **two solar cells having different bandgaps and spectrum-splitting filters to boost conversion efficiency close to 25%,** have been tested out at Centro Informazione Studi Esperienze (CISE), a research center owned jointly by ENEL, the Italian electricity board, and the municipal energy agency of Milan. The module's design calls for eight square Fresnel lenses, 40 cm on a side. Each lens beams sunlight onto a pair of 1.4-cm² solar cells—gallium aluminum arsenide for high-energy radiation and either gallium arsenide or silicon for low-energy radiation. The spectrum-splitting filters are a 5-mm-thick sandwich of 30 alternating dielectric layers of aluminum fluoride and zinc sulphide. A similar approach was tried by Varian Associates in the U. S. [*Electronics*, July 20, 1978, p. 42].

East Germany to beef up electronics production

East Germany's new five-year economic plan, to run through 1985, calls for ambitious, though in some parts vaguely defined, efforts in electronics. Top priority are activities in microelectronics, robot technology, machine-tool controls, and data processing. For example, by 1985, the output of microelectronic devices of all kinds is to be at least twice that of last year. Among other tasks, such devices are to speed up the development of digital communications equipment and networks for both domestic use and export. More specific are the plans for **industrial robots: between 40,000 and 45,000 units are slated to be built by mid-decade.** In addition, production capacities for consumer equipment will be expanded and the share of stereophonic transmissions on the fm band increased.

International newsletter

System reads kanji characters into word processors

A promising solution to the hoary problems of entering Chinese-character (kanji) text into Japanese-language word processors has been developed by Nippon Telegraph & Telephone Public Corp. Called Aesop (for advanced editor with script input and print output), the device can be used with any existing word processor. It **employs pattern recognition technology to "read" about 1,900 characters of written text with 99.5% accuracy,** so that it could obviate unwieldy and difficult-to-learn kanji keyboards and kana-to-kanji conversion systems. The operator writes characters with a special pen onto paper that covers a special grid. The recognition unit compares three to six aspects of the character against its dictionary and chooses the most likely match within 0.5 second—faster than the normal writing speed. NTT is not ready to reveal how soon Aesop will go on the market or its likely price.

Mullard chip simplifies IR detection

Now in production at Mullard Ltd.'s Southampton plant is an integrated infrared-light detector element combining eight n-type cadmium mercury telluride sensing elements on a single sapphire substrate. It is designed for use in serial-parallel systems in which a mirror scans a vertical linear image usually across several horizontal rows of discrete detectors: but to combine the sequence of signals from a single image element, the output from each detector must then be suitably time-delayed before summing. The device, called Sprite, performs this function internally **by merging each row of detectors into one sensing element,** thus eliminating external electronic circuitry and greatly simplifying scanner design. Developed in conjunction with Britain's Royal Signals and Radar Establishment research laboratories in Malvern, Sprite operates in the 8-to-14-μm waveband and achieves rates of 10^6 picture elements per second.

Thermal-imaging system attains military reliability

Two French firms have developed a thermal-imaging video system for military equipment that uses a serial-parallel scanning monitor to significantly improve reliability. The SMT thermal modular system is a joint venture of the Société Anonyme de Télécommunications (SAT) and Télécommunications Radioélectriques et Téléphoniques (TRT), both based in Paris. Destined for use in night reconnaissance, enemy detection, and weapon guidance by future French tanks, armored personnel carriers, and military aircraft, **it owes its improved reliability to the fact that the columns of screen sensors are scanned in series** so that the loss of any one sensor has a minimal effect on the overall quality of the image. The SMT has a spectral bandwidth of 8 to 12 μm, is compatible with standard television, has a range of up to 15.5 km, and weighs between 7 and 9.5 kg.

Pan-European conglomerate forms for NATO bids

In a bid to avoid the winner-take-all wrangles over how the North Atlantic Treaty Organization should share its contracts, European and U. S. manufacturers of electronic capital equipment have assembled one of the largest consortiums yet **to work on NATO's upcoming Air Command and Control System (ACCS) program.** To be registered as ACCSSCO SA, the company will be jointly owned by West Germany's AEG-Telefunken and Siemens; Hughes Aircraft of the U. S.; Marconi and Plessey of the UK; Belgium's MBLE; Italy's Selenia; Hollandse Signaal-Apparaten of the Netherlands; and France's Thomson-CSF.

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GENERAL INSTRUMENT

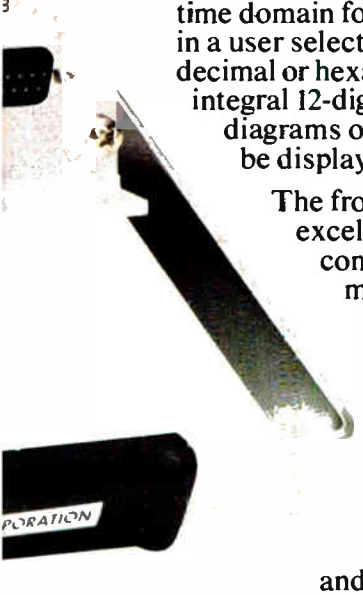
Now the logic is clear... B&K-PRECISION is the new choice for logic analyzers.

Announcing a new line of logic analyzers ready to face all comparisons.

The very latest word in logic analysis is B&K-PRECISION. Not just another "L-A" line, B&K-PRECISION's new instruments offer real user advantages.

Both new analyzers, the LA-1020 and LA-1025, are 16 channel, 20MHz instruments. In addition to logic analysis, the LA-1025 "Digital Systems Analyzer" offers the added capability of signature analysis. Signatures are displayed in industry-accepted coding for modified hexadecimal format. The LA-1025 is also capable of recording the occurrence of unstable signatures.

An important feature of both instruments is the ability to present data in both state and time domain formats. State data is formatted in a user selected code... binary, octal, decimal or hexadecimal and displayed via the integral 12-digit LED display. Timing diagrams of 16 channels by 16 words can be displayed on most oscilloscopes.



The front panel controls provide excellent interactive capability, and complete control over a powerful measurement system. After hearing industry complaints of unnecessarily complex logic analyzer operation, B&K-PRECISION engineers devoted a considerable amount of design time to maximizing the instruments' ease-of-use and efficiency. The results are impressive. Not only is set-up time faster than on competitive instruments, but the new B&K-PRECISION instruments reduce the chance of user set-up errors.

Model LA-1020 $2075 **Model LA-1025 $2475**

A new trigger system was developed for these instruments. An 18-bit pattern recognition trigger is used to initiate storage into the 16-bit x 250 word system memory. Sixteen qualifiable channels are featured, plus two additional qualifiers to aid in meeting unique trigger requirements. Convenient front panel switches select a logic 1, 0 or "DON'T CARE" for all 18 inputs.

Trigger event and/or clock delays can be rapidly set from 0 to 999. The trigger word may be located anywhere within the 250 word memory. This provides PRE, POST and variable PRE/POST trigger recording.

The LA-1020 and LA-1025 interface to the circuit under test through two Model LP-1, TTL compatible, probes or LP-2 CMOS probes. Trigger capability can be increased to 34 qualifiers by adding the optional LP-3 qualifier expander probe.

An event pulse-output is provided on both analyzers, allowing interconnection of two units to expand system versatility to 32 channels, 67 qualifiers, at speeds to 10MHz.

B&K-PRECISION's LA-1020 and LA-1025 are available now for delivery or demonstration. If you're currently using logic analysis or considering a system, call B&K-PRECISION toll-free at **800/621-4627** for a no-obligation demonstration. It's the only way to see the clear choice.

For service applications, the SA-1010 Signature Analyzer is the time saving choice.

Model SA-1010 $825

(Price includes a set of user ordered probes, additional probes available as accessories).

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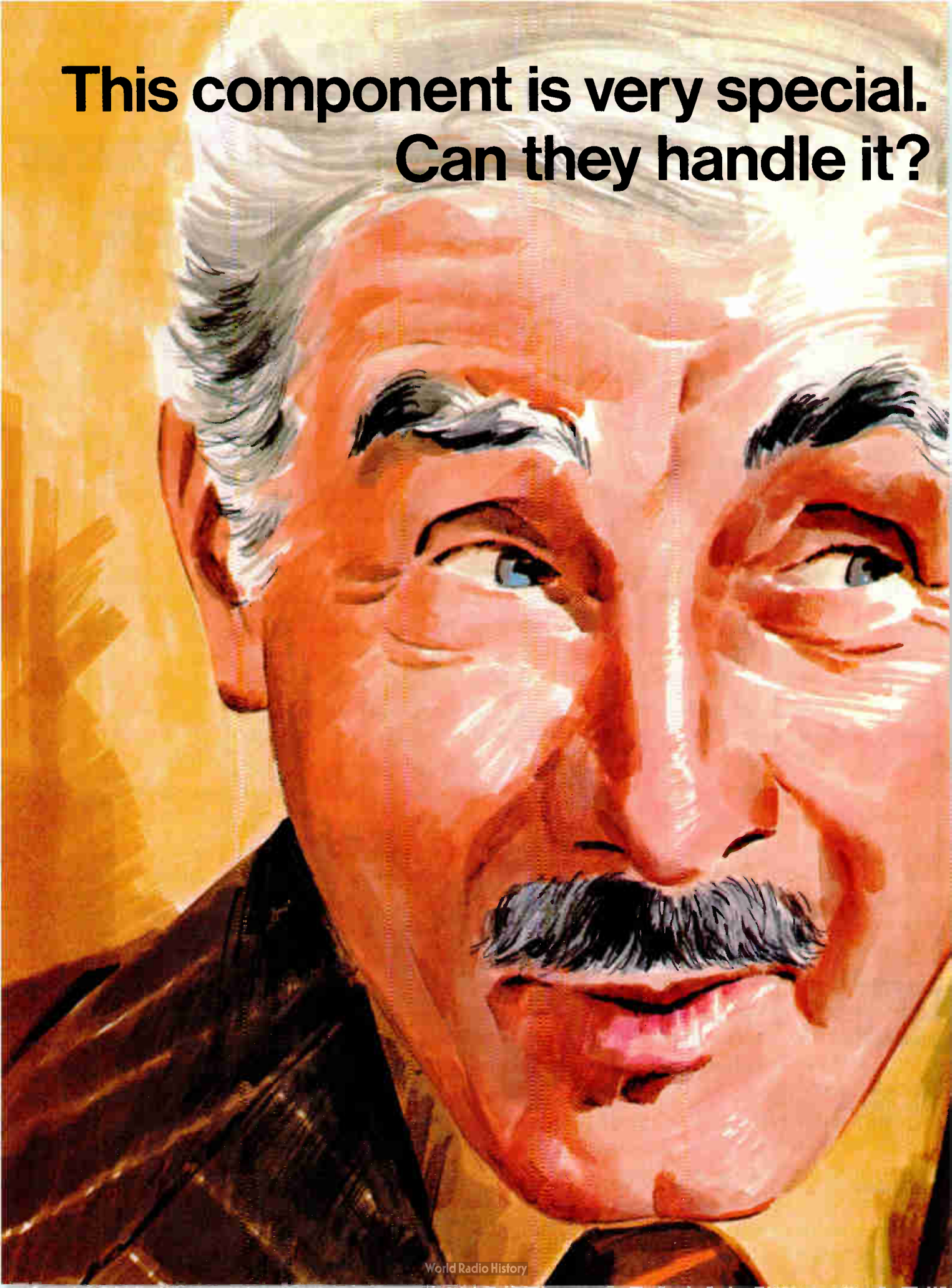

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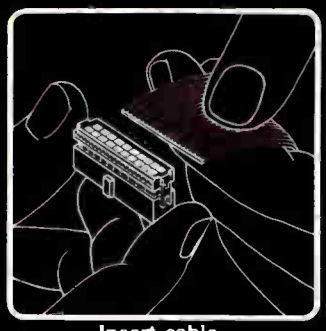

Insert cable.

Place in fixture.

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The Berg "Quickie" connector was well named. But it soon had many imitators. Now meet "Quickie" II, the new connector that makes the others play catch-up all over again while you save even more time and money. Because "Quickie" II terminates in just 7 seconds with the Berg QP 106 pneumatic applicator.

It's a simple two-step operation. One: Insert the cable into either lead-in slot. Two: Place the cable/connector in the press and terminate. It's that easy! A pre-assembled cover and base gives you fewer parts to assemble and fewer chances to damage components. The cable installs quickly and accurately through an exclusive double-serrated slot with lead-in from either side. The serrations guide the cable to assure precise positioning over the contacts. As a result, mis-assemblies are virtually eliminated.

You can't beat the system. Berg offers you a total IDC System which includes cable, "Quickie"

takes you more than to Berg's new Quickie* II.

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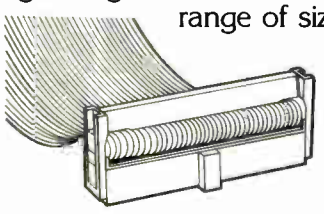

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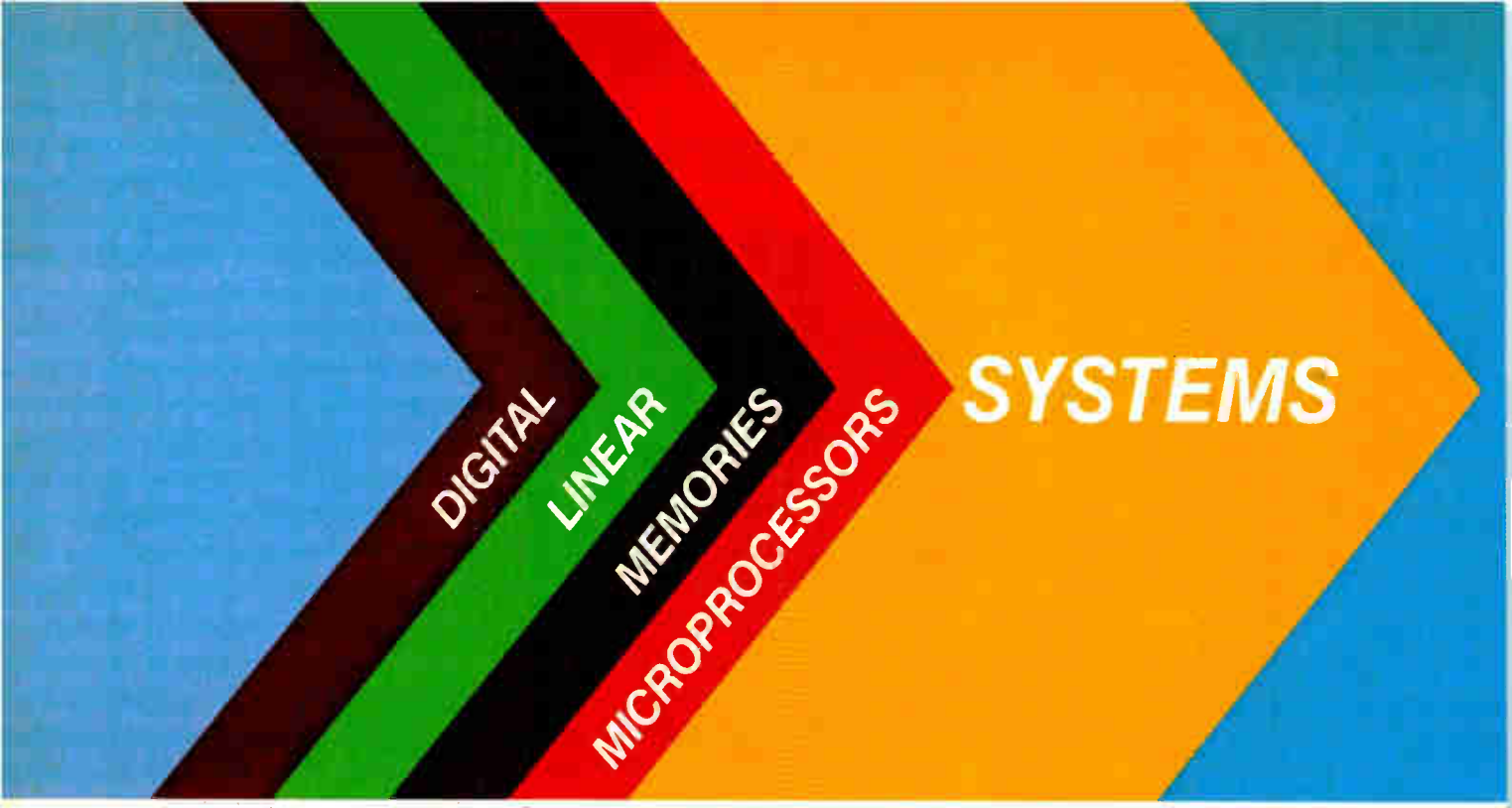

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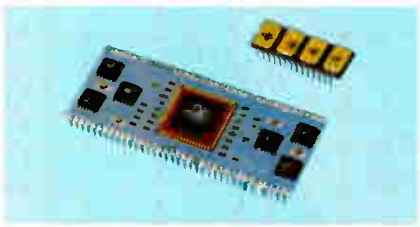
For the past few months we've been telling you about all the benefits of chip carrier IC devices — benefits like reliability, ease of use, versatility, increased densities, board space and weight and production cost savings. We've talked about leadless ceramic chip carriers (LCCCs) for TI digital, linear, memory, and microprocessor ICs — and now, all the features, functions and many benefits of the individual components mean dramatic improvements in systems production, size, cost, and, of course, performance. The system solution for VLSI ... and beyond.

LCCCs and System Production

Compared with conventional IC devices, TI LCCCs provide many system production advantages. They can be placed automatically on PC boards by magazine-fed machines, always properly aligned, with address board pins top or bottom. So, production is faster because fewer assembly steps are required.



LCCCs and System Cost/Performance

One-sixth the surface area, one-twelfth the weight of conventional DIPs, TI's square-shaped, 100-mil thin, single-layer JEDEC standard type C chip carriers feature contacts with 50-mil-center spacing. So, you're saving board space. And you're using fewer boards. For example, with chip carrier packages you can get 4 64K DRAMs (256K bits) on one 28-pin DIP — using only one square inch of board space. of course, overall system costs are greatly reduced.

TI LCCCs provide measurable improvements in system performance. High-frequency and high-speed switching are enhanced because lead inductance and resistance are lower. Signal paths shorter. It's the ideal way devised to achieve packaging for VLSI circuits with more than 64 I/O counts.

LCCCs and VLSI

When you're ready for VLSI, TI's chip carriers will help you make the transition with speed, ease and economy. Developed to meet future IC packaging demands caused by improvements in chip technology such as increased complexity, circuit size and number of pin-outs, LCCCs are being looked at by forward-looking designers for use in future projects as well as for those in the early design stages. All TI chip carriers can be processed to MIL-STD-883B. Fully tested, guaranteed and AC/DC characterized.

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TEXAS INSTRUMENTS
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82930

Circle 72 on reader service card

Polymer doubles as photoresist and insulator

by John Gosch, Frankfurt bureau manager

West German researchers build photoreactive groups into polyimide and temper it to make it heat-resistant

Integrated circuit technology is moving another step ahead, now that researchers at Siemens AG have come up with a photoreactive material that can be used both as a photoresist for pattern generation and, after a tempering process, as an insulating, passivating, or protective layer. Developed at the West German company's research laboratories in Erlangen, the material is a polymer with a special chemical structure.

As a photoresist, the material is thermally more stable and exhibits a higher chemical resistance than conventional resists. It thus easily meets the stringent demands of dry etching and ion implantation techniques. As an insulator or passivator, the organic material has excellent electrical, mechanical, chemical, and thermal properties, some of them superior to those of common inorganic insulators like silicon dioxide or silicon nitride. The photopolymer will soon be used in production at various Siemens facilities and should be available worldwide within a year through firms licensed to make it.

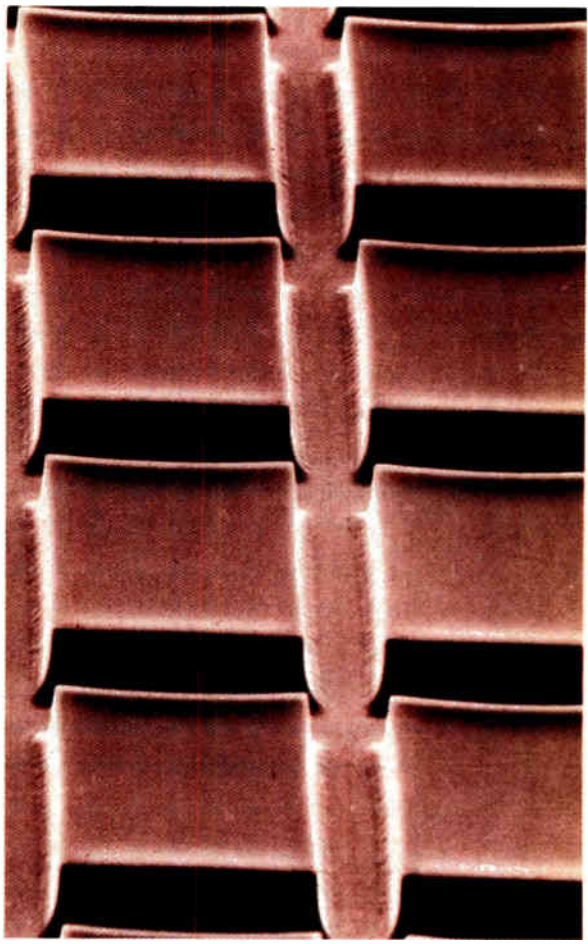
Aim. "Our research goal was a photoresist that, after patterning, could also serve as a highly heat-resistant insulating layer," says Roland Rubner, head of the team of Siemens chemists that developed the material. "We also aimed for a material that could be applied by standard photoresist technology."

Photoreactive polymers, the Erlangen researchers believe, will give semiconductor technology new and extended possibilities. For one thing, the materials have the thermal, mechanical, and chemical stability characteristic of many organic substances. For another, a single layer can perform several functions, so they greatly simplify device fabrication and therefore raise yield.

In general, highly heat-resistant polymers are insoluble and thus cannot be used as photoresists. However, in their intermediate, or precursor, stage, they are soluble. According to Rubner, firms in the U. S. and Japan have been investigating soluble polymeric precursors for some time, with the same objectives as Siemens, but being nonphotoreactive, their precursors required as many as a dozen fabrication steps or else suffered from limitations such as poor adhesion at the edges.

Four-step procedure. Applying the Siemens material, on the other hand, entails only four steps. The key is a precursor with chemically built-in photoreactive groups—usually acrylic types bound in esterlike fashion to the polymer molecules.

This polymeric precursor is applied just like an everyday photoresist. It is spin-coated onto a substrate, patterned by selective exposure to ultraviolet light, and then has the unexposed parts chemically dissolved. If it is also to serve as an insulating layer, tempering it at 270°C for 30 minutes turns it into a polyimide. A second 30-min step is performed at 400°C if high-temperature processes such as metal-layer deposition are to follow. Such tempering makes the polyimide layer resistant to long- and short-term temperature levels as high as 200° and 450°C respectively—performance on a par with that of silicon dioxide or nitride insulating layers.



Multifaceted. This polyimide photoresist-turned-insulating layer, deposited on a silicon dioxide substrate, is 17 μm thick. Each segment is 100 μm square.

Far superior are the polyimide's mechanical properties, however. Whereas in an inorganic insulating

layer the different thermal expansion coefficients of various device regions often lead to tiny cracks, an organic layer resists such crack formation, Rubner says. Also, a polyimide layer may be cut with a razor blade without splitting or cracking at the edges.

Noteworthy, too, is a polyimide layer's high adhesive strength of better than 28 newtons per square millimeter; its high flexural strength; and its high electric breakdown strength—up to 200 kilovolts per millimeter.

Great Britain

10,000-gate ULAs are in the offing

Though Ferranti Electronics Ltd. was among the first to commercially exploit the uncommitted logic array back in the early 1970s, new technologies, among them high-density complementary-MOS arrays, have threatened to eclipse its elegantly simple version of Bell Laboratories' collector-diffusion isolation (CDI) process—just at a time when the market is primed for takeoff.

But now the Manchester-based company is counterattacking. After a two-year development, it is introducing a stretched CDI process that doubles logic densities, making 10,000-gate arrays entirely feasible. First samples for internal use are due out this year, but volume production of the ULAs is not scheduled for before 1983.

The processing tweaks introduced by Ferranti in its stretched CDI process—the addition of a more compact washed-emitter structure plus an extra masking stage—have increased complexity comparatively little yet have yielded handsome dividends: they halve CDI transistor area, give an f_t figure of 1 to 2 gigahertz, and best of all should reduce speed-power product eightfold—a bonus that can be exploited to achieve either subnanosecond speeds or C-MOS power levels at typical TTL speeds.

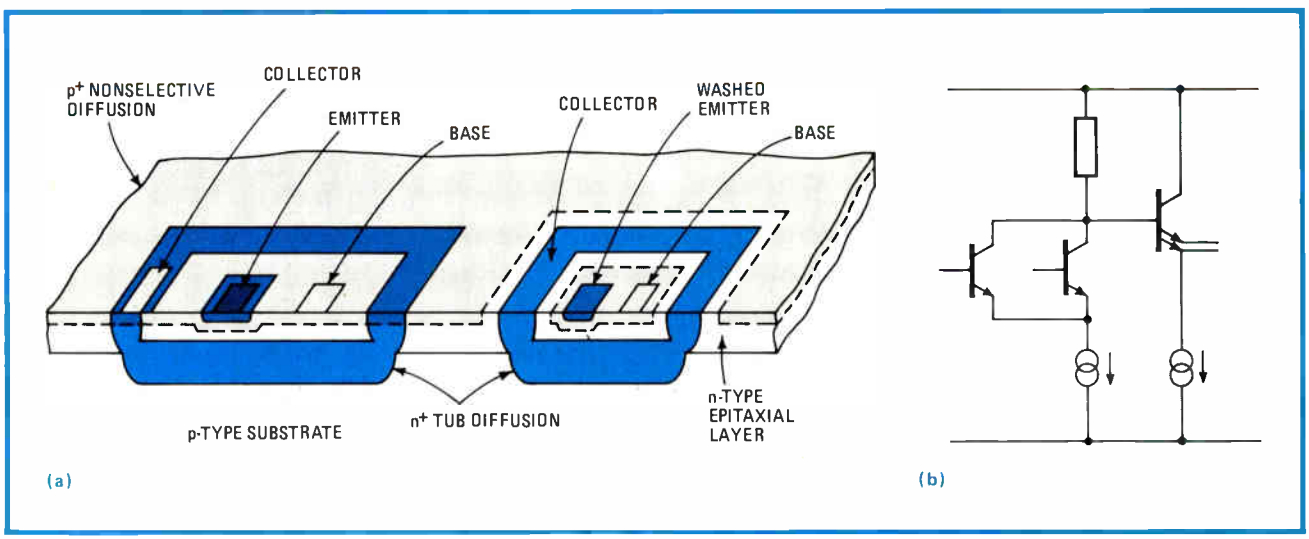
Origin. In the CDI transistor initially developed but now abandoned by Bell Labs, both emitter and base regions are contained in a single n-type tub diffusion, which serves both as a collector and as an isolation barrier from the p-type substrate. Elimination of the usual bipolar isolation barrier makes for a compact transistor structure.

The extra masking stage rids the isolation diffusion of the nonselective p^+ diffusion (needed to adjust the epitaxial layer's sheet resistance and to prevent the formation of inversion layers). This reduces the capacitance at the critical collector-base junction and results in a lower speed-power product, the ability to withstand higher voltages of at least 12 to 15 volts, and the availability of a p-channel junction field-effect transistor by further masking of the p^+ region under the transistor emitter, as shown in (a).

Swinging. The washed-emitter structure further reduces nodal capacitance and improves packing density. It also permits integration of an emitter-follower buffered-output resistor without sacrificing chip real estate, thus dropping the logic swing to 250 millivolts today and to 120 mV in future.

The process will be the basis of three families consisting of 20 ULAs and covering a very wide range in density, speed, and power consumption. Though all 20 are digital, the new CDI process's ability to incorporate J-FETs on chip, notes Ferranti marketing manager Allan Williamson, is particularly relevant to linear circuits—in low-level multiplexers or high-input impedance devices, for example.

Apart from speed, the new arrays offer some of the niceties of ECL. By adding a buffered output to Ferranti's basic nonsaturating current-mode logic cell (b), gate delay has been made independent of fanout. The two-output emitter-follower buffer also permits a wired-OR function. And that, says engineering



Tweaked CDI. In the new process, shown at right in (a), the transistor is more compact and the emitter in particular is a mere 3 μm square instead of 4 by 9 μm (left). Adding a buffered output (tinted area) to cell (b) makes gate delay independent of output.

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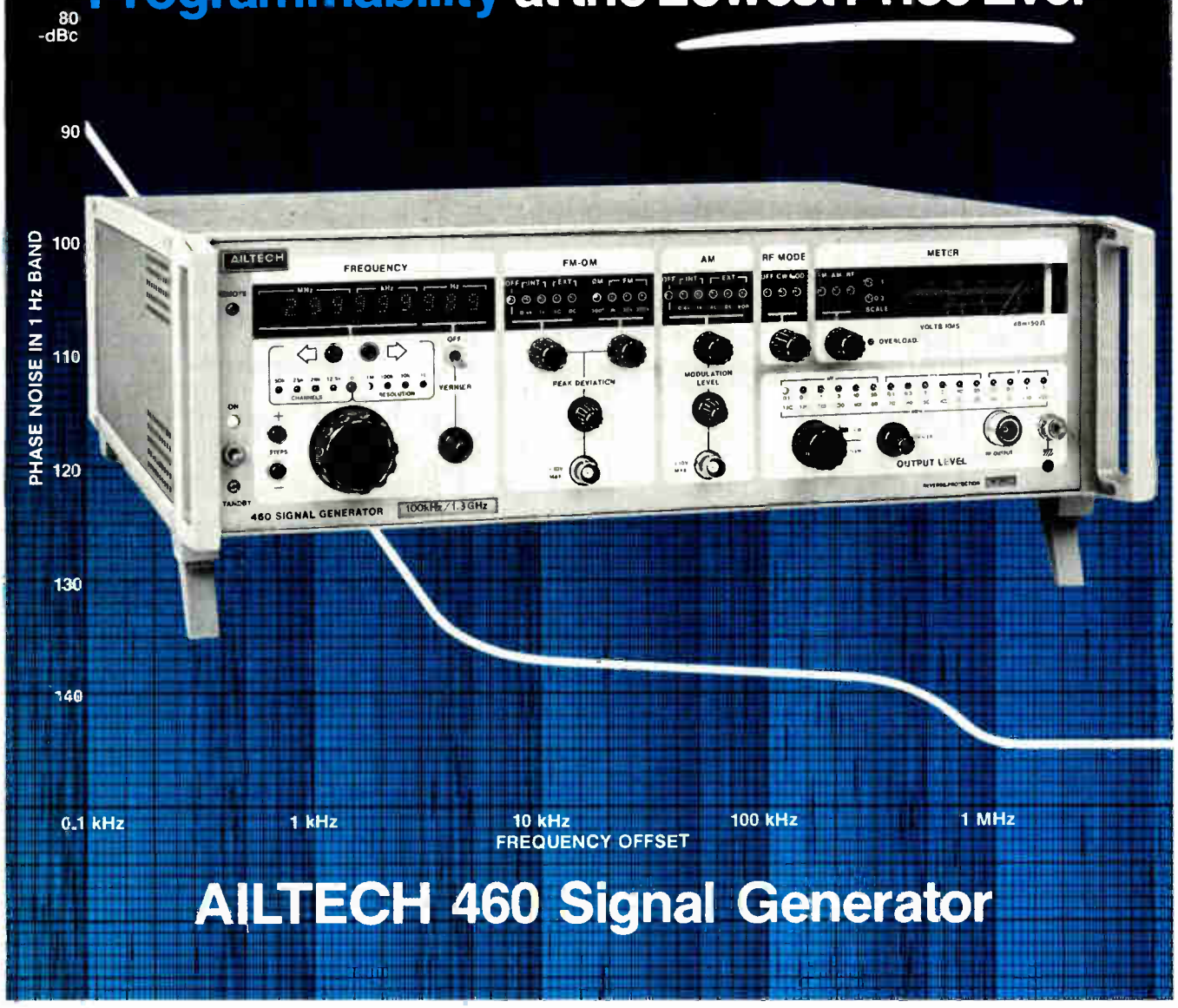

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manager David Grundy, can cut down on the number of logic gates needed for a system by 30%.

LSI first. The company will launch its large-scale integrated-circuit family first—15 ULAs having 500 to 2,000 gates and spanning three performance categories. They include: a speedy 2.5-nanosecond gate delay and 300-microwatt-per-gate power consumption; a general-purpose variant with a 7.5-ns gate delay and 60-μW-per-gate consumption; and a low-power version with a 15-ns gate delay (roughly a 13-megahertz clock rate) and using 30 μW per gate. These parts will be introduced over the next six months.

Ferranti says this new R series is no more power-hungry than C-MOS arrays in typical logic systems. "C-MOS parts take power only when they are switched," explains Grundy. A study conducted by his group found that in a typical logic system, between 1 and 2 gates in 10 switch on every clock pulse, on which comparison basis the R series array stands up well.

To follow the LSI trio in the first quarter of 1982 is the subnanosecond logic family that brings Ferranti into head-on competition with high-performance emitter-coupled-logic arrays. Fastest of the three parts is a 1,000-gate array with a 0.5-ns gate delay (equivalent to a 300-MHz clock rate). Its 1.5-milliwatt-per-gate power consumption, however, means that it will be dissipating 1.5 watts, about all that can be managed per package without additional cooling. So for the other two members of the family, with 2,000- and 4,000-gate complexity, respectively, speed has been traded for power economy and gate delays are 1 ns with 7-mW-per-gate consumption in both cases. (The figures quoted are for an optional 2.5-V supply line.)

Jumbo. The group is also planning its first family of very-large-scale integrated ULA parts. As a result of its 10 years of experience with the CDI process, Grundy can now talk with equanimity of producing jumbo-sized chips nearly 0.4 inch (10 millimeters) on a side. So he believes 10,000-gate arrays will be achieved by 1983—initially by moving to bigger chips and not by shrinking design rules. "It's an exceptionally high-yielding process," confirms Williamson, contrasting its 6 masking steps with the 8 to 12 needed for C-MOS processes. **-Kevin Smith**

Japan

Less than $1,000 buys personal computer equipped with dual processors

Multiple processors (two 6809s), a multilayer printed-circuit board, and U. S.-originated operating systems are among the features that one of Japan's most innovative personal computers shares with the larger mainframes developed by the same manufacturer. Fujitsu Ltd. says that the outstanding trait of its Micro 8 computer [*Electronics*, June 2, p. 64], which has 128-K bytes of memory, is relatively high performance for the low price of $975.

When sales start in Japan at the end of July, the main competition there will be two Z80-based computers. Nippon Electric Co.'s PC-8001 sells for $750 with 24-K bytes of read-only memory and 16-K bytes of random-access memory, each expandable to 32-K bytes; a separate 32-K RAM board goes for an extra $192. Sharp Corp.'s MZ-80B, a redesign of its -80C, has a price tag of $1,241, for which the buyer gets a 4-megahertz Z80A with 64-K of RAM. ROM for boot loading and character generation only, a built-in 10-inch cathode-ray tube, and a built-in tape deck.

Also running. Trailing far behind the two leaders is Hitachi Ltd.'s $1,330 MB-6890, also 6809-based and equipped with 24-K bytes of ROM and 32-K bytes of RAM.

In the U. S., the Zenith Data Systems division of Zenith Radio Corp. builds the Z-89 computer around two Z80s, used as in the Fujitsu machine for computing and display, respectively, and sells it complete with 48-K bytes of RAM and a CRT for $2,595. An Apple II with 48-K bytes of RAM is $1,530. Fujitsu will not, however, attempt to export its Micro 8 before 1981 is out.

The Micro 8 makes essentially the entire 64-K byte memory area of one of its 6809 microprocessors available to the user, with the other 6809 providing as much memory again for fine-pattern multicolor video display and character generation. Actual keyboard scanning is performed by a 4-bit microcomputer original to Fujitsu, while bubble memories (when installed) are controlled by a Fujitsu 8049-compatible microcomputer.

The single four-layer glass-epoxy pc board holds all the Micro 8's many semiconductor devices yet fits under its keyboard. The signal lines have negligible coupling to parallel lines on either side of the board.

Software. The Micro 8 is shipped with a 30-K-byte enhanced version of Microsoft Basic that overlies 32-K bytes of user memory. This version of Basic includes DO . . . WHILE loops for Pascal-like structured programming, plus some instructions added by Fujitsu.

For more flexible operating systems, the user will have to purchase a dual minifloppy-disk drive for an additional $1,400 and also one among a menu of U. S. operating systems. The most obvious are UCSD Pascal (which supports Pascal, Fortran, and Basic) and Flex—the microprocessor disk operating system that supports the same languages plus assembler. Uniflex is coming, and OS/9 is also suitable. The Z80 softcard, an idea that Fujitsu picked up from Microsoft, enables the computer to support CP/M.

For applications where a nonvolatile memory is required at lower cost than disks, Fujitsu offers a $385 bubble holder unit that will accept two bubble cassettes. At present, 32-K-byte cassettes are available at $156 each, but early next year the firm expects to offer 128-K-byte cas-

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settes using 1-megabit bubble chips.

At the other end of the spectrum, business users who want to exchange data with mainframes can use full-sized floppy-disk drives with an IBM-compatible format and maintain their own data bases in 10- and 20-megabyte hard disks. They can also communicate with mainframes at speeds of up to 9,600 bits per second through an RS-232 interface either asynchronously or using a built-in IBM binary synchronous protocol—which is probably a first for microcomputers.

Control. Control applications are supported, too. The computer has built-in analog-to-digital conversion. An IEEE-488 interface will be available as an option.

The display processor's memory map is dominated by 48-K bytes used as video RAM. This gives a display of 640 dots across the screen by 200 top to bottom, with eight colors for each dot. **-Charles Cohen**

Personal computers accept oral input

Two Japanese firms chose the late May Microcomputer Show '81 in Tokyo to unveil voice recognition units for entering data on personal computers. Both use large-scale integrated circuits and the dynamic programming matching approach to voice recognition, but their similarities stop there. Nippon Electric Co. designed its PC-8012-03 voice recognition board exclusively for use with its PC-8001 personal computer. Sanyo Electric Co.'s SSR-16 and -32 boards, on the other hand, are stand-alone; containing their own microprocessor, they can be used with an array of computers, machine controllers, and other machines requiring simple data input.

Origins. NEC's unit actually consists of two 220-by-95-millimeter circuit boards and a microphone. It uses a simplified version of the dynamic programming, or time-normalized pattern-matching, method found in NEC's larger and more expensive DP series of voice input devices. The number of analytic channels has been halved to eight and the analog-to-digital conversion of voice amplitude conversion halved to 4 bits. In addition, the volume of operations and data was reduced to the point where an 8-bit central processing unit could handle it.

With 5-K-bytes of random-access memory to hold the reference pattern, NEC's unit can recognize up to 60 isolated words uttered by a specified speaker with a claimed accuracy of over 98%. The largest reference pattern size for any word is 80 bytes, and the average response time is 0.7 second. The host computer can display numerically the relative difficulty of recognizing each word registered, so that the user can determine the rejection threshold. With a mini-disk, the vocabulary or number of other specified speakers can be increased almost indefinitely.

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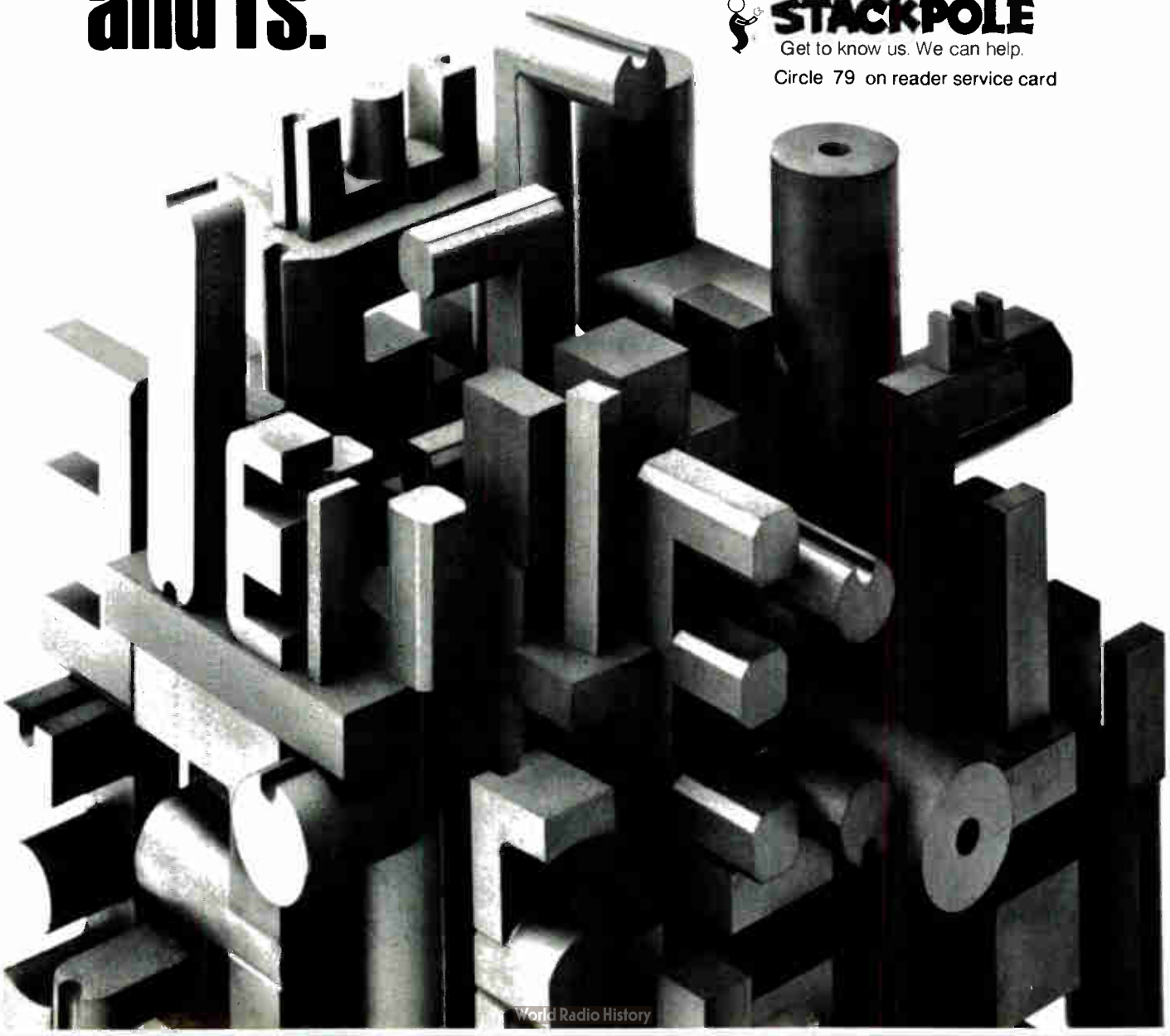


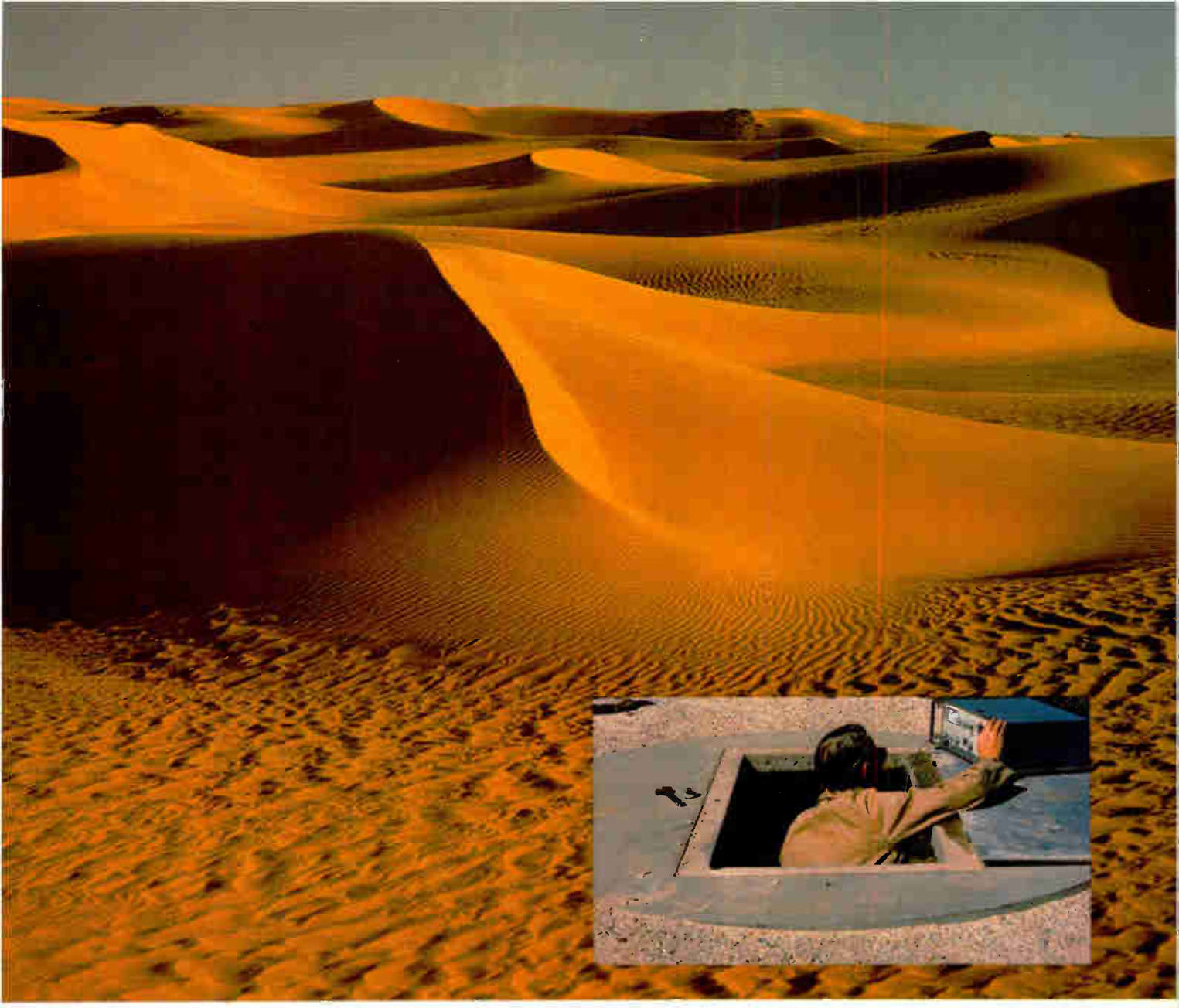
in Japan in July at a suggested retail price of $422. Sample exports are slated to start in September. "We think this will significantly increase demand for personal computers," says Tomio Goto. A supervisor in NEC's personal computer engineering department, he foresees demand from laboratory technicians, product inspectors, document handlers, and others who typically must stop all their other business to enter data via a keyboard.

Terser. Boasting their own onboard 8088 microprocessors, Sanyo's units offer a much smaller vocabulary at a much higher price. The SSR-16, for example, can recognize 16 words uttered by either of two specified speakers and will sell for $722 to $902 when it reaches the market in late June. A price for the SSR-32, which recognizes up to 32 words and will go on sale in the fall, has not been set. As the Sanyo units cannot be connected to disk drives, their vocabulary cannot be expanded. But their 98.7% accuracy and 0.5-second response time are an easy match for the NEC units and their versatility is superior.

Although first shown at the Microcomputer Show, the units' major initial applications will be with machine controllers operating with five to six switches, says Kiyoshi Tajima, chief engineer at Sanyo's research center. He adds that Sanyo late this year will announce a 48-word model using an 8086 16-bit processor. He says the company has not decided on production volumes for either the SSR-16 or -32 or on its export plans, but will respond to orders from overseas.

Sanyo's 192-by-260-mm boards contain two 32-K erasable programmable read-only memories and three 16-K complementary-MOS RAMs, eight hybrid LSI bandpath filters, and a 5-volt battery-backed power supply, in addition to the microcomputer and a tiny display. Also, a switch lets it designate one of two specified speakers.

In the U. S., Heuristics Inc. introduced its $275 H-2000 board module for insertion in the Apple computer in 1979. **-Robert Neff**



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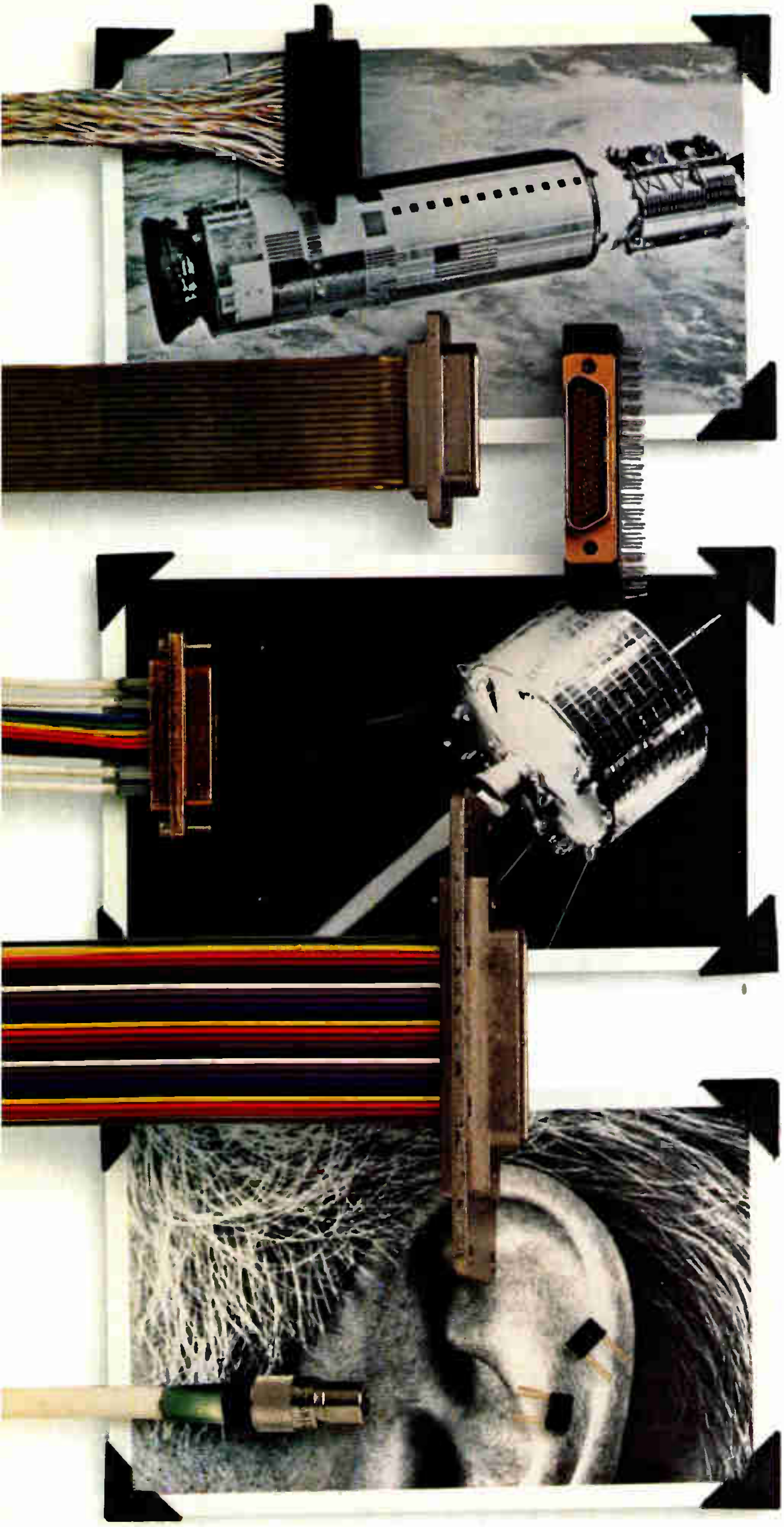

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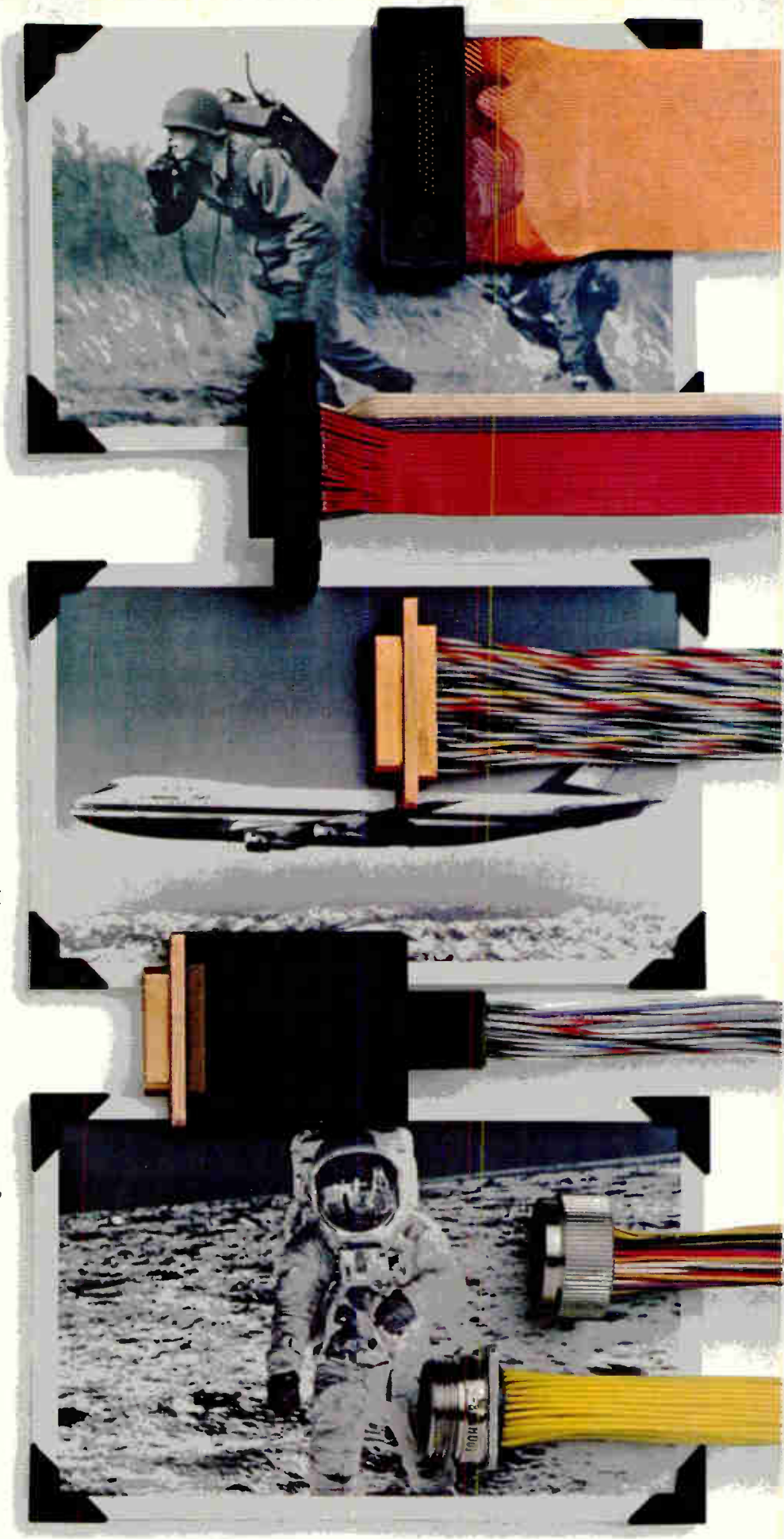

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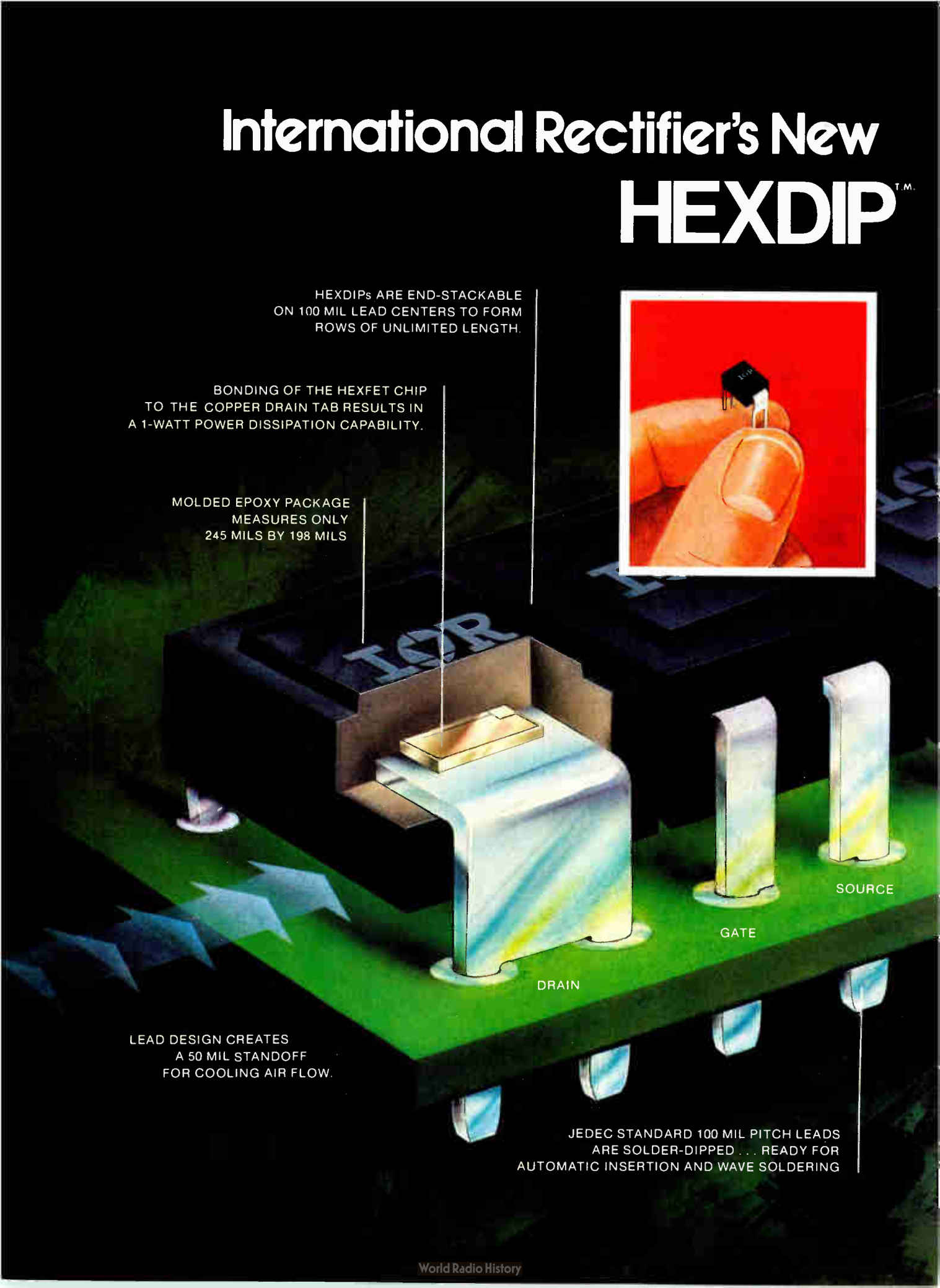

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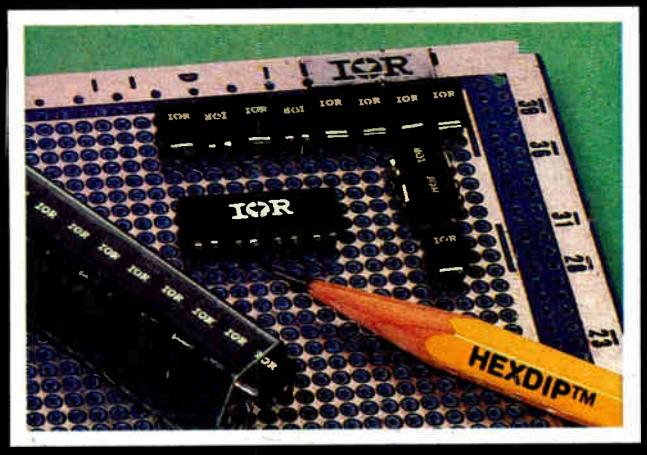

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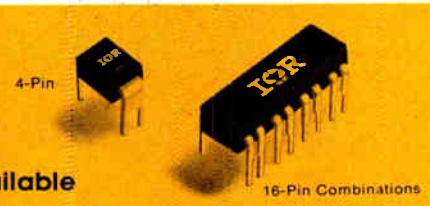

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	IRFD9121	-60V	0.6Ω	-1.0A
	IRFD9122	-100V	0.8Ω	-0.8A
	IRFD9123	-60V	0.8Ω	-0.8A

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	IRFE113	FOUR IRFD113 4-PIN HEXDIPs
P CHANNEL	IRFE9120	FOUR IRFD9120 4-PIN HEXDIPs
	IRFE9121	FOUR IRFD9121 4-PIN HEXDIPs
	IRFE9122	FOUR IRFD9122 4-PIN HEXDIPs
	IRFE9123	FOUR IRFD9123 4-PIN HEXDIPs
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Bumpy disks, CCDs dazzle CLEO

Conference on Lasers and Electro-Optics hears of 3M's recording technique and Hughes's method of converting electrical input into images

by Harvey J. Hindin, Communications & Microwave Editor

Two leading-edge technologies guaranteed to draw a crowd these days are video disks and video displays. Proof of this fact was offered at last week's CLEO—the Conference on Lasers and Electro Optics—in Washington, D. C., where a new laser blistering technique and a charge-coupled-device display captured the interests of the conference's participants.

The description of a technique utilizing laser-induced blisters, rather than the usual laser-burned pits, for information storage on audio-video disks was one of CLEO's highlights. The technique yields a high signal-to-noise ratio.

Developed by the 3M Co. in St. Paul, Minn., the method is seen as a replacement for the usual system by which optical recordings are made: a precisely focused laser burns out a pit on a recording platter to represent a digital bit. Thus, the beginning and end of the pit must be sharply defined to avoid optical and acoustic or visual noise.

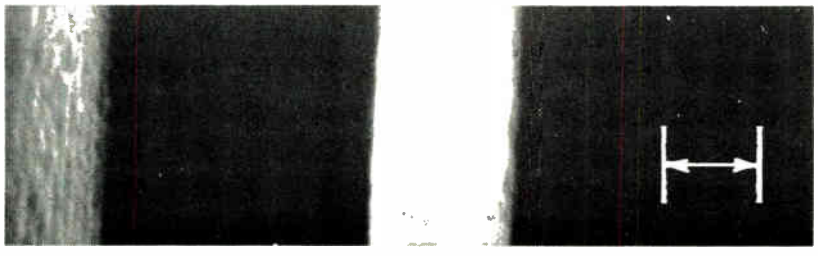
To achieve sharpness, 3M has replaced the hole with a bump. William Robbins and his colleagues placed a heat-resistant layer on top of the disk base material that rises, or bubbles, under the momentary 1,500° to 2,000°C temperature produced by the recording laser. According to Robbins, "the playback system can more readily differentiate a blister than it can a hole against a flat surface. A signal-to-noise ratio of 67 dB—which is more than adequate—has been achieved."

A disk the size of a 10½-inch phonograph record can hold 10 billion blisters, or binary digits. Each blister can be read or written in 50 nanoseconds, which corresponds to a data-transfer rate of 10 megahertz. "We are now working on making this rate higher," Robbins notes. Commercial feasibility of the blister disk is under study and a marketing decision is expected in the near-future, he adds.

Insiders believe the technique could provide a boost for the burgeoning digital optical-recorder–player industry. However, there is also the disk-playback problem. For example, the shortcomings of the laser diodes illuminating video or audio disks are well known. What is needed is a laser diode with a sym-

Photolithography: twice the resolution

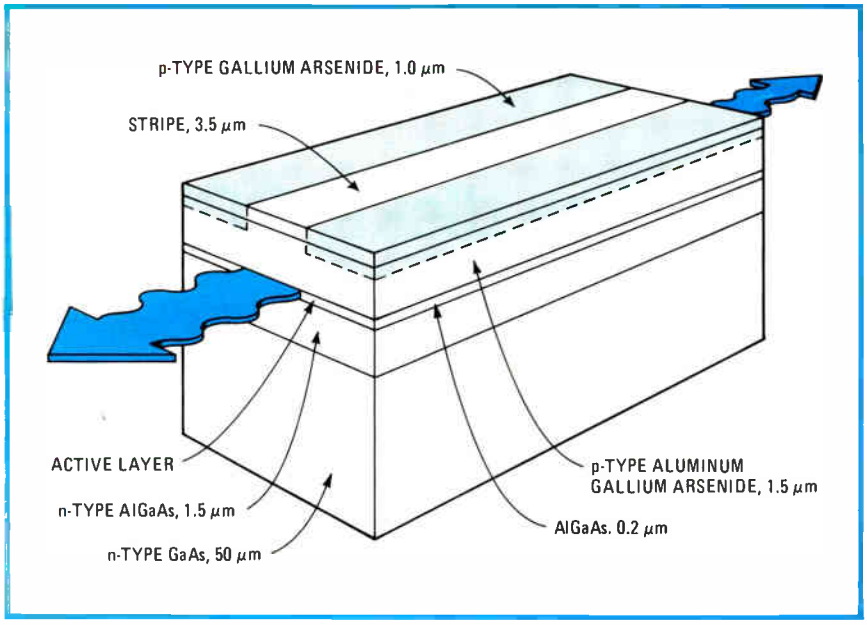
Researchers at International Business Machines Corp.'s San Jose (Calif.) Research Laboratory have developed a photolithography technique that offers great promise in very-large-scale integrated-circuit work. Called phase-conjugate waveform generation by degenerate four-wave mixing, it was described by Marc D. Levenson and J. K. Chiang at the Conference on



Lasers and Electro-Optics. Shown here is the 0.5-micrometer line they obtained with their method.

Levenson and Chiang report that this approach has already achieved twice the resolution of conventional methods and eliminates many of the problems of conventional optics. They use laser beams to project a perfect, distortion-free replica of a master pattern or mask into a photosensitive layer that covers a silicon substrate. The layer dissolves where light has been absorbed, baring the surface beneath for further processing. The developers say that their holography-like process, still under development to obtain brighter images, should be able to project images several inches in diameter with similar resolution.

In the IBM approach, light is transmitted through a mask carrying the pattern and interacts with two oppositely directed laser beams in an optical medium called the conjugator crystal. A new beam—the fourth wave mentioned in the title of the technique—that duplicates the beam from the mask is produced. Known as a conjugate wavefront, it behaves mathematically as if it propagated backward in time. The wave is then separated from the other beams by a beam splitter and directed onto the photosensitive material. This process is superior to conventional optical techniques because there are no lenses to cause aberrations. There also are no diffraction losses. **-H. J. H.**



Constrained. Philips semiconductor diode's low-index refractive layers constrain emitted light vertically. Laterally, confinement is accomplished by shallow proton bombardment, which leaves active stripe width undisturbed. The diode illuminates video disks.

metric, but not too narrow, beam, with stable, low-noise operation and no sensitivity to interference from light reflected back from the disk into the laser. And equally important to prospective users, any such laser diode must be relatively simple and economical to manufacture.

One company that is well aware of these needs because it manufactures a video-disk system is Philips Gloeilampenfabrieken in Eindhoven, Holland. Its researchers have come up with a hermetically sealed semiconductor-diode laser that Philips maintains will go a long way toward solving the audio-video disk illumination problem. As described at CLEO, the laser contains a monocrystalline gallium arsenide substrate carrying layers of the same material in which part of the gallium has been replaced by aluminum.

According to G. A. Acket of the research labs, "the laser beam is confined vertically by the active layer's being put between cladding layers that have a lower refractive index and act as a light guide." But the beam must also be laterally confined. "Normally, this is done by restricting the light generation to a narrow stripe-shaped region," Acket says. This is achieved by changing the resistivity of the material outside the stripe by high-energy proton bombardment.

While proton bombardment is simple and makes the diodes immune to reflected light, it also makes them somewhat nonlinear and unstable. The Philips scientists solve this problem by keeping the proton implantation shallow. This leaves the desirable properties of the active layer undisturbed. The result: a laser with a 3-to-4-micrometer stripe width that is stable up to 50 or even 100 milliwatts of output power.

No more scopes? The Philips diode and the 3M disk can go a long way to reducing the signal-to-noise ratio or error rate of a video–data-communication or processing system. But such information often must be processed and displayed. In conventional cathode-ray tubes, the variation in light output caused by decay in phosphor brightness as the CRT is scanned limits its usefulness for real-time optical data processing. So Jan Grinberg and a group of coworkers at the Hughes Aircraft Co.'s research labs in Malibu, Calif., have combined liquid crystals and a silicon substrate to directly convert an electrical input into a projectable optical image that does not fade out.

The Hughes group has demonstrated a 64-by-64-picture-element configuration that can be operated at rates up to 100 frames per second. This permits the creation and display of real-time video information in much the same manner as a standard home television, Grinberg says. Though the resolution of this first-generation device is limited to just a proof of feasibility, Grinberg notes that a second-generation (256-by-256-pixel) device will have resolution "approaching that available from 350-by-512 standard CRTs." Moreover, he anticipates it will have a high brightness, low operating voltages, and simultaneous output of all picture elements in the image.

The Hughes researchers made use of the fact that, as an electrically insulating material, a liquid crystal can sustain a two-dimensional pattern of local voltage variation imposed across it. This voltage variation in turn induces a replicating pattern of optical index variation that can generate an image whose brightness is directly controlled by the intensity of an illuminating laser.

The key to the success of the device is the means by which the two-dimensional pattern is applied to the liquid crystal. A thin, high-purity silicon substrate has one of its planar surfaces in direct contact with the liquid crystal. The opposite side of the substrate is attached to a charge-coupled array. As usual, each of the array cells represents one picture element and can store an amount of charge directly proportional to the amplitude of a signal applied to it.

The individual storage cells of the CCD are controlled by electrodes that, when activated, shift the signal charge in one element to the neighboring cell, as in any CCD array. This transfer process can be performed in both array dimensions. Thus, the array of picture elements is serially loaded to create a two-dimensional charge pattern that replicates the desired image.

After the picture fills the entire array, all the charges are transferred through the silicon substrate to its opposite face on the liquid crystal by means of an applied electric field. In the final step of the process, the charge pattern automatically imposes a corresponding voltage pattern on the liquid crystal. □

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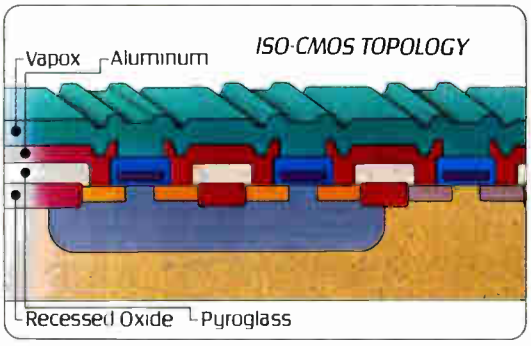

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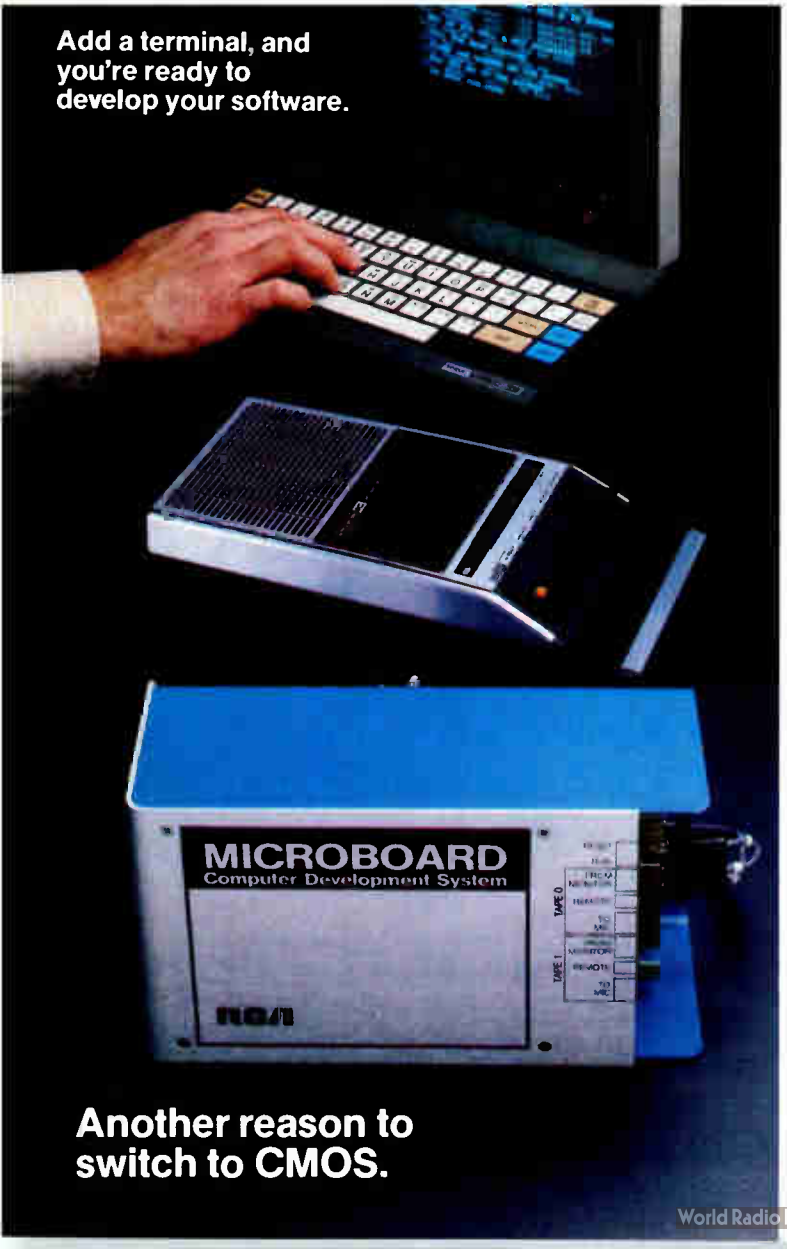
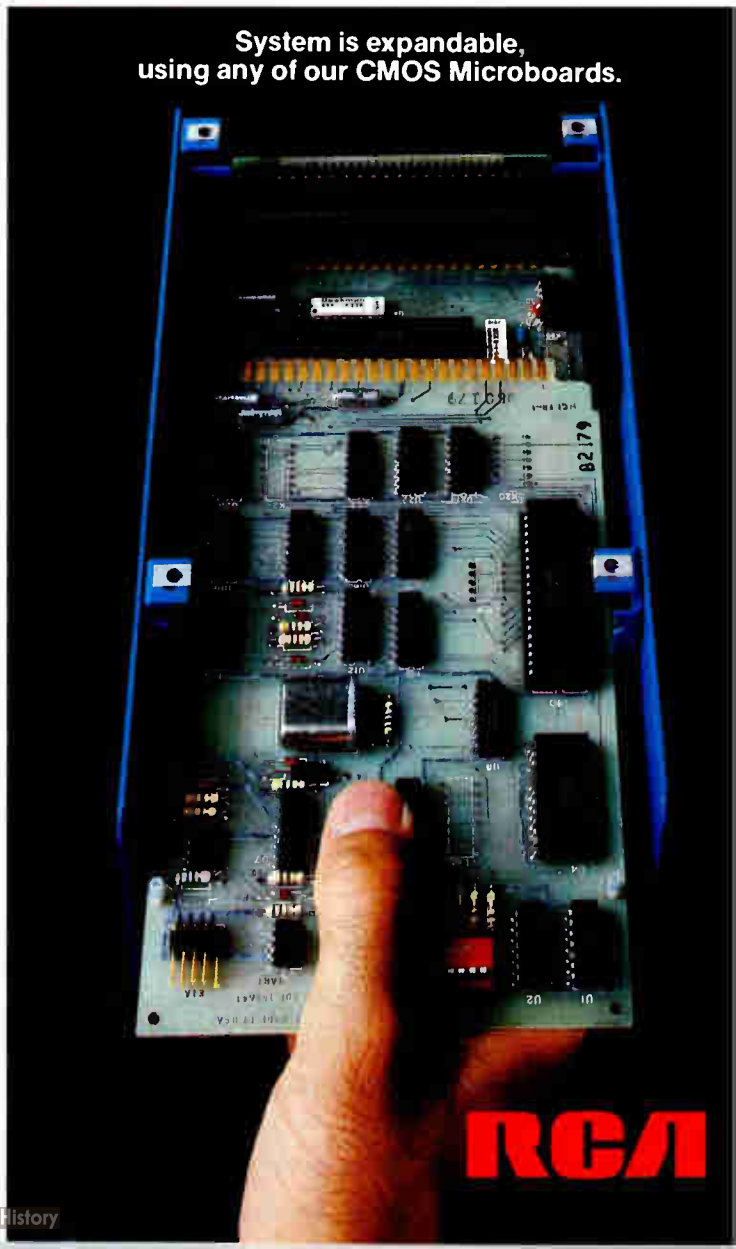




Memories

Will TI's defection pop the bubble?

Texas company's decision to quit bubble memories surprises some, but remaining makers say they still like what they see

by Howard Wolff, Associate Managing Editor

Can bubble memories compete against other magnetic mass-storage media—or, for that matter, dynamic random-access memories? For years, the three or four manufacturers of the solid-state devices had the same answer: their products would make it big when capacity and price-crossover goals were attained.

But now that Texas Instruments Inc. has changed its answer by deciding to drop out of the business, following Rockwell International Corp. by a few months, doubts about the viability of bubbles are surfacing. The TI move underscores the growing strength of competitors for the market as fast dynamic RAMs become less expensive at the top of the line and disk technologies, such as micro-Winchesters, gain capacity at the bottom of the market.

The problem that TI saw is that the potential market is not as large as the industry predicted, says Haller M. Moyers, assistant vice president and manager of the bubble memory program in Dallas. "It is a niche market," he concludes, "a market for a much smaller range of applications than we had envisioned back in the 1970s when the whole effort started to expand. Now nobody is saying seriously that it's billions of dollars in 1985, or anything like that." TI decided late last month that bubbles and other product lines were not earning their way (see "TI decides it's time to go," p. 94).

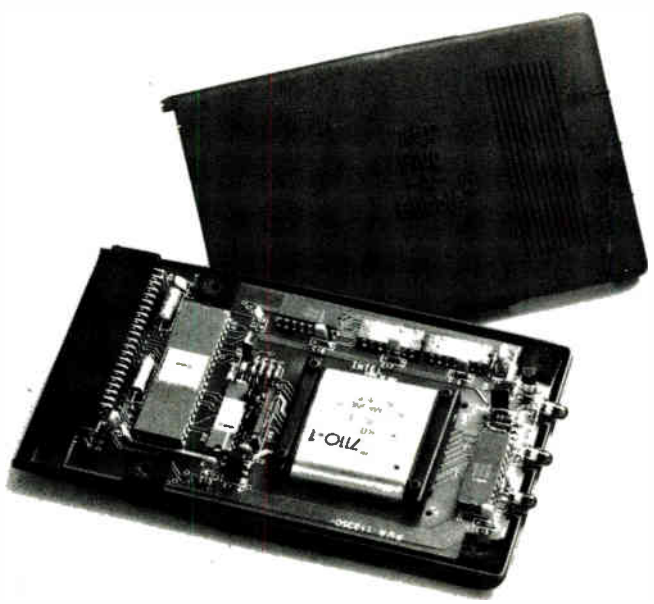
The decision surprised many industry observers. The Dallas operation, which in 1976 offered the first commercial bubble memory, an oddly configured 92-kilobit device followed by an equally nonbinary 254-k part, had begun delivery of its first 1-megabit parts this quarter. For its Silent 700 data terminals, TI will continue to use bubbles in four models. The company "will make a lifetime buy from the operation and also consider possible alternative sources," stresses a spokesman for the company.

The group. TI's departure leaves the commercial field to Intel, National—and its second source, Motorola—Fujitsu, and Hitachi. To them, the promise of bubbles is still seductive: they tend to see TI's move as a reflection of its own production problems rather than disappointment at the market potential.

There is no change in his company's commitment, says Stewart F. Sando Jr., marketing manager of the magnetics operation at Intel Corp. in Santa Clara, Calif. "Intel's approach is on course," he says. Though it has no second source, it believes that its guaranteed pricing program will assuage customer fears. What's more, last month it committed an extra $3 million for assembly and final test equipment and has been adding personnel since January.

Sando says that the world market for bubble components and large-scale integrated circuit support chips will be $30 million in 1980, $45 million in 1981, $90 million in 1982, and $350 million in 1984. He breaks it down as 40% to 45% in Japan and the rest in the U. S.

Jim Cunningham, director of bubble memories at National Semiconductor Corp. in Santa Clara, Calif., says yields were too low for TI's taste on the quarter-, half-, and 1-Mb models. "TI tried to leapfrog the industry with its top-down process, which promised greater density," he says. "The problem was in getting it to work. They announced it two years ago with support circuits,



Disk competitor. Intel's plug-in bubble memory cassette occupies the same space as a 5.25-in. mini floppy system. It is aimed at applications in harsh environments or where nonvolatile data storage is required.

Probing the news

and as far as I know they still don't have the support circuits." In fact, when TI told of its plans for two families of those circuits, only one was to have error-correction capability, betraying the uncertainty about the market on TI's part.

However, Cunningham concedes the rosy view that bubbles would supplant RAMs in many areas has evaporated. The reason, he says, is that "RAM prices dropped well below the curves that were extrapolated from experience." But he points out that RAMs are volatile, and the "nonvolatile memory market is where we are seeing design-ins."

The overall market, Cunningham estimates, totals about $45 million a year in Japan by all vendors, and $25 million to $30 million in the U. S. In Europe, samples are just starting to be shown. In those markets, says Cunningham, "we weren't seeing TI in the field, but we were seeing Intel and sometimes Fujitsu."

New plant. For Motorola Inc.'s part, one gage of its commitment to bubbles is an 11,000-square-foot plant in Tempe, Ariz., that will be completed next month. The Motorola Integrated Circuit Applications Research Laboratory will move its bubble production into the facility, says Leonard Call, bubble systems marketing manager.

"We see a lot of activity and growth, with a lot of interest in the smaller size systems and subsystems—the 1-to-2-Mb range," says Call. "The 1-Mb device level is the area where market shares are going to be determined and it will be the battleground." He foresees only a short-term negative feeling.

In Japan, Fujitsu Ltd.'s intentions can be judged by its introduction of two microcomputers incorporating 32-K-byte bubble cassettes now with 128-K bytes later [*Electronics*, June 2, p. 63].

As for the future of the technology, perhaps National's Cunningham best sums up the consensus of those in the business when he says that TI's decision must be viewed in the context of its total adjustment. "TI had a general cutback; I believe that is the way to view it, rather than as a marketing statement about bubbles. I think they just decided that the processing and support-circuit effort that they would need to compete was not worth the resources they would have to commit." □

TI decides it's time to go

Texas Instruments Inc. didn't limit its retrenchment to a decision to get out of bubble memories. The big Dallas firm also decided to stop making digital wristwatches as well as plasma displays—although the display effort was relatively new—and laid off 2,800 employees.

On the watch front, erstwhile TI competitors interviewed at last week's Consumer Electronics Show in Chicago saw its move in a variety of ways. Some of the opinions were that the company's timing in the business and its understanding of it were both poor and that the effects of the pullout wouldn't last very long. Frank McMahon, vice president of marketing for Casio Inc.'s timepiece division, says TI's first mistake was to stick too long with light-emitting-diode displays. "Part of TI's problem is they got into the market with their own technology," says McMahon. "It's a classic story of an organization that grew strong because of its technology and then changed slower than the technology."

Another mistake was TI's marketing tactics, according to Keith A. Drucker, marketing manager for Marcel Watch Corp., New York, N. Y., a major independent watch supplier. "They came out with a $10 watch and lost $10 million to $20 million to gain market share. That's all right where the margins are good, but there are no margins in the watch business. An efficiently run outfit has maybe a 20% markup," says Drucker. The pullout will mean a drop in prices at first, and then a rise after the end of the year, says Drucker. "Initially, there will be a scare in the market" because of dumping, he predicts. Also, "merchandise will be short," says McMahon. "I don't know if we can handle the retailers who were committed to TI." Casio sold 2.5 million watches in 1980 and expects to sell twice as many this year. **-Gil Bassak**

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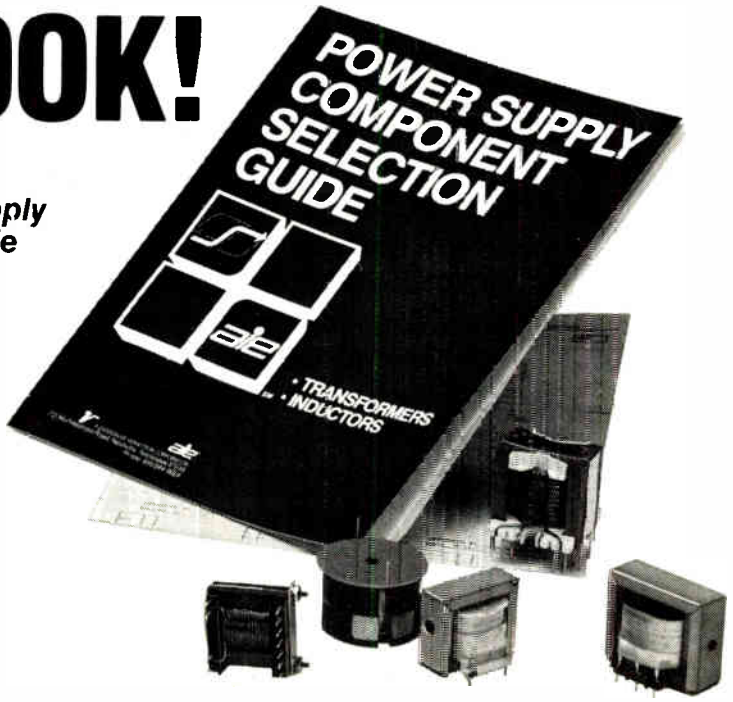

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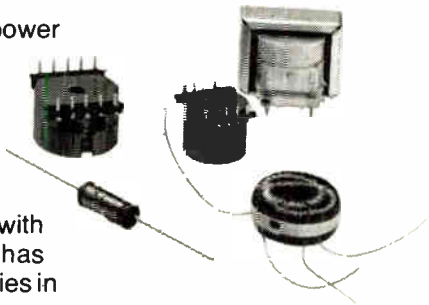

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Business

Electronics firms avoid layoffs

Despite TI's and Mostek's moves, difficulties after 1974–75 slump inspire alternative methods of dealing with slowdown

by J. Robert Lineback, Dallas bureau manager

With the presence of Japanese memory manufacturers heavily on the minds of U. S. electronics executives, their companies are playing a worrisome waiting game with soft markets, lofty interest rates, and troubled world economies.

Not wanting to jeopardize their ability to bounce back when the recovery finally arrives, a number of manufacturers are taking whatever actions possible to avoid the costly move that many took in the last major recession—layoffs. Across the nation, electronics companies are reporting reduced work schedules, curbed hirings, and planned plant shutdowns for mass vacations.

Reflecting on the past, most experts agree that the 1974–75 layoffs and cutbacks in capital spending and research and development severely impaired the U. S. industry's ability to match market demands when the economy got back on its feet later in the decade—thereby opening the door for greater Japanese import activities. Today, most industry analysts conclude that the long-awaited economic upturn must appear within sight by the beginning of 1982 or many firms will begin to do what they are desperately trying to avoid.

But in a surprise move late last month, industry giant Texas Instruments Inc. stunned the experts by announcing the reduction of its worldwide work force by 3%—2,800 jobs—and the phasing out of over a half-dozen product lines, including the firm's highly visible magnetic-bubble memories and digital watches (see p. 93). On top of that, the Dallas firm is considering further trims in capital outlays this year, by as much as 10%.

R&D funding untouched. Earlier this year, TI had set capital spending at $450 million for 1981, 18% below the previous year's figure. But the corporation says that TI-funded research and development will remain intact at $220 million, 16% higher than in 1980.

"We went ahead and bit the bullet, I guess," says TI senior vice president Grant A. Dove, a member of the firm's operating policy committee who also is in charge of corporate marketing. "We had the option of continuing the short work schedules [*Electronics*, May 5, p. 46] or going ahead and making adjustments to get back to 'normal.' " With the layoffs and early retirements, TI hopes to end the reduced work schedules in the third quarter. At the beginning of the year, the company placed 17% of its 90,000 employees on shortened work weeks, but that number was reduced to 10% in the spring.

Meanwhile, industry reaction to the layoff has been consistent: few other electronic firms are planning future permanent layoffs. But that's not to say other manufacturers are not feeling the squeeze. One that is, in TI's own Texas neighborhood, is Mostek Corp. in Carrollton, which is continuing its reduced work schedule after laying off 82 workers in April and 333 more last week. Mostek, like most semiconductor makers, is

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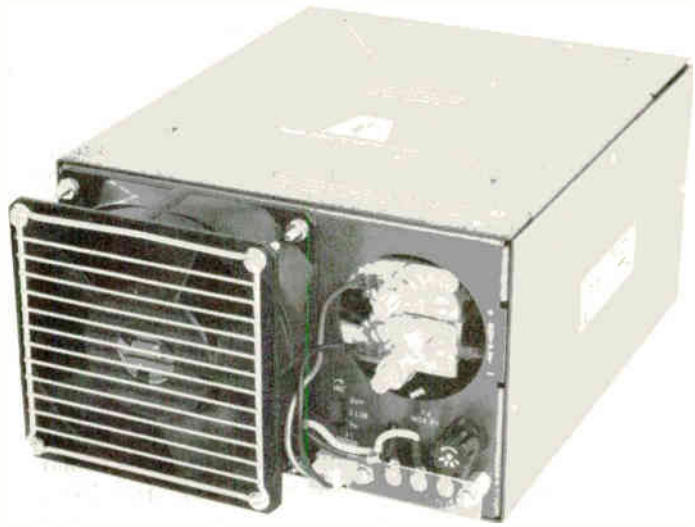

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also closing its main plant for two-week mass vacations this summer. Mostek plans to return to full work schedules on July 13.

In Santa Clara, Calif., Monolithic Memories Inc. has scheduled a series of week-long plant closings—the next to come the week of July 4. Elsewhere in Silicon Valley, American Microsystems Inc. has implemented a hiring-wage freeze this quarter. National Semiconductor Corp. and Tektronix Inc. have both pared production schedules during recent holidays, and Advanced Micro Devices Inc. plans to shut down its facilities for two weeks of mandatory vacations.

Intel Corp., also in Santa Clara, appears to be bucking the trend, with chairman Gordon Moore announcing at last month's annual meeting that the firm is, in fact, "actually hiring at a modest rate." Most firms indicate they are continuing to hire new college graduates and are still recruiting for their R&D operations.

No gloom. Cautious optimism prevails in other parts of the nation. At Motorola Inc., William Howard, vice president and director of technology and planning for the Semiconductor Group in Austin, Texas, says, "We feel that there are still going to be months of slowness in the market as a whole coming up, and we're certainly not expanding." Motorola's semiconductor operations in Arizona and Austin are not anticipating furloughs but are reporting a curb on hiring.

But at Sperry Univac's captive semiconductor operation in Minneapolis, activities have been brisk for the past year. Its work force has shot up from 240 to 540 in just a year's time. Control Data Corp., also in Minneapolis, says it is looking for "continued steady growth, and that implies a certain level of stability for the labor force." And in Colorado Springs, Colo., Inmos Corp., the British-majority–owned MOS maker that is planning to introduce its second memory product soon, says hiring has improved a bit.

Meanwhile, conditions appear to be better for electronic distributors, according to George E. Greene, director of systems business development for Hall-Mark Electronics Corp. in Dallas. "As far as the work forces, distributors are not seeing the same problems as the semiconductor manufacturers," Greene explains. "We are actually shipping more semiconductor products at this time but at the same amount of dollars." He also says that system product markets are stable, with the exception of development systems and board level products. He cites the customer switching from 8-bit to 16-bit systems as being a major reason for these slumps.

Problems abroad. Most analysts, too, are not expecting other electronics manufacturers to follow TI's lead. Many say the dramatic move can be linked directly to TI's own trouble spots: a slumping European economy, lack of solid 8-bit and 16-bit microprocessor business, too much dependence on MOS (in particular memories), and a sputtering consumer electronics operation.

But TI maintains that its No. 1 problem is not Europe or product mix. "From where I sit, the major question is what is going to happen with the interest rates," Dove says. "That's probably the most significant factor that is affecting our customers' decisions on whether to buy or when to buy. There are a lot of postponements, in particular by smaller companies, which have an impact on end-equipment markets and therefore component markets."

TI's phaseout operations—which also covers plasma panel displays, distribution in the U.S., appliance electronics, and "selected lines of low-margin discrete semiconductors" (silicon small-signal devices)—are being made because "returns are inadequate and prospects for future returns are judged insufficient to justify continued investment," the firm says. TI has already said that it will sell its electronics distribution inventory and certain other assets to Kierulff Electronics Inc. of Los Angeles.

TI says the work-force reduction and possible cut in capital spending will not impair its ability to bounce back once the economy recovers. "We'll be prepared to go full speed ahead," Dove vows. □

Consumer electronics

Walk-around radio market crowded

Lightweight stereos with headphones have attracted 30 or more manufacturers to a market that was opened by Sony in 1979

by Wesley R. Iversen, Chicago bureau, and Gil Bassak, Industrial/Consumer Editor

Much to the surprise of audio equipment manufacturers and industry observers alike, the new genre of portable mini-micro stereo cassette decks has become one of the hottest audio consumer items going. Sales are going nowhere but up. And the products themselves are going everywhere with buyers, from jogging to shopping to commuting.

"When we first introduced these, we were asking ourselves who was going to want a $200 tape player that didn't even record," admits one official at Sony Corp., where a brainstorm by board chairman Akio Morita is said to have been the genesis of the Sony Walkman introduced two years ago in Japan.

Since the Walkman was brought to America in December 1979, 30 to 50 competitors have jumped in with similar products. The most optimistic forecasters are expecting a 6.5-million-unit worldwide market for the product type this year. Sony is believed to have 50% of the market.

The key to the miniaturization and sound quality is a samarium cobalt magnet in the headphones. It produces a very high flux density and hence more sound from less energy. Also important is the Mylar drive element, which is small and lightweight. It is housed in a tuned cavity, open-air enclosure, which also bolsters sound quality.

The portable, "personal" machines—now available in a variety of iterations, including a-m and stereo fm radio as well as record-playback cassette—are the next step in a natural progression for consumers who have been conditioned to high-quality stereo music, figures Mark Friedman, national sales manager for Onkyo USA Corp. of New York. Or as Yao Hwong, president of Simon Electronics Corp. of Taiwan puts it: "People will expect their hi-fi equipment to be as compact or convenient as their calculators and cameras."

Setting up shop at this month's Summer Consumer Electronics Show in Chicago, a year-old Houston firm known as Technidyne Corp. was one of the splashiest among the multitudes showing personal portable stereo products. The Technidyne booth featured young women wearing the firm's new model 140 hip pocket stereo while riding a bucking mechanical bull. Nearby, company officials touted the benefits of the $139.95 unit's built-in dynamic noise-reduction chip supplied by National Semiconductor Corp., Santa Clara, Calif.

Toshiba, Panasonic, and General Electric were among industry heavyweights showing off their personal stereo product lines at the show. And Sony Corp., not resting on its laurels, brought out three new Walkman family members. The SRF-40W, an fm stereo receiver version, comes with a suggested $89.95 retail price. The new Walkman II, priced at

Sound moves. With the burgeoning success of the market for portable cassette players, Sony is coming out with three new models (below). Also in the field are such firms as Technidyne (right).

Zilog's Z80® family: The industry's number one choice.

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Probing the news

$179.95, will replace the original Walkman. The play-only cassette machine offers soft-touch controls and an improved counter-inertial flywheel system that Sony says enhances sound quality. In addition, Sony says it is actually smaller than a typical plastic cassette holder. The third new machine, known as the Walkman I, is a larger, cassette-play unit priced at a more economical $99.95 in a move designed to appeal to the teenage market with a limited disposable income.

The future. While the world is seemingly rushing to standard cassette-size products, a few firms at CES were giving a glimpse of what may be the size and shape of things to come. Panasonic Co., Secaucus, N. J. demonstrated its GZ-7, a playback-only unit that uses smaller microcassette tapes. Currently being sold in Japan, the GZ-7 is not yet available in the U. S.

Fisher Corp. of Chatsworth, Calif., has been offering since January the PH M20, a $199.95 play-only microcassette personal portable. And at the Chicago show, the firm unveiled a combination unit known as the Micro Kangaroo. That system consists of a 13-by-3.66-by-2-inch a-m–fm stereo receiver "mother" unit with two 3-in. speakers that also houses a drop-in microcassette record-playback "baby" unit. Measuring 5.25 by 2.5 by 1 in., the baby has its own set of headphones and can be used by itself as a portable unit to play radio programming recorded from the mother. The Micro Kangaroo carries a suggested selling price of $399.95.

Interestingly, the new personal stereo products seem to be creating their own market. They are not cutting into sales of the larger, heavier, portable chrome-laden boxes. According to Michael Koss, an official with Koss Corp. of Milwaukee, the trend bodes well for the portable audio industry. Koss expects a $2 billion annual U. S. market to emerge by 1985 for mini-micro personal stereo and boom box type products combined. And that, he points out, is nearly equal to the entire U. S. hi-fi market today. □

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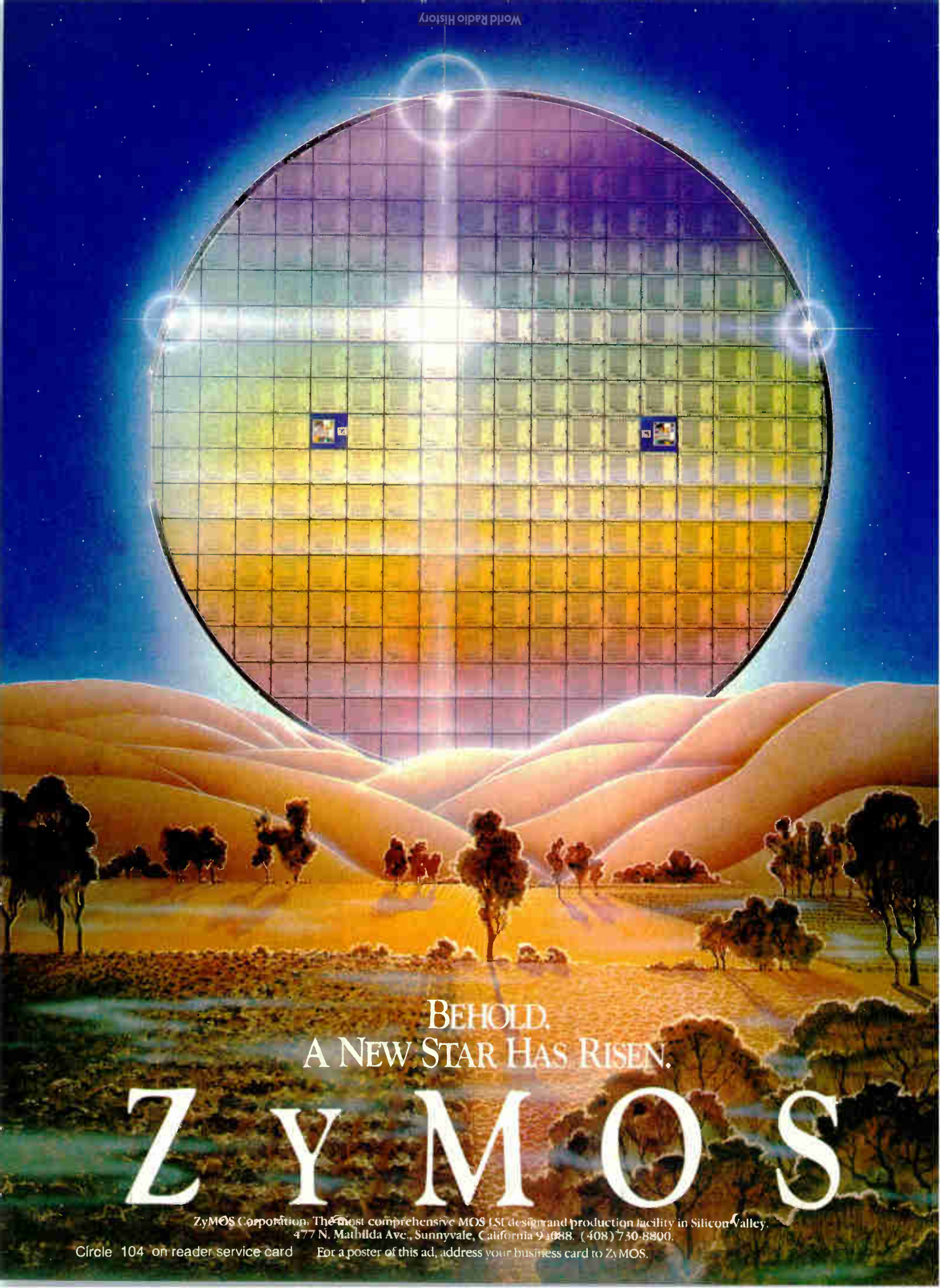

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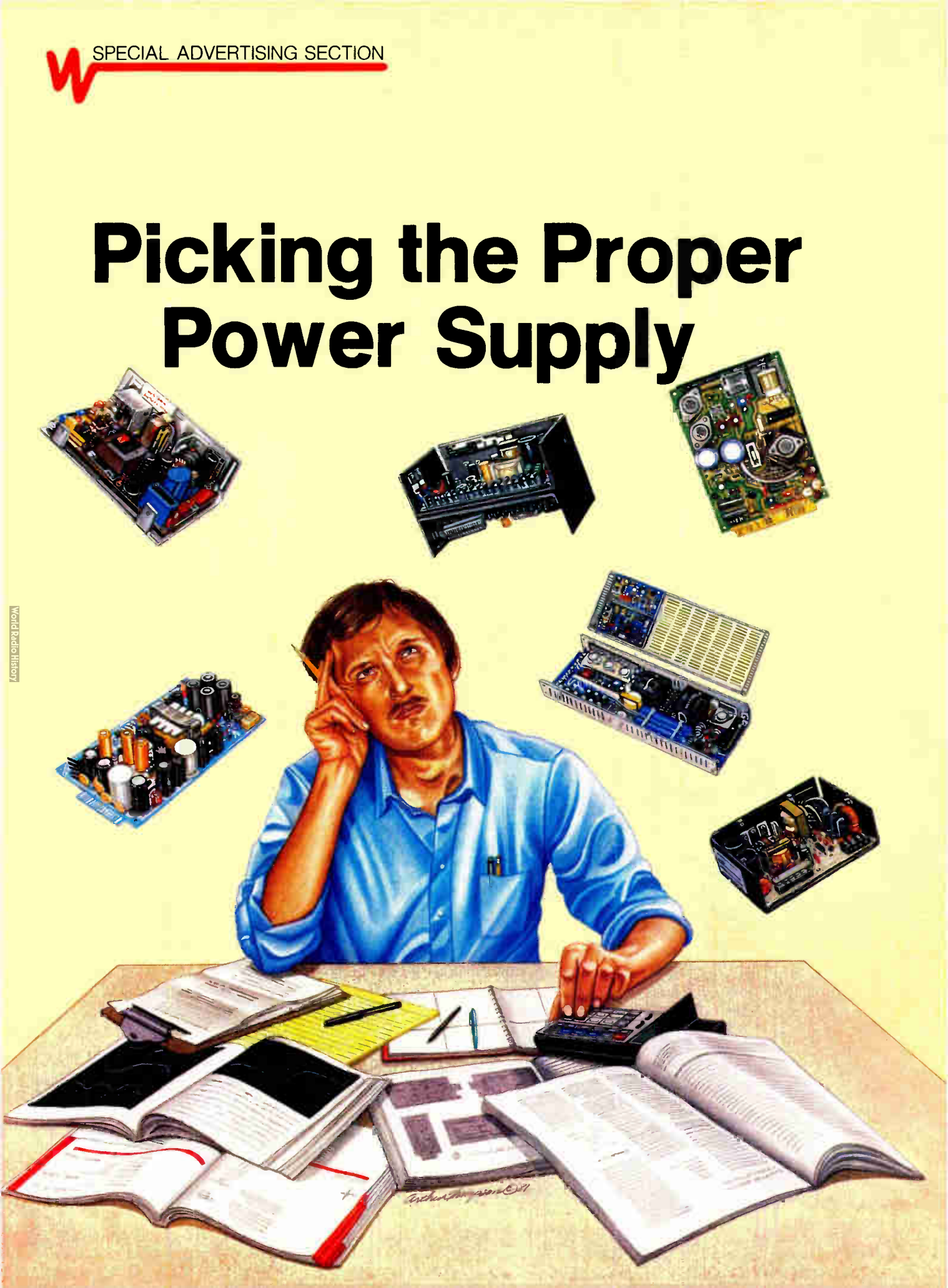
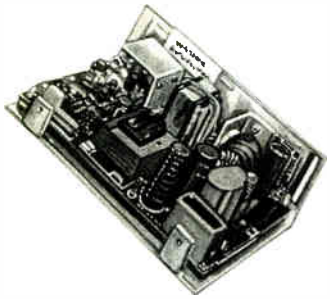
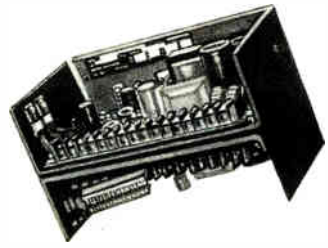
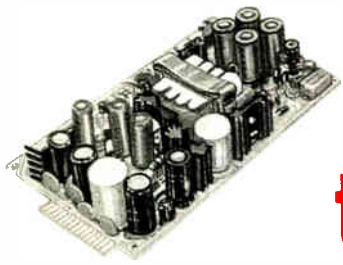
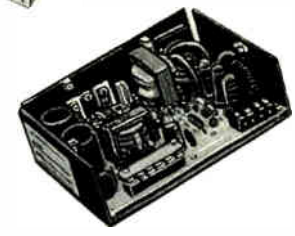
Picking the Proper Power Supply











Picking the Proper Power Supply

For the most part, the power supply is the silent partner among the gear that makes up a typical electronic system—and that's as it should be. Everyone involved, from the designer to the user of the equipment, expects the supply to perform consistently and reliably without calling attention to itself.

However, in these days of more exacting demands on efficiency and ever increasing cost pressures, power supply specifiers are taking new looks at their choices. Are they getting a supply that uses the least amount of power possible for a given application? Does the unit specified deliver the reliability needed at the lowest possible price?

Other longstanding concerns are assuming new prominence, too, for today's increasingly complex electronic system can be much less tolerant of supply foibles than in the past. So specifiers are taking a new look at parameters like line and load regulation, heat, and noise.

Sometimes, in fact, picking the proper power supply can be an exercise in frustration and bewilderment—especially if the specifier is essentially a system designer who comes to the task with little experience or practical knowledge of supplies. Then, too, the task is made no easier by the myriad of potential sources for the proper supply, each of them firmly convinced he has the only answer to the question, "Which supply?"

So, whether one is an old hand at specifying power supplies or new to the job, it pays to review the major considerations that go into the decision. The four sections that follow help in doing just that, for they are designed to serve as an update for the experienced hand and a thorough introduction for the neophyte.

One good source of information on power supplies is their manufacturers, and a number of them contributed their comments in response to a questionaire sent out during the planning of this special advertising section. Not surprisingly, their opinions sometimes differ, but the spectrum of responses will aid the specifier in learning more about power supplies.□

The editorial matter in this special advertising section on power supplies was prepared by Peter N. Budzilovich, a consultant in corporate and technical communications with a background in editorial, engineering, and marketing work.

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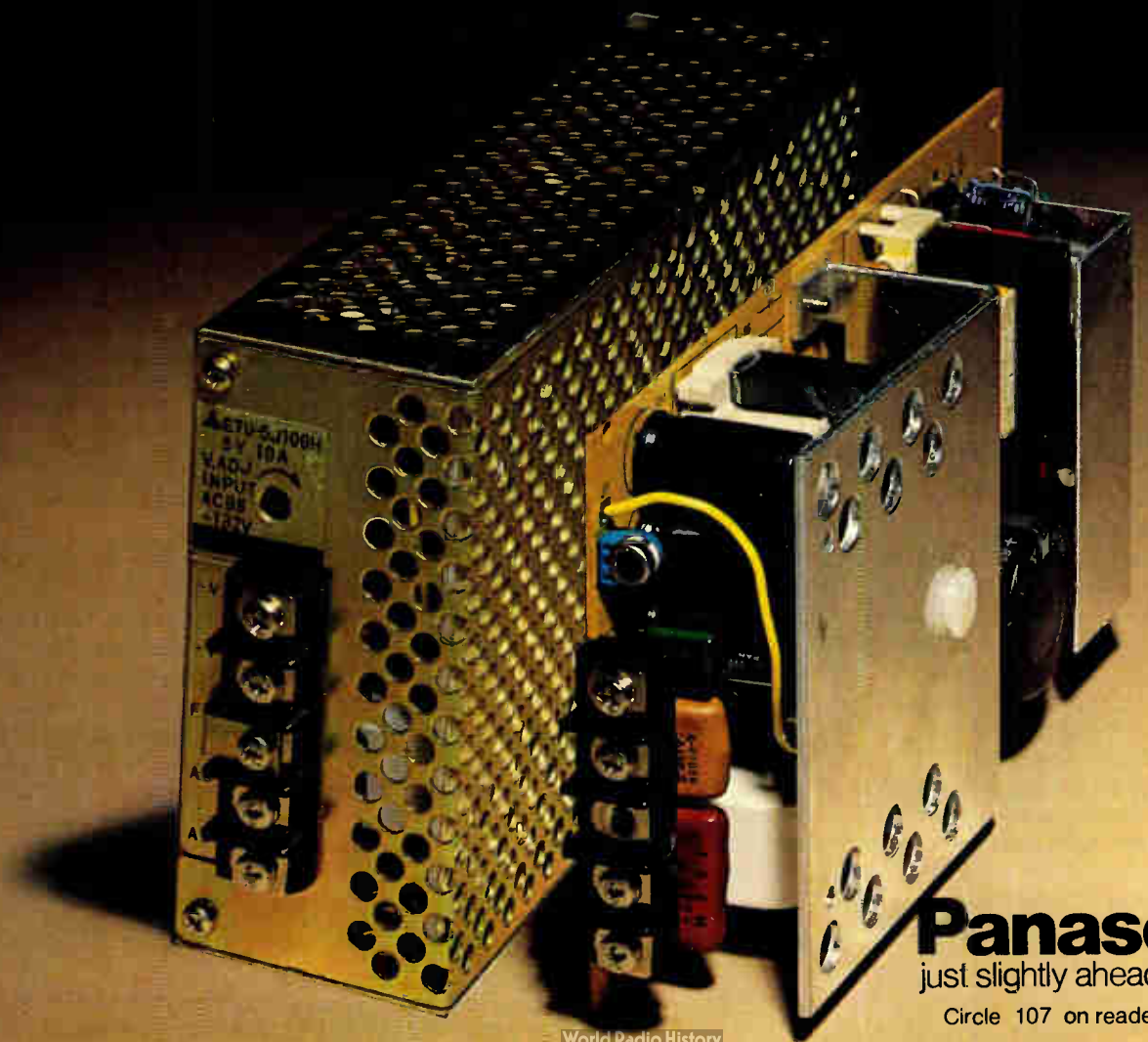

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THE SUPPLY SPECIFIER HAS A BASIC CHOICE

There are Two Main Types of Power Supplies: Linear and Switcher; And Each Has its Advantages to be Considered Carefully

The first question for any electrical engineer choosing a supply is whether to opt for a linear unit or a switched-mode power supply. The tried and true linear supply is getting a tough run for its money from the newer SMPS that regulates power through pulse-width modulation.

Advocates of the linear supply argue that the battle is far from over. On the other side of the field are such confident switcher supporters as Richard D. Okada, vice president for marketing at RO Associates Inc.: "The future of power supplies is switchers, and the future of switchers is open frame. Switching companies will capture a large portion of the captive [in-house] market, not due to economics of marketing, but due to the technological expertise needed to build switchers.

"Two years ago, switchers accounted for 10% of the power supply market. Today switchers make up 25%. By 1985, it is predicted that 50% of all power supplies will be switchers, and by 1990, 90% of all power supplies will be of the switching type."

Prices are dropping

Behind such predictions of a rosy future for switching supplies lies comparisons such as those made by Kenneth S. Lauchner, vice president of engineering at Sierracin/Power Systems. He contrasts the prices of 30- and 60-watt linear supplies from a competitor with equivalent Sierracin SMPS models (actually, at the 30-W level, the linear puts out 5 volts dc at 6 amperes versus 5 Vdc at 7 A for his unit).

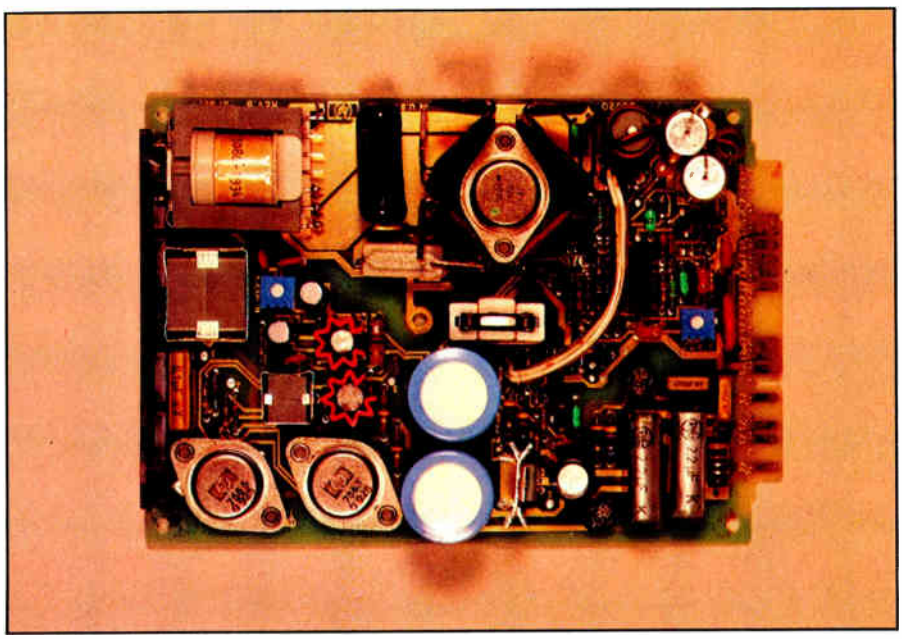
At these lower power levels, switchers have dropped below the competition on pricing. The 1-to-9 prices for the linears are $49.95 for the 30-W model and $79.95 for the 60-W unit. This compares with $45 and $75 for the switchers, respectively.

"In addition to being priced considerably lower than the comparable linear supplies, these switching supplies operate with input voltage fluctuations over twice as wide as linears and have 16 milliseconds of hold-up time [the ability to maintain an output voltage and current for a short time after an input interruption]," says Lauchner. "Also, they offer the traditional size, weight, and efficiency improvements characteristic of switching supplies."

However, the switcher versus linear choice is not that clearcut, according to Steve Cole, executive vice president of Power-One Inc. "Obviously, each has its advantages," he says.

"Linears are low in cost, have time-proven reliability, availability, and a good understanding by people in all industries of the operation of linear regulators. This means that field repairs can be accomplished by most any level of competent technician.

"Switchers offer higher efficiency, smaller size, less heat dissipation, lighter weight, and a general evolution of switching technology towards higher



Proving their 200-kHz switching approach with high-voltage power MOS FETs, Hewlett-Packard Co. has a family of 50-W switchers. It consists of eight different models ranging from a single- to a six-output units with 1,000-lot prices varying from $154 to $209, respectively.

reliability," he continues. "In other words, many applications could be filled with either linears or switchers, and in most cases the decision is made on cost and availability of the product and the reputation of the potential vendor."

Another switcher enthusiast, Robert Lloyd, president of Conver Corp., puts it this way: "Switched-mode *will be* more reliable and lower cost across the board. Reliability is primarily a function of the number of highly stressed components, not total component count. Certain switched-mode designs have fewer stressed components than linear supplies.

Linear vs. Switching Power Supplies

	Linear	Switching
Power output, W.	300	300
Output voltage, Vdc	5	5
Output current, A	60	60
Ripple voltage, p-p	5 mV	50 mV
Line regulation, %	0.2	0.3
Load regulation (50%), %	0.2	0.3
Efficiency, %	35	75
Case temperature, °C	100	35
Weight, lbs.	30	8
Volume, in^3	730	200

Inherent Reliability

"This, coupled with the fact that the higher efficiency makes the average temperature lower in SMPSs, means that they are inherently more reliable," he adds. "Since most of the industry volume will go to SMPSs due to their other advantages, their reliabilty will become superior to linear due to practice and engineering emphasis."

Until recently, price competition has existed only at higher power levels—but Lloyd says the cost will become less for SMPSs at all power levels because they use less raw materials and labor; with higher production, the learning curve will come into play and more engineering dollars will be spent to make them less costly; and the higher volumes will bring more competition. "SMPSs are or will be much smaller, much lighter, much more efficient, more reliable, and lower cost; therefore, the whole market will want to change over"

A somewhat more restrained opinion comes from Mord Shamir, product manager at Hewlett-Packard Co.: "Regulation and low ripple will continue to be the forte of linear supplies, but their choice over switchers will come with growing economic penalties." Similarly, Wally Resnick, product manager at Panasonic Co., says, "The new development that might happen in the 'battle' between switchers and linears is that the switchers will come down in price and will improve their regulation."

Linear Support

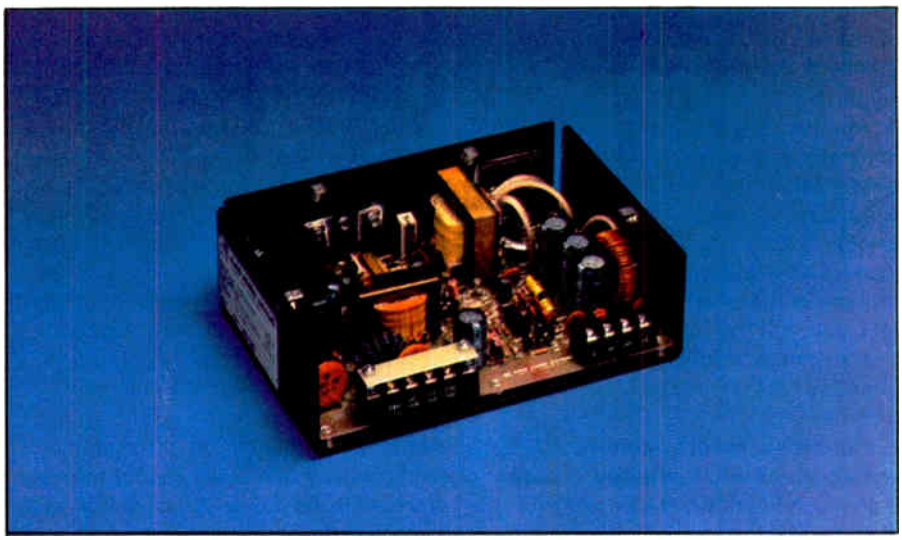
On the other side, a strong argument for linear supplies comes from Kurt Monsell of Acme Electric Corp. who says, "Contrary to popular belief, the linear regulated power supply is not an endangered species." He presents a list of linear advantages:

- Lower component count.
- Better reliability.
- Well-proven technology.
- Extremely low output ripple and noise.
- Inherent lack of electromagnetic interference.
- Easy meeting of UL and VDE safety requirements.
- Lower cost.
- Simplicity in testing and troubleshooting in the field.
- Readily available parts.

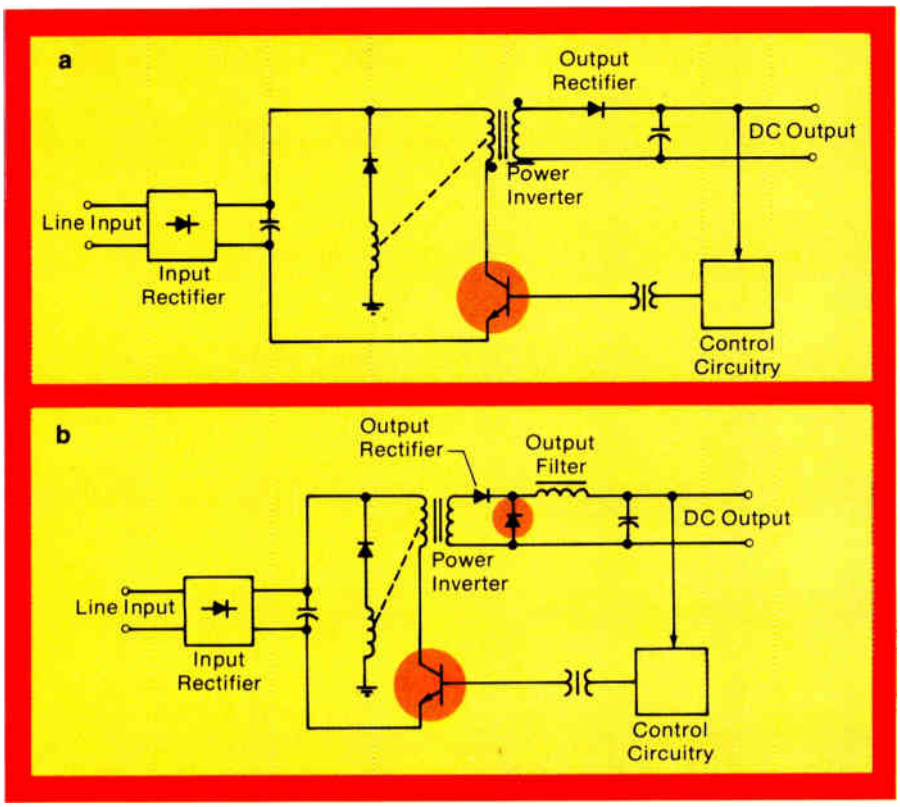
So the answer to the question of linear versus switcher does not come easily. However, some generalizations are in order based on a comparison of specifications (see table).

Linears are and will be used in applications where it is desirable to have a very tight envelope on such disturbances as line change, load change, temperature change, ripple, and noise deviations. The response of a linear supply is very fast; thus when there is an abrupt change in the load, a fast recovery takes place because of the speed of the linear error amplifier. As far as periodic and random deviations (noise) are concerned, a linear supply will overcome them much better than other supply types.

In terms of weight and size, switchers beat linears by a factor of about 4 to 1. Also, they offer efficiencies between 60% and 90%, versus 30% to 50% for the linears. They can be built with volume factors between 0.5 to 1.0 cubic inch per watt, compared with 2 to 3 in^3/W for the competition. Finally, switchers have a much greater output hold-up time, typically 20 to 40 ms. Since short power failures (for the



A family of switchers from Elpac Power Systems, the Series ES130, demonstrates the low component count used in this second-generation power supply. Putting out 150 W via its four outputs, this model sells for $182 as open-frame and $189 enclosed, in quantities.



1. The simple circuitry of the flyback switcher (a) is best used for under-300-W supplies. It is a bit noisier and less efficient than either the push-pull or the feed-forward types, but if these parameters are not factors, then money can be saved. The development of high-voltage semiconductors is behind the trend toward the feed-forward switchers (b). They can provide high efficiency and less output noise than the flybacks.

duration of a single cycle) are fairly frequent, this property is rather important.

Another neat feature of switchers is their ability to operate in parallel by simply tying them across a common load. Just like two dc generators sharing a load, one will load up to its current level and the other will take over the rest of the load. With linears, it is generally not recommended to parallel outputs, unless some elaborate measures are undertaken to equalize the loads.

But it is not all roses with the switchers. As was mentioned, linears fare much better when it comes to handling line and load changes. Furthermore, switchers are much noisier: a typical model will put out 50 millivolts (peak-to-peak) of noise, versus 5 mv or less for a linear supply.

In addition, switchers are not simple to design. This not only makes it difficult to build supplies in house, but also complicates hardware and vendor selection process. Some of these design problems include: the selection of power switching transistors that must operate with inductive loads (the dV/dt problem); the design of power inductors that must operate nonlinearly; feedback loop stabilization, which is inherently nonlinear; selection of high-energy capacitors (giving that long hold-up time) that can handle the associated ripple current; and power diodes that can handle the power and have fast switching characteristics.

It should also be kept in mind that noise penalty in switchers is bidirectional: they produce noise at the output that requires decoupling networks to be provided by the user; secondly, they inject noise into the ac line where it might be picked up by other equipment on the same line. So switchers must be equipped with filters for radio-frequency interference.

Finally, there is radiated rfi that might affect operation of such components as display cathode-ray tubes with magnetic deflection and other circuits sensitive to electromagnetic radiation. This implies the necessity to provide reliable shielding either for the circuit generating this interference or for the whole supply.

Which Type of Switcher?

While the linear-vs.-switching battle is far from over, it does appear there will be a rapid increase in the use of switching power supplies. Thus it would make sense to become familiar with the predominant types of switchers and their advantages and disadvantages. Broadly speaking, SMPSs fall into three categories: flyback, feed-forward, and push-pull.

The flyback switcher (Fig. 1a), is the simplest of the three types. Since it uses the smallest number of more expensive power-supply components, it is also the least expensive. While simplicity and low cost of a flyback switchers are certainly desirable, there are tradeoffs.

For one, a flyback unit is less efficient than either the feed-forward or push-pull types, which is partly due to inefficient utilization of the switching transistor. Secondly, a flyback switcher generates more noise at the output. Finally, a flyback switcher is limited to under-300-W supplies.

The feed-forward switchers (Fig. 1b) have not been as popular in the U.S. as in Europe. One reason is their requirement for high-voltage switching transistors. Recent advances that resulted in the development of inexpensive high-voltage transistors are starting a trend toward feed-forward switchers in the U.S., particularly for higher-power uses.

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In the input portion, a feed-forward circuit is quite similar to a flyback. The secondary side, however, is quite different. Thus there is a power feed diode and a commutating diode, connected to an output filter. The filter stores energy during each off cycle and the commutating diode feeds the stored energy into the load. This results in a smoother overall supply operation, hence lower noise in the output.

From the point of view of efficiency, push-pull switchers are the best. Of course, they use the largest number of magnetic and semiconductor devices: a full-wave bridge circuit uses four switching transistors, and single-ended full bridge and half-wave bridge circuits call for at least two.

While there are only two transistors in the single-ended version of the full bridge (Fig. 2a), they see voltages that are twice the input voltage. Also, because of the leakage inductance of the power transformer, there is a voltage spike riding above each voltage pulse. This spike has to be clipped (usually by a pair of diodes across the primaries of the transformer), since it may have enough energy to cause a breakdown in the switching transistors.

A Way Out

These disadvantages can be sidestepped by the use of a half-bridge circuit (Fig. 2b). Here transistors switch at the input voltage (rather than twice the input); leakage inductance spikes are eliminated (they are conducted back to the dc bus); and power transformer utilization is 100% (since the transformer core is excited alternately in both directions). Finally, with the ripple doubled in frequency, filtering becomes easier.

In terms of power-handling capability, push-pull switchers can be used across the board. Of course, at lower power levels, their relative cost/effectiveness decreases, but if top performance is desired, they are preferred.

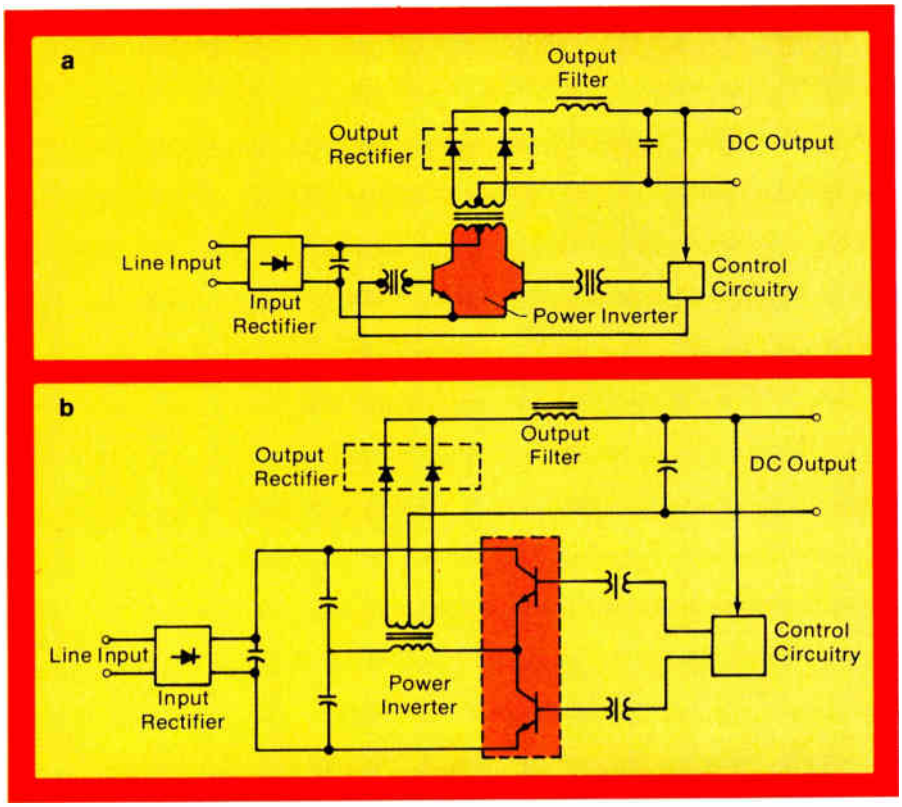
As always, the selection is a matter of tradeoffs. Power supply manufacturers do have strong opinions here, depending, of course, on what they manufacture.

Advizes Carl Mitchell, national sales manager for Elpac Electronics Inc.: "For a single or a multiple off-line switcher, consider power dissipation, magnetic utilization, and voltage rating of switching transistors, [and select] half-bridge for lower power below 350 W, and full-bridge for above. This is the designer's choice, particularly when proportional drive utilizing a single driver transformer and an anti-saturation baker clamp is used. These types of supplies have distinct advantages in noise management, transistor selection, and best transformer utilization."

On the other hand, a spokesman for Adtech Power, Inc. says laconically: "Adtech believes the feed-forward, pulse-width-modulated type of switcher is superior."

Robert Lloyd of Conver Corp. counters this with: "The flyback approach is the lowest cost to build, the most reliable (fewest stressed components) and the toughest to design. Most people believe that it can't be used at high power (especially as a multiple-output). Conver has proved them wrong and now has a 200-W multioutput flyback SMPS."

Joseph Geronimo, vice president of marketing, Power/Mate Corp. feels that "feed-forward and flyback are good for low wattage, up to 100 W; half-bridge to 600 to 700 W, and then the full-bridge should take over." He cites the simplicity of the feed-forward and flyback designs as their pluses. On the other hand, he points out that a failure of a bridge-type switcher does not mean a complete disaster, and this type



2. If efficiency is the biggest consideration, then push-pull switchers like this single-ended version of the full bridge (a) should be considered at the cost of higher component count and higher frequency ripple than in feed-forward designs. Half-bridge switchers (b) feature the best transformer utilization and less stress on the switching transistors (since they switch at the input voltage), and ripple that makes them easier to filter.

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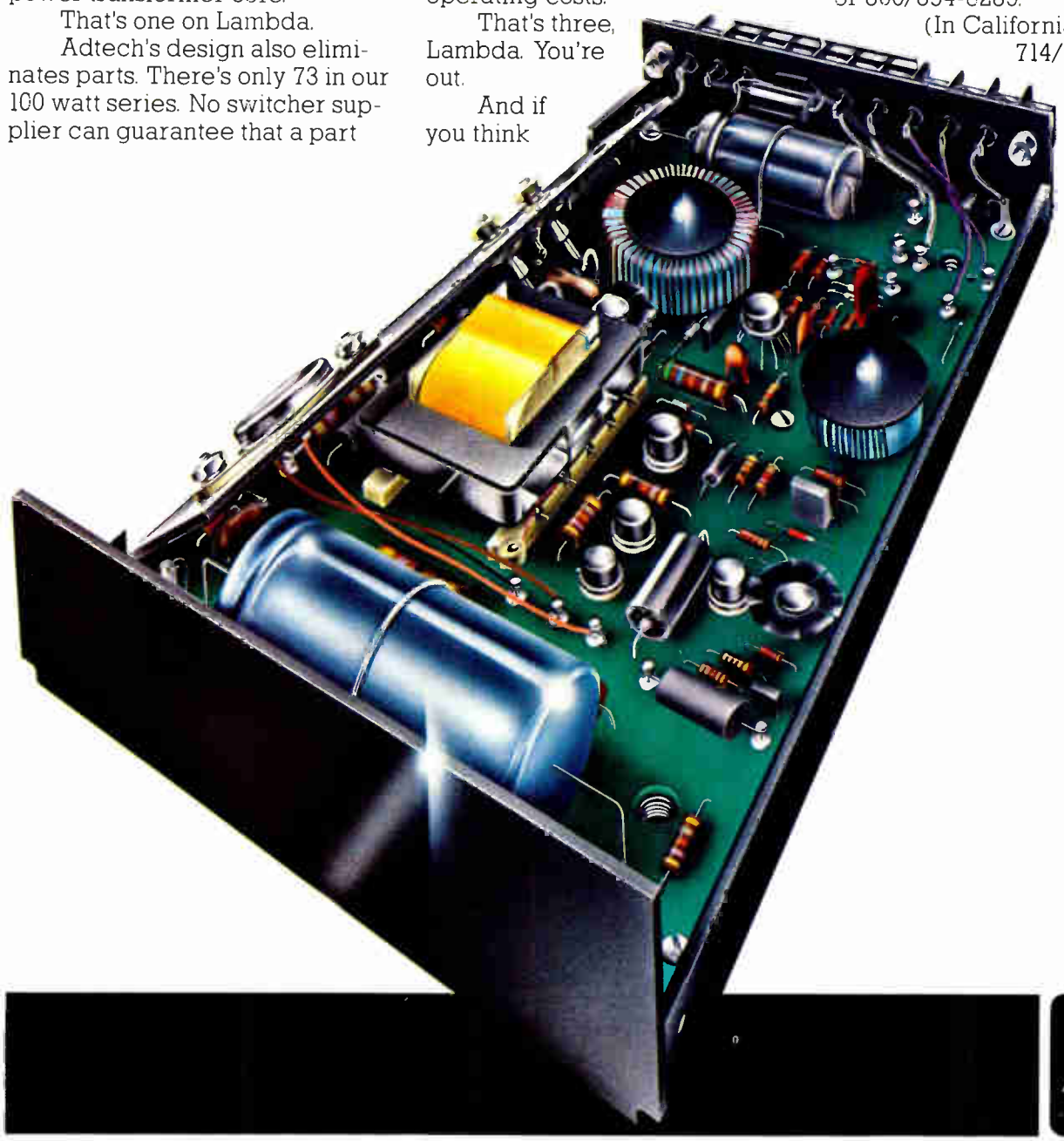

ADTECH POWER

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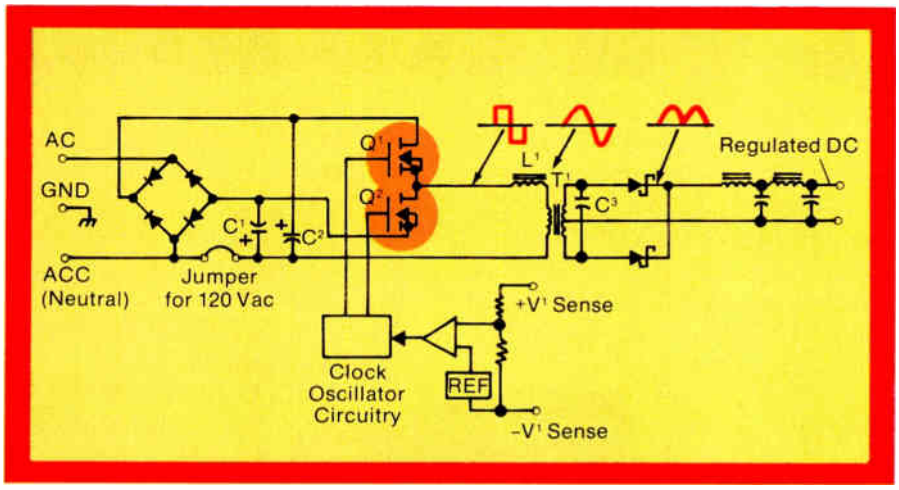


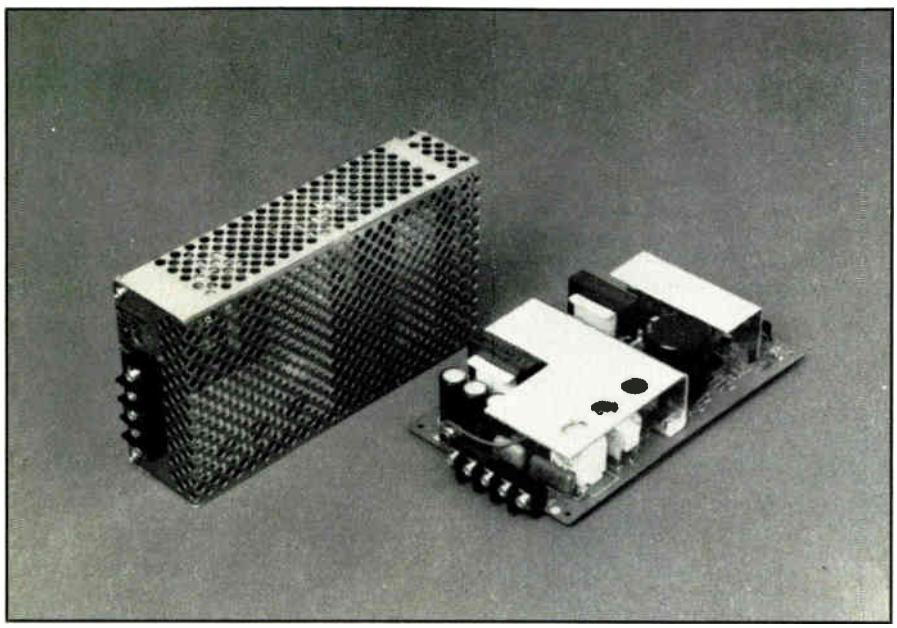
3. Instead of the conventional pulse-width-modulation approach, HP relies on frequency modulation for sinewave power conversion. Proprietary high-voltage power MOS FETs (Q_1 and Q_2) are at the heart of this circuit, switching at frequencies up to 200 kHz.

lends itself to 115-/230-Vac input.

"For very-low-cost, low-power switchers, flyback and feed-forward offer many advantages," says Power-One's Steve Cole. "These are mainly low cost, simplicity of design, and low parts count.

"Feed-forward tends to bridge the gap between the upper power levels possible using flyback technology (100 W) and the lower power levels of push-pull technology. Other technologies, including push-pull bridge configurations, tend to be more suitable for higher power levels, 500 W and above.

"The feed-forward, and push-pull switching configurations are easily adaptable to many of the common integrated circuits available on the market today. Flyback types tend to be configured on a discrete component basis, and therefore performance between manufacturers of flyback switching supplies tends to vary greatly."



A "buck-a-watt" switcher from Panasonic Co., offers 50 W of output for less than $50 in OEM quantities. Designated as the J series, it accepts 98 to 132 Vac or 140 to 180 Vdc and can be purchased either with or without the enclosure.

A Fourth Way

The three basic configurations of switchers all regulate their output by pulse wave modulation. An interesting departure is being turned out by HP, which has come up with an approach it calls sinewave power conversion in which regulation is by frequency modulation.

At the heart of sinewave power conversion are the HP-developed high-voltage power MOS field-effect transistors, Q_1 and Q_2 in Fig. 3, which switch at 200 kilohertz. The 340-V peak-to-peak square-wave output from Q_1 and Q_2 drives a series-resonant tank circuit consisting of inductor L_1, the leakage inductance of transformer T_1, and the reflected capacitance of capacitor C_3.

The nominal frequency of the clock driving the FETs is set above the tank resonant frequency. When the control circuit slows down the clock and FETs' switching rate, the voltage across capacitor C_3 increases and thus increases the rectified and filtered output voltage V_1. When the clock speeds up, the output voltage V_1 decreases.

The control circuit adjusts the frequency to provide 0.1% line and load regulation for the V_1 output. More outputs can be provided by extra secondaries on the T_1 transformer.

"The reduced component count [compared to feed-forward and push-pull] with this technique provides calculated mean times before failures in excess of 100,000 hours for single-output models," says HP's Shamir. "And since sine waves don't have the harmonics of square waves, electromagnetic interference is typically 15 decibels less than in PWM switchers." □

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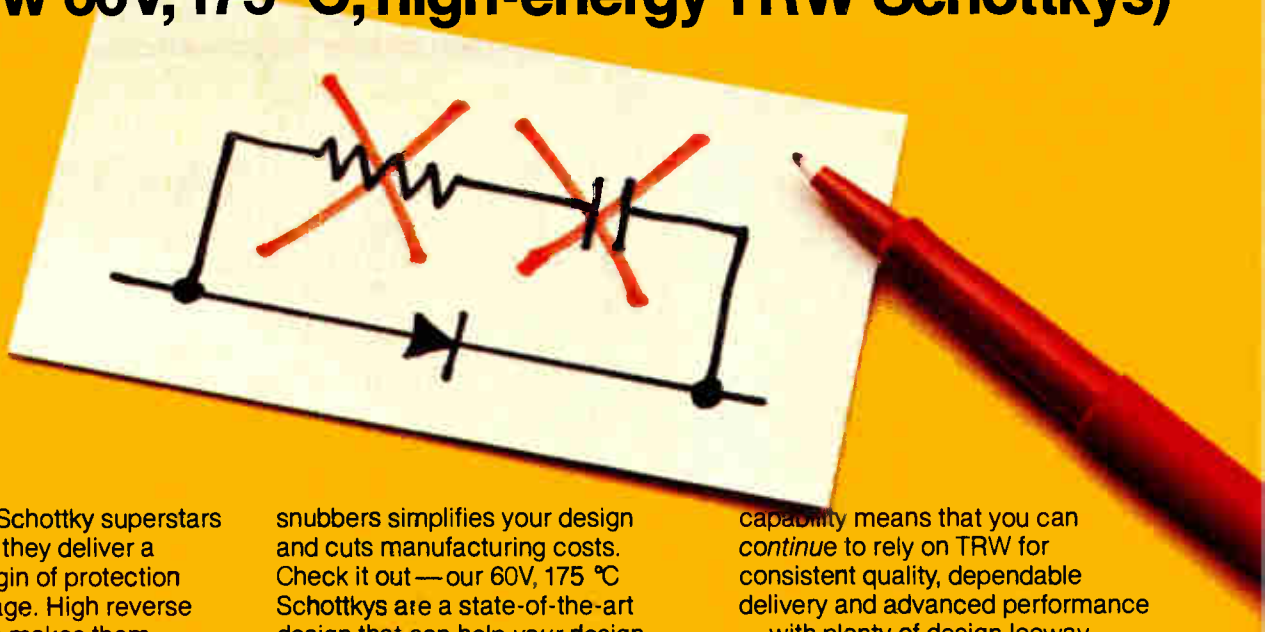

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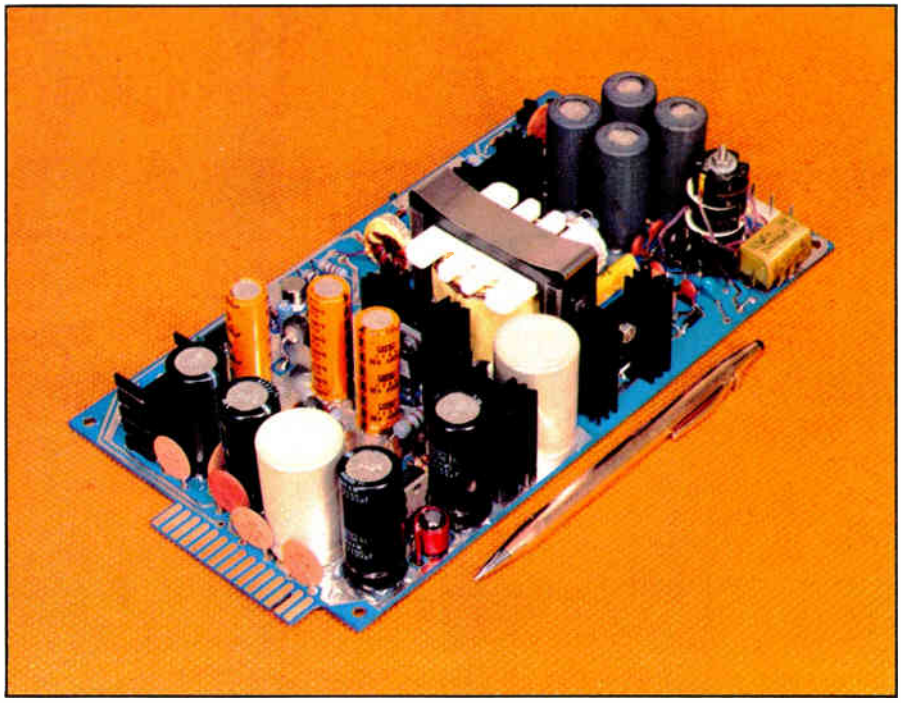
CLOSE CONSIDERATION OF SPECS PAYS OFF

Certain Performance Parameters are Important in Selecting The Most Efficient Supply for the Least Amount of Money

To the unwary, choosing a power supply seems like a simple chore, since it has such a simple job to do. Indeed, it is possible to make a quick and dirty decision and wind up with a better than adequate choice, because today's power supplies are flexible enough to suit a wide range of uses without fuss.

But for maximum efficiency, cost reduction, and reliability in a power supply, the specifier needs to go beyond the black-box approach to consider certain performance specifications closely. It is not only that these parameters are vital to making a better buying decision. Also, there is on the one hand a lack of understanding on the part of users of what the specs mean, and on the other hand the natural desire by manufacturers to put the best foot forward—which, if overdone, results in specmanship.

A good example of a key parameter is line and load regulation. Other vital specs include ripple, response time, hold-up time, and temperature specs. A final point to consider is the way the manufacturer presents these specifications in his catalog.



A five-output, 65-W switcher by Conver Corp. offers an input range of 80 to 140 and 160 to 264 Vac, user-selectable. The company says it meets UL478, CSA22.2 #154, and VDE 0804 and 0730.

Regulation Deserves Attention

In considering line regulation, the specifier must keep in mind that there are two kinds of regulation: static and dynamic.

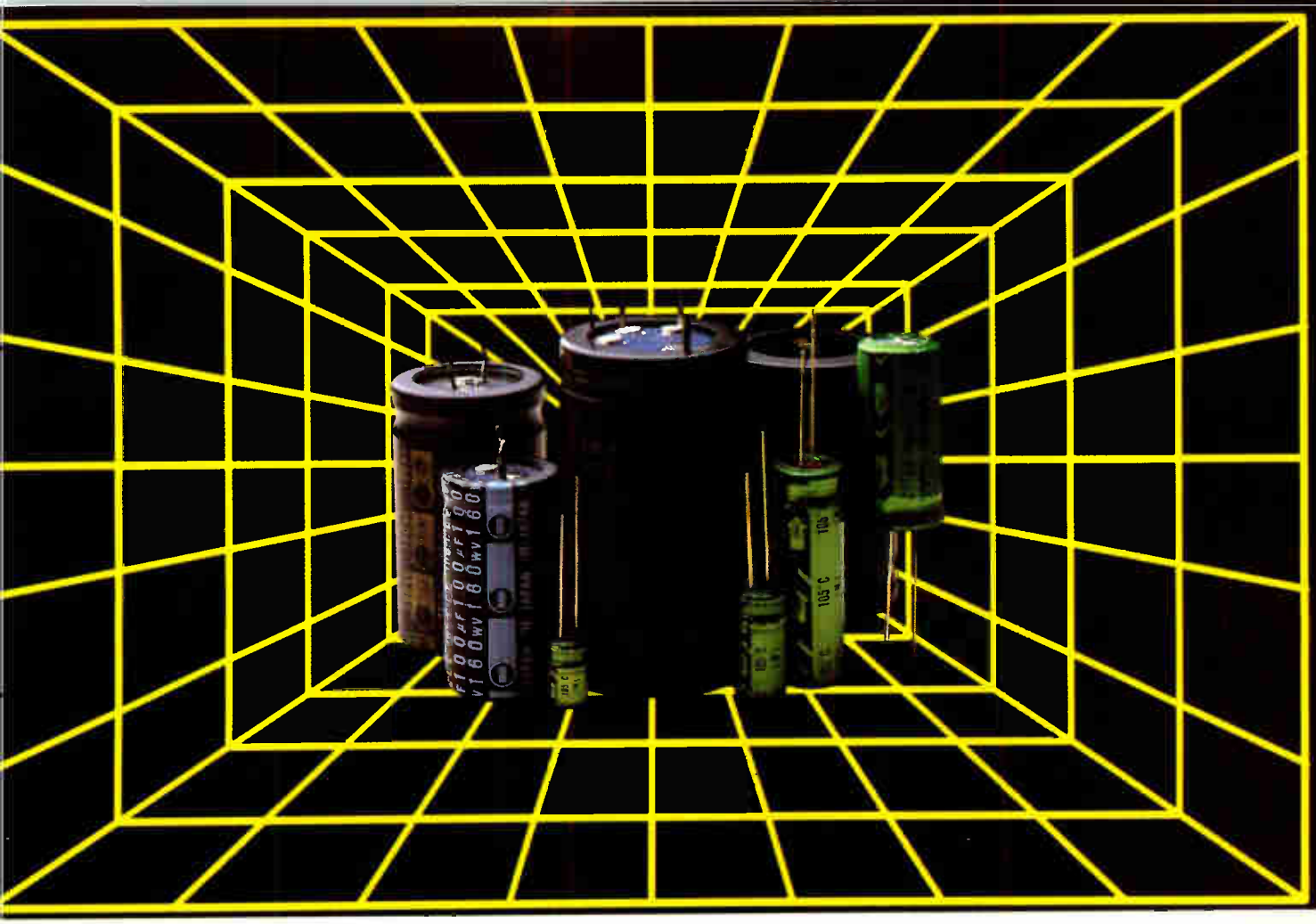
Static line regulation pertains to slow line changes, occurring over some appreciable period of time. For this reason, many a user tends to overlook it altogether, simply stating in his spec that "The supply will operate between 130 and 95 Vac."

Dynamic line regulation refers to a step change in line voltage and the immediate effect (in micro- or milliseconds) thereafter. On some specification lists, this appears under the name of "transient response." Both the dynamic line regulation and transient performance of a switcher are worse than those of a linear supply by as much as two orders of magnitude.

With a constant load, of course, the switcher transient behavior is of little consequence. Incidentally, if the load constant (or nearly so), why specify for 0.01% load regulation? Indeed, nowadays it is the rare equipment that really needs 0.01% (or anywhere near it) load regulation.

Modern semiconductor circuits are becoming less susceptible to noise. Overspecifying in this area means money down the drain: yes, 0.01% load regulation does not come cheap. For some reason, computer and computer-peripheral designers are among the worst offenders when it comes to overspecifying.

A hearty second on this point comes from Conver's Lloyd. "Linear power supplies give very good regulation at no premium cost," he notes. "SMPSs (especially multiple-outlet) can be



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Circle 117 on reader service card

made more reliable and lower cost if the regulation specs are relaxed. Many users are slow to learn this and arbitrarily specify tight tolerances because they are used to getting it free."

Watch the Application

In drawing up those tight and costly load-regulation specs, the user must realize that voltage drop in the equipment's power distribution bus may make a shambles of those neat figures. That is to say, when a vendor builds a power supply with a given regulation spec, it means that the promised regulation is assured at the power-supply output terminals, not at the load. Surely, when load currents are small, the impedance of the distribution bus may be of no consequence. But in a 5-V, 200-A or so logic supply, a 50-A step change in loading may destroy those dynamic specs—at no fault of the vendor.

For instance, as few as 5 feet of heavy-gauge wire may add as much as 5 microhenries of inductance. Now suppose the load will change 100 A in, say, 10 μs (not unreasonable in real life). Plugging these numbers into the L(di/dt) formula gives a drop of 50 V across those relatively short leads.

Pitfalls Can Entrap

Many a user tends to view remote sensing as a solution for such problems. This static technique works well in systems involving high currents and remote loads. But what about the bus resistance? Hooking up a 5-V, 200-A supply to a bus with "only" 5 milliohms of resistance produces a drop at the load of 1 V. For a TTL system with 4.5 V as the lower limit, that is unacceptable. Note, once more, that the supply did not deliver through no fault of the vendor.

The voltage drop is not the whole story. Plugging the numbers into the I^2R formula produces a 200-W loss, or, since the starting point was a hefty 1,000-W supply, 20% of its probably expensive capability. Obviously, remote sensing whereby the distribution bus is internal to the power supply (since the load voltage is sensed directly across the load) will not eliminate this loss.

All in all, specifying a power supply can take a lot careful attention to detail, thinking through the requirements of the application, and searching for the proper supply that meets these. Too often the supply specifier envisions a straightforward and simple job ahead and thus runs into problems of his or her own making.

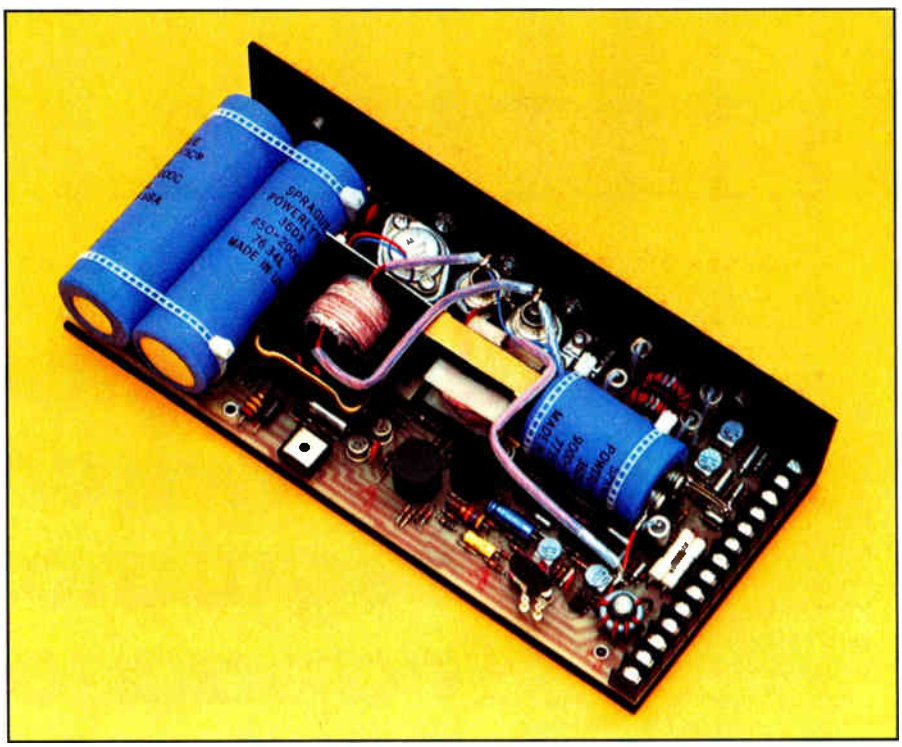
"The biggest pitfall is the 'phantom supply,' " says HP's Shamir. "Design engineers—especially digital design engineers without an appreciation of the analog realities of power supplies—have a proven propensity toward picking the best specs from various power supply houses, combining with the lowest price, and sending the resulting package to the purchasing department. Thus the phantom supply is sent out for bid with disappointing results."

So it behooves specifiers to pay close attention to what they are specifying and to understand the implications of their demands and the intricacies of some specs. Also, they must be alert to points of dispute among supply manufacturers on just what values to publish for a given spec.

Watch RMS Values

An example is ripple, which some makers specify in rms values. The user should avoid falling into this trap, says Walt Nareshni, vice president of engineering at Elpac Power Systems.

"There are high-frequency spikes on the 'corner' frequencies, and rms measuring equipment doesn't have the bandwidth required," he says. "Specify switching in peak-to-peak (20 kHz, etc.), which should also include 120-hertz low-frequency, as well as high-frequency, noise with a specific



One of the latest entries of switchers from RO Associates is the Series 900 units, putting out about 150 W. They are available either as single- or multiple-output units (up to four outputs).

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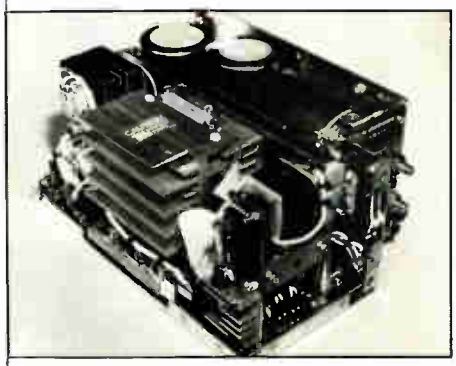
bandwidth. For example, 50 mV p-p and 10 to 25 mV of noise as measured with a 50-megahertz scope."

On the other hand, rms values do have their place, says Conver's Lloyd. "SMPSs are designed to deliver certain rms values of output current (not peak or average). Since they are particularly good at supplying pulsed loads (for printers, disk drives, tape drives, etc.), the output should be specified in rms. This is the only way to match the application to the supply."

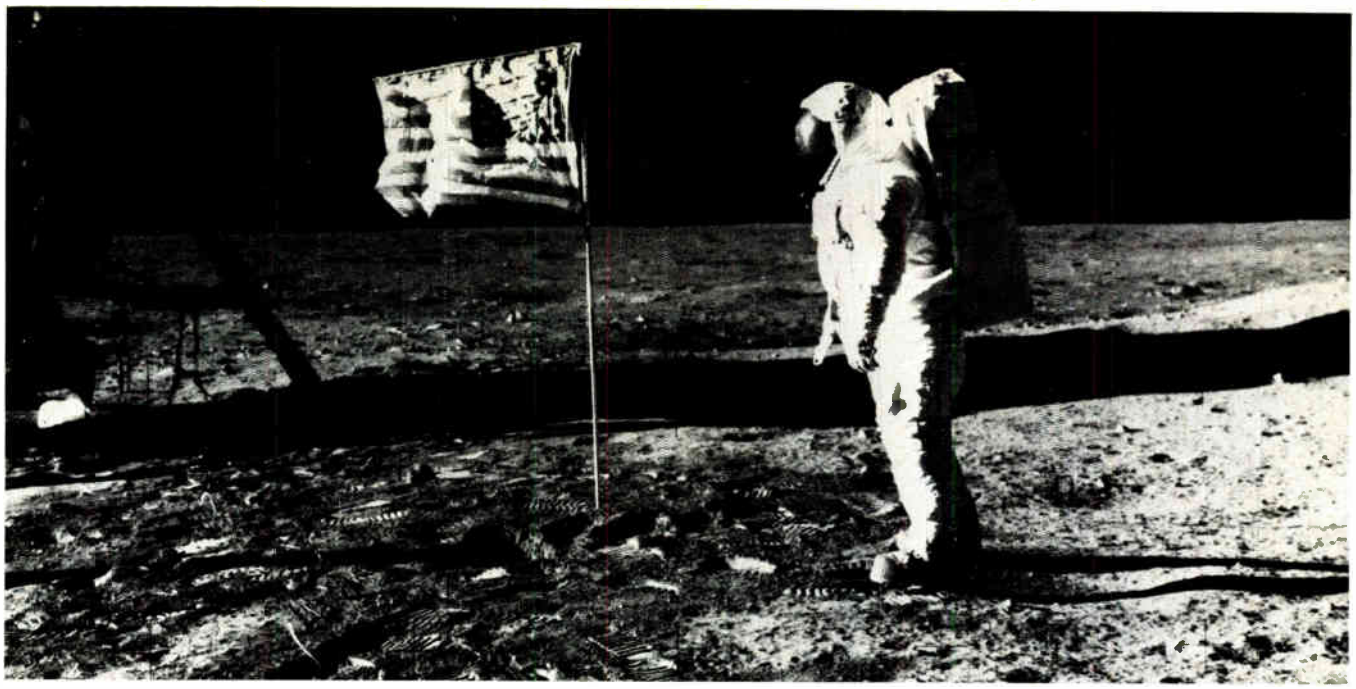
Another bit of advice on ripple specs comes from Walter Omdal, chief engineer of Electronic Research Associates Inc. "Our pet gripe is a specification calling for 800 microvolts of ripple for relay operation. We are saying, 'tailor the specs to the usage and save money and size and increase the mean-time-between-failure number.' "

A warning of another pitfall comes from David Kemp, marketing manager at Sola Electric, a unit of General Signal. "Potentially the most confusing power supply spec is response time," he says. "An acceptable response time is critical for today's extremely sensitive electronic circuit designs, and the engineer must take care to understand exactly what the manufacturer means when he uses the term.

"Response time is a measure of a power supply's recovery from line or load changes. But what is really being measured? Is response time a measure of how long the output voltage takes to return to its regulation envelope or to a plus/minus percent of that envelope? Is it the time taken to reach steady-state regulation within that envelope? Or is it the elapsed time from line or load



A 1-kW (5 V at 200 A) switcher from ACDC Electronics has been added to the company's JF-P series of standard 5-by-8-by-11-in. fan-cooled supplies.



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B	626,000	5-500	2-170
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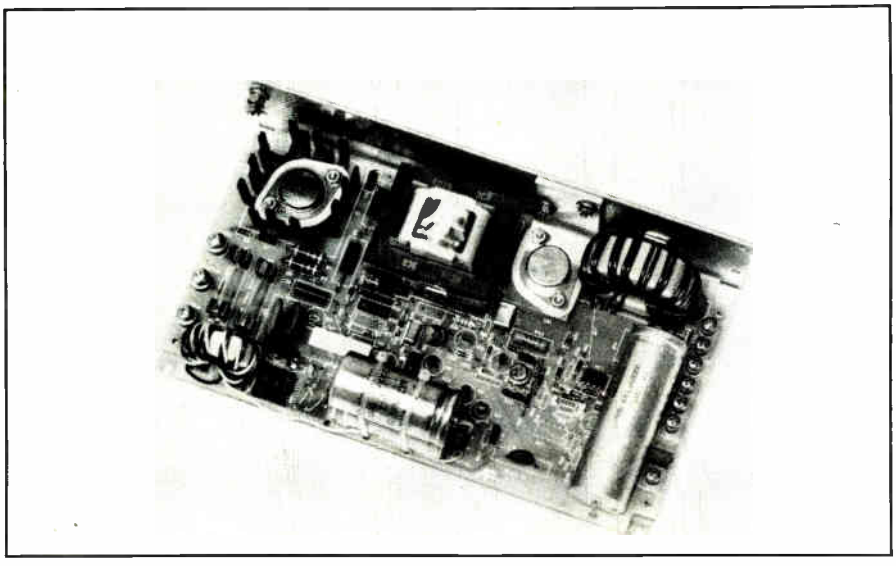


One of the most recent introductions by Adtech Power Inc. is this 5-V, 20-A switcher, Model S5-20, designed around the company's patented Univerter circuit. Its efficiency is more than 72% at full load

change to the beginning of output voltage recovery?"

Wally Resnick of Panasonic offers another couple of pointers. "Assuming a good degree of knowledge on the part of the specifying engineer, there are two specifications that may mislead or confuse him," he says.

- "Operating temperature range: the number entirely depends on how conservative the company is. In other words, there is no indication or criteria on performance at various temperatures.
- "Drop-out (or hold-up) time: many companies don't specify what levels at the output are considered as limiting values. In our case, for instance, we spec drop-out time at 20 ms, meaning that after this period the supply will go out of regulation, i.e., the output will start to decrease."

The issue of specmanship is a sensitive one, but many power supply manufacturers are quick to condemn certain practices. Such outspokeness serves the user well; in fact, the best way to learn about spec manipulation is to ask the maker for his views.

"The biggest trick used in specmanship is to tamper with test conditions," says HP's Shamir. "Carryover time looks much better at nominal line voltage than it does at low line voltage. Transient response looks better with a 10% load change than it does with a 50% load change. 'Competitive' specs can be achieved and the unwary user deceived by relaxing the test conditions."

Some Tricky Specs

"Efficiency and hold-up time are also specifications subject to manipulations," says Richard W. Swift, sales manager for standard power products of Acme Electric Corp. "Excellent power-supply efficiency can be measured at full load, with the output voltage at its maximum setting and the input at its lowest allowable level. But how will that supply operate under the line and load conditions at which you want to operate?

"Hold-up time is a function of both the input voltage level before it is lost and the output load. A mere statement of hold-up time that does not include the line and load conditions doesn't tell the real story."

Another specmanship item (or perhaps an oversight) dealing with efficiency comes into play with fan-cooled power supplies. Fans do use electric power, so the question comes up: is that power included in the overall efficiency calculation? Many a spec sheet will tell you that the addition of fan cooling (at some cubic-feet-per-minute) will greatly extend the operating temperature range of a power supply. But nowhere will such a spec hint at a lowered efficiency.

No discussion of power-supply parameters would be complete without a comment or two on the manufacturers' catalogs. Except for a few, most of them seem to be designed to propagate the user's ignorance of parameters.

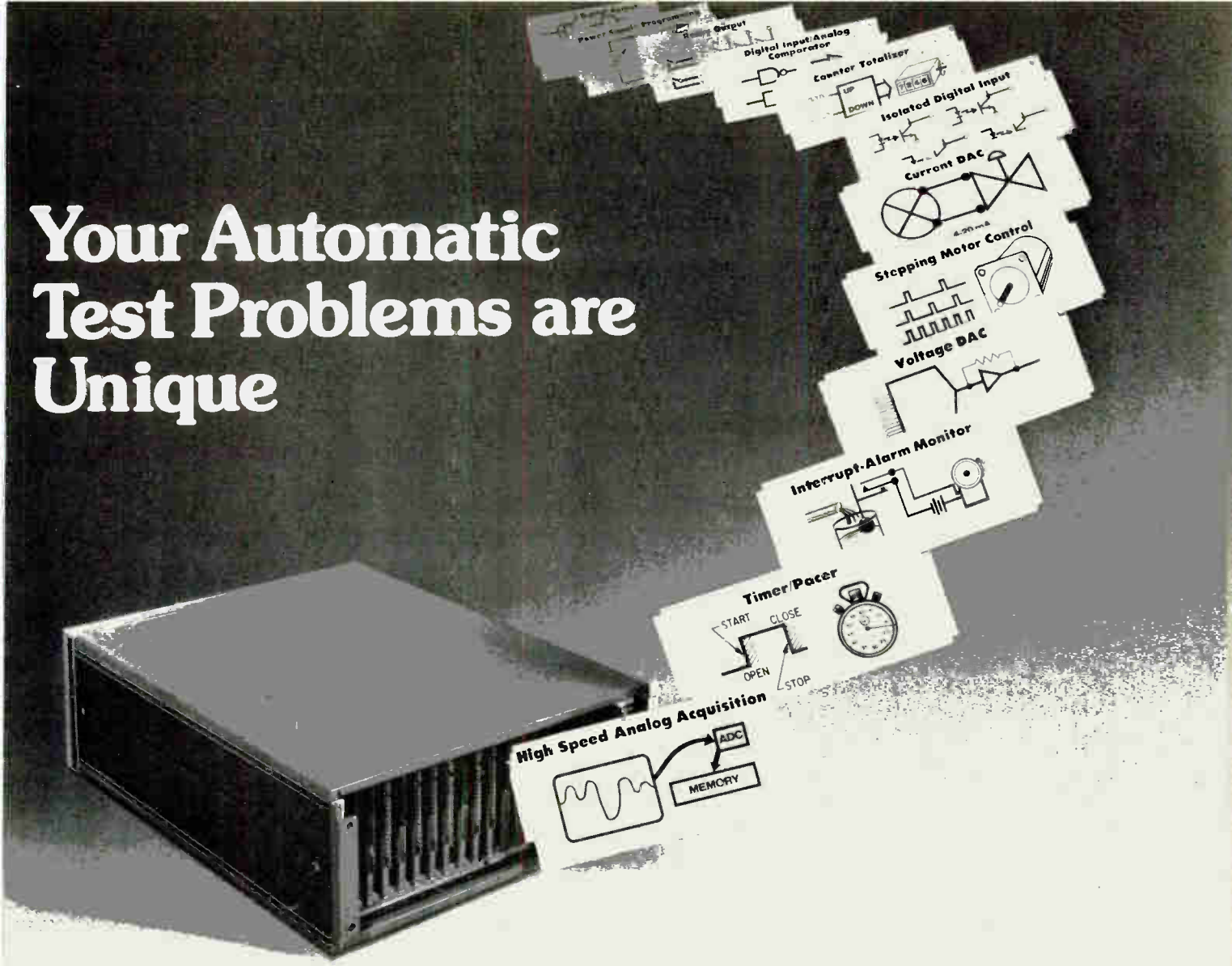
Indeed, if a specifier scans a few catalog, he will soon discover that most of them are guilty of one or more sins mentioned above. Moreover, what seems to be lacking nearly across the board is any kind of an attempt to interpret specifications for the user.

What Does it Mean?

Spec sheets use words like "typical," "up to," "better than," etc. For instance, what does a spec like this mean: "Efficiency: (Typical) 60%"? What if the specifier buys a few and wind up with some "nontypical" units with, say, efficiency of just 40%?

When cooling is required (with the fan up to be supplied by the user), the fan requirements can be rather vague. Obviously, saying that "forced air of 10 cfm is needed" is equivalent to saying that it takes 10 A to operate this load. The rate of flow is meaningless without the pressure at the intake, just as current is meaningless without the supply voltage.

The moral of this chapter is: both users and manufacturers are at fault in this communications gap—with manufacturers probably bearing greater responsibility, for they are the experts. On the other hand, in shopping for a power supply, a dilligent user must do a lot of homework and keep asking questions until definitive answers are supplied. It may take some time, effort, and aggravation but it will be worth it. □



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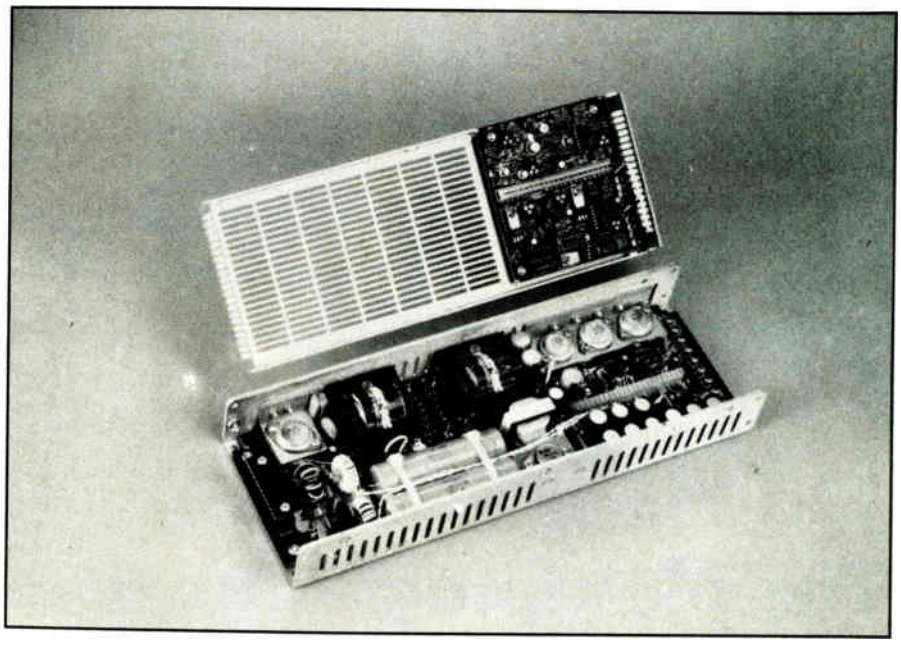
OPERATING CONDITIONS MAKE A DIFFERENCE

Sometimes Multiple-Output Supplies Make Sense;
Heat and Factors like Brownout and Overvoltage are Keys

The world of power supplies is a varied one, with the user getting a good many choices to consider. One major category is the multiple-outlet supply, which attracts equipment makers for potential cost savings in applications where more than one output is required. However, there are some characteristics of such units that may make a difference in a given use, so the choice warrants some careful consideration.

No matter the type of supply, heat dissipation is a factor and users must take it into account. Then, too, brownout and overvoltage usually come into play and require some specifier decisions. Again the point is that the buyer of the supply must know what the seller is offering.

With multiple-output supplies enjoying a good degree of popularity, some understanding of these on the user's part is a must. As in most cases, multiple-output supplies have advantages and drawbacks.



A new quad output, 150-W switcher by Power-One Inc. boasts all fully regulated outputs (±1%), 115-/230-Vac input ranges, 20-ms holdup, a 14-by-4.87-by 2-in. package, and a $295 unit price tag.

Multiple-Output can be Tricky

Starting with regulation, a spec sheet more often than not will scream "Model XYZ multiple output switching regulated power supply." Obviously, the first impression is: "Ah, so I am going to get four (or five or six) regulated outputs!" Not so: In considerably smaller print, the spec sheet whispers: "Primary output fully regulated, other outputs semi-regulated."

Just what does "semi-regulated" mean? A close review of the available data may reveal that regulation of the semi-regulated outputs is three to four times worse than that for the primary output and the temperature coefficient may be twice as large as for the regulated output. Also, the specifier must learn a new term "centering" (or initial setting), meaning that as the primary output is adjusted to its nominal (center) value, the semi-regulated outputs will settle to some voltage within their prescribed tolerance (on the order of ±5%) while under some load (usually 50%).

Then there is another new term, cross regulation, signifying the fact that in a multiple-output power supply the load variation of one output will cause a voltage shift in other outputs. Cross regulation is of particular significance. In a typical switcher with multiple outputs, a common transformer is used with individual windings for every output. This results in literally unforseeable interactions.

For instance, what happens if the primary regulated output unloads while secondary semi-regulated outputs are running at high loads? The primary output tells the control to reduce the width of current pulses since it needs less power and since the primary output commands the control. As this happens, secondary outputs fail to carry their loads since they do not receive adequate power.

On a related subject, crosstalk noise, Elpac's Nareshni notes, "Floating of outputs on a multiple-outlet supply reduces crosstalk. It also provides better regulation on each individual

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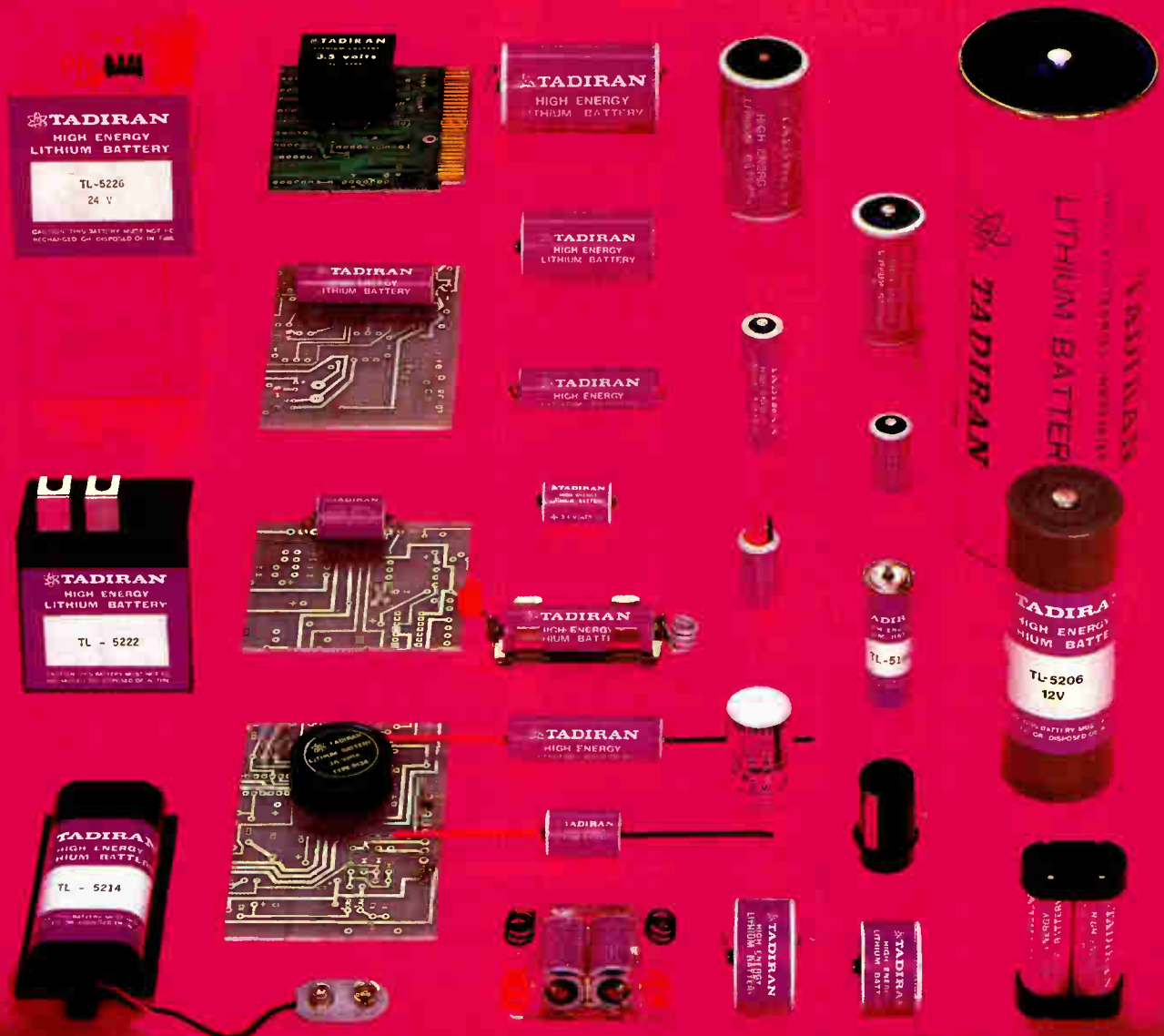

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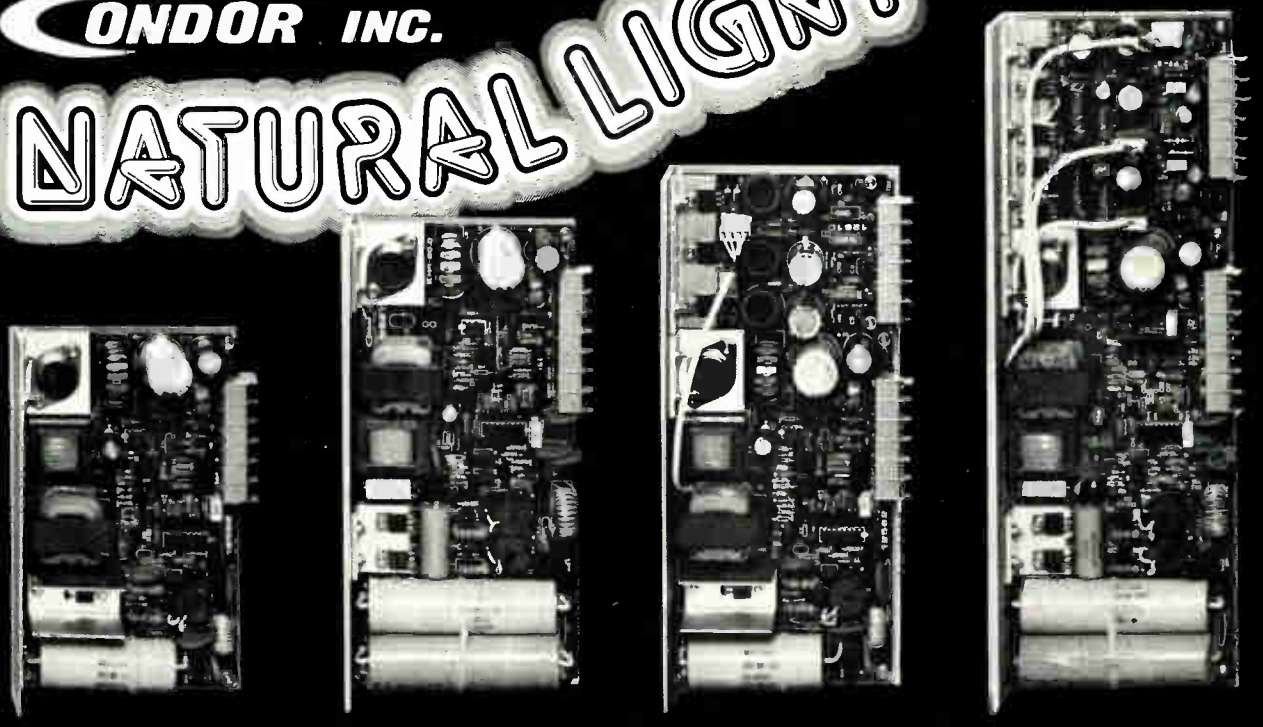
NATURAL LIGHT SWITCHERS



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CONDOR SWITCHERS

MODEL	INPUT	OUT #1	OUT #2	OUT #3	OUT #4	PRICE 1-9
KE5-15	115 VAC	5V@15A				$145.00
KE12-6.5	115 VAC	12V@6.5A				$145.00
KE15-5	115 VAC	15V@5A				$145.00
KFT301	115 VAC	5V@15A	12V@1A	12V@1A		$186.00
KFT302	115 VAC	5V@15A	15V@1A	15V@1A		$186.00
KFT303	115 VAC	5V@15A	5V@1A	15V@1A		$186.00
KFT304	115 VAC	5V@15A	5V@1A	15V@1A		$186.00
KGM401	115 VAC	5V@15A	5V@1A	12V@1A	12V@1A	$200.00
KGM402	115 VAC	5V@15A	5V@1A	15V@1A	15V@1A	$200.00
KH5-20	115/230 VAC	5V@20A				$167.00
KH12-12.5	115/230 VAC	12V@12.5A				$167.00
KH15-10	115/230 VAC	15V@10A				$167.00
KJT301	115/230 VAC	5V@20A	12V@3A	12V@3A		$290.00
KJT302	115/230 VAC	5V@20A	15V@2,4A	15V@2.4A		$290.00
KJT303	115/230 VAC	5V@20A	5V@3A	12V@3A		$290.00
KJT304	115/230 VAC	5V@20A	5V@3A	15V@2.4A		$290.00
KJT305	115/230 VAC	5V@20A	5V@3A	24V@1.7A		$290.00
KLT305	115/230 VAC	5V@20A	5V@1A	24V@1.7A		$260.00
KPM401	115/230 VAC	5V@20A	5V@1A	12V@3A	12V@3A	$300.00
KPM402	115/230 VAC	5V@20A	5V@1A	15V@2.4A	15V@2.4	$300.00

Condor has a permanent cure for your switcher problems. It's Condor's all new line of NATURAL LIGHT Switchers. A wide range of inputs, low prices, plus Condor's advanced design and quality make these switchers your best buy. For your 1st aid problems, take advantage of our FREE 1st Aid Kit in a Can offer. Details below.

FEATURES:

- All outputs are isolated and independent
- Output regulation of 1%
- ±20% line tolerance
- Inrush limiting on turn-on
- Thermal protection
- Output ripple and noise ≤ 50 MV PK-PK
- Temperature 0 to 40°C
- 70% minimum efficiency at full load
- OVP optional on main output
- Current limit with automatic foldback

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With every order for 5 or more Natural Light Switchers, we'll send you this unique and complete 1st aid kit in a can. Includes 10 plastic strip band-aids, 5 sterile pads, roll of gauze, roll of adhesive and tube of antiseptic solution, sealed in a pull top can with plastic lid for resealing. Lid has a coin slot, converting it into a savings bank when kit is used up.

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output." Crosstalk can be a sticking point in going to multiple-outlet supplies, argues Geronimo of Power/Mate. "Oftentimes a system will require separation of auxiliary outputs to minimize crosstalk." he says. "Separate ground returns add to the size and cost of a power supply."

Regulation Specs Vary

"Among major manufacturers of power supplies, there appear to be wide differences in regulation performance, especially in multiple-output power supplies," he adds. "Auxiliary outputs can achieve regulation either as dc-dc converters with individual controls using three-terminal linear regulators on each output (if the load currents will allow it) or merely by tracking the main output.

"The latter does not allow for individual adjustments, and therefore the total regulation should include variations due to line and load changes, as well as crossregulation and centering tolerance. The quasi-regulated, tracking, multiple-output power supply suffices for many applications. But because of the possibilities of accumulating errors due to the above variations, the system designer must often opt for closer tolerances."

It might appear that specifying no load on an output might be a way out, but this is an unrealistic requirement, says Nareshni. "When designing an LC filter, minimum loading on the main and auxiliary outputs plays an important role, since the size of the inductors is determined by the minimum on time and minimum load," he says. "If no load is a requirement, power supply manufacturers provide their own pre-load in the form of a resistor, which dissipates power, as well as larger inductors with more turns to keep the minimum inductor current to a value which will not allow any discontinuity in inductor current.

"This costs money; the power supply becomes less efficient; there is additional internal heating and additional cost for components. Therefore, a power supply designed to operate at no load is not a better supply than that requiring a minimum load—it's only more costly.

Think Unregulated

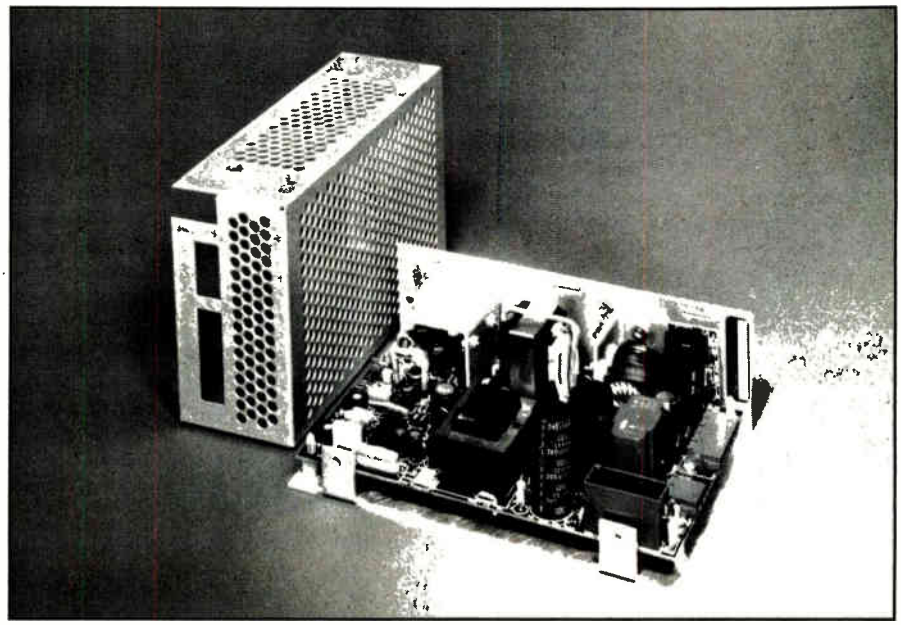
"If you can use unregulated outputs, specify so," he adds. "Regulators only add to the cost and reduce reliability and efficiency. However, consider noise and ripple—since there is no regulator to attenuate these parameters. A loosely regulated output does not requre low noise and ripple specs."

Specifiers who do settle on multiple-output power supplies must keep in mind, as always, that catalog specs require close reading. For example, it is possible to glance at a unit's individual output voltage and current ratings and decide that it is adequate, while overlooking another innocent-looking term, "maximum continuous output power." Invariably, it is considerably lower than the total of individual maximum power outputs, by as much as 50%.

All in all, multiple-output supplies may be a good buy if the application really fits their idiosyncracies. It appears that microprocessor-based systems can be well served by such supplies with ±5- and ±12-or-15-Vdc outputs. Here the secondary loads are relatively light compared to the regulated load, so that load interactions will be minimal. But the multiple-output approach should be avoided when one of the loads is used to drive a heavy, pulsed-type load while other outputs are driving relatively light, continuous loads.

As with so many electronics components, heat in a power supply is the No. 1 killer. Indeed, every power supply, regardless how efficient, will dissipate some heat. The only difference among them is how much.

An 80% efficient 1,000-W switcher, for instance, will dissipate 200 W. This admittedly low number (from an efficiency point of view) must be viewed as the minimum dissipated heat, for most efficiency figures in spec sheets are given at such favorable conditions as full line voltage and full load. Under



Introduced by Power/Mate Corp. as the first VDE switcher in 50-W area, the Model VDE-50 can provide up to three regulated outputs. In quantities nine or less, it sells for $199, cover included. Its long list of features includes a filter conforming to VDE 0871/6.78 level A and FCC 20780.

Where line voltage fluctuations cannot be tolerated, Superior Electric's TVS series of Stabiline transient voltage suppressors come into play. Models are available for 120- or 240-V service in ratings of 15, 30, or 60 A with 99% efficiency.

off-design conditions, efficiency figures should be adjusted downward at least 3% to 5%.

One of three problems can crop up under excessive heat. The supply will burn out, or its life will be shortened drastically, or its performance will be altered. Important also, is the fact that MTBF figures are, more often than not, computed at 25°C. If a supply is taken to the extreme of its operating temperature span of, say, 55°C, the MTBF will have to be drastically derated—by as much as 75%.

Many a user is quick to blame the supply vendor for a heat-related failure of a supply—but chances are that it is the specifier who should shoulder the blame. In 9 out of 10 cases, power supply is one of those items that get selected at the last minute in system design.

Hasty Decisions

As such, they get stuck in whatever space is available at that 11th hour before the prototype is shipped. And, as was just mentioned, even the highly efficient switchers do dissipate heat. In fact, since switchers are considerably smaller than their linear counterparts, heat dissipation might occur at a higher rate.

Fortunately, cooling of a power supply is a fairly straightforward task, provided the user is aware of it. There are at least three proven ways to do it: heat sink, natural convection, and forced air.

The choice of a specific method is totally application-dependent. In some cases, a given supply might be used with any of these methods, depending on how and where it is mounted, the amount of free air passing over it, proximity to other hot equipment, etc.

The point is that it is up to the user to check that the specified power supply will perform as hoped for from the point of view of operating temperature. Theoretically it is possible to calculate heat dissipation over a given thermal path, but in practice it turns out that an experiment is much more reliable. There are just too many empirical variables involved for a theoretical answer—the amount of heat generated by a supply under different operating conditions being one of them.

Taking Brownouts in Stride

The ability to handle the low line voltages of brownouts is an inherent property of switchers and constitutes one of their advantages over linears. Many a switcher spec will list ac input as 90 to 130 and 180 to 260 Vac, where an equivalent linear spec might give a ± 10% line tolerance, i.e., 105 to 125 and 210 to 250 Vac. The reason lies in the way a switcher operates: its internal dc level can vary widely so long as the switching frequency and the range of the pulse-width modulator are adequate.

There are other line-related areas, however, that a user must be aware of. Most any switcher spec carries an entry more often than not designated as "soft start", followed by a statement that the unit provides inrush current limiting at turn-on. That is, it offers some means of limiting the high inrush current into the input filter capacitor so that it does not look like a short circuit is occurring at turn-on.

A common, inexpensive, and reliable way of providing such limiting is a thermistor that opens up as it gets hot. This way, the filter capacitor charges up gradually while the thermistor value approaches zero resistance.

This inrush limiter works well, provided that input line changes occur

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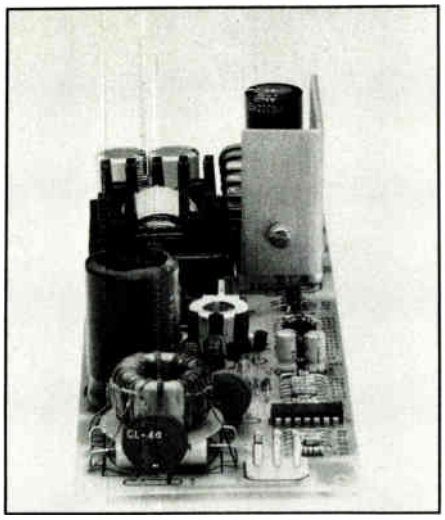
with the thermistor cold, i.e., at initial turn-on. But the supply may be riding through a severe brownout (down to or below its spec), and then suddenly the line comes back up to its nominal state or, worse yet, to its high condition. The inrush limiting circuit is useless here, since the thermistor is hot and its resistance is close to its steady-state value of 0—after all, it performed its limiting duty at turn-on as promised.

A Solution

Just as is the case with heat dissipation, this is not an insurmountable problem, as long as the user is aware of it. If the supply does use a thermistor limiter and will operate in a brownout-prone region, then some additional inrush protection must be provided. Some heart-to-heart talks with vendors on the subject might be useful.



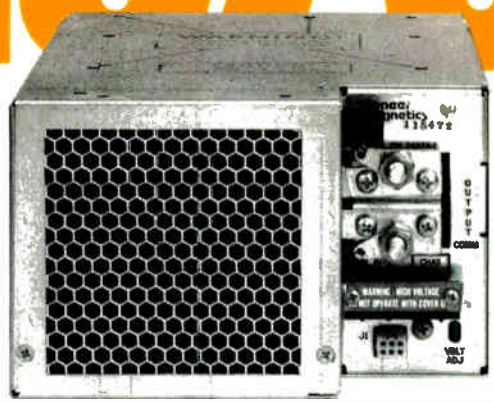
The Model 5031 three-output 50-W switcher from Power Systems Inc. is only 3 in. long by 9½ in. wide by 2 in. high.

As important as protecting the power supply from line overvoltage is protecting the equipment it serves from possible output overvoltage. That is, if a supply fails in such a manner as to develop a high output voltage, an overvoltage circuit should be there to clamp it to some safe value. Obviously, overvoltage circuit settings must be reviewed before purchasing a supply.

Spec-sheet data is mostly given for certain loaded operations of a supply. In real life, depending on the application, loads can vary from open to short circuit. Before buying, it is well to find out just what happens as the load varies over the expected range. □

Dependable Switchers...

1973 1981



The PM2497

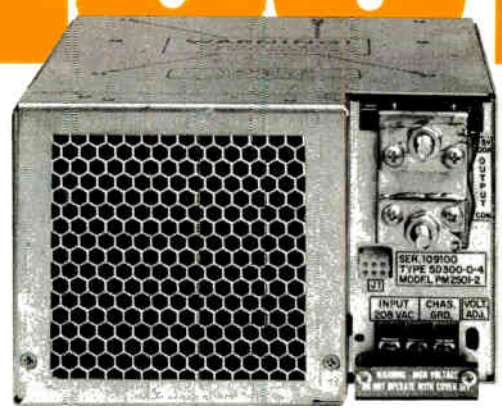
5V@100A/5"x8"x11"

In 1973 Pioneer Magnetics started building a 5VDC @ 100A switching power supply for applications requiring compact and efficient DC power. At the time, commercial switchers were considered state-of-the-art. We solved reliability and delivery problems for our customers that our contemporaries couldn't. As a result, our customers referred to the power supplies as the DEPENDABLES. In fact we're still delivering that same power supply to those same valued customers. We're proud to say that they've depended on us and we've responded by shipping over 100,000 high power switchers. After 8 years our supplies are still out there and running. A continuation of a tradition started in 1958.

STANDARD DC OUTPUT RATINGS.

MODEL	2V	3V	5V	12V	15V	18V	24V	28V	48V	60V	CASE SIZE
PM2496A	100A	60A	50A	30A	25A	22A	16A	13A	8A	6A	5"X8"X11"
PM2497A	200A	100A	100A 120A 150A	60A	50A	45A	33A	27A	16A	12A	5"X8"X11"
PM2500A		200A	200A	85A	70A	60A	45A	40A	24A	19A	5"X8"X11"
PM2498B	400A	300A	200A 300A	120A	100A	90A	66A	54A	32A	25A	5"X16"X11"
PM2501	400A	300A	300A	120A	100A	90A	66A	54A	32A	25A	5"X8"X11"
PM2502	500A	450A	450A	180A	150A	125A	90A	80A	47A	35A	5"X16"X11"

NOTES: 92-138VAC or 184-250VAC single phase, 47 to 63Hz.
DC input available.



The New PM2501

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Since 1973, we've been accepting new challenges. Within the same outline as the PM2497, we've developed output ratings of 5V @ 120A, 150A, 200A and now a new 5V @ 300, with full delivered power at 50°C.

The new PM2501 exhibits excellent dynamic response. Proven design concepts enable close control over those parameters that insure reliability. For instance, our unique heat transfer technology results in low component thermal stress, even lower than the PM2497. At three times the power level the PM2501 features an exceptionally high power density package.

Our product line includes switchers that deliver up to 2250 watts in single output and from 375 to 1500 watts in dual through quad output channels. AC or DC input.

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GETTING TO THE COUNTDOWN TAKES MORE WORK

MTBF, Noise Filtering, and the Like are Important;
So, Too, is Deciding Which Vendor to Choose

No matter the application, no user wants the power supply to be a service problem. So it behooves specifiers to consider MTBF figures, keeping in mind once again that reliability is subject to different definitions by manufacturers, and, for that matter, to differing fates in different applications.

A factor that is fast becoming of equal importance in specifying a power supply is noise filtering, and so users should be aware of the ramifications of the ins and outs of interference quenching. Another consideration may be whether a backup or redundant power supply is needed for maximum reliability.

Choosing a Supplier

Finally, after considering all the elements that go into the choice of a power supply, the specifier must then think of one more important input: which supplier. To that end, it is useful to read what manufacturers themselves think is important in selecting any one over another. Also, there are certain steps a specifier can take to winnow down the list of potential suppliers.

It is a sad fact of life that the term MTBF—which after all stands for mean time between failure and so is a statistical value—is often represented as a measure of a power supply's operating life. That is to say, there is a marked tendency to believe that it means a minimum time between failures.

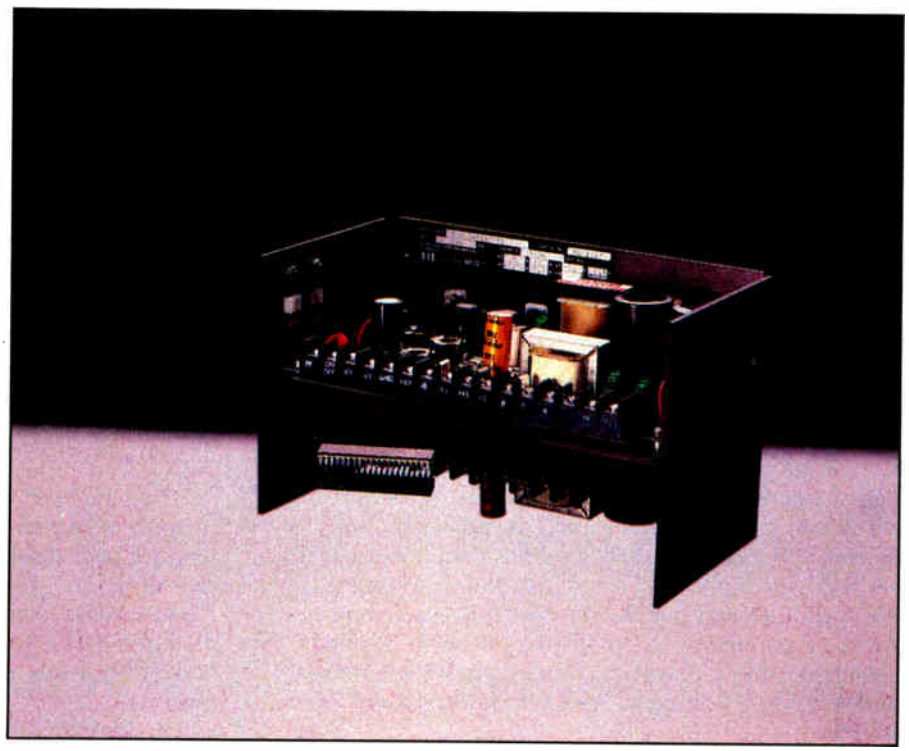
If viewed in this manner, a number like 50,000 hours that a specifier can notice on some spec sheets looks really great. Why, 50,000 hours, it's almost six years. With some luck (this being a minimum time between failure), the equipment will last forever!

The true point of interest should be the reliability of a power supply in an application or the ability of a supply to deliver the required power over the life span of the equipment. And practical reliability is a function of many nonmathematical factors.

Checking Reliability

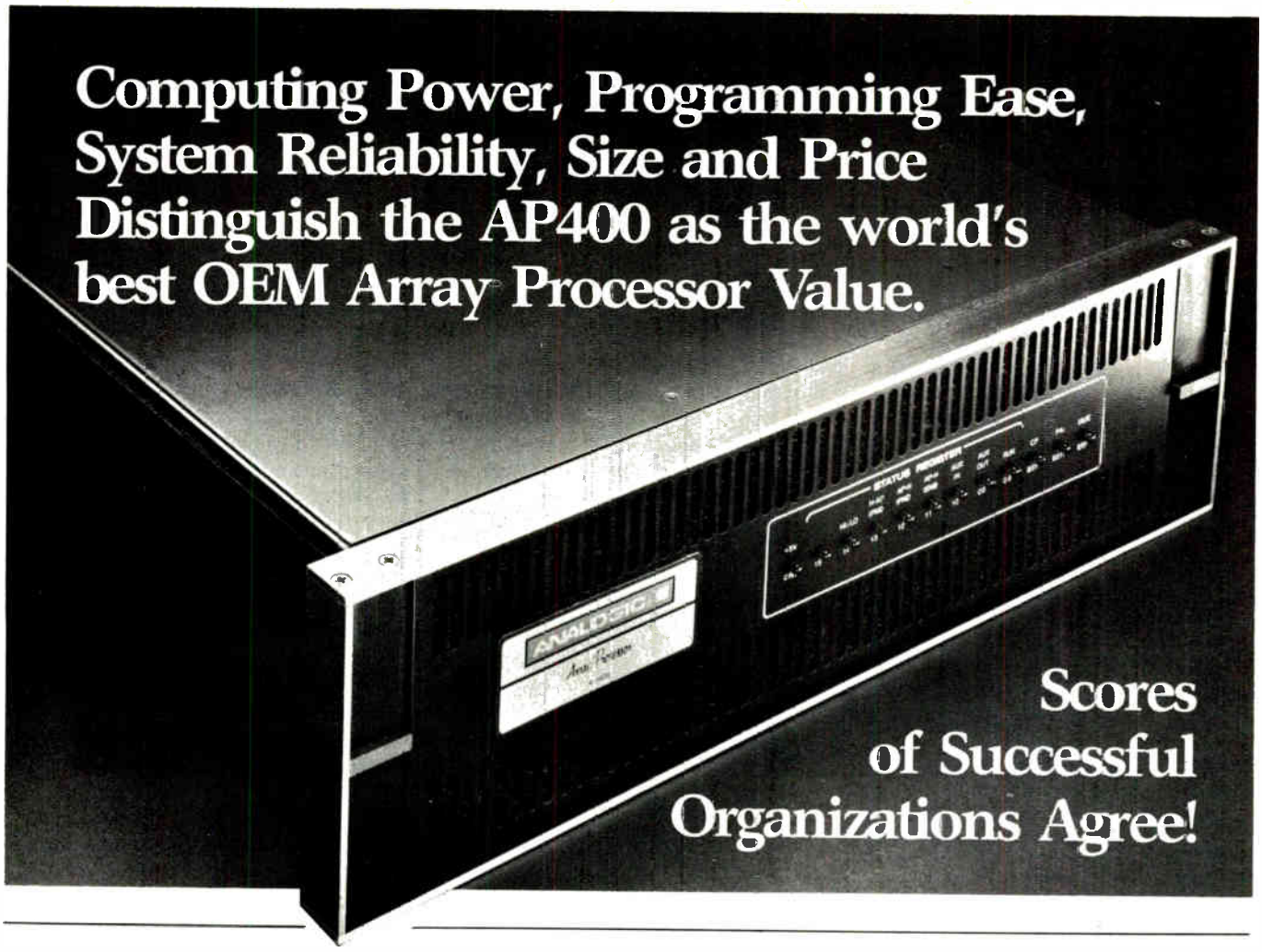
To begin with, it is a well-known fact that infant mortality in semiconductors can be fairly high. At the same time, once all these bad chips have been weeded out, chances are that the remaining ones will last a long time. The question is: how do you induce those SMPS components that have a tendency to fail early in the game to do just that?

Burn-in has been the traditional way to do it. In recent times, however, static burn-in (whereby tested devices would be turned on and left on for some predetermined amount of time) has been giving way to power cycling, whereby the equipment under test would be turned on and off at some



Reduced component count has been achieved by LH Research in their TM and SM series of switchers through the use of a proprietary LSI control chip. The TM series multiple output switching power supply uses the control chip.

Computing Power, Programming Ease, System Reliability, Size and Price Distinguish the AP400 as the world's best OEM Array Processor Value.



Analogic began the design of the AP400 with the knowledge that OEM array processor users needed an order of magnitude more reliability, software maintainability and economy than anything available at that time. Now, less than two years since its introduction, system engineers, scientists and computer designers appreciate its performance and have designed-in over 500 AP400s in such diverse applications as ☐ X-Ray Tomography ☐ Ultrasonics ☐ Nuclear Magnetic Resonance ☐ Spectral Analysis ☐ Seismic Exploration ☐ Music Synthesis ☐ Digital Filtering ☐ Satellite Communications and more. Consider the advantages to the OEM.

You get just what you need

In its simplest form* the AP400 will tuck into your package, using your 5-volt power and your front panel. At the other extreme, the AP400 may incorporate 64K words of memory, and come as a complete, stand-alone, self-powered package. They can even be chained together to deliver total throughput equal to that of super computers — but at a fraction of the cost.

You pay far less for what you get!

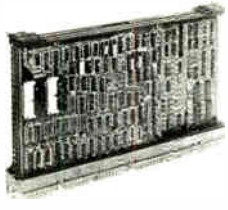
We know that OEMs are concerned with the total cost picture: initial price, costs of inventory, costs of software development and maintenance and costs of hardware maintenance.

In response to these concerns, the basic AP400 has been priced to reflect OEM quantity requirements. Software is inexpensive because we provide complete utility, application and system software and support in Host FORTRAN, Host Assembly and AP Assembly language...in standard or custom configurations. Further, the AP400 employs a familiar minicomputer-like hardware and software architecture and instruction set, similar to the host computer you're probably using now!

In addition, the AP400's straightforward system architecture and comprehensive diagnostics enhance reliability and simplify maintenance procedures. Analogic's sophisticated engineering design and reliability minimizes hardware maintenance cost.

The AP400 has a long product life expectancy

Continual development of a family of software-compatible machines ensures that all systems using the AP400 will keep their competitive edge for years to come.



**In its simplest configuration the AP400 is composed of 4-PC cards. It measures only 15½ x 10 x 2¼ inches.*

Technical information is available

Write for our comprehensive AP400 information package which includes a product selection guide, and a description of our technical services. Should you feel that a design conference would be helpful, tell us about your needs and we'll assemble a group of system architects, engineers and scientists to help you with your program. Analogic staff members are experienced professionals in meeting special customer needs such as inventory scheduling, special packaging and service arrangements.

Summary Specifications

- 10 million arithmetic computations per second
- 1024 point real FFT — 3.6msec, complex FFT — 7.4msec.
- Standard memory: 4K by 24-bit bipolar RAM
- Expandable 64K words in increments of 4K
- Power Requirements: 4-card set — 5Vdc @ 20A nominal; complete system with line-separated power supply — 117Vac or 240Vac, 50/60Hz, 130W nominal.
- 24-bit auxiliary input and output ports, standard

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Circle 133 on reader service card

predetermined and variable rate.

An authoritative description of this technique by Michael Strange appeared in the September 1980 issue of Quality magazine. The article presents the power cycling burn-in performed on an electronic cash register.

This testing would be first performed on individual subsystems, including the power supply, then on the complete cash register. Each module would go through its own cycling sequence, based on the kind of components it contained—made possible by a programmable timer also described in the article.

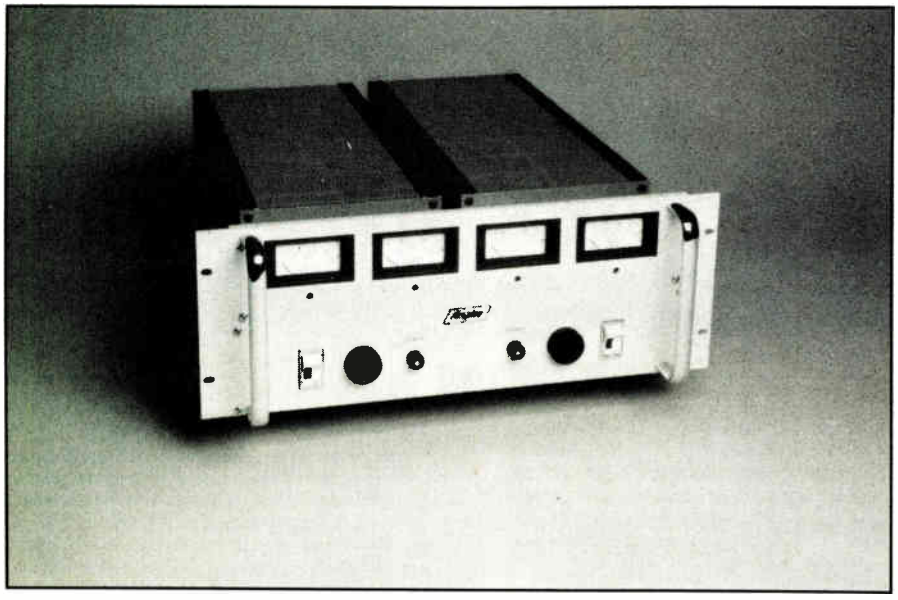
The application of power cycling cut the static burn-in time of 24 hours to just 2 hours. Even more important, it proved to be a more effective way for getting rid of infant failures. The author did point out, however, that the ultimate success of power cycling heavily hinges on the on and off sequences.

So a supply builder's claim that its units went through a 100% burn-in program should be probed in depth. That is, a potential user should find out just how those units have been burned in. The number of hours of static burn-in may not tell the whole story, as Strange's procedure suggests.

A host of other concerns also affect reliability. Among these are:

- Do the filter capacitors operate within their ac ripple current specifications?
- Are ¼-W resistors being used to dissipate .249 W?
- Are the diodes operated close to their surge and voltage limits?
- Are heat sinks really heat sinks, or are they buried well within the unit?
- Are the switching transistors doing what they are supposed to do—switching clean and sharp?
- In two-transistor schemes, are the on times so close that there might be a slight overlap leading to a blown transistor?

Even items as mundane as standoffs should be examined. Indeed, standoffs in power supplies are often used as current-carrying electrical connections. At the same time, in normal assembly, one can fairly easily break such a connection in tightening the associated screw.



One approach to ensure functional reliability of a power source is through redundancy, i.e., by having two power supplies with each capable of carrying the full load but with only one actually supplying power at any given time. Available from Acopian Corp. with voltage ranging between 5 and 28 Vdc and currents between 5 and 55 A, these units command prices ranging from $1,095 (for a 140-W unit) to $2,190 (750-W).

Interference is Important

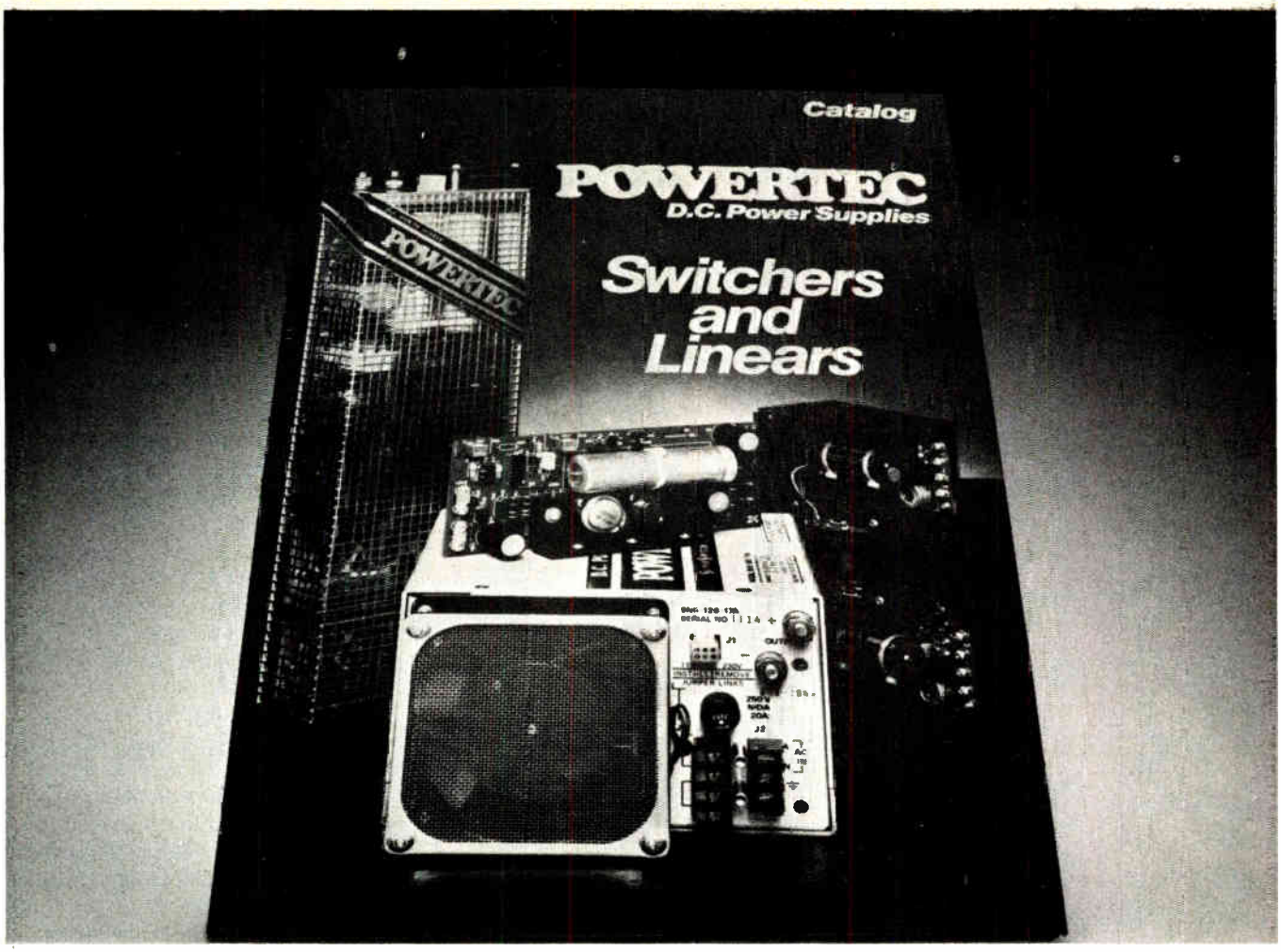
During the long and peaceful pre-switcher era, rfi and emi was not of much concern to either the designer or the user of power supplies. But the advent of the switcher changed all that. Its (ever faster) switching action tends to pollute both the output and input, as well as to generate considerable levels of interference. While this had been true all along, it is becoming more pressing than ever as tougher Federal Communications Commission regulations are becoming effective. Home computers have to comply as of Jan. 1, while other computing devices must comply by Oct. 1.

"To a large degree, the power supply industry had not addressed the noise limit specifications of the VDE, the FCC, and other bodies with much zeal," says Power-One's Cole. "We strongly believe that the serious power supply companies that will emerge to the top 10 in the 1980s will be forced to address the knotty problem of noise specifications from many fronts."

"The ability to meet European safety and rfi standards will become the standard for all power supplies," says Conver Corp.'s Lloyd. "They are the toughest, and ways are being developed to do it at small additional cost.

Look to VDE

"Many users think VDE spec 0804, Telecommunications Apparatus Including Information Processing Equipment, is the right VDE spec for data-processing and office equipment. This is wrong. Part 2P, Special Requirements for Office Machines, of VDE spec 0730, Electric Motor-Operated Appliances for Domestic and Similar Purpose, is the right spec and is much tougher than 0804. International Electrotechnical Commission #380 will become the right spec this year. It is based in part on VDE 0730.



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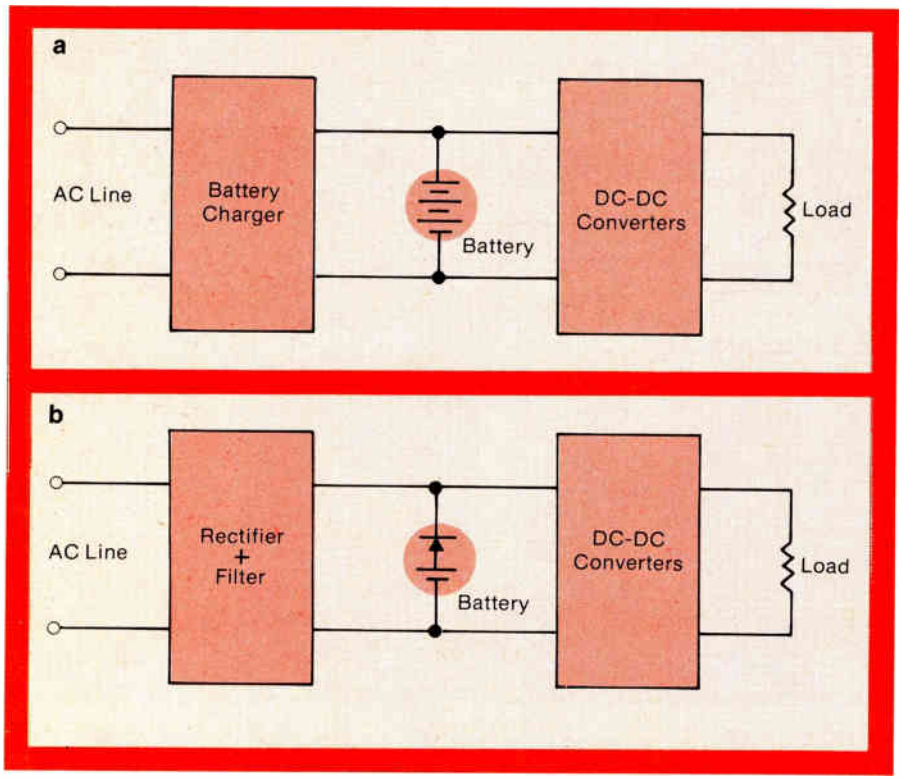


4. One configuration of a UPS, by Acme Electric Corp., (a) looks very much like a switcher without its input rectifiers and filters, but with a battery charger and a rechargeable battery. One way to provide a battery backup using a dry cell battery, (b) is to place it at the dc-to-dc converter input with a blocking diode.

"One of the most important differences is that 0804 calls for 2,500 Vac input-to-output Hi-pot while 0730 calls for 3,750 Vac. This is a big problem for most SMPS designs, especially if they use opto-couplers for feedback. The spec also calls for 0.5-millimeter insulation thickness. Opto-couplers don't work very well when they have this much insulation between the LED and phototransistor."

The lesson is clear: some kind of filtering will have to be added in the very near future to every switcher design. One impact of this will, undoubtedly, be an increase in their cost (perhaps as much as 10%)—as well as some decrease in their volumetric efficiency, since those additional filters will need to occupy some extra space.

What counts, of course, is the noise regulation of the entire system, points out Elpac's Nareshni. "Power supplies by themselves can meet these requirements with good input filtering and proper enclosures," he says. "However, in a system, these filters at the input of the supply (located somewhere within the system) will not insure the system will meet these requirements.

Position is Important

"Costly VDE filters, if not located at the power entrance to the enclosure, are useless since the system designer has to use additional filters. Generally, an enclosed power supply will provide good enough attenuation of radiated energy, but the final test is performed at the system level, which itself requires an enclosure."

While line outages of a few milliseconds can be handled by switching power supplies, longer power failures may lead to the loss of data, interruptions in some vital functions, and possible damage to certain equipment. To prevent this, a variety of methods have been devised.

Backup and Redundancy

There are two generally accepted ways of doing this with supplies: battery backup and uninterruptable power supplies, or UPSs. Actually, except for applications with kVA loads, a UPS essentially is a power supply with a battery backup. To a degree, this is also a matter of how the backup battery is connected.

For example, a rather simple UPS configuration from Acme Electric Corp. (Fig. 4a) is a battery charger connected across the ac line, followed by a rechargeable battery, and then a dc-to-dc converter operating the load. Among the advantages of this approach, says Acme, are:

- Constant operation from the backup source (no transfer to backup only to find it does not work).
- Batteries act as a buffer filter between input and output.
- Minimum of power transformation stages (charger and the dc-to-dc converter).
- Easily varied holdup time by selection of battery or charger.

A battery-backup configuration, on the other hand, is shown in Fig 4b. Here a dry cell is used, rather than a rechargeable battery. A blocking diode prevents positive voltage from destroying the dry cell.

In those cases when it is necessary to guard against a loss of a dc output due to a supply failure, redundant power supplies may be used. These configurations employ two power supplies, each capable of powering the application, connected across a common load. The supply outputs are isolated from one another by means of blocking diodes.

To make sure that only one power supply operates under load, the output voltage of the primary unit is set somewhat above that of the backup unit. Should the output voltage of the

primary supply decrease, the secondary unit steps in and takes over.

Working with a Vendor

Only through a close contact and cooperation with the potential power supply vendor, can one come up with a power supply that will truly fit each particular application at the lowest possible cost. But before working with a vendor, it is necessary to select one from a substantial number of candidates by wading through a maze of claims and counterclaims. In this connection it is interesting to see what points power supply manufacturers cite as reasons for buying their wares.

David Kemp of Sola Electric puts it this way: "Since product functions and power ratings are fairly similar throughout the industry, competition among power supply manufacturers breaks down into three areas—reliability, availability and, of course, unit cost." He also lists breadth of the product line and fast delivery on small orders. "In addition, all of Sola's power supplies are manufactured in the U.S. and are not subject to imbalances in world currencies, as are units which have been imported for private labeling," he says.

Compact and lightweight, the line of nickel-cadmium batteries from Tadiran are interchangeable with conventional dry cells and can serve as power-supply backups. Capacity runs from 0.45 to 7.0 Ah.

Offshore manufacturing was also stressed by RO Associates' Okada: "Most of the major linear power supply companies import their switchers. They will tell you it is due to cheaper labor offshore, but the fact is they tried very

hard to make them in this country and failed. The designs that they are selling are foreign, as well as the manufacturing."

The number of units in the field are a favorite point among companies to prove their soundness. Jeff Shepard of LH Research, for instance, put it this way: "LH has produced more switching regulated power supplies than any other power supply company in the world (more than 250,000 units in the field)."

Consider Warranties

Long warranties also seemed to be worthy of emphasis. Thus, says Robert Hill, president of Electronic Measurements, Inc.: "Customers tend to return to E/M because of a high level of quality, the company's five-year warranty, and its more than 40 years of experience."

A number of manufacturers would cite technological superiority as a good reason for a user to specify their products. A spokesman from Adtech Power, Inc. says: "Adtech's claim to fame is its Univerter design. This is a patented feed-forward, pulse-width-modulated inverter using only one switching transistor."

Mord Shamir also pinpoints technology in HP's use of the flyback principle with power MOSFETs for accurate control. "Also, reliability was achieved by conservatively rating components and by use of a new technology—200-kHz sinewave power conversion—which reduced component count a quarter to a third over conventional pulse-width-modulation topologies."

Other points made by various companies included service, application assistance, reputation, financial stability, fast company growth, large inventories for off-the-shelf shipment, etc. Yet, the all-important question remains: how does one go about selecting a vendor?

It appears that a good way might be as follows. After a quick catalog search, the user should evaluate technical competency of several prospective vendors. This can be done over the telephone by asking various questions pertaining to product performance—a good way to check those claims of the availability of in-depth application assistance. Obviously, if the user gets a runaround at this stage, chances are that he will receive the same treatment as a customer,so this can help cut down the list.

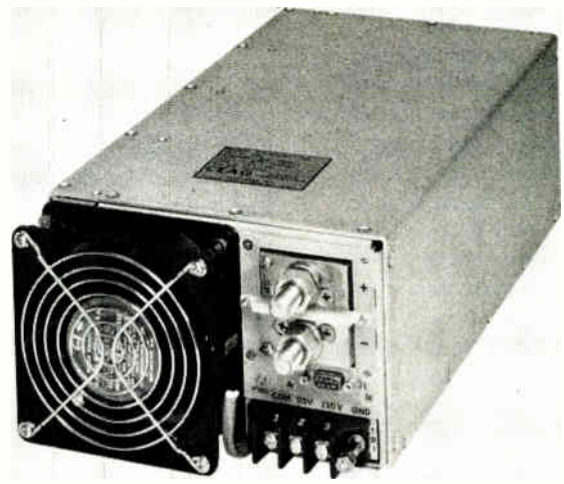
Doing a Search

Once the number of prospective vendors has been narrowed down, the next step might be to touch base with their customers (preferably in the same line of business as the specifier). Of course, these inputs must be treated as possibly subjective, i.e., not all failures of power supplies are the manufacturer's fault.

This step may reduce the vendor list some more. Then the potential user is ready to visit prospective suppliers. To get the most out of such visits, it may be advisable to go as a team, someone from manufacturing, someone from quality control and the test department, someone from the system design group, etc.

"We recommend getting to know your potential vendors by paying a visit to their facilities and discussing your needs in detail with their applications personnel," says Power-One's Cole, "Get a feeling for the company and people you'll be buying from . . . The reputation of the vendor is a key point in this selection process and very important in avoiding specmanship pitfalls."

In other words, vendor selection process in this business boils down to locating a vendor capable of successfully providing answers to a lot of questions, some of which have been brought out in this article. The following partial list of suppliers of power supplies and some related equipment may also be of help. □



Military or industrial versions of this 70% efficient supply are available from Ceag Electric Corp. There are two models with differing outputs; the model 4001, giving 5 Vdc at 300 A, and the model 4008, giving 5 Vdc at 200 A. The supplies offer 30-ms holdup time, 115 or 230 Vac input operation, and they satisfy VDE safety requirements.

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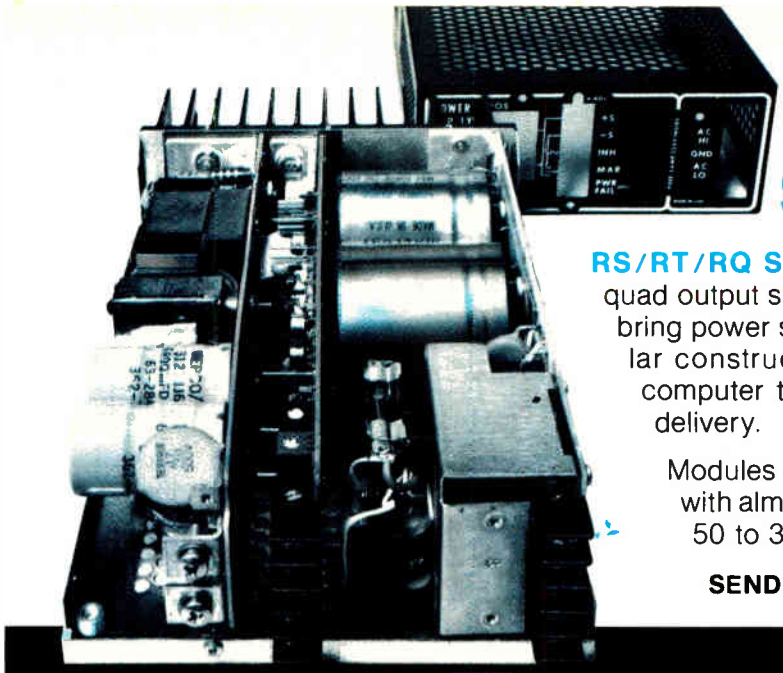

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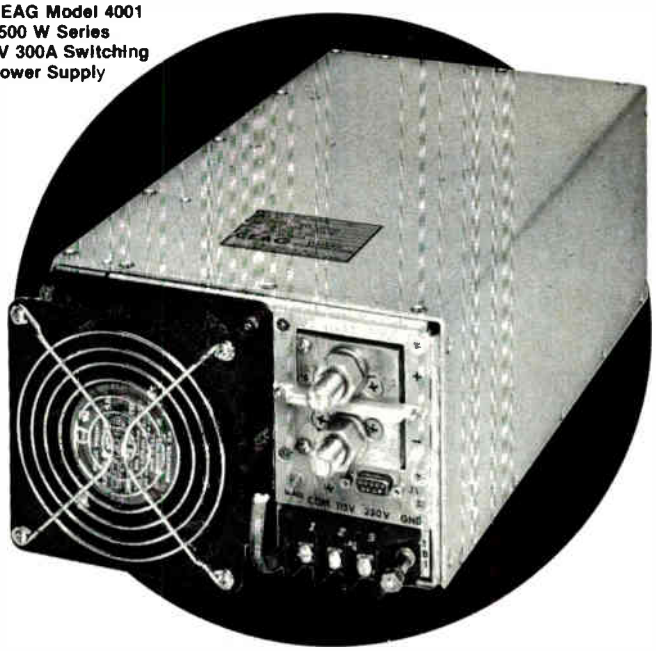

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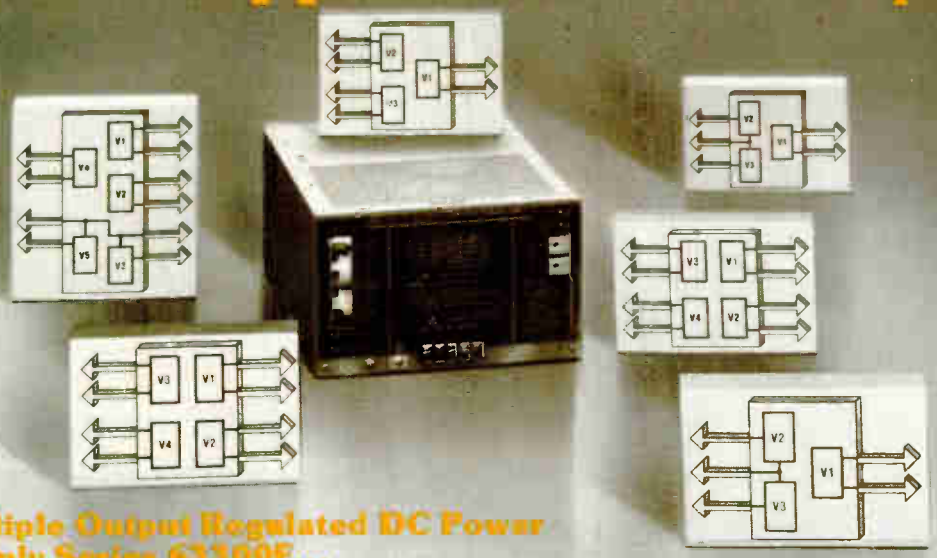

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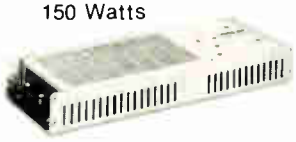

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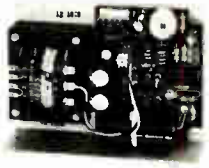

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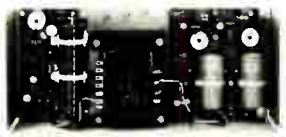

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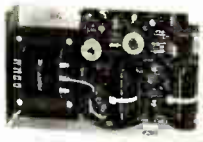

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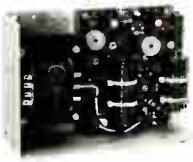

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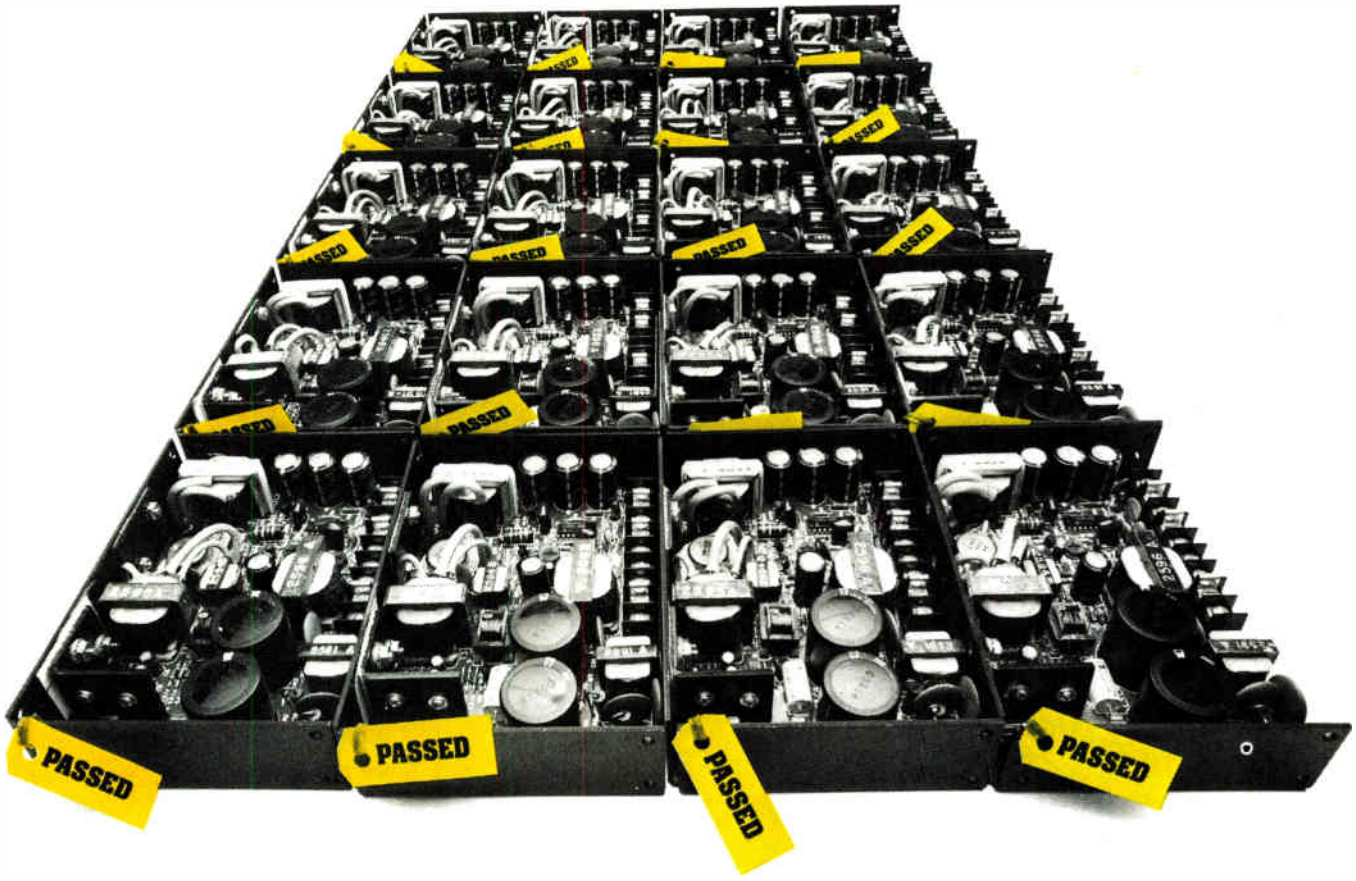

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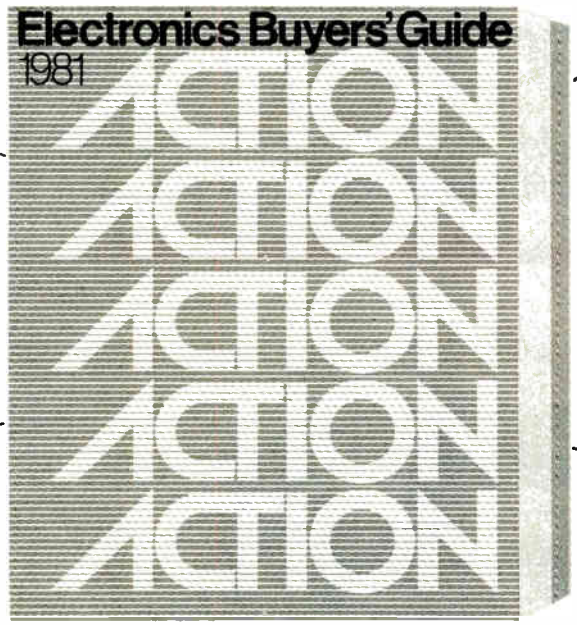

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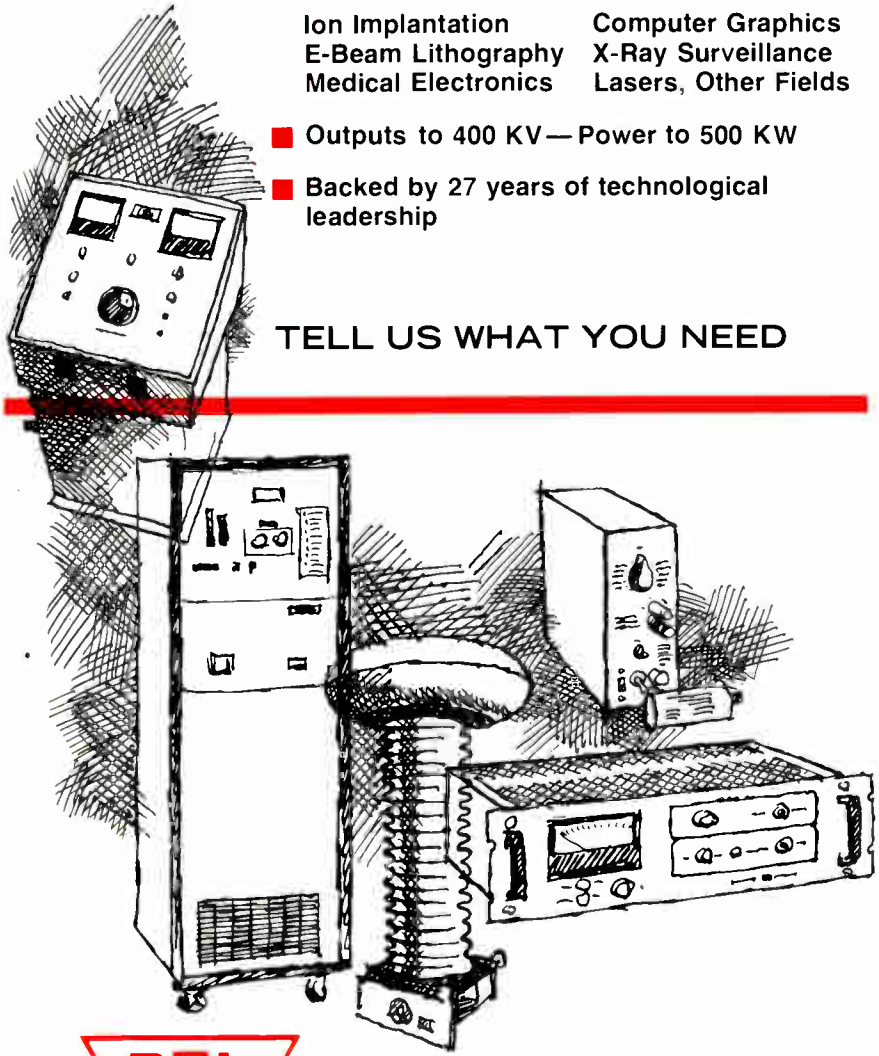

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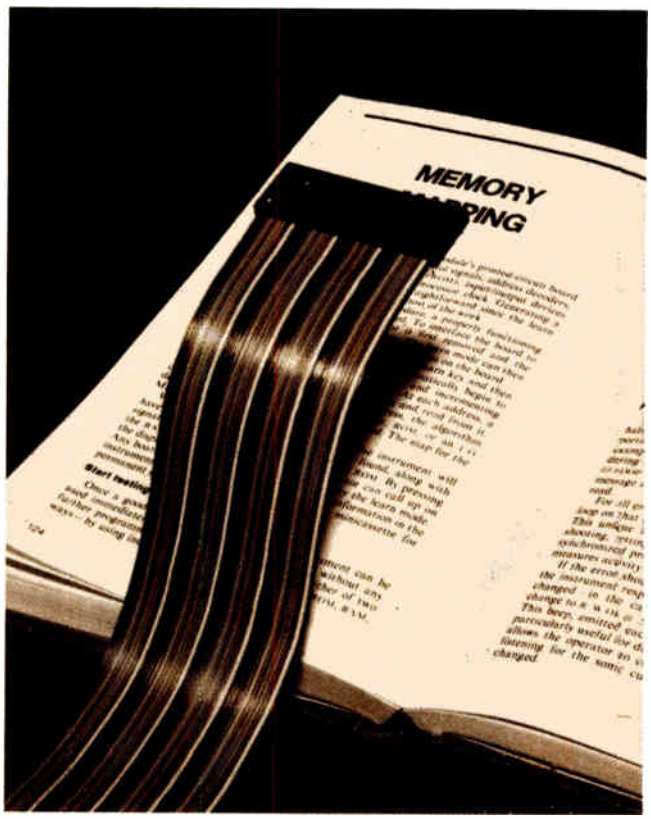
Portable tester learns boards to simplify service

By mapping address space, unit lets an unskilled operator check complex systems with canned tests and guided-probe routines

by Don Cassas, *John Fluke Manufacturing Co., Mountlake Terrace, Wash.*

☐ Since the introduction of the microprocessor, the electronics industry has faced a serious challenge—how to service processor-based printed-circuit boards and the products that use them. Ironically, while microprocessors have advanced product design capabilities and shortened design cycles, their electronic makeup has made testing and troubleshooting them a difficult and time-consuming task. Thus, there is a shortage of people capable of thoroughly examining them.

The industry has therefore been searching for a tool that can be used in the field, at a local depot, or on the production line by technicians who are unfamiliar with the complex technology on which today's products are based. The Fluke 9010A Micro System Troubleshooter (Fig. 1) is such a tool. It is the first portable tester able to automatically learn the memory map of a microprocessor-based product and, once it has done so, immediately begin to automatically test a product by using what it has learned. It is a useful tool for the test engineer or technician, permitting not only instantaneous testing but programming capability for easily creating routines that will support comprehensive system servicing.



Hardware elements

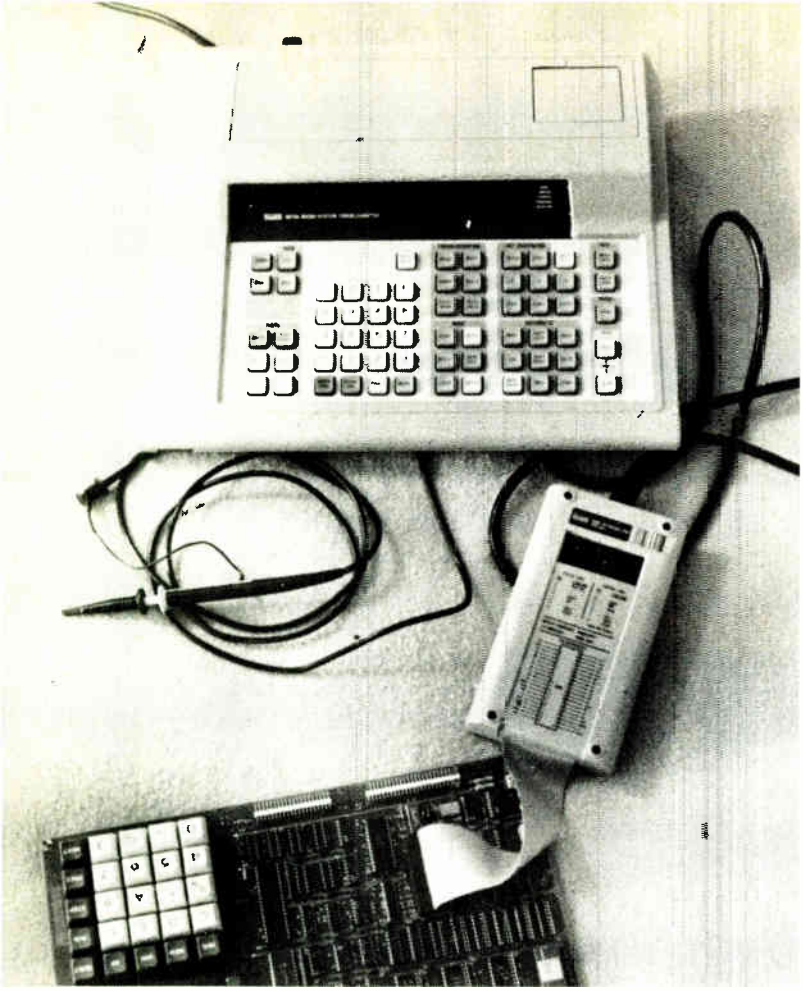
The major physical elements of the 9010A are the mainframe, the microprocessor interface pod, and the synchronizable logic probe. The mainframe holds the system microprocessor, associated memory, minicassette drive, control logic, power supply, and interface circuitry for the pod and probe. It also puts the operator in touch with the unit under test (UUT) via a keyboard and a 32-character vacuum fluorescent display (Fig. 2). In addition, the mainframe of the 9010A accepts a minicassette on which programs and test parameters can be stored for later downloading in a production or service setting.

The interface pod is tailored to a particular type of processor, and versions are currently available for the 6502, 6800, 8080, 8085, Z80, and the 9900. Each pod contains a microprocessor of the same type it is designed to support, along with the associated circuitry. A 64-conductor transmission cable connects the pod to the mainframe; a ribbon cable and 40-pin plug interface the pod with the board that is to be tested (see "The go-between," p. 156).

Inherently, the pod-mainframe architecture is capable of taking on 8-, 16-, and 32-bit microprocessors. Only the pod need be changed to do so, and so the mainframe will not be outdated with each new generation of microprocessor.

The 9010A's logic probe can, at any point in the UUT, read logic-state information or provide a stimulus. What makes the probe a powerful feature is that it can read or stimulate in sync other operations of the UUT.

The hardware for the 9010A can be operated in any of three basic modes: immediate, programming, or executing. The selected mode will be shown on the mainframe



1. A new breed. The 9010A shown above is a new type of instrument, one that can turn an inexperienced technician into a professional troubleshooter. Its processor pod (right) and synchronizable probe (left) are key to its versatility and flexibility.

display. In the immediate mode, a process such as learn or auto test is initiated as soon as the ENTER button is pressed. In the programming mode, the operations and commands chosen, by pressing various keys, to make up a test program are stored in the mainframe's read/write memory, from where they can be transferred to a minicassette for long-term storage. The program thus created can be run either when it is written or later when it is downloaded from tape, by selecting the executing mode.

Examining the test plan for an actual microprocessor-based system is the best way of understanding the capabilities and advantages of the different operating levels of the 9010A. For this example, Motorola's M6800 evaluation kit (MD2) will be used since it contains the major elements currently found in many microprocessor-based products. As shown in Fig. 3, the MD2 has a microcomputer module, a keyboard-display module, and an audio–cassette-drive module.

Memory mapping

A properly functioning board generates the procedure. Its 6800 microprocessor is first removed and the interface pod's dual–in-line–package plug is inserted in its place. This completes the interfacing of the tester with the board. The learn mode can then be used to identify and locate the addressable devices on the board.

The learn mode is initiated by pressing the LEARN key and then the ENTER key. A learn algorithm will automatically begin to explore the system, starting at address 0000_{16} and incrementing through the processor's entire address space. Each address has a variety of complex patterns written into and read from it. Depending on the data read, the algorithm dimensions and classifies the address space as random-access or read-only memory or an input/output device or else designates the location as unclassified. The map for the MD2 is shown in Fig. 4.

When this process has been completed, the instrument will have in its memory a map of all the devices found, along with signatures for groups of the locations identified as ROM. By pressing the RAM, ROM, and I/O view keys, an operator can receive from the display the device addresses that were found by the learn mode. It is necessary to learn a board only once, since the learn parameters contained in the instrument's memory can be transferred to a minicassette for permanent storage and later reused as part of a test plan.

Start testing

Once a good board has been learned, the instrument can be used to troubleshoot identical boards without any programming. Operators can do this in two ways: by using individual test routines for the buses, ROM, RAM, and I/O if they can guess where the problem lies or by using the autotest function, which runs through all the tests sequentially. All tests can be initiated with a single keystroke, with the instrument providing all stimuli and simultaneously detecting and displaying all errors found in the address space.

The bus test checks the electrical integrity of the address, data, and control buses. Control lines that cannot be driven will be identified, as well as all data or address lines that are tied high, low, or shorted to other lines within that bus.

For other push-button tests, the instrument uses the address descriptors generated during the learn mode operation to identify the type, size, and location of the tested function. The short RAM test is a fast means of identifying hard (consistently repeated) failures. It writes a series of complex test patterns into each RAM, checking to see that the data written at each location can properly be read as well as testing for address decoding errors. I/O testing uses the same type of patterns as the RAM test, also checking the write- and read-ability of all I/O bits identified in the learn mode.

Testing ROMs is done by reading the data from each ROM location and then performing a cyclic redundancy check with software to form a signature. This signature can then be compared to the good ROM signature that was generated and stored during the learn mode.

Any time a fault is encountered during a test, the instrument halts the test sequence and allows the operator to loop onto that portion of the test routine in which the failure occurred. For example, if a read-write error occurred at RAM address $A000_{16}$ during autotest or a RAM test, the message R/W ERR @ A000 BTS 03-LOOP? would appear in the display. The hexadecimal 03 in the displayed message indicates that bit positions 0 and 1 are not read-writable.

For all errors, the instrument asks the operator if he

2. User interface. The instrument's keyboard is laid out in a clear and highly functional manner, so that it takes little time to become familiar with it. The learn, view, and test keys (left) allow a user to start checking a board in minutes with the displayed operating mode (right).

wishes to loop onto the portion of the routine in which the error was discovered. This unique looping capability permits more detailed troubleshooting, letting the operator probe the fault location with the synchronized probe while the system continually stimulates and measures that location.

If the error disappears while the test routine is looping, the instrument responds in two ways. The displayed message is changed—in the case of the example cited earlier, it would change to R/W OK @ A000 BTS00—and an audible beep is emitted. This audible beep, emitted each time the displayed message changes, is particularly useful in detecting intermittent (soft) errors, since it allows the operator to concentrate on probing the board while listening for the sonic cue that tells him circuit conditions have changed.

In addition to performing tests selected by the operator, the instrument continually monitors various conditions—such as the drivability of the buses and the state of the power supply—in a background mode. If a background error is detected during the course of a test, a message such as ADDR ERR @ A020–LOOP? or BAD PWR SUPPLY @ A040–LOOP? will be displayed, with the address indicating the location that was being exercised when the condition was found. Obviously, such conditions must be fixed before any other testing procedures are tried. Looping onto the address gives the operator an opportunity to find these problems.

However, error conditions that may hide other errors are given high priority by a built-in hierarchy feature in the 9010A. Thus, if a high-level error occurs in the course of looping onto a fault, the instrument will alert the user to it and permit him to loop onto the portion of the routine that caused it. When the higher-priority error is cleared, the instrument will automatically return to the lower-priority one and resume testing.

More skilled

While the 9010A's ability to learn test and background features make it usable by any operator, its troubleshooting characteristics can greatly simplify and speed up the work of experienced technicians and engineers.

Any of six troubleshooting functions can be automatically performed at an address specified by the user. These functions are: read, write, address toggle, data toggle, and two patterns—ramp, in which the data progresses from 0000 0000, to 0000 0001, to 0000 0011, and so on to 1111 1111, and walking 1s, where the data progresses from 0000 0001, to 0000 0010, to 0000 0100, and so on. Each function can be selected by pressing the desired function key.

Once a function is selected, the display will prompt the user to specify the address where the function is to be

The go-between

The 9010A's interface pod design is key to the instrument's ability to adapt to present and future processors. This is possible because of the pod's functional partitioning into three sections, as shown in the figure below.

The processor section has a microprocessor of the same type as that used on the unit under test (UUT) and an input/output interface to the mainframe. These elements create a small computer system that receives mainframe commands and directs all pod operations during execution. All resets, nonmaskable interrupts, and other disrupting inputs that may occur on the UUT are hardware-buffered to prevent UUT failures from disabling testing operations.

The UTT interface section includes data and address buffers, protection circuits, and logic-level detection for data, address, status, and control lines. Data and address buffers can connect the pod to the UTT or be disabled to isolate the pod from it. Buffer control is maintained by the pod timing section.

The interface section's protection circuits consist of a series of resistors and clipping diodes that prevent over- or under-voltage conditions from damaging pod components if the pod is plugged in incorrectly. The detection circuits in the 9010A contain a set of latches that, at the conclusion of each UUT operation, store the condition of the UUT's lines. These latches are then individually addressed and read by the pod's processor section. For detecting various UUT faults, their contents are compared with the desired results, as determined by the mainframe when an operation is set up.

The primary function of the pod's timing section is to switch the microprocessor to operate either with the pod's processing section or with the UUT interface section after a predetermined, microprocessor-timed interval. Two subsections contained in the pod are required to do this: an interval timer and the timing circuits.

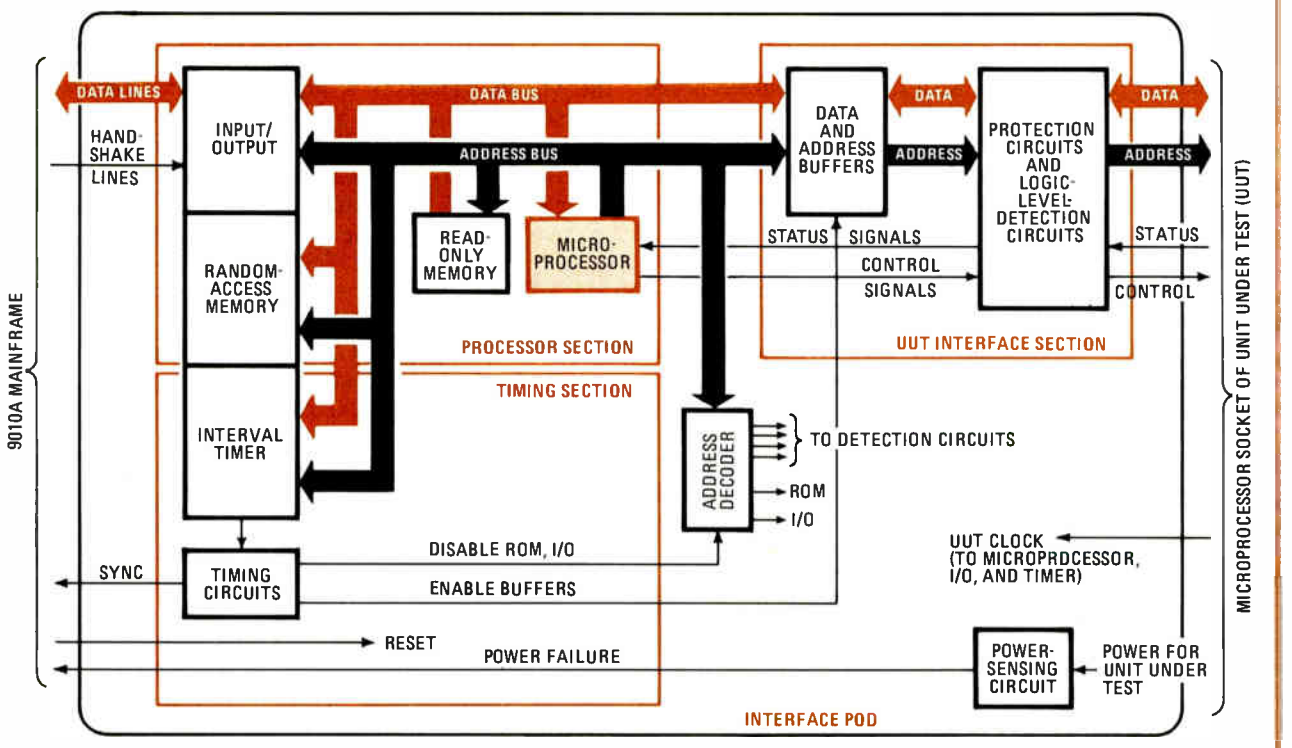
The interval timer, preset by the microprocessor, determines the time at which the microprocessor switches from addressing one section to another. This timing is critical, since any attempt by the processor to address the processor section with addresses meant for the UUT interface section, or vice versa, would result in improper testing.

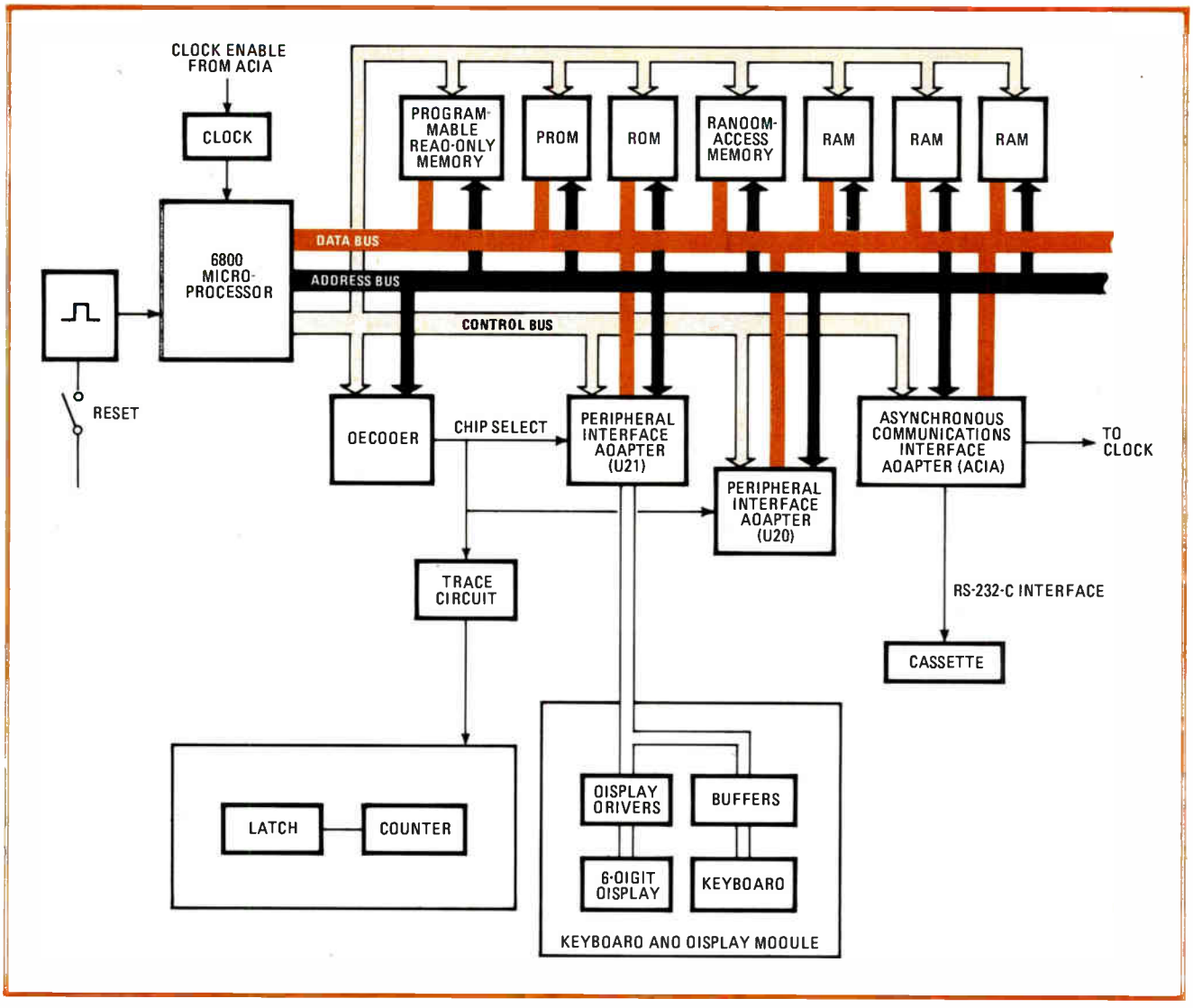
When in the reset state, the timing circuits cause the microprocessor to operate as part of the processor section, which includes the I/O port to the 9010A mainframe. When the mainframe issues a command calling for a UUT read or write operation, the microprocessor sets the interval timer to a specific value, corresponding to the execution time that is needed prior to addressing the UUT.

When the interval timer reaches time-out, the timing circuits produce an output disabling the processor section read-only memory and I/O and enables the buffers of the UUT interface section. This causes the microprocessor to switch to the latter section. At the same time, the microprocessor, having completed preparation for command execution, places a UUT address on the address bus and reads or writes data on the UUT data bus.

After the required period of time, the timing circuits terminate the UUT addressing and the microprocessor returns to controlling the processor section. The timing circuits also operate the latches within the logic-level detection circuits to store the results of the UUT read or write operation.

The pod receives all of its power from the mainframe and uses only the UUT's on-board clock. Using the UUT clock assures that the pod operations will be in correct time intervals. Due to the switching scheme, all bus transactions occur at the UUT's bus cycle speed and thus all communications and testing operations stimulate the UUT's normal operation.





3. Typical challenge. The M6800 evaluation kit 2 (MD2) is a typical board, containing RAM, ROM, PROMs, and several I/O devices. Able to locate and test such bus-resident devices automatically, the 9010A does away with the need for voluminous software documentation.

applied and, in the case of write, the data to be written. For example, if the ramp function is selected, the 9010A would display RAMP and the operator would enter a hexadecimal address. By pressing the ENTER key, the function will be executed.

Using these troubleshooting functions, the remaining portions of the MD2's microcomputer module—the balance of the decoding logic, the programmable interface adapters (PIAs), and the asynchronous communications interface adapter (ACIA) can easily be checked, as can the display and keyboard.

One logical place to begin checking the remaining logic would be the display circuitry. If the technician did not know the address of the PIA that controlled the display, the 9010A could help him find it and thus begin testing the unit.

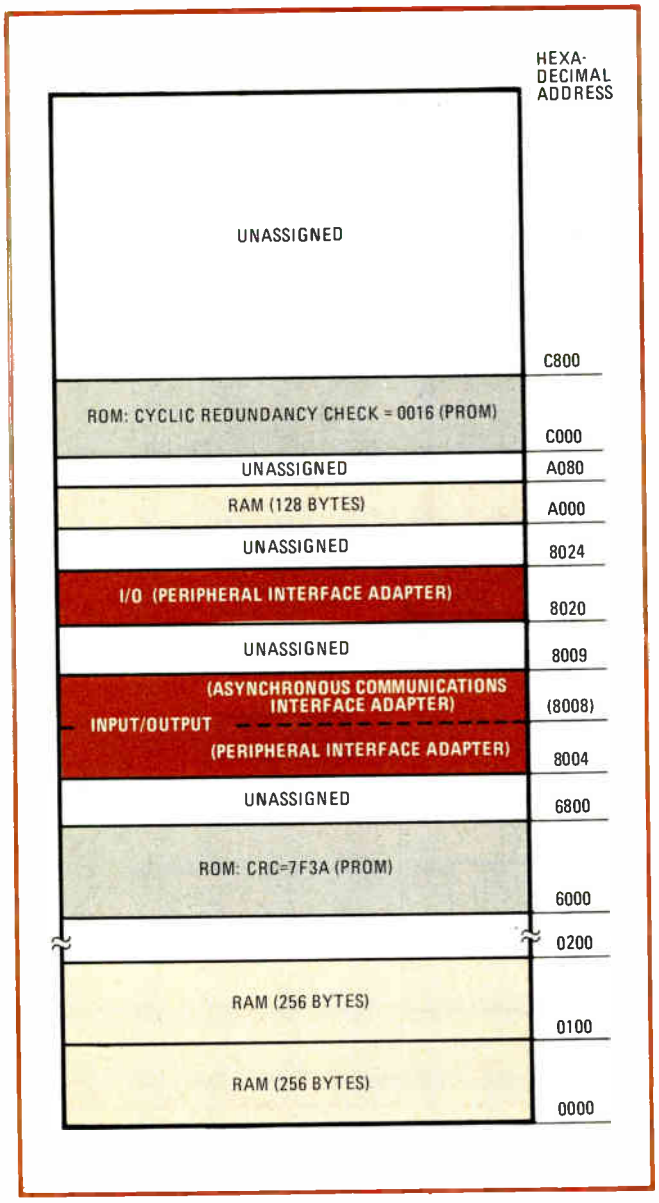
During the learn operation, it was found that the MD2's I/O was located at addresses 8004_{16} through 8009_{16} and 8020_{16} through 8023_{16}. It also established the readability and writability of bits within the address and stored them as 3F. Decoded, this represents 0010 1111: a 1 indicates that the bit can be written into and read from and a 0 indicates to the 9010A that it can be read.

If operators are unaware of the PIA's address, which controls the MD2's six-digit light-emitting-diode display, they can use the ramp function by applying it to each address until the display lights. Noting the address location tells them where to start.

Who's on 0001?

On the MD2, address 8020_{16} selects port A of PIA U21, which controls the individual segments of each LED and address 8022_{16} selects PIA port B, which selects one of the six LED digits of the display. By writing a hexadecimal code to each port (for example, 78 selects digit 7, 0E selects the segments that make up the character F), using the write function, and observing the display, it is possible to check each segment of every digit.

In a similar manner, the PIA's keyboard control and the ACIA's control of the tape drive can also be checked manually. But since these tests require many steps, it would be useful if this test procedure could be stored by



4. Mapped. After going through a learn operation on the good board, the 9010A contains in effect a map of the address space of the board, such as that for the MD2 above. Pressing one of the front-panel view keys gives the operator the device addresses, along with a CRC signature for ROM-type devices.

the 9010A. This aspect will be further examined when the programming mode is discussed.

To check address spaces in a system that are not identified in the learn mode, the synchronizable logic probe is used (see "Probing in sync," p. 159).

In this instance, the operator selects one of the troubleshooting functions, such as ramp or walking 1s, synchronizes the probe to the data pattern, and walks down the board's data lines with the probe, following the bit stream. Even though the data bus is continually running, synchronization allows the operator to determine the correct logic state at the exact time that data becomes valid. For off-bus logic, a free-run mode lets the probe examine logic that is not synchronized to the microprocessor clock of the UUT.

To examine complex data streams, the READ PROBE key is used. The logic probe is continually gathering data and, by depressing the READ PROBE key, the operator can see what is in the data-collection window. Data is then stored in an internal register that will contain the transition count, a cyclic redundancy check signature, and the logic level. In the immediate operation mode, this data will be displayed on the 9010A so the operator can evaluate it.

In addition to its response measurement capabilities, the probe can be used to drive a node high or low or to toggle it. This is useful for stimulating nodes off the bus or for injecting faults into the nodes so that their effect on the system may be determined. Furthermore, the 9010A can trigger an oscilloscope, permitting actual waveforms to be viewed in synchronization with events in the system, particularly those that would otherwise not recur and very difficult to observe.

Although these troubleshooting operations do require a certain level of skill from the operator, the particular advantage of the 9010A is that it allows this skill level to be automated and transferred to lower-skill personnel. This is done by operating the instrument in the programming mode.

Technology transfer

Creating a test program that is sophisticated enough to guide an unskilled operator through a troubleshooting procedure is a surprisingly simple task. When the program key is pressed, virtually every key on the instrument, including the test and troubleshooting keys, can be used as a program statement.

To create a complete test program, the operator—or in this case, the programmer—would follow the operating procedures that have already been demonstrated. Thus, an operator would start to program by letting the 9010A learn a good board. Then, by using the programming mode, the programmer would call for the preprogrammed tests, which automatically provide both stimulus and fault isolation. Next, that person would turn to the preprogrammed troubleshooting stimuli and, using them, create a program such as that for the MD2's display PIA shown on page 160.

The overall test program consists of a number of subroutines that take up 383 bytes of memory. A wait loop in the program (program 2) enables the operator to make a visual check of the display. At the end of the program (program 5), the 9010A is programmed to display a message asking the operator for the test results. If the display fails to pass the test, the mainframe software calls a guided fault routine that directs the operator to pinpoint the fault's exact cause.

The remaining MD2 logic—the ACIA and the other PIA—are also tested most efficiently by using programs developed on the 9010A. Since the other PIA is not functionally connected to any external logic circuits, a loop-back technique is used. This is accomplished by wiring a test connector to its off-bus side and tying port A to port B. The PIA control register can then be set up so that port A becomes an input port and B an output port. Thus data written to A can be read from B.

The ACIA controlling the tape drive is also tested by

Probing in sync

By using the probe sync function, an operator can synchronize the probe's operation with a particular address or data period. With this feature, data appears static at the probe tip even though the actual signals may be wildly fluctuating. It is much easier to troubleshoot the system when the signals appear static.

The communication among the 9010A mainframe, interface pod, and probe is shown in the block diagram below. The timing of the interface pod is derived from the unit under test, so operations occur at the UUT's speed. When the interface pod is communicating with the mainframe, the UUT's timing and control signals continue uninterrupted to ensure that any dynamic-memory access and refresh activities occur in a normal manner.

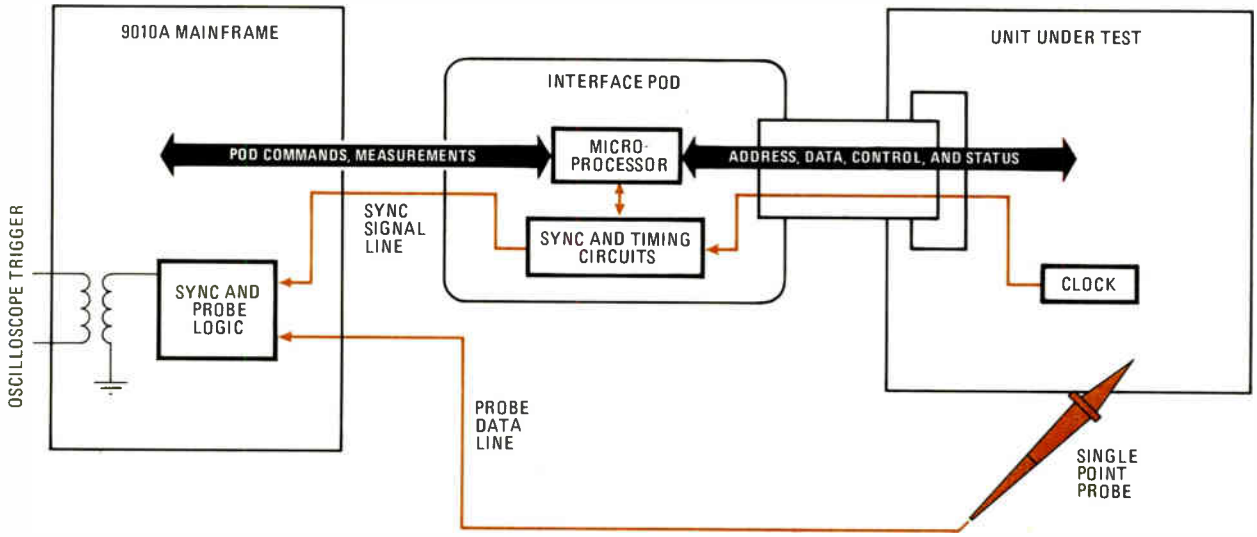
When the user or a program statement selects the sync mode, a set-up synchronization command from the mainframe sets the pod to generate sync signals on all subsequent operations. The sync mode remains in effect until it is changed by the user or program.

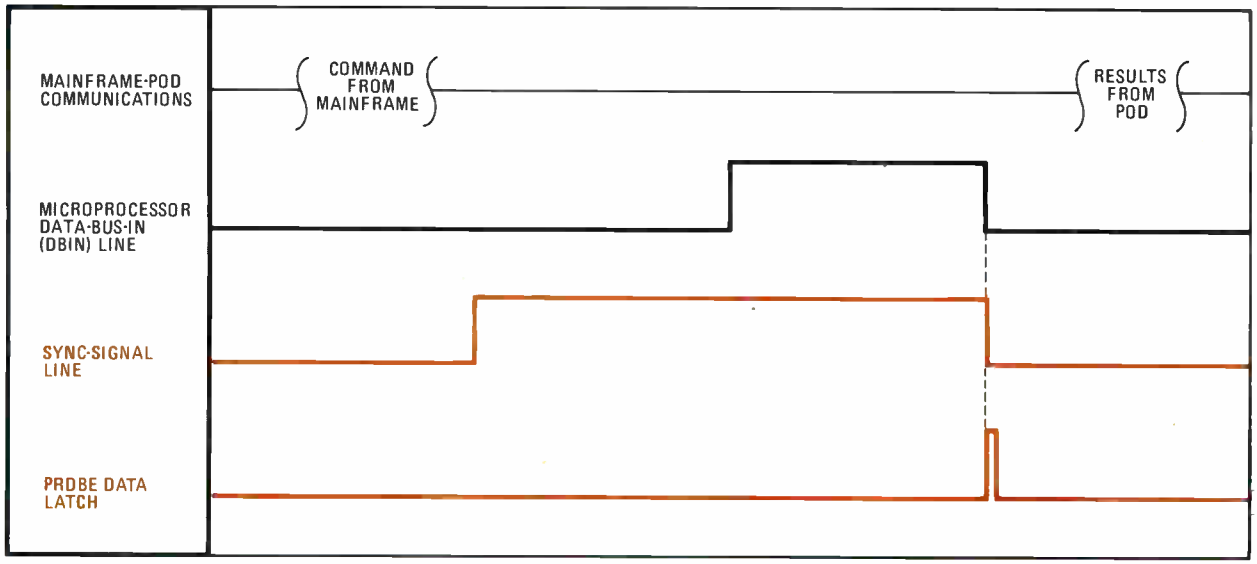
The timing of signals between the mainframe, pod, and probe is also shown. When a UUT operation, such as read address 8020_{16} is requested, the mainframe sends this command to the pod. Since the pod is running on the UUT clock, it knows exactly when the read will occur. It can therefore put out a signal on the sync line that runs back to the mainframe.

For the timing example shown, an 8080 microprocessor has data latched into the microprocessor on the falling edge of the data-bus-in signal. In the 8080 interface pod, the synchronization signal is also turned off at the same time the data is latched, and the falling edge is used to latch the probe data in the mainframe. Thus, data from the probe is captured at the instant it should be valid.

In addition to driving the data-valid indicator lamps, the latched data is employed for signature generation. The interface pod sync signal also drives a pulse transformer generating an oscilloscope triggering signal. Thus real, nonrepetitive waveforms can be viewed.

The probe can generate a stimulus pulse to drive the UUT nodes high or low, in sync with the UUT. Thus, pulses may be very short, yet occur precisely when the UUT is being read by the processor.





DISPLAY TEST PROGRAM FOR THE MD2 6800 EVALUATION KIT

Program	Comments
PROGRAM 0	character generation subroutine
DPY–MD2 DISPLAY TEST	message for 9010A display
WRITE @ 8021 7F	initializes display control register
WRITE @ 8020 BF	blanks MD2 displays
0: LABEL 0	
REG9 = 8020	display address
REG8 = 40	0 display character
EXECUTE PROGRAM 1	calls display-write subroutine
REG8 = 79	1 display character
EXECUTE PROGRAM 1	
REG8 = 24	2 display character
EXECUTE PROGRAM 1	} 3 through 9 and A through E display characters and display-write-subroutine calls
⋮	
REG8 = OE	F display character
EXECUTE PROGRAM 1	
EXECUTE PROGRAM 3	
PROGRAM 1	display-write subroutine
1: LABEL 1	
WRITE @ REG9 = REG8	writes character to display
EXECUTE PROGRAM 2	
PROGRAM 2	wait-loop subroutine
REG3 = 50	
1: LABEL 1	permits visual inspection of display
DEC REG3	
IF REG3 > 0 GOTO 1	

Program	Comments
PROGRAM 3	control-value-generation subroutine
REGA = 40	control value for display 1
EXECUTE PROGRAM 4	calls display-select subroutine
REGA = 80	control value for display 2
EXECUTE PROGRAM 4	} control values and display-select-subroutine calls for displays 3 through 5
REGA = 08	control value for display 6
EXECUTE PROGRAM 4	
EXECUTE PROGRAM 5	
PROGRAM 4	display-select subroutine
REGA = REG6	
1: LABEL 1	
REG4 = 8022	
WRITE @ REG4 = REG5	select display (0–6)
EXECUTE PROGRAM 1	calls display-write subroutine
PROGRAM 5	test-result subroutine
DPY–DID DISPLAY PASS TEST?6	display message waits for yes/no key input from operator, places value in register 6
IF REG6 = 1 GOTO 1	if no (reg 6 = 1), branch to label 2
GOTO 2	
1: LABEL 1	
DPY–END OF DISPLAY TEST	
GOTO 3	
2: LABEL 2	
EXECUTE PROGRAM 10	calls guided-fault subroutine
3: LABEL 3	
DPY–END OF MD2 DISPLAY TEST	

using a variety of stimuli that are provided by the 9010A. Test results can be obtained by observing the tape drive's operation.

The key to easy development of such programs is that many of the normal stimulus patterns required to excite the UUT are already preprogrammed. This reduces the number of read/write operations that would have to be written in other circumstances.

Once the basic stimulus program is developed, the programmer can then begin developing a prompting routine leading an unskilled operator back through a fault sequence to the fault's initial cause. Such a routine is needed only for off-bus logic since all preprogrammed tests with the 9010A have their own fault-handling routines for on-bus logic.

Further simplifying routine generation is the fact that off-bus logic is generally the most straightforward portion of the UUT to create a fault tree for. The synchronous logic probe can also be called into the program so that state and signature analysis event counting can be used to simplify fault finding.

As the program is generated, it is sorted in the mainframe's 10-K-byte volatile memory. The mainframe uses interpretive programming, so a programmer can quickly close and execute each segment of the program as it is completed. Thus, an operator can get immediate feedback without waiting for a program to be assembled and compiled. Two editing keys permit the user to scroll through the program, deleting or inserting lines if the program does not perform as intended.

Once the programmer is satisfied with the result, the program can be transferred to permanent storage on a minicassette. This tape can then be given to factory and field personnel and in effect transfers the know-how of the person who best understands the board quickly and easily to those who need it.

Up to 100 separate programs can be called by the 9010A, each consisting of virtually hundreds of steps. For controlling program flow, the programmer is provided with eight sequencing keys. They permit conditional or unconditional branching, calling subroutines, and display of user-prompting messages. Mode controls such as STOP or LOOP can also be used to control the execution of the program.

Eight arithmetic keys perform logic functions such as AND, OR, and DECREMENT on data that is stored in user registers. There are 16 32-bit registers available for programmer use; they enable parameters to be passed from one routine to the next as well as allowing data manipulations for counting and timing. □

Single chip encrypts data at 14 Mb/s

Three on-board write-only registers ensure key security under standard microprocessor or bit-slice control

by Dave MacMillan
Advanced Micro Devices Inc., Sunnyvale, Calif.

☐ When the U. S. government wants to protect sensitive data from prying eyes, it requires the data to be enciphered according to the National Bureau of Standards' data-encryption standard (DES). With the Am9518, a microprocessor peripheral chip from Advanced Micro Devices, this code can now be implemented at 14 megabits per second—fast enough to encrypt or decrypt on the fly as data is read from or written onto disk. Moreover, this rate is high enough to accommodate most telecommunications systems without the need for buffers. The resultant savings in memory and interfacing circuitry is considerable for both computer and communications applications.

High encryption and decryption speed is not the only feature of the 40-pin n-channel MOS chip (Fig. 1). The 9518 (and the AmZ8000 microprocessor family's identical AmZ8068) supports bidirectional, half-duplex operations at its top speed. Furthermore it contains three write-only key registers for enhanced security and can be configured in any of the three encryption/decryption modes recommended by the NBS [*Electronics*, June 5, 1980, p. 96].

Telecom and data storage

Called the data-cipher processor, or DCP, the 9518 is intended for two markets: telecommunications and data storage. In telecommunications applications, it will usually be controlled by a standard microprocessor. In data-storage applications, it will encipher data as it is passed to (or from) a tape or disk drive and will be controlled by the tape or disk controller. Most of these tape and hard-disk controllers are based on microprogrammable bit-slice logic designs. To simplify system design in these applications, the 9518 has a special microprogrammed interface (called the direct control configuration), in addition to a standard microprocessor interface.

As part of the latter, there are two additional interface options. To attain this flexibility, the DCP uses three ports: a master port, a slave port, and an auxiliary port. The master port is bus-compatible with the Z8000 microprocessor and has an address-strobe ($\overline{AS}$), a data-strobe ($\overline{DS}$) and a chip-select ($\overline{CS}$) input, in addition to eight bidirectional address/data lines. The slave and auxiliary ports, with eight data lines, are subsets of the

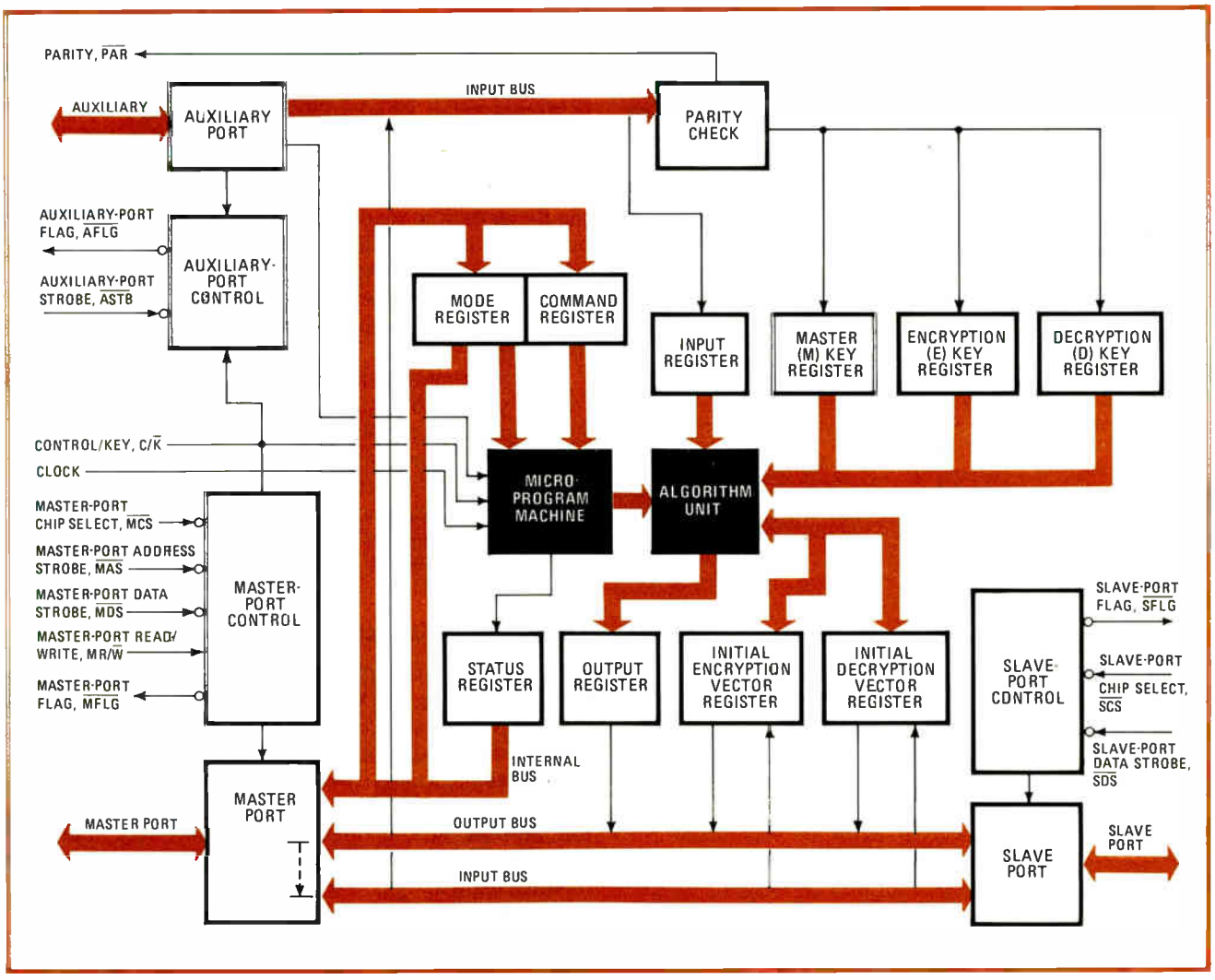
Why a single data-encryption chip?

In addition to the usual reasons of lower power consumption, a smaller space requirement, increased performance, and easier system design for a one-chip instead of a multichip encryption and decryption scheme, there is another little-known rationale unique to the data encryption standard. Although the Government's regulations specifying the DES requirements are still being developed, it is likely that all DES equipment will have to be able to verify that it is operating correctly using one of two approaches as chosen by the system designer.

The first requires that whenever the DES device is not actively enciphering real data, test data must be pumped through it and compared with the expected output to verify correct device operation. This approach demands of both single- and multiple-chip encryption devices the almost full-time support of a microprocessor, in addition to special test software.

The other approach is to operate two DES devices in parallel and compare their outputs. With a single-chip device, the implementation of this approach is straightforward and requires minimal board space and overhead. On the other hand, DES devices using multiple chips for enciphering and a handful of interface components to connect to the system, the space requirements are formidable, and the user is forced to take the first approach.

Thus, with a single-chip device, the user can select either approach to best fit his space, speed, and cost constraints.



1. Versatile. The n-MOS Am9518 peripheral device can be controlled by a standard microprocessor or bit-slice processor for either telecommunications or disk-drive applications, respectively. For security, its key registers are write-only.

Z8000 bus interface. The interface flexibility results from the way these ports can be configured.

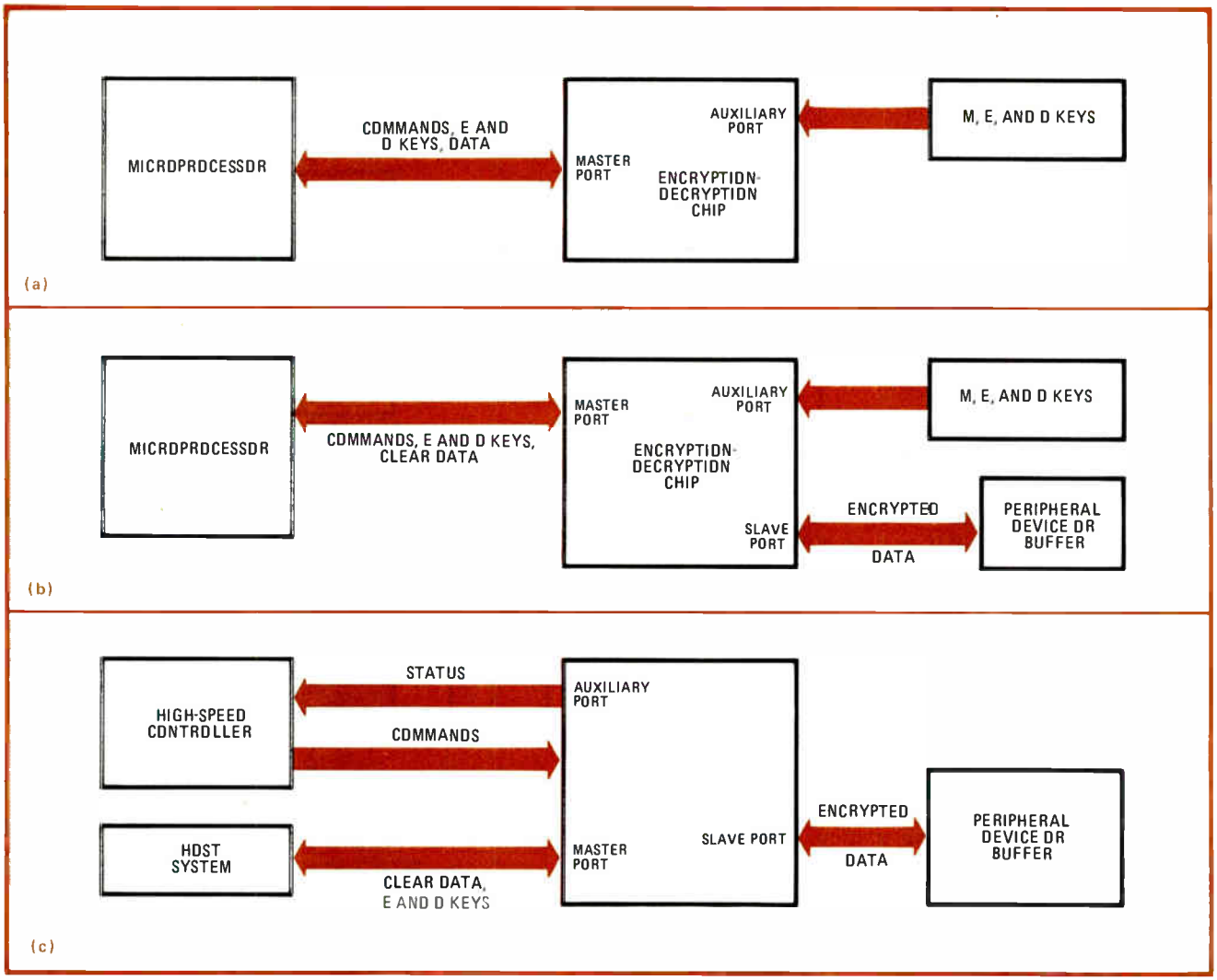
The most straightforward interface configuration is the master-port–only interface (Fig. 2a). In this mode, all commands and data are passed between the host microprocessor and the DCP through the master port. The encryption and decryption keys (described below) may be entered through either the master or the auxiliary port. In contrast, the master key may be entered only through the auxiliary port. The use of the separate auxiliary port to enter key data, perhaps directly from a keypad attached to the port, means that hardware separates data being enciphered from key data. Such a separation eliminates the possibility of a software error's jeopardizing the security of the keys.

In the second microprocessor-based interface (Fig. 2b), both the slave and the master port are used to pass data, although all commands pass through the master port only. In this mode, the DCP behaves like a bidirectional, half-duplex pipeline. The user selects which side (either the slave or the master port) is to handle encrypted data and which side is to handle clear data. The DCP can then be programmed either to encrypt, accepting data from the clear-data side and passing it on from the encrypted-data side, or to decrypt, passing data in the opposite direction.

The architecture of the DCP is highly pipelined, so that the user can enter one 8-byte block of data while a previously entered block is being enciphered and while a third previously coded block is being read out. This pipelining yields enciphering rates of more than 14 Mb/s.

As is the case with the master-port–only configuration, hardware separation between the clear and the encrypted data enhances system security. For example, in an application like a telecommunications concentrator, separate microprocessors might be used on the clear- and encrypted-data sides to provide high throughput and to ensure that the two types of data never mix. Also, as with the master-port–only configuration, the user may enter encryption and decryption keys through the master port or, for enhanced security, encryption, decryption, and master keys through the auxiliary port.

The third possible interface applies to systems with a bit-slice processor. The DCP may be configured for such designs by applying a high signal to its control/key



2. Three configurations. The 40-pin encryption chip can be hooked up as a single-port (a) or dual-port (b) device under time-multiplexed control or as a dual-port device under the management of a high-speed controller (c). All configurations are bidirectional and half-duplex.

(C/$\overline{K}$) pin. The auxiliary port is now reconfigured from an address/data multiplexed control to a direct control that interfaces directly with the bit-slice controller (Fig. 2c). Three of the port's signals are inputs, used to tell the DCP what operation to perform (encrypt or decrypt, load keys, start/stop). These lines may come directly from microcode memory.

In addition, status lines come out to indicate the state of the DCP. These outputs would typically be connected to the bit-slice sequencer for conditional branching based on the DCP's status. In the direct control mode, as in the microprocessor mode, data is passed via pipelining into the master port and out of the slave port or vice versa, depending on whether encryption or decryption is being performed.

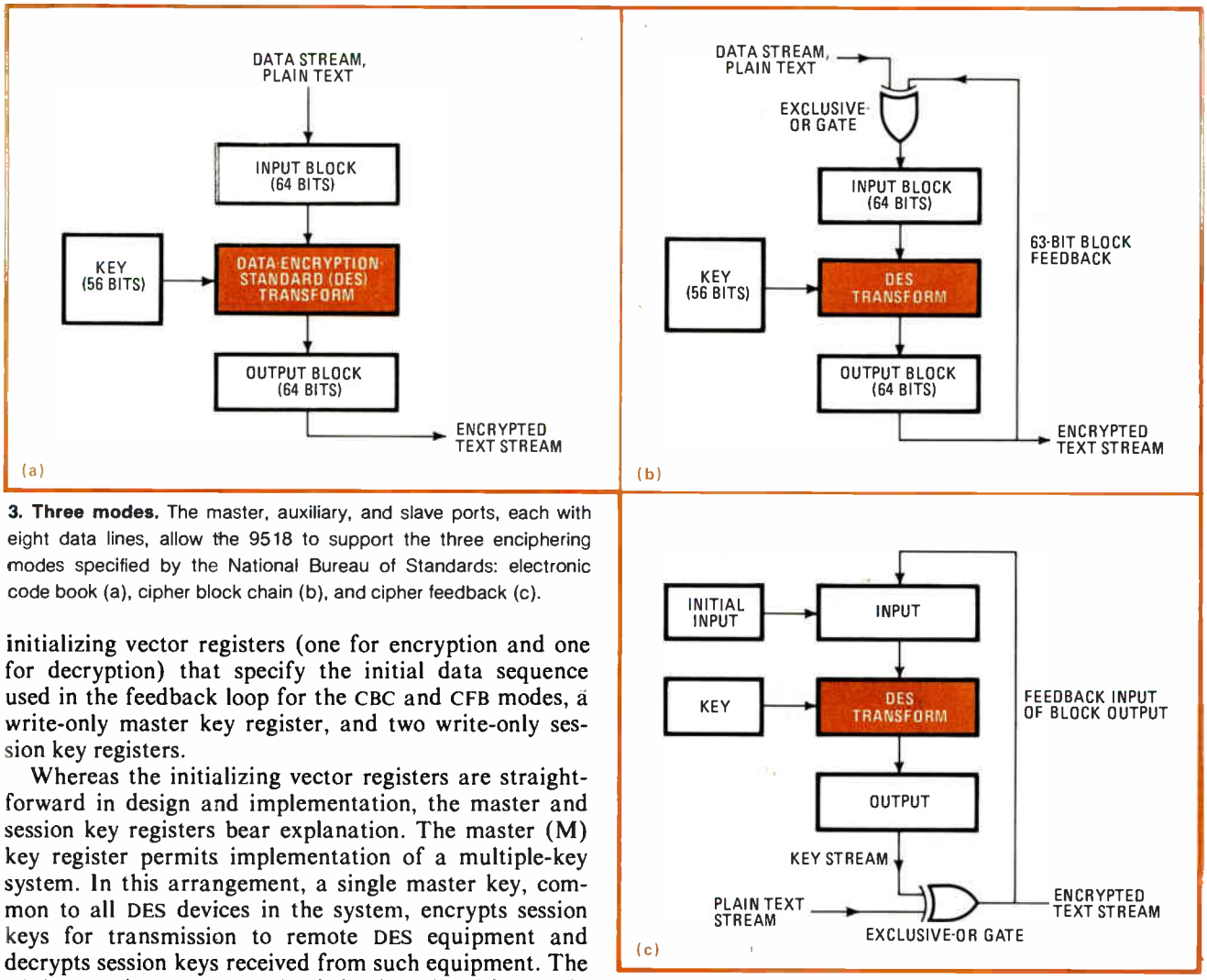
Three modes

The DCP takes care of the three NBS-required enciphering modes by selecting from a 2-bit field of its mode register. These modes are known as the electronic code book (ECB), the cipher block chain (CBC), and the cipher feedback (CFB). Any enciphering option can be used with any of the interface options discussed earlier. The electronic-code-book mode (Fig. 3a) is a straightforward implementation of the DES: 64 bits of clear data in, 64 bits of coded text out, with no cryptographic dependence between blocks. It will be used mostly in disk applications, because the disk's need for random access and independence between data blocks is important.

The cipher-block-chain mode (Fig. 3b) also operates on blocks of 64 bits but includes a feedback step that chains consecutive blocks so that repetitive data in the plain text (such as ASCII blanks or runs of 1s and 0s) does not yield repetitive coded text. This approach also allows the data receiver to detect fraudulent data insertions and deletions. It will be widely used in telecommunication applications because of its message-tampering protection.

The cipher-feedback mode (Fig. 3c) is similar to the second in that it includes the logical linking of blocks required for detection of message insertion or deletion. Unlike CBC, however, it is byte-oriented, encrypting 8 bits of data at a time.

The DCP also contains three features that must be added to other encryption chips using external logic or host system software if they are desired. These are



3. Three modes. The master, auxiliary, and slave ports, each with eight data lines, allow the 9518 to support the three enciphering modes specified by the National Bureau of Standards: electronic code book (a), cipher block chain (b), and cipher feedback (c).

initializing vector registers (one for encryption and one for decryption) that specify the initial data sequence used in the feedback loop for the CBC and CFB modes, a write-only master key register, and two write-only session key registers.

Whereas the initializing vector registers are straightforward in design and implementation, the master and session key registers bear explanation. The master (M) key register permits implementation of a multiple-key system. In this arrangement, a single master key, common to all DES devices in the system, encrypts session keys for transmission to remote DES equipment and decrypts session keys received from such equipment. The M key register may be loaded with clear data only through the auxiliary port.

The session keys

The two session key registers are an encryption (E) key register for encoding plain text and a decryption (D) key register to decode enciphered text. These keys may be loaded through either the master or the auxiliary port. In some telecommunication environments, E and D keys will be transmitted from a user at a terminal to the host computer. To provide security for the transmitted keys, the key data will be enciphered using the M key.

When the host computer receives the encryption and decryption keys, it decodes them using the master key. All subsequent communication between the host and the user uses the E and D keys. To support this type of interchange, the DCP has provisions to receive an encrypted E or D key, decrypt the key information using the M key, and store the decrypted E or D key in the appropriate key register. Because the entire operation is done on chip, the host will never see clear E or D keys. Thus the system is highly secure.

Although in most systems the same key will be used for encryption and decryption, it is not a DES requirement. Because of its separate registers, the 9518 can work easily in systems employing separate encryption and decryption keys. The use of separate keys is readily accomplished, since the time-consuming reloading of the key register when changing from encryption to decryption and vice versa (required for DES devices with one key register) is eliminated.

The NBS standard specifies that each key byte must include a parity bit. Therefore, as a validation procedure, a parity-checking circuit is activated on the chip whenever the host central processing unit enters any E, D or M key in clear or encrypted form. The output of the parity detection circuit is connected to a parity (PAR) pin (see Fig. 1 again) and the state of this pin is reflected in the DCP's status register. In addition to the PAR bit, the status register has a latched parity (LPAR) bit that is set to 1 if the status-register PAR bit goes to 1. Once set, the LPAR bit is not cleared until a reset occurs or a new load-key command is entered.

The 9518, however, goes one step further than is required to ensure data integrity by adding an abort sequence. Because of the complex nature of the encoding processor, considerable internal checking is needed for internal consistency, and an abort will be generated if basic operating rules are violated. For example, writing a command into the command register before a previous command is completed triggers an abort.

Data encryption: a future market?

Over the next few years, the U. S. government will pass regulations requiring the use of encryption devices that conform to the National Bureau of Standards' data-encryption standard on all nonmilitary Government archiving of data on disks and tapes, as well as in data communications. These regulations, which are being drafted by various Federal agencies, will be significant for any computer manufacturer who wishes to sell his equipment to the Government. Their impact is also well appreciated by the semiconductor manufacturers, as shown by the dozen or so DES-compatible encryption chips of varying capabilities that are currently available for evaluation.

Although few pieces of computer equipment now have encryption capabilities, as the regulations are developed and the communications protocols are made final, manufacturers will start to include DES devices in their products. In addition, "black boxes" will be developed with encryption capabilities to fit older products. Initially, most firms will simply have an extra-cost socket for these devices. Then, as the use of the data encryption standard spreads to industries concerned with confidentiality, they will become a regular part of most computer equipment.

The 9518 is faster than any other DES device sold today. This feat was accomplished by processing a complete 64-bit data word in parallel, rather than serially, as many other devices do, and by using a pipelined architecture, as mentioned earlier.

Up to speed

As noted, the three-stage pipelined architecture allows the user to simultaneously put a 64-bit input on one 9518 port while the chip is enciphering a previously entered block and while the user is reading out (from a second 9518 port) a previously processed data block. Although data is transferred into and out of the two 9518 data ports in bytes, it is internally assembled into a 64-bit word. This word is processed in a 64-bit parallel fashion, instead of a bit or byte at a time.

Because processing can occur while data is being transferred into and out of the 9518, the chip can be internally manipulating data 100% of the time. In a typical system design exploiting the pipelined architecture, a direct-memory-access device, such as the 16-bit AmZ8016 (operated in the byte mode) or the 8-bit Am9517/Intel 8237, is used to transfer data fast enough to keep the 9518 operating at its maximum rate, with control pins conveying the hardware DMA requests.

Since two data ports are used for pipelined operation, it is easy to design the 9518 into disk-based computer and telecommunications systems. The designer need only determine where in the data path through the system he wishes the enciphering to be performed. The 9518 is then inserted at this point. One port is configured to handle clear data and the other port to handle encrypted data, as explained.

The flexibility of this architecture has been enhanced by making each port interact with the system by means of the standard Z8000 bus protocol. Further convenience is accomplished by allowing the user to dynamically program the direction of data flow and to define which port is the clear-data and which the encrypted-data port. Internal safeguards have been included in the logic to ensure that reprogramming of the chip cannot cause clear and encrypted data to appear on the same port of the device.

It must be remembered that a pipelined architecture is not ideal for all systems. There are some applications where the user may wish to place the encoding device on a separate bus rather than in the middle of a data path. In that case, an interface for two ports is undesirable because it requires extra address decoding. Such a single-port requirement, usually found in systems designed for minimal cost rather than maximum performance, can be implemented with the 9518 by programming it to operate in its single-port mode, thus deactivating one of the two data ports. Data can still be read from and sent to the device while it is actively enciphering, as in the pipelined mode. However, there is some loss of overall performance, because data cannot be read from and sent to the device through the single port fast enough to keep it enciphering all the time. Encryption is so fast that it must occasionally halt to wait either for new data to be entered or for data already processed to be read out.

Slice that bit

Both the pipelined and the single-port mode accept commands from a microprocessor through one of the three ports. In some disk and telecommunications systems, however, the controlling computer may be built from bit-slice components.

In a bit-slice design, issuing commands to a peripheral device usually takes many instructions and tends to be slow. To facilitate use of the 9518 in bit-slice systems without significantly affecting system performance, a special bit-slice interface has been included. This interface lets the user control the 9518 by directly manipulating the voltage levels on certain pins, instead of by writing into an internal command register.

Since a bit-slice architecture is chosen to maximize performance, the designers of the 9518 decided to require that in a bit-slice system, the device must be used in the dual–data-port configuration. One port then handles clear data and one encrypted data, as in the pipelined mode. In other words, a bit-slice single-port configuration does not make sense in a bit-slice environment because of its reduced performance.

The dual-port configuration lets the internal enciphering processor work at full speed and, in addition, makes possible novel configuration possibilities. For example, the 9518 can be included within the data path of a bit-slice arithmetic and logic unit. The bit-slice control inputs on the chip can be driven directly from microcode memory and the status output lines can go directly to the microsequencer to control microcode branching. This design can have directly executable macroinstructions for encryption and decryption. □

High-current voltage regulator works with negative supplies

by Robert A. Pease
National Semiconductor Corp., Santa Clara, Calif.

Monolithic voltage regulators combine the voltage-stabilizing and power-protection circuitry of discrete component designs into a single package. As a result, current-limiting, voltage-limiting, and even thermal limiting features are built into the regulating function and therefore require no further consideration by the designer. Unfortunately, most high-power monolithic voltage regulators are intended for positive-supply voltages.

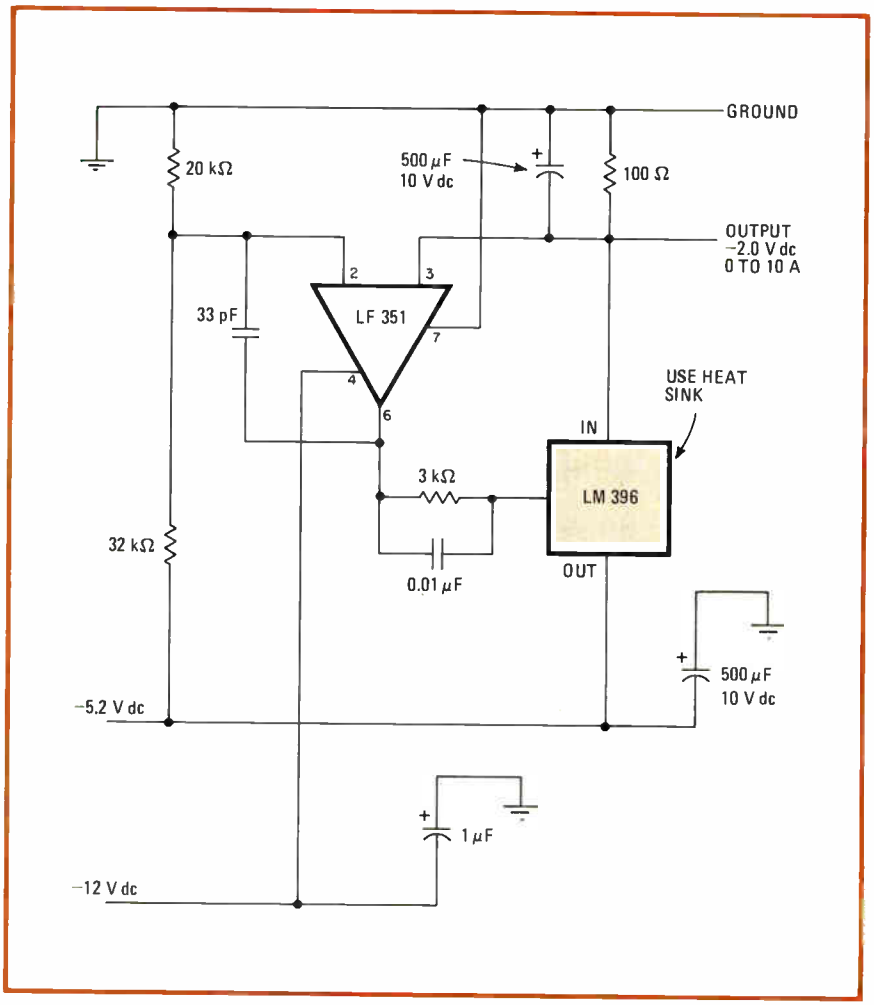
Currently, the only negative-voltage monolithic regulators that are available are those with 1.5 or 3 amperes of rated output current. The LM337 adjustable and LM345 fixed −5-volt regulators are two such devices. New high-current monolithic regulators, such as the LM338, rated at 5 A, and the LM396, rated at 10 A, are normally characterized as positive regulators. Yet they can also be used in applications calling for negative regulators, such as in an emitter-coupled-logic computer where several amperes at −2 V are often required.

The figure shows an LM396 that is controlled by an LF351 operational amplifier that holds the LM396's adjust pin at 1.25 V below the −5.2-V bus.

The accuracy of the output voltage depends on the −5.2-V supply, which is used as a reference. Short-circuit limiting to 15 A and thermal-limit protection to 170°C are provided by the LM396. Although the −12 V dc need not be closely regulated, it must be present or else the −2-V supply will fall toward −3 or −4 V, which is excessively negative.

Similarly, a positive regulator such as an LM338 or one or more LM396s have been used to regulate 5, 10, 20 A, or more of −5.2 V dc when a 9-V dc power and a −15-V dc bias supply are used. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $75 for each item published.



Both ways. An LM396 monolithic positive-voltage regulator can be used, as shown here, to regulate a 10-ampere negative supply. Feedback to the regulator chip is furnished by an LF351 operational amplifier. The LM396 regulator provides full short-circuit protection to 15 A, as well as temperature protection to 170°C.

Fewer parts resolve shaft encoder data

by Bill McClelland
Digicomp, Darien, Conn.

This circuit achieves the same resolution as the circuit proposed by Amthor [*Electronics*, Sept. 11, 1980, p. 139] but requires only one integrated circuit, instead of seven, and half the number of discrete components.

A standard shaft encoder has two ports, A and B, each generating a square wave as the shaft encoder is turned. The square wave from port A will either lead or follow port B's square wave by 90°, depending on the direction of the rotation of the encoder (a).

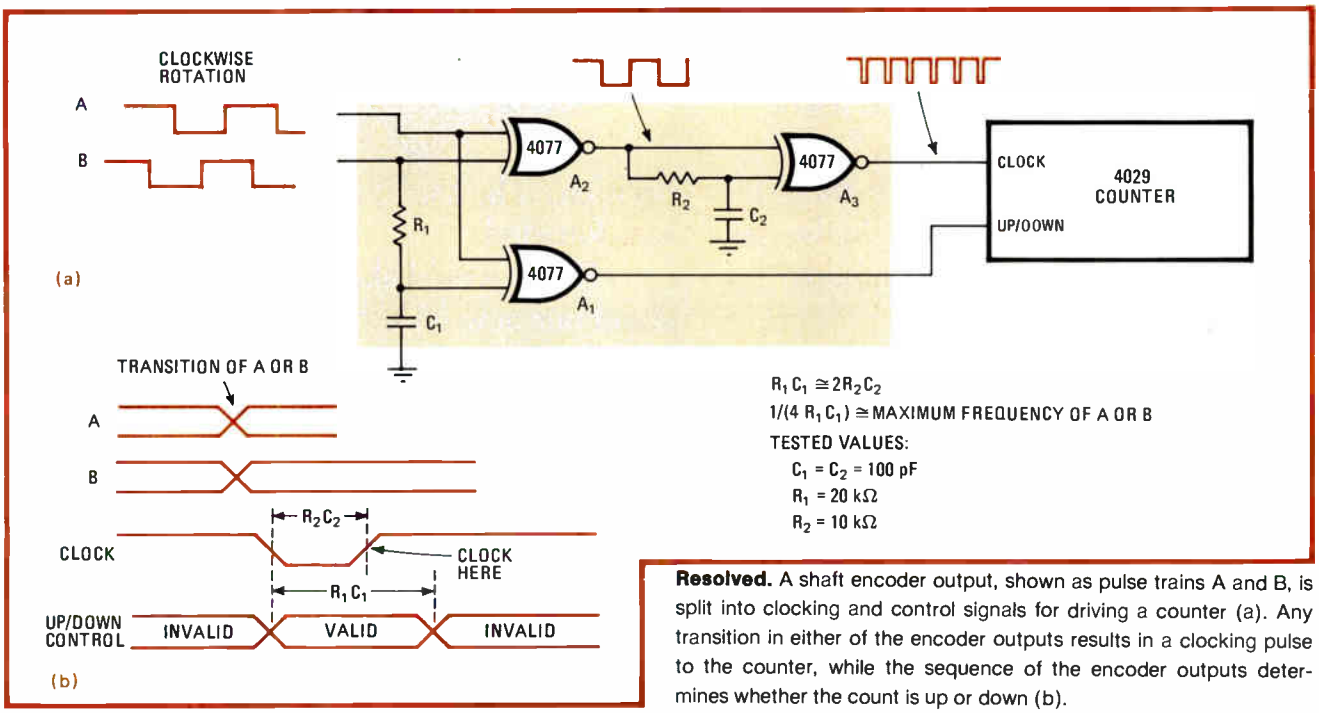
To get the maximum resolution out of the shaft encoder, every change of state for both A and B must be counted. Depending on the direction of rotation of the shaft encoder, the counter will count up or down. By exclusive-NOR-ing square waves A and B at gate A_2, a square wave that changes state whenever there is a change of state of either A or B can be obtained. The output of exclusive-NOR gate A_3 is high except when a change of state at gate A_2 occurs. Whenever the output of gate A_2 changes state, the two inputs of gate A_3 will be of opposite state for a time determined by R_2 and C_2, generating a short, low-going pulse. By using complementary-MOS exclusive-NOR gates, the pulse at the output of gate A_3 will have about the same duration for both the positive and negative transitions of gate A_2. The trailing edge of this pulse is used to clock the counter, allowing setup time for the up-down control (b).

The up-down control is generated by R_1, C_1, and gate A_1. R_1 and C_1 act as a latch, holding the value of B prior to a change of state of A or B during the clock pulse at gate A_3. Exclusive-NOR-ing the value of A just after a change of state in A or B, with the value of B set just prior to a change of state of A or B, achieves the proper up-down control.

The operation of gate 1 can be demonstrated as follows: square waves A and B are out of phase with each other by 90°. Adding −90° to B would change the phase shift to 0° or −180°, depending on the direction of rotation of the shaft encoder.

As a result, the output of exclusive-NOR gate A_1 would be high when A and B are in phase and low when A and B are 180° out of phase. Since the only concern is the output of gate A_1 when the counter is clocked, R_1 and C_1 give enough time lag to phase-shift B for the duration of the clock pulse at gate A_3. For this reason the time constant R_1C_1 is greater than R_2C_2.

The polarity of the up-down control may be inverted by swapping the A and B wires or by using the fourth exclusive-NOR gate in the 4077 integrated circuit as a selectable inverter-buffer. If the clock signal needs to be inverted for another type of counter, the entire 4077 exclusive-NOR–gate package can be changed to a 4070 exclusive-OR package. If standard C-MOS rise and fall times at the A and B inputs cannot be guaranteed, it becomes necessary to buffer the A and B inputs with a Schmitt trigger, such as a 74C914. □



Resolved. A shaft encoder output, shown as pulse trains A and B, is split into clocking and control signals for driving a counter (a). Any transition in either of the encoder outputs results in a clocking pulse to the counter, while the sequence of the encoder outputs determines whether the count is up or down (b).

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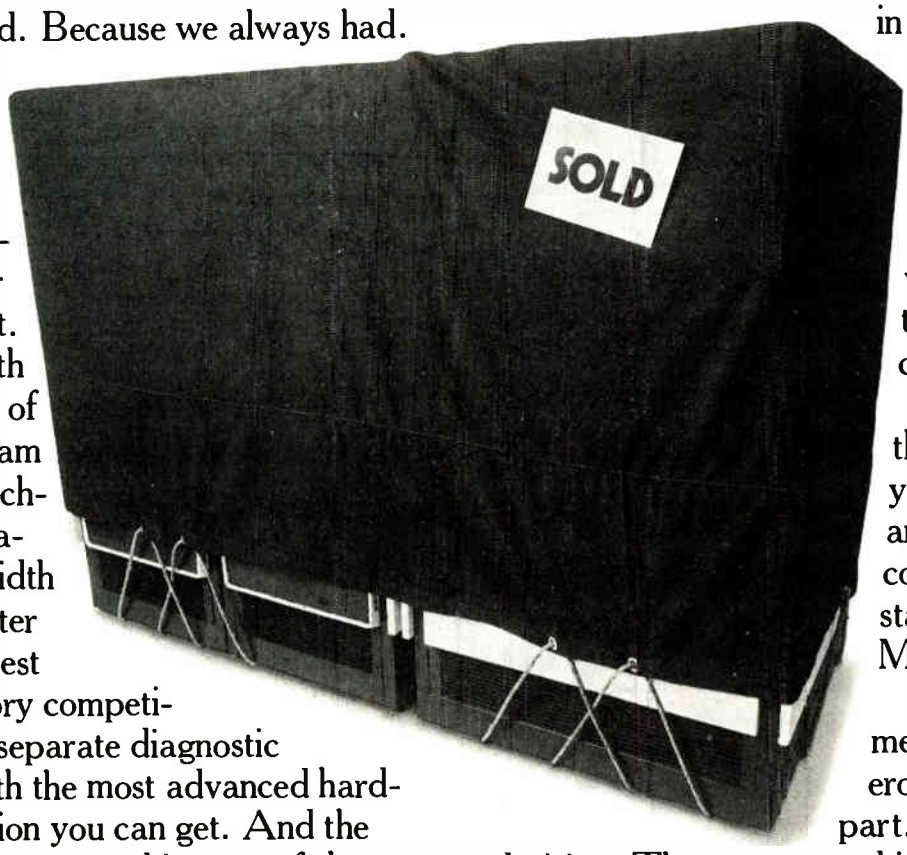

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Dual tones advance slides automatically

by J. A. Connelly and Douglas Martin
Georgia Institute of Technology, School of Electrical Engineering, Atlanta, Ga.

This circuit generates dual audio tones that are recorded on a tape so a slide projector will advance whenever both tones are present during playback. Two LM567 tone decoders are the heart of the circuit and the individual voltage-controlled–oscillator frequencies are set by R_1, C_1 and R_2, C_2.

For the circuit shown, $f_1 = 1/(R_1C_1) = 10$ kilohertz and $f_2 = 1/(R_2C_2) = 7.7$ kHz. The highest frequencies that the recorder can reliably reproduce were chosen to minimize possible annoyance to the listener. Two phase-locked–loop tone decoders prevent false triggering that would allow music or voices to be recorded with the tones.

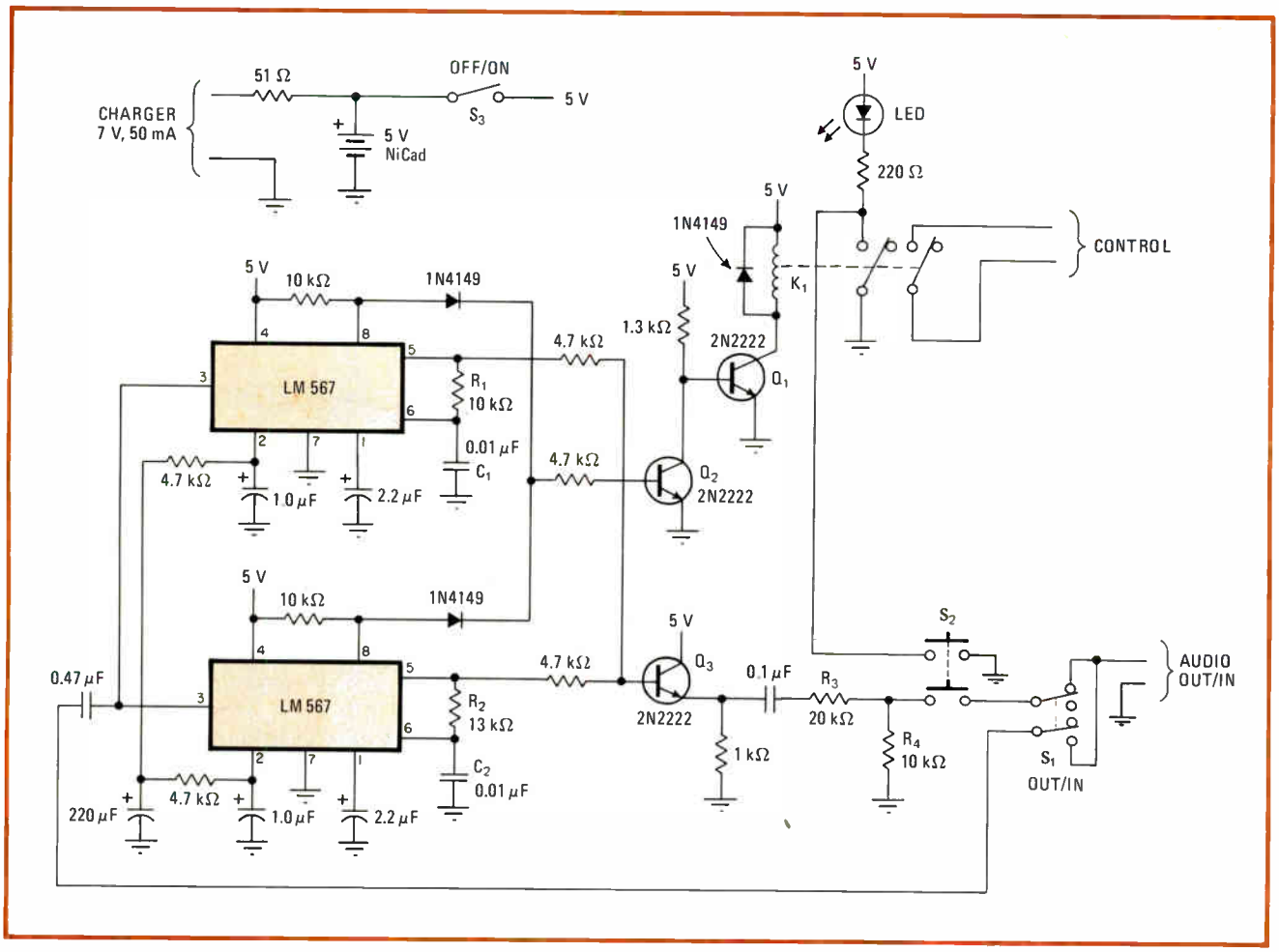
The VCO frequencies from pin 5 of both tone decoders are summed at the base of Q_3, which buffers the output tones. This prevents any recorder loading from changing the VCO frequencies. When the VCO frequency is present at the pin 3 inputs, the PLL locks and an internal transistor saturates, shorting pin 8, an open-collector output, to ground. The outputs at pin 8 of the two PLLs are diode-OR-ed, so that only when both VCO frequencies are present at the input does the transistor Q_2 switch off.

This action switches Q_1 on, also turning on relay K_1. One set of the contacts of K_1 are used to advance the projector. The other set of contacts serves to turn on a light-emitting diode that provides a visual indication of when the tone is received. This same LED is also connected with switch S_2 so that it indicates when the tones are being recorded onto the tape. This switch, which is used during recording, is pressed for about 1 second at each point on the tape at which it is desired to advance the slide projector.

Switch S_1 prevents feedback between the output and input tones. If both are connected to the recorder at the same time, the outputs at pin 8 will oscillate as the LM567s try to track their own VCO frequencies.

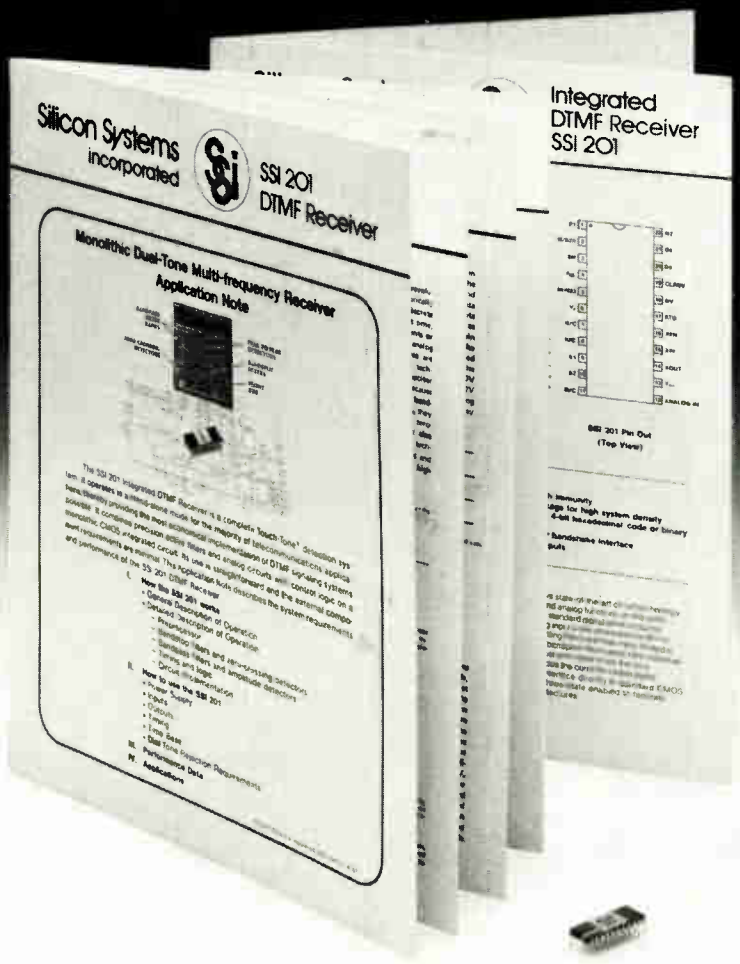
The tone-output–attenuating resistors, R_3 and R_4, should be chosen so that when the tones are recorded at normal levels for music and voice, their playback level is close to 200 millivolts peak to peak. This level will assure reliable phase lock by the PLLs.

The circuit draws a small standby current of 17 milliamperes and can therefore run off a battery. □



Double duty. Two tones are simultaneously recorded onto a cassette tape when switch S_2 is pressed. The LM567 tone decoders, which generate the tones, also decode them from the tape and trigger Q_2 to energize relay K_1, which in turn advances a slide projector.

THE STANDARD ONE-CHIP SOLUTION FOR DTMF RECEIVER APPLICATIONS



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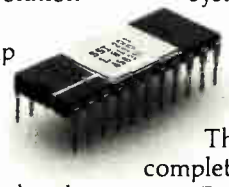

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Local network links personal computers in a multiuser, multifunction system

Apple II computers can share data and peripherals over a 240-kilobit-per-second network through a 16-wire cable

by Edward P. Stritter and Leonard J. Shustek, *Nestar Systems Inc., Palo Alto, Calif.*

☐ Personal computers are powerful enough for even ambitious user applications when they are integrated into local networks. By emphasizing a systems rather than a hardware approach, local computer networks like the Nestar Cluster/One model A can dramatically increase the individual user's productivity while accommodating the overall organization's constantly changing structure (Fig. 1).

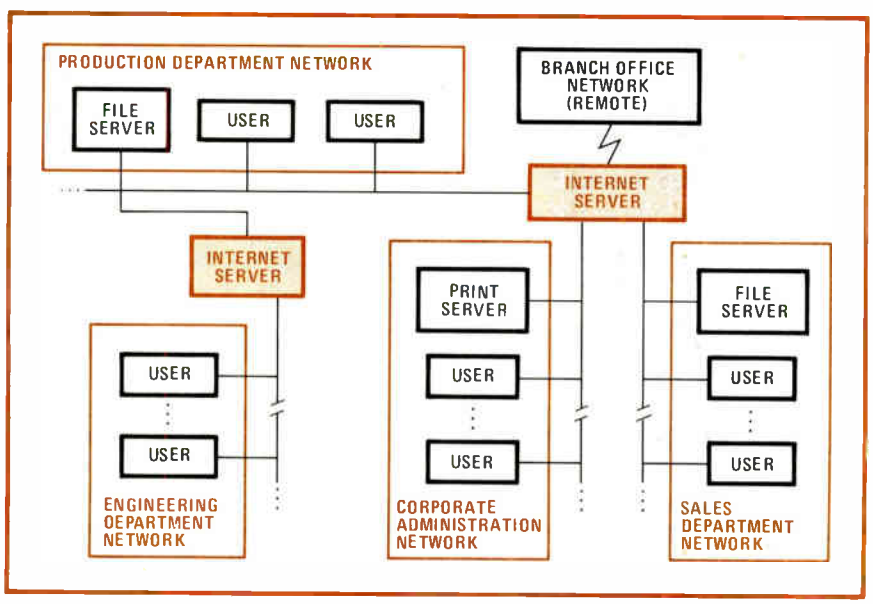
Designing local networks for personal computers requires a different set of goals and decisions from those involved in designing networks for larger computer systems. The fundamental goal in designing the Cluster/One network [*Electronics*, Jan. 31, 1980, p. 43] was to deliver a useful computation and communication tool within the cost constraints imposed by the pricing of today's personal computers. A personal computer is defined here as a readily available off-the-shelf desktop unit—currently an 8-bit microcomputer with 64 K bytes of memory, keyboard and display, and possibly a floppy disk—that costs between $1,000 and $2,000.

The hardware and software for a personal computer network must be designed to cost no more—in fact, preferably much less—than the computers themselves. In other words, the network interface should not be a dominant part of the total system cost.

These cost factors lead naturally to several clear-cut design choices and tradeoffs. For example, when a function may be implemented in hardware or software, maintaining cost compatibility with personal computers often implies opting for simple, programmable hardware, while assigning responsibility for most of the function to the software. Another decision influenced by such cost factors concerns network speed. Two issues are important here: a network performance level that can be supported at reasonable cost by a personal computer and the bandwidth requirements for the work typically done by personal computers on a network.

The speed chosen for Cluster/One is 240 kilobits per second—the fastest rate that could be supported by a software-driven network interface running on a host personal computer based on an 8-bit processor such as the 6502 in the Apple II, without large amounts of supporting hardware. This speed easily handles normal network transaction traffic generated by a collection of Apple II computers, which the first version of Cluster/One is designed to support.

The choice of a network medium—the cable—is also influenced by the basic cost goal. In this case, the cable chosen contains 16 parallel wires, either in a flat cable or packaged, twisted pairs. This type of cable requires only



1. Connections. This is one possible multiple local-network configuration using the Nestar Cluster/One system. Here two internet servers connect five local networks for different departments of a company.

COMPARING NESTAR CLUSTER/ONE MODEL A WITH ETHERNET

	Cluster/One	Ethernet
Cable	16-wire	coaxial
Topology	unconstrained	linear bus
Address size	8 bits	48 bits
Speed	240 kb/s	10 Mb/s
Carrier	separate line	presence of signal
Acknowledgment	acknowledged datagrams	separate acknowledgments
Multiple packets	without releasing cable	must release and reacquire

minimum-cost hardware drivers and permits eight times the network throughput of a bit-serial cable, since data is sent as 8 bits in parallel, or 1 byte at a time. Though all modern carrier-sense, multiple-access (CSMA) collision-detection local networks function similarly regardless of the medium chosen, the details of implementation can be quite different. The table above details the fundamental differences between Cluster/One and Ethernet, both CSMA networks with collision detection. The implementation differences result in different cost and performance characteristics.

Issues and answers

A number of other technological issues need be considered in specifying a local computer network installation. The following were incorporated into the detailed design goals of Cluster/One:

- Critical resources: there can be no critical devices that can impair either reliability or performance of the network. Thus, the model A has no central controllers, polling multiplexers, or any other components that cannot be powered off while the network is running.
- Station-to-station communication: direct station-to-station communication must be possible without the intervention of a central controller station.
- Passive connection: the network interconnection scheme must be passive so that connections can be made and broken without affecting network operation.
- Topological flexibility: the network configuration cannot be constrained to straight line, ring, or any other fixed configuration; on the model A, spurs can be added to the existing network anywhere they are needed, even while the system is running.
- Software installation: complete software should be provided with the network so that large amounts of programming are not needed to use the system.
- Software integration: network software must be transparent to existing local operating systems, so that no operating system redesign is needed.
- Software support: software support is needed for synchronizing shared resources, interactive operation, and electronic mail and other applications.
- Internetworking: internetting (networks of networks) configurations must be possible.
- Layered structure: the various components of the system should be independent and implemented in a layered fashion such that components can be changed without affecting others. For example, the network's transmission format could be changed from parallel to serial without affecting any but the two lowest layers.

The various protocols in network transmission are commonly defined in a number of layers. The first two, the physical layer and the data-link layer, are usually hidden from the user and user-level programs.

The physical layer protocol specifies the mechanical and electrical requirements and the procedures of the physical medium that connect the devices in the network. The medium could be a twisted pair of wires, a multiwire cable, a coaxial cable, a fiber-optic cable, or some other data path. The mechanical requirements refer to the connectors chosen for the system, and the electrical aspects specify the transmitting and receiving signals necessitated by the particular medium used. Also specified in the physical layer protocol is the set of procedures for exchanging data and controlling and timing the network-wide data flow.

A matter of definition

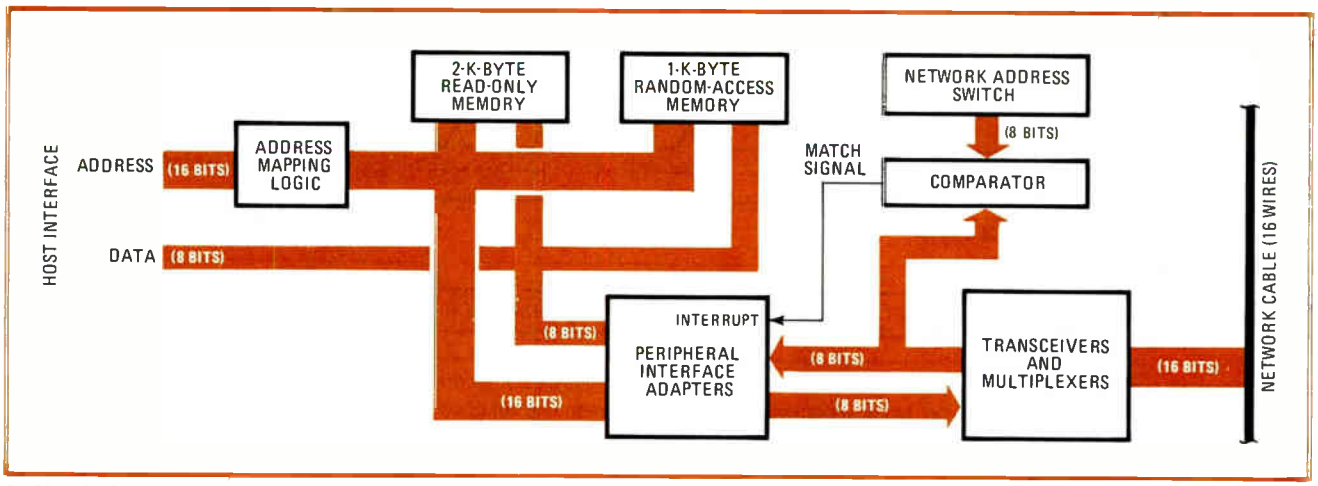
The data-link layer protocol defines how the information is formed into discrete data units—the rules for forming data packets, media-access scheduling, addressing, and error handling. Important functions of the data-link layer protocol are detecting and possibly correcting errors occurring in the physical layer, controlling the data flow to prevent overloading of the network, and providing network access and acknowledgment capabilities to ensure the correct transmission and receipt of the data units or packets. In the Nestar system, the physical and data-link layer protocols are implemented through a combination of hardware and firmware in read-only memory on the network interface board. The higher-level network layers are implemented with host software using the facilities provided by the two lower levels.

At the physical layer of the Cluster/One, 8 of the wires in the 16-wire cable carry bidirectional data, 4 convey handshake and control information, and 4 function as grounds (the cable shield, if any, may provide an additional ground). The interface to the cable (Fig. 2) is through transceiver-multiplexers that allow the data being put on the cable to be read back at the same time. This read-while-write facility makes it possible for collisions to be detected when more than one station attempts to gain access to the network cable at the same time, because the immediate read-back will be garbled if the data entering the network collides with transmissions already in transit on the cable.

Form follows function

The nonrestrictive topology of the Nestar network results from both the hardware and software design. The handshake and control-line receivers have hysteresis inputs to minimize noise. The data-line receivers do not, because the network is designed to tolerate a moderate amount of transient noise during transmission. When data is placed on the data lines, the software recognizes that it will take some time for the reflections from unterminated stubs on the network to die down and does not consider the data valid until then. Even multiple transitions of the handshake lines within specified time limits will not cause errors.

The error tolerance of the network is due, in part, to



2. Simple interface. The network interface board uses a small number of components to create a low-cost local network for personal computers. Most functions are stored in firmware on a 2-K read-only memory and executed by the host processor.

the parallel transmission of data. If the same bit rate were to be maintained on a serial network, then there would have to be much tighter control over the electrical characteristics of the cable because the bit-rate per wire would be eight times higher.

The interface logic contains hardware that recognizes its own station address in a data packet on the network. One of the control lines in the network cable indicates that a station address is on the data lines and triggers a comparator that notifies the interface processor when the address in the network matches that programmed into the address switch on the interface. This particular control line serves a dual purpose: it triggers the address comparator and also serves as the carrier signal indicating that a transmission is in progress. Stations wishing to transmit do so only when the carrier signal, as well as the data lines, are inactive.

Separate control lines

In Ethernet-like networks, the carrier signal is detected as the presence of data on the network cable; in the Nestar system, the carrier is implemented as a separate control line. This allows the carrier to remain asserted between data transmissions. Thus, other stations are kept off the network so that the receipt of packets can be acknowledged and multiple-packet two-way transmission can occur.

Two other control lines are used to synchronize byte transmission in a variation of the standard data-offered, data-accepted protocol. Transmission is thus asynchronous and can proceed at the maximum rate that the processors will accept.

Since the network interface should disturb the host operating system as little as possible, it is necessary to provide local read-only- and random-access-memory space for the network software. Although processor time can almost always be stolen from the host without undesirable side effects, memory cannot. Using RAM in addition to ROM allows modifications to and upgrading of the network interface software to be downloaded to affected sites through the network, without changing the system hardware or reprogramming ROMs. The RAM is typically not used for buffering packets, which are usually sent directly to host memory.

In the data-link control layer the Cluster/One uses a CSMA protocol. The carrier line is asserted whenever the cable is in use. Stations desiring to use the cable must check for presence of the carrier signal and can only access the cable when it appears to be idle. As in Ethernet this is a noncentralized access-control mechanism with the same priority for all stations.

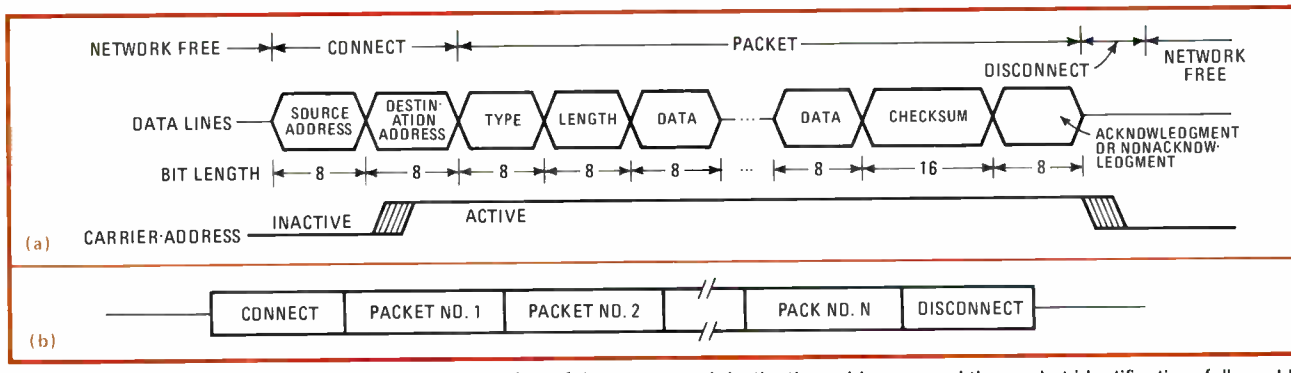
Collision coverage

It is possible that two or more stations will try to access the cable at the same time because of the nonzero transmission and detection time of a newly asserted carrier. Collisions are detected by software during the first several bytes of packet transfer. The colliding stations back off, jam the cable, and wait before retrying. Later collisions during transmission of the packet are unlikely because the carrier line is asserted. In order to speed up the data transmission, later collisions are not checked; but they will be detected by bad checksums at the end of the colliding packets. Both colliding packets will have to be retransmitted.

Stations can acquire the cable whenever the carrier lines and the data lines are inactive. Cable allocation occurs when a station puts its source address on the data lines. If other stations attempt to gain control of the cable at the same time, then at least one station will recognize an address collision because all source addresses are different. All stations that recognize a collision will jam the cable for a short time to guarantee that all participants recognize the collision.

When the cable has been allocated, the source station puts the destination address on the data lines, and after a suitable delay, the carrier line is activated. The destination station-address comparator will trigger the software in the destination interface, causing it to start receiving a packet, which consists of four fields: type, length, data and checksum (Fig. 3a).

Another important advantage of parallel transmission comes into play at this point. Since the byte-transfer rate is slow compared with the propagation rate in the cable, it is possible to reverse the direction of the data flow with almost no time penalty. This allows the positive or



3. Special delivery. A single-packet transmission consists of the source and destination addresses and the packet identification, followed by data, checksum, and acknowledgment (a). Multiple packets can be sent between one set of connect and disconnect operations (b).

negative acknowledgment of successful transmission to be sent back to the sender with no significant delay.

If the packet needs to be retransmitted, that, too, happens immediately. This almost instantaneous acknowledgment considerably simplifies the higher levels of the transmission protocol, since it ensures that a packet that has been successfully transmitted has also been successfully received. Packets are never received out of order, and transmit-data buffers can thus be freed as soon as the packet is sent. Also, no extra network overhead is generated by sending separate acknowledgment messages.

In the simplest case, the cable is released at this point—a complete packet having been sent—by removing the carrier signal. Other stations detect that the network is idle and initiate transfers.

A variety of errors can be detected by the data-link protocol, including timeout errors (handshake or control-line changes that do not occur within a specified time), checksum errors, collisions caused by interference with other stations, packet-length errors, and station-address errors. Those errors may be transient and cause the transmission to be retried several times; others are returned to the higher levels of the protocol routines.

Holding a conversation

The next level of protocol in the Cluster/One system is the message-transport layer, which manages the handling of messages and conversations among stations. The simplest message on the network is a one-way, single-packet communication often called a datagram. As discussed above, however, the datagram in this system is an acknowledged datagram in contrast to Ethernet datagrams, which must be acknowledged by a separate acknowledgment message.

Useful communication between stations often requires a conversation consisting of several datagrams flowing in both directions. This virtual-circuit type of connection can be accomplished without interruption over relatively long time spans by cooperating processes sending datagrams back and forth to each other.

For short-term conversations, network overhead can be avoided by permitting multiple-packet two-way physical connections on the network. A multiple-packet connection (shown in Fig. 3b) allows several packets to be sent between a pair of stations without having to free and reallocate the cable between packet transmissions. This results in a modest performance increase for an operation that requires the exchange of several small data packets. Most importantly, it allows the construction of indivisible operations analogous to a standard read-modify-write memory cycle that are necessary for synchronization of multiple independent processes. Thus, semaphores and test/set flags can be implemented within the network in an efficient manner.

Another way to view the multiple-packet connection is as a short-duration nonmultiplexed virtual circuit established between two stations. Of course, since the network is allocated for the duration of the circuit, care must be taken not to let long connections monopolize the network. Thus, the various system timeouts are set by the user to prevent accidental hogging.

Long-duration, time-multiplexed, virtual circuits must be implemented in a higher-level protocol. For instance, file transfers or program loads are accomplished through a sequence of individual packet transmissions.

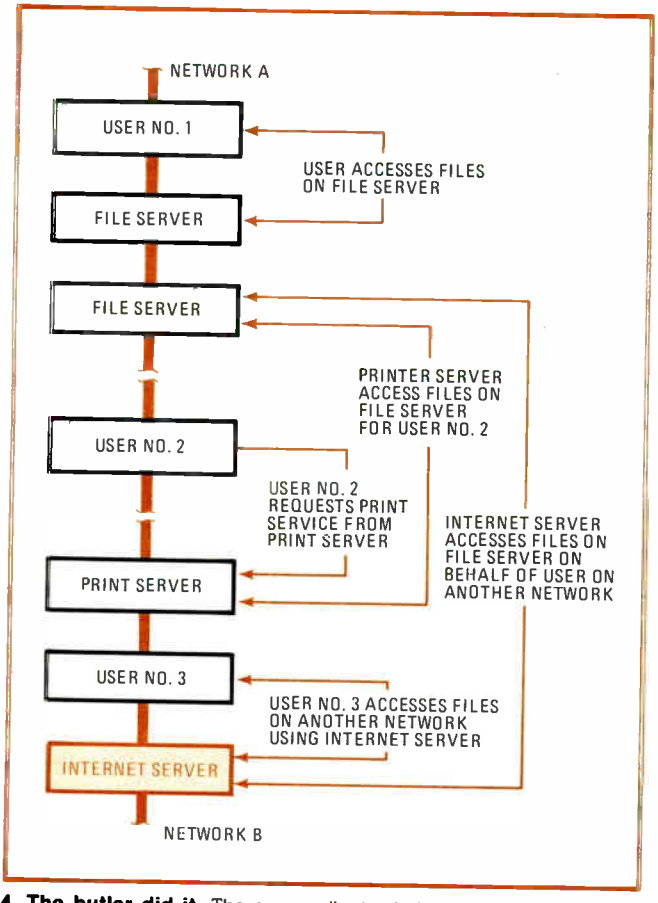
The ordinary user is not concerned with the three lowest-level protocols—the physical layer, the data-link layer, and the message-transport layer. Likewise, the network-interface software is automatically merged into the operating system of the personal computer when the station is started up. This software includes input/output drivers that allow a station to access disk storage or use printers that are attached to other stations exactly as it would control a locally attached peripheral.

Network transparency

This concept of virtual I/O makes the network transparent to most users and programs; they need not change at all the way they think about the file system or I/O. Most existing software for personal computers runs on the network without modification, and the modifications necessary to adapt existing single-user software for simultaneous multiple-user applications in a distributed environment are easy to make.

Some stations on the network are designed to serve other stations, providing additional resources for all the personal computers on the network. An example is the Nestar File Server, which supplies extensive shared disk-storage, sophisticated file-system operations, and a real-time clock for the other stations. The file server also implements file-protection and controlled file-sharing mechanisms for its client stations that share data.

At any given time, each file server may maintain



4. The butler did it. The server-client relationship among network stations is very flexible but can become complex. Some servers need other servers to carry out requested services for their clients. Server requests can cross network boundaries through network servers.

many virtual circuits to processes running in other stations that may also be on other networks (Fig. 4). One type of circuit that is always available is the command channel through which a station can send text messages with file-server requests.

Networks free computer hardware from having to be located where specific computations take place. The Cluster/One system supports any configuration within a limit of 1,000 feet of network cable. The stations on the network can therefore be located where needed. Any network station can become a server station merely by running a program that listens to the network for requests for resources or devices available to it. There may be, for instance, multiple file-servers (one for each business department) and printer servers wherever they are most convenient—for example, on each floor of a building.

Staying flexible

Another kind of flexibility results from the autostart facility of the network. The system can be configured so that specific stations, when turned on, automatically download specific programs to themselves or other stations from a network file-server. This action makes possible such facilities as no-operator server stations, turnkey applications, and secure, publicly available stations.

The perceived performance of a network-based system depends on many factors, including transmission bandwidth, the number of stations, the interaction patterns, and the power of the individual stations. In systems where the stations are powerful and have adequate local resources, the network is used relatively infrequently and seldom appears to be a bottleneck regardless of the number of stations. In systems where the stations depend more heavily on the various servers because of a lack of local resources—if, for example, they have no local disk storage—the network is more heavily used and performance degrades more quickly as the number of stations that require shared services increases.

Making a match

The network described here is matched to the various speeds of the personal computers that make up its user and server stations. In most configurations, the network and file server respond more quickly to I/O requests than would a locally attached floppy-disk drive, which is the usual disk peripheral for these computers.

When the file server is actively responding to virtual-disk requests, the overall system time spent to satisfy each request is about equally divided into three components: transmission time over the network, disk-seek and transfer time by the file server, and processing time by the server and user stations.

Local computer networks may be viewed from a number of perspectives. From the personal computer user's viewpoint, the Cluster/One should necessitate little change in work habits. The system has been designed to be easy to learn and the software aimed toward enhancing productivity through its combined computing and communication capabilities.

A critical element in a productive organizational structure is communication. However, isolated computer technology will not improve communication. From an organizational point of view, local computer networks provide a new style of computing: communication enhanced by flexible, personalized computing power. And if the networks can change dynamically to match an organization's changing structure, they will promote the upscaling of computing power as the organization grows.

Applying the network

The Cluster/One system has been implemented in a wide variety of applications. These include general office-automation environments, engineering and software-development sites, educational and entertainment uses, and special turnkey applications, such as travel-agency and real-estate systems.

To support this variety of uses, Nestar provides some general-purpose distributed-computing program products. For example, the Messenger electronic mail program is a full-function intra-office electronic mail system whose facilities include commands to send, receive, answer, forward, file, review, and print mail and memos.

Other applications, such as a teleconferencing program that permits multiple simultaneous conversations to be carried on between network stations and an installation-wide data-base (with user-specific views of the data), are in use or in development at Nestar and at customer locations. □

Nodes sound off to control access to local network

Novel scheme prevents collisions while guaranteeing minimum throughput

by Dan Scavezze, *Motorola Inc., Communications Group, Schaumburg, Ill.*

☐ Local networks like Ethernet, Z-Net, and Net/One are rushing onto the scene to hook up diverse data-processing gear in an office or other local site. These networks all employ a shared-channel topology without a central controller, so that the terminals, or nodes, can communicate directly. And in general, to organize their communications, they also adopt the simple but delay-prone contention-arbitration procedure. This approach, in effect a trial-and-error scheme, requires each node to access the network at random and to resolve any collisions between its messages and those of other users by simply trying again later until it is successful.

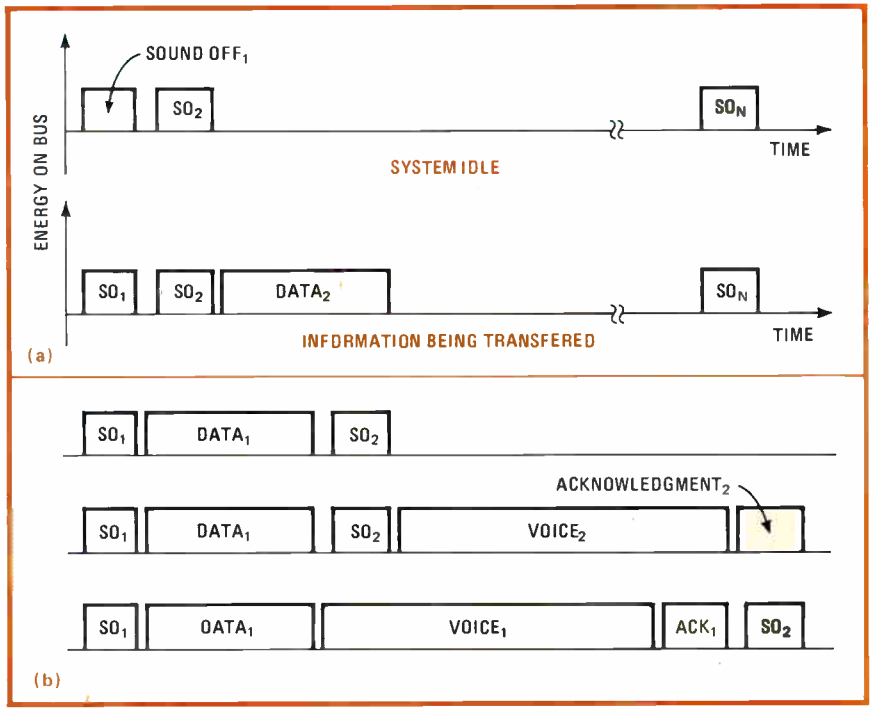
Collision-free operation, however, can be achieved by a recently devised method known as a sound-off procedure. This distributed control scheme guarantees that throughput will never fall below a certain rate and, conversely that delays will never exceed a certain maximum—benefits that can be significant in certain high-security data networks where messages must go through quickly. Furthermore, unlike all the other schemes for distributed control of a common channel, this method needs no central synchronization of the network.

Such a distributed control approach, called the sound-off control scheme, has been implemented at Motorola. Here, a microprocessor, the Signetics 8X300, is dedicated to handling the communications protocol. A prototype system constructed for test purposes runs at a channel bit rate of 8 megabits/second and allows 70 network nodes simultaneously to each generate 64 kilobits/second of voice and 8 kb/s of data.

Sound-off control

With sound-off control, the channel is never truly idle, even when all user nodes have nothing to transmit. When nominally idle, each node is actually continually sounding off in sequence by sending a packet that identifies it as the current user of the channel (Fig. 1a). All other nodes hear these sound-off packets, and synchronize to them. Thus, each node finds its place in the sequence and knows when it is time to seize the channel.

If a user node has information (either data or an acknowledgment) to transmit, it sends the information



1. Sounds of silence. In the sound-off scheme for distributed control of a local network each node sends a packet to the channel even if it has no data to transmit (a). When voice or data is transmitted, these packets follow the sound-off packet (b).

How long does a node wait?

In the sound-off scheme devised for distributed control of local networks, there are three times when the channel is idle. The first is the interpacket, intraslot time. This idle interval is purposely created by a transmitting node between packets in its own slot. It allows receiving nodes to separate the packets. The second, longer period—the interpacket, interslot time—is necessary for a node (say, $i+1$) to determine that the previous node in the sound-off sequence has finished its slot. If node $i+1$ is working, it will transmit a sound-off packet after node i is finished.

If node $i+1$ has failed and thus is silent, the third type of idle interval, the failed-node interpacket time, will occur. In this situation, if the channel is idle longer than the maximum value of the interpacket, interslot time, it is apparent that a node has failed. Therefore, the minimum waiting time necessary to determine node failure is the maximum value of the interpacket, interslot time.

To compute the minimum wait, consider the perfect observer, who knows exactly when user i's packet ends. But an actual observer's node in the system detects the end of the packet by means of a hardware circuit. Therefore an observer node cannot expect user $i+1$ to begin to react until TE seconds after it detects the end of the packet, TE being the maximum difference in the time for any two nodes to detect the end of a packet.

Some propagation delay also exists on the channel. Consequently, it may be $TE+T$ seconds before user $i+1$ begins to react, where T is the maximum propagation delay in the system. If it takes TR seconds for node $i+1$ to react and begin to send a packet and T seconds of propagation delay for this packet to arrive at the observer node, it is $2T+TE+TR$ seconds before the observer can even begin to sense the packet. Since a real hardware circuit is used to detect the beginning of the packet, TB, an observer must wait $2T+TE+TR+TB$ seconds before determining that another node has failed.

In the prototype sound-off system described in the main text, these parameters (in microseconds) are: $T = 2.0$, $TE = 0.5$, $TR = 10.0$, and $TB = 0.5$. Therefore the minimum waiting time, TW, is 15 μs. In the prototype, actual waiting time was 18 μs. It is important to note, however, that decreasing the length of TW has no effect on the efficiency of a normal system, and it yields only a slight increase in the efficiency of a system with failed nodes.

immediately after its sound-off packet, up to a predefined time limit. All other nodes monitor the channel and can determine when it has finished occupying the channel, so that the following user will proceed in turn.

If all users have information to send, each node will be able to transmit at the minimum guaranteed rate. However, as nodes become idle and send only the sound-off packets, each node will get its turn to transmit more frequently. In that way, the scheme dynamically allocates channel capacity.

When a user node fails, thereby becoming completely silent, the other users detect the failure by sensing that the channel has been idle longer than the prescribed waiting time (see "How long does a node wait?" above). When that happens, all users know who is next to transmit in the sequence and update their expected-user counters. If all the timers were identical, this process could continue indefinitely, but in practice, they are not and will begin to drift out of synchronization. The system will be resynchronized, however, by the next sound-off packet from a functioning node. In any event, the system can survive any number of node failures.

Because they contain source-address information that can be omitted from the following packets, the sound-off packets do not contribute heavily to the data-communications overhead of a busy system. Furthermore, when the system is not busy, the channel capacity is unneeded. The presence of the sound-off packets also gives additional maintenance information, indicating that a node is at least partly functional.

New users can be added to a running system in a two-step process. First, the memory at each user site is changed to indicate the new, as yet nonexistent users. This step will create out-of-sequence error messages that can be ignored during the system changeover. Secondly, the new users are added to the running system and any error messages again become meaningful.

In the sound-off system, each node gets a turn to transmit on what is known as a slot on the bus. This slot varies in length. Clearly, the shortest slot contains only a sound-off packet. On the other hand, the longest slot contains one sound-off packet, one voice packet, one data packet, and one acknowledgment packet (Fig. 1b). A typical packet consists of five fields, some of which have a variable or zero length, depending on the packet type.

Packet fields

The first packet field is known as the start field. It consists of 2 bytes containing 15 1s and a final 0 (the start bit). The control code field is next. It has 1 byte that contains the code for the packet type. The control-code cyclic-redundancy-check (CRC) field is third. It has 2 bytes of error-checking procedure computed on the control code. Fourth is the variable-length address and information (A/I) field. Finally, the packet has a closing CRC field containing 2 bytes of error checking computed on the address/information field. This field is not used in voice packets, since retransmission of a voice packet is not allowed in the system.

The contents of the address/information field must be interpreted with respect to the packet type. Therefore correct reception of the control code is vital. That is why a separate CRC check is included for the control code.

In order to understand the properties of the A/I field, its addressing structure must be explained. That is readily done, since in the sound-off scheme each node has two 7-bit addresses to which it will respond—a unique address and a group address. All addresses, unique or group, must be assigned from what amounts to a 128-address spectrum. Note that in a sound-off packet the A/I field contains but 1 byte, the sound-off address.

In a data packet, the beginning of the A/I field is used for a destination address, with the remainder conveying

data. The address subfield contains 1 byte per destination address, the most significant bit of which is zero unless another address byte follows.

The information subfield, too, varies in length. It is a maximum of 127 bytes long minus the length of the address field. This restriction arises from the use of 127-byte buffer memories to transfer the packet between the channel controller and the node processor. The maximum length of the data subfield for a node that can also generate voice packets is 17 bytes minus the length of the address field. This restriction is somewhat arbitrary, but the amount of data that can be sent suffices for typical sound-off network applications. It guarantees a minimum data throughput of 8 kb/s for singly addressed data transmission.

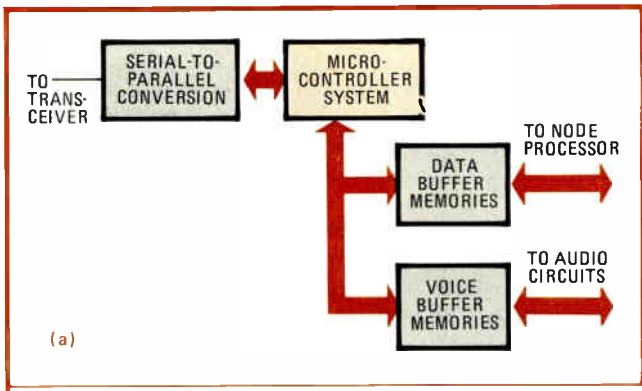
The acknowledgment packet, the last in a transmission, can be viewed as a special case of the data packet. It contains a 1-byte source address in the information field. Since that allows a multibyte address field, a node can acknowledge many other nodes in one packet.

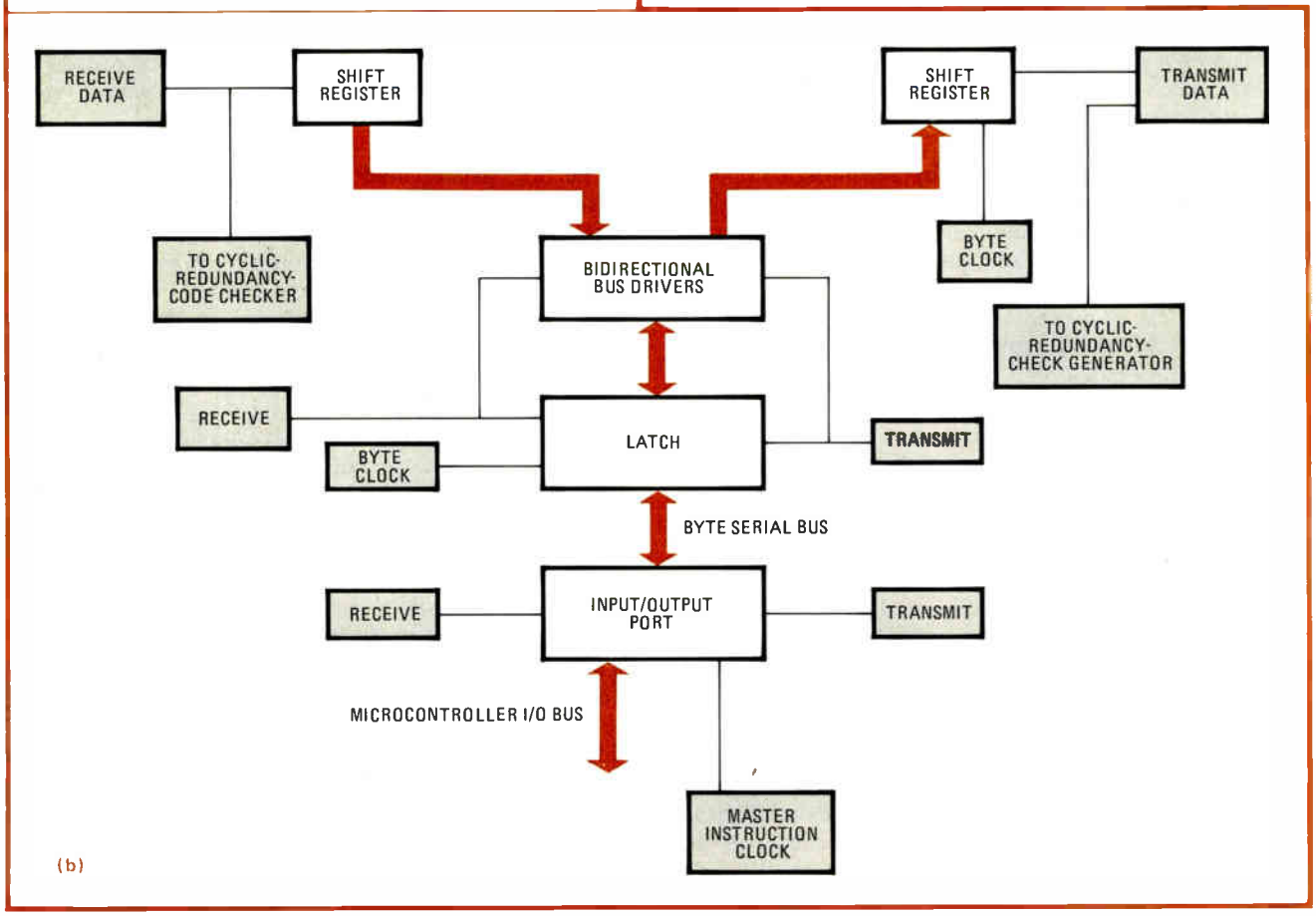
If voice information is to be transmitted on the sound-off network, the packet structure is somewhat different. For example, in a voice packet the length of the A/I field is 128 bytes, and the content is 128 samples of digitized voice. Furthermore, no destination address is included. Each node must decide whether or not to accept the voice packet based on the source of the voice signal only.

System design

The design of sound-off equipment for a network's data-communication nodes is divided into three sections—the transceiver, the channel controller, and the node processor. The transceiver is connected to the local network coaxial cable. At the other end, it is connected to the channel controller, which is connected in turn to the node processor.

The function of the transceiver is to convert between the TTL-level, nonreturn-to-zero–coded data and control signals used by the channel controller and the Manchester-coded, level-shifted data stream used on the network's coaxial cable. The transceiver itself is built with TTL integrated circuits and discrete components and has





2. Controller architecture. The channel control architecture is straightforward. All information flows through the microprocessor except when speed is critial (a). An exploded view of the serial-to-parallel conversion block shows the network data flow (b).

an extremely straightforward design.

The function of the channel controller is to control the communication channel based on the condition of the other nodes in the system. It has four types of tasks to perform. They are serial-parallel conversion, error-code generation and error detection, formatting and unformatting of packets, and manipulation of control signals to the transceiver and the node processor. All these tasks must be performed in conjunction with the timing constraints imposed by the sound-off scheme.

The channel controller also contains the network's voice circuitry. Although this function is not really a channel-control function, it is easily performed because of the ready availability of high-speed circuitry necessary to form and unform the voice packets. The channel controller's circuitry is implemented with TTL and an 8X300 bipolar microprocesser.

The node processor's function is to control voice or data-communications equipment at the node. In the prototype system, the processor was used to provide the human interface. As such, it drove indicator light-emitting diodes and switches. It also interfaced with the node's data terminal.

Controller hardware

The block diagram of the controller shows the basic data flow of the system as represented by the microcontroller's input/output bus (Fig. 2a). Data flows through the microcontroller to minimize external hardware and is routed around it only when that is demanded by speed considerations. All data is transferred between the channel controller and the transceiver using a 1-byte first-in, first-out arrangement and between the channel controller and the node processor using shared memory.

The 8X300 microcontroller was selected for the channel controller processor. This bipolar microprocessor is an 8-bit unit with an instruction set oriented more toward control than computing. Only eight instructions are available, but they are powerful for data movement and control.

Each 8X300 instruction takes only one clock cycle (250 nanoseconds) to execute. As a result, a byte can be read in from an I/O port of the system (such as the transceiver FIFO latch), operated on, and written to another port (such as the data buffer memory) in 250 ns.

The transfer of information between the channel controller and the transceiver can be explained using an expanded diagram of the serial-to-parallel conversion block (Fig. 2b). As the data stream arrives on the channel, a bit clock is recovered by the transceiver and divided to produce a synchronized byte clock. This type clock, in turn, is used to write each byte into the latch. One half-byte time later (if there is no clock skew), the microprocessor reads the latch using its master instruction clock. With the 8X300 controller employed in this system, all instructions are executed in one clock cycle. Here one byte time corresponds to four master-clock cycles, or four instructions.

This alternative read and write access to the latch can be thought of as a first-in, first-out stack of length 1. This length is sufficient to account for clock skew for the longest packet, which is 134 bytes.

For information integrity, a cyclic redundancy code is added to each packet as an error check, as indicated earlier. Because of speed limitations on the code-generating circuitry, the code is generated and checked outside the microcontroller in a separate IC. The node processor is not notified that a packet has arrived unless the CRC check is passed for the packet.

Data and voice buffers

Both data and voice buffers are needed in the channel controller. In the data buffer memory circuit, the memory address latch is needed to hold the address sent by the 8X300 because the I/O bus is a time-multiplexed data and address bus (Fig. 3a). Control pins tell the I/O chips—in this case, the address latch—whether the information in the bus is address or data. The memory data latches are needed to permit the use of slower, cheaper memories for the data buffers. Without the latches, memories compatible with the 8X300 bus speed (65-ns access time) are required.

Separate transmitter and receiver buffers are provided to transfer data in mailbox fashion. For example, to transmit a packet, the node processor writes into the transmitter buffer (the mailbox) and sets a flag to tell the microcontroller to send the packet. After the packet is sent, the microcontroller clears the flag to tell the node processor the buffer is empty and available for reuse.

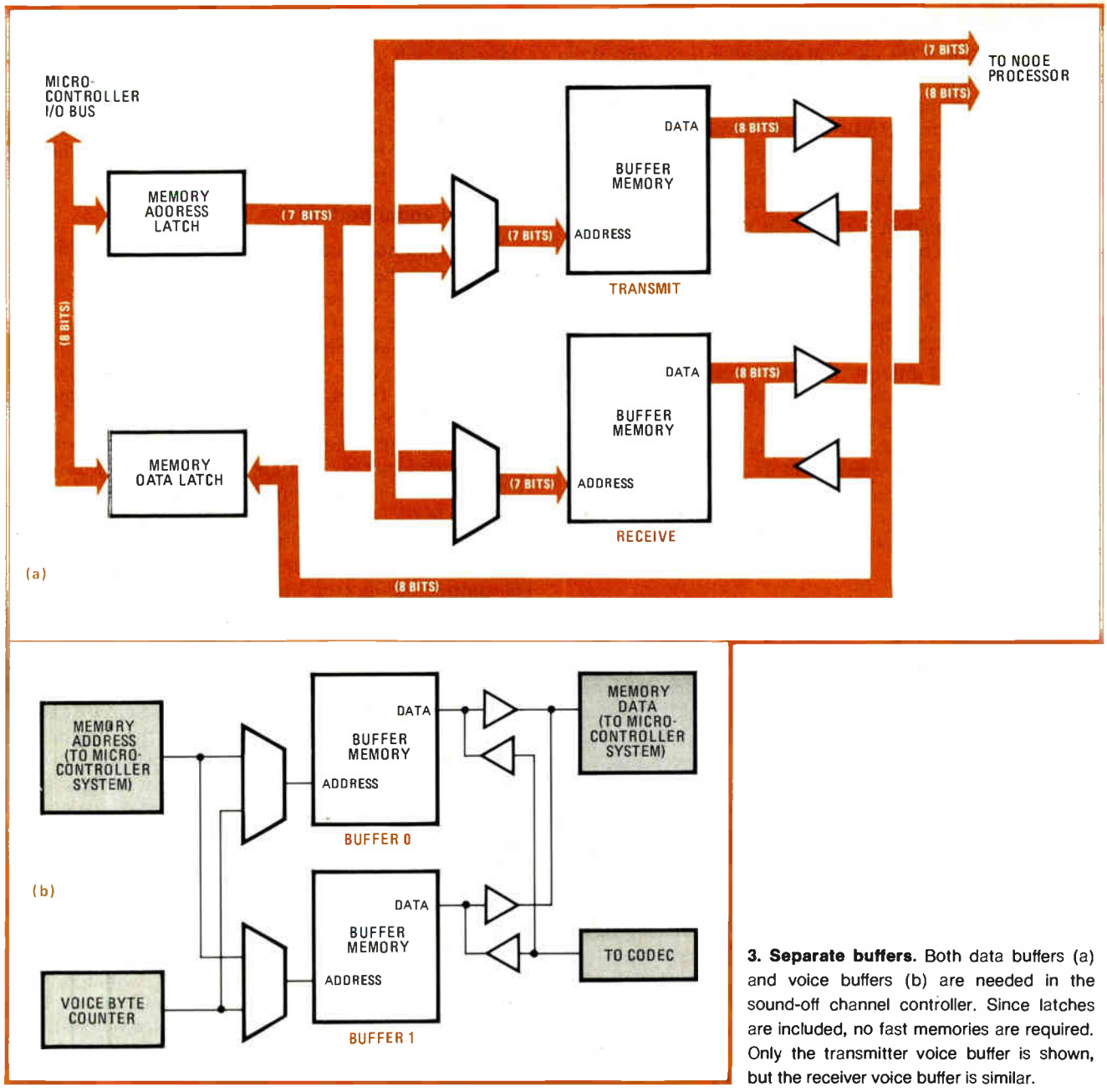
The transmitter voice buffer memory and receiver voice buffer are similar (Fig. 3b). These circuits resemble the data buffer circuit, except that the remote (non-microcontroller) buses are controlled by dedicated hardware rather than by a processor. The address bus is driven by a modulus-128 voice byte counter that accesses the buffers at a sampling rate of 8 kilohertz. The data bus is directly connected to codec chips, which convert the analog voice waveform to its digitized voice representation and vice versa. Standard pulse-code-modulation devices are used.

To allow continuous transmission of voice, the transmitter and receiver voice buffers are actually double buffers. Thus, while buffer 0 is being loaded at the 8-kHz rate, buffer 1 is being unloaded by the sending of a voice packet. Then a hardware switch is made and the buffers' roles are reversed.

Interrupt circuit

The 8X300 does not offer a hardware interrupt, but there is one case that requires interrupt operation. As the circuit is designed, only four instructions are available per byte time during packet reception. Since the processor is kept busy with data handling, there is really no time to poll a status pin to determine if a packet has ended. An added interrupt circuit is therefore enabled by the arriving packet to generate a system-reset signal after four instruction-execution times unless cleared by the arrival of a byte from the channel. As a result, a reset signal is generated four cycles after the last byte of the packet is read. The software then determines if a power-fail reset or an interrupt has occurred. Four cycles is long enough to guarantee that the program is exited in a known state, regardless of clock skew.

The relation between the system's performance



3. Separate buffers. Both data buffers (a) and voice buffers (b) are needed in the sound-off channel controller. Since latches are included, no fast memories are required. Only the transmitter voice buffer is shown, but the receiver voice buffer is similar.

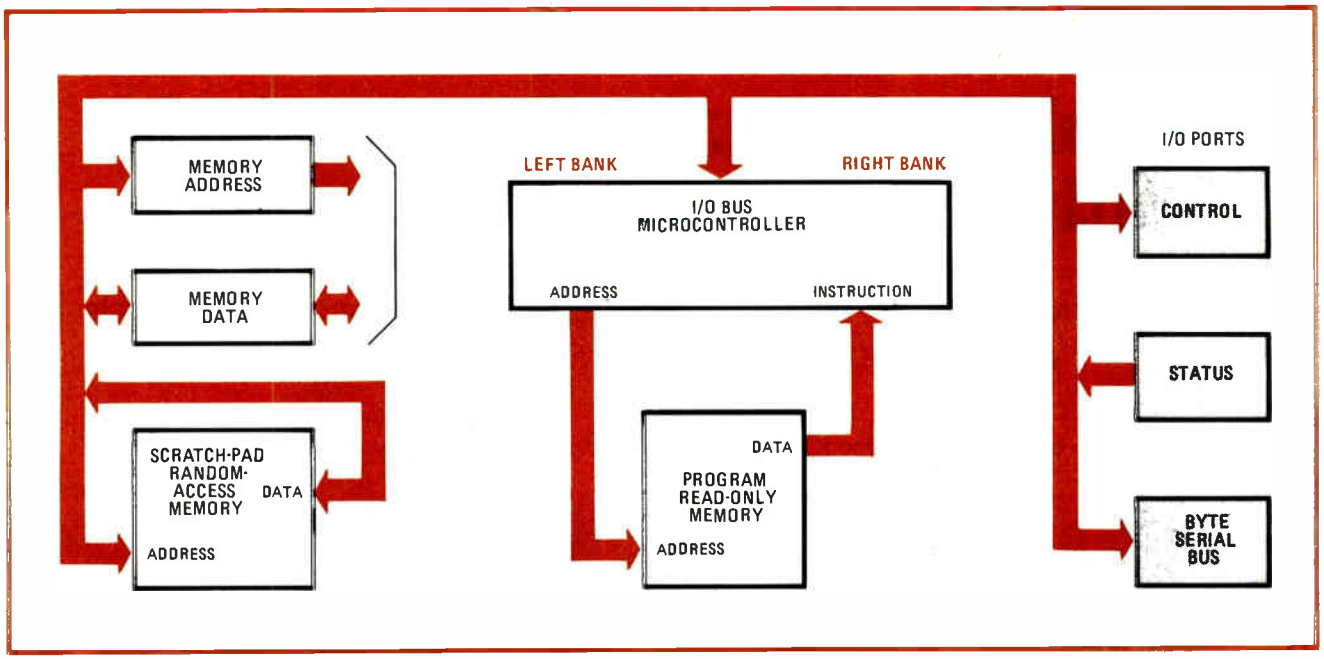
parameters and the software structure is a close one. For example, the length of time required by software routines to clean up after packets sets the minimum limit on the interpacket time, and the system bit rate sets the amount of time available for the software to keep in step with an arriving packet—1 microsecond per byte. This last requirement dictates the use of a fast processor.

A diagram of the microcontroller system is shown in Fig. 4. To explain the software, it is sufficient to view each of the external devices (connected to the microcontroller as in Fig. 2a) as an I/O port, even though some ports have different requirements—for example, two writes to the data buffer memories must not occur in consecutive instructions. This restriction arises because the data has to be left to incubate in the memory data latches for at least two instruction-execution times in order to be written into these slower-access memories.

The 8-bit I/O bus is arranged into right and left banks. The bus contents (data or address) are determined by the state of control lines. One control signal takes care of selecting either the left or the right bank. This signal is used as a ninth address bit to allow direct addressing of 512 locations—256 on each bank. The address and instruction buses are used only to fetch instructions from read-only memory.

Program flow

The program flow, or sequence of events, is synchronized to the channel data stream except during idle periods, at which times it is synchronized to the programs in the other nodes. That means that the program acquires and maintains synchronism with the data stream—four instructions per byte—when there is data on the channel. During idle periods, program synchronism is maintained



4. Lots of parts. The sound-off controller is an 8X300 8-bit microprocessor. Though only eight instructions are available, they are geared to data movement and control. Each instruction takes only 250 nanoseconds, which is more than adequate for local networks.

by timing signals only.

In order to implement the time-out system, the programs synchronize (if there was no channel propagation delay and all clocks were of identical frequency) at exactly the same moment in all the nodes in the system. This synchronization requires instruction counting and the insertion of stall instructions to ensure that the execution time for each program and each program branch is identical. Thus the channel-control program is a fairly rigid sequencer.

On a power-up command, the hardware generates a reset signal and the microcontroller enters the reset routine. It determines that the signal is a power-up reset when it finds the power-fail flag set. Next, it proceeds to initialize memory and also clears the power-fail flag. The program then monitors the channel long enough to hear sound-off packets from every node in the system. If the controller hears a sound-off packet, it becomes synchronized to and joins the existing sound-off structure. If not, the channel controller enters the sound-off scheme as if node zero had just finished transmitting. It then initiates the sound-off structure by sending a sound-off packet at the appropriate time.

Transmitting and receiving routines

After transmitting a sound-off packet, the controller checks the data, voice, and acknowledgment flags to see if it should transmit any of these packets. If so, the appropriate transmission routines are entered. These routines generate the packets by stepping through a rigid script that requires few decisions. For proper network operation, the controller must return to the time and monitor state in synchronism with the other node controllers, whether or not any or all of the packet handlers are entered. Therefore stall instructions must be inserted at the beginning and end of each transmission routine.

If a packet arrives while the controller is monitoring the channel, the controller jumps to the common-reception routine. This routine monitors the channel for 12 consecutive instructions, searching for the start bit. In this way, the microcontroller is synchronized to the channel to within one instruction time (two bit times). If the start bit is never received, the program falls through the 12 instructions and goes back to monitoring for the arrival of a packet.

When the start bit is received, the common-reception routine examines the control code and branches to the appropriate packet-receiving routine—sound off, data, voice, or do nothing. The last routine is entered if the control code is invalid or if the control-code CRC indicates that an error has occurred.

End of a packet

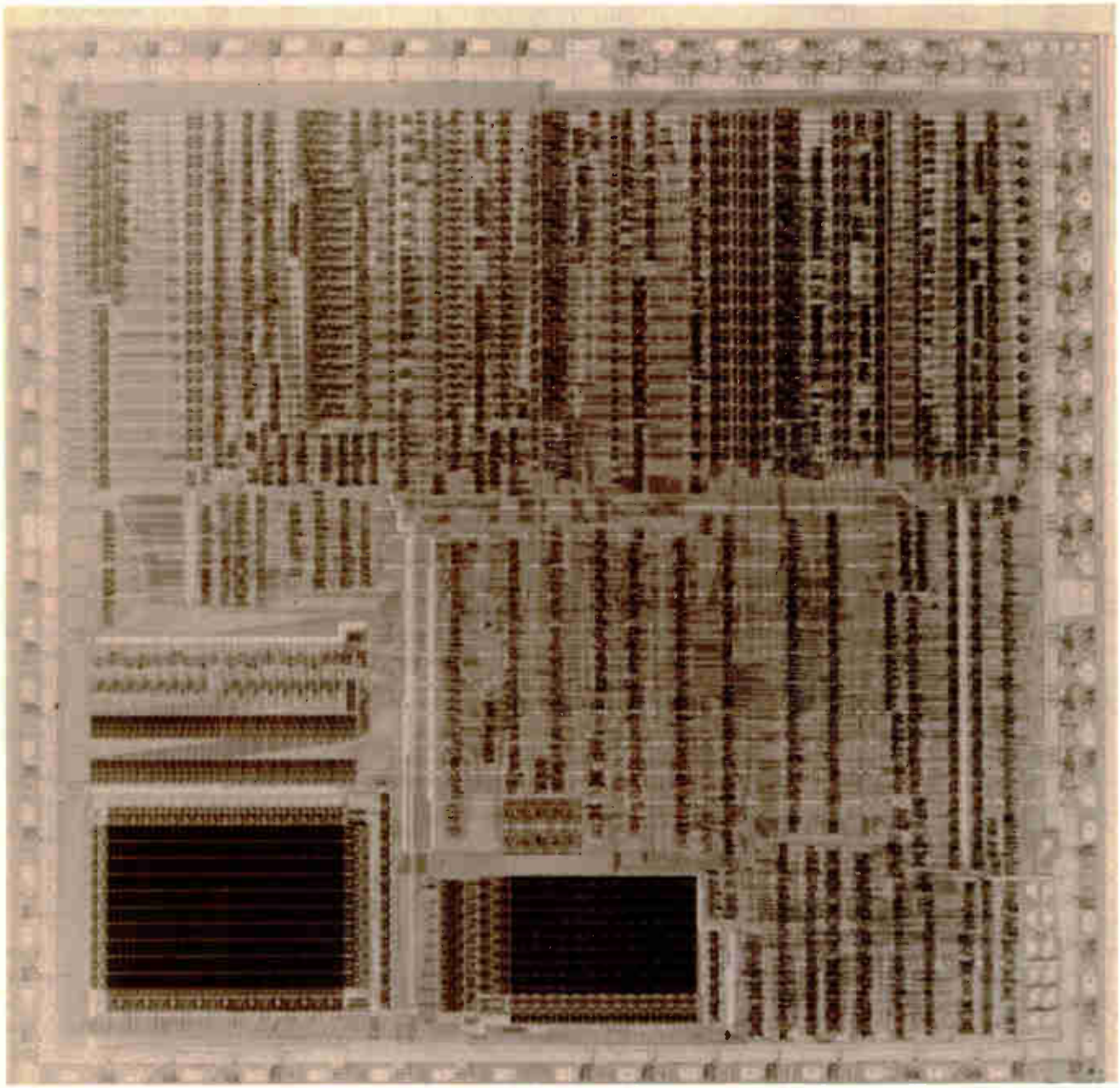
As noted earlier, since the reception routines handle the incoming data as it arrives, four instructions per byte, and the microcontroller is too busy to poll a status pin to determine when the variable-length packets have ended, hardware circuitry must be added to simulate an interrupt. The circuit designed for this purpose generates a reset pulse 2 μs after the packet has ended. The microcontroller then enters the reset handler. There it determines if an interrupt has occurred by reading the power-fail flag. Next, the program retrieves the stored control code or sets the control code to do nothing if the final CRC is in error. Finally, it branches back to the appropriate packet routine.

At the end of each packet-reception routine is a reception clean-up section. This section perform actions that must be deferred until the closing CRC bytes have been verified. Examples include loading the sound-off address into the current user register and notifying the node processor that a packet has arrived. After the clean-up section, the microcontroller returns to the timing and monitoring state. □

16-bit C-MOS processor packs in hardware for business computers

On-chip error detection, virtual memory support, and four operating levels equip 10,000-gate circuit for multiuser applications

by Norio Inui, Hideo Kikuchi, and Toshihiro Sakai, *Fujitsu Ltd., Kawasaki, Japan*



1. A real CAD. The FSSP 16-bit complementary-MOS microprocessor makes extensive use of computer-aided design, which acccounts for the regularity of its layout. Its multiple register sets occupy a large area on the die, but they speed along context switches.

☐ Sixteen-bit microprocessors have attained the speed and sophistication that enable them to serve as the central data-processing unit for multiuser applications like small-business computer systems or as a cluster-control device for intelligent terminals. The small-system processor, dubbed the FSSP, from Fujitsu is one such device that carries an added advantage—it can be microprogrammed to emulate an existing processor, though in the Facom V series of small-business computers it emulates the Unios architecture developed in 1974.

Today's small-business computer systems perform on-site processing with a typical configuration consisting of a work station centered around a display unit at each work site. The improvement in processor capabilities and storage capacity, along with the decline in the price of terminal equipment, has made it possible to place work stations wherever needed and given rise to multiple work-station processing.

The FSSP (Fig. 1) aims at processing universality in this emerging market through its ability to emulate the Unios architecture of the Facom series, as well as the high-level architectures of other machines. It uses microcode to support virtual memory management in the Facom V series, though in the Facom system 80 it handles only real physical addresses. In both, the FSSP executes such multiuser channel functions as input/output control in microcode, in addition to its normal data-processing function, and high system reliability has been achieved by virtue of full error detection on all internal and external buses.

Designed with a silicon-gate complementary-MOS process the FSSP uses a double layer of metal for connecting over 40,000 transistors that make up 10,000 gates, each of which has a propagation delay between 4 to 10 nanoseconds. The chip is housed in a 64-pin package, requires only a 5-volt supply, and dissipates about 130 milliwatts at a 2.5-megahertz clock rate. It can address 16 megabytes of main memory, has decimal arithmetic, and uses four hierarchical levels of operation to efficiently handle multiprocessing.

The FSSP's architecture permits emulation of the architectures of other machines at the lowest level possible. That means that if the operating system is viewed as the highest level, then the machine language can be considered the next level, and the native microprogram-controlled architecture of the FSSP will be at the lowest.

To efficiently emulate the Unios architecture of the Facom V and Facom system 80 computers, the FSSP has special microinstructions, registers, and other hardware.

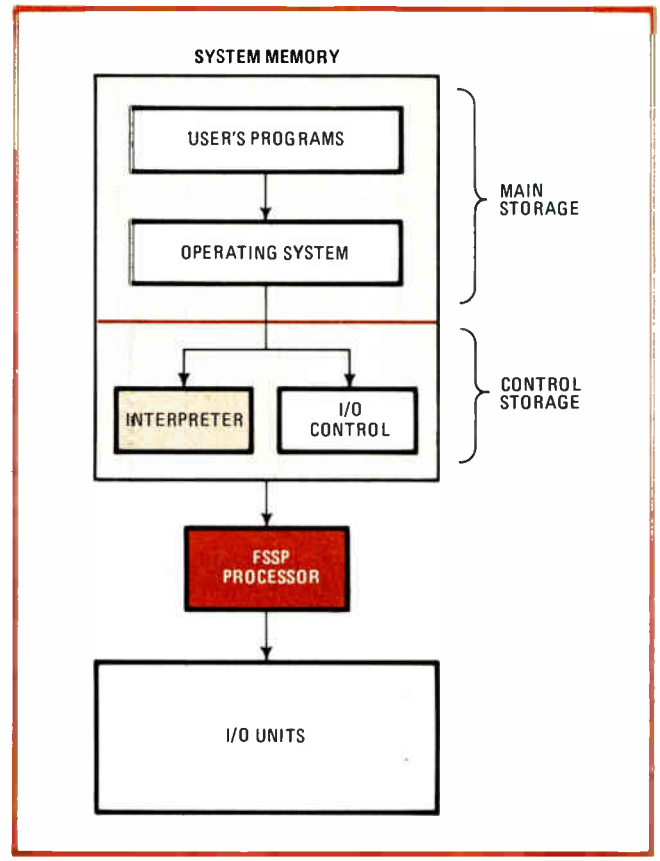
The microprogram is pulled up to the machine-language level of other computer architectures by an interpreter. Most of the other 16-bit microprocessors on the market have a preprogrammed machine language (see table). Under those circumstances, emulating the machine language of another computer through an interpreter can seriously degrade performance.

In order to efficiently emulate different architectures, it is necessary to have access to the microarchitecture of a machine, since it is the microinstructions that are executed at the highest speed. Although emulating machine language through the interpreter inevitably affects a processor's performance, this degradation can

COMPARING 16-BIT MICROPROCESSORS

	Fujitsu FSSP	Intel 8086	Motorola 68000
Addressable memory	16 megabytes (possible to support virtual storage)	1 megabyte (64-K bytes segment mapping)	16 megabytes (possible to support virtual storage)
Architecture	variable (oriented by microprogram on control storage)	fixed	fixed
Operating levels	4 levels	1 level	2 levels
Interrupt levels	3 levels	3 levels	7 levels
Addressing modes	3	6	12
Features of instructions	bit manipulation decimal addition and subtraction (packed/unpacked data) — — branch for codes	— decimal adjustment (packed/unpacked data) multiply and divide string manipulation —	bit manipulation decimal addition and subtraction (packed data) multiply and divide — —
Registers	⟨central processing unit level⟩ general registers, 16 bits by 16 words address registers, 16 bits by 8 words working registers, 16 bits by 8 words ⟨machine-check level⟩ working registers, 16 bits by 8 words ⟨input/output 1 level⟩ working registers, 16 bits by 8 words ⟨I/O 2 level⟩ working registers, 16 bits by 8 words	general registers, 16 bits by 4 words pointer registers, 16 bits by 2 words index registers, 16 bits by 2 words segment registers, 16 bits by 4 words	data registers, 32 bits by 8 words address registers, 32 bits by 7 words stack pointers, 32 bits by 2 words

2. Separate stores. A separate control store allows the FSSP chip to emulate the instruction set of other machines. A microcoded interpreter converts each instruction of the emulated machine into a series of microinstructions for the FSSP.



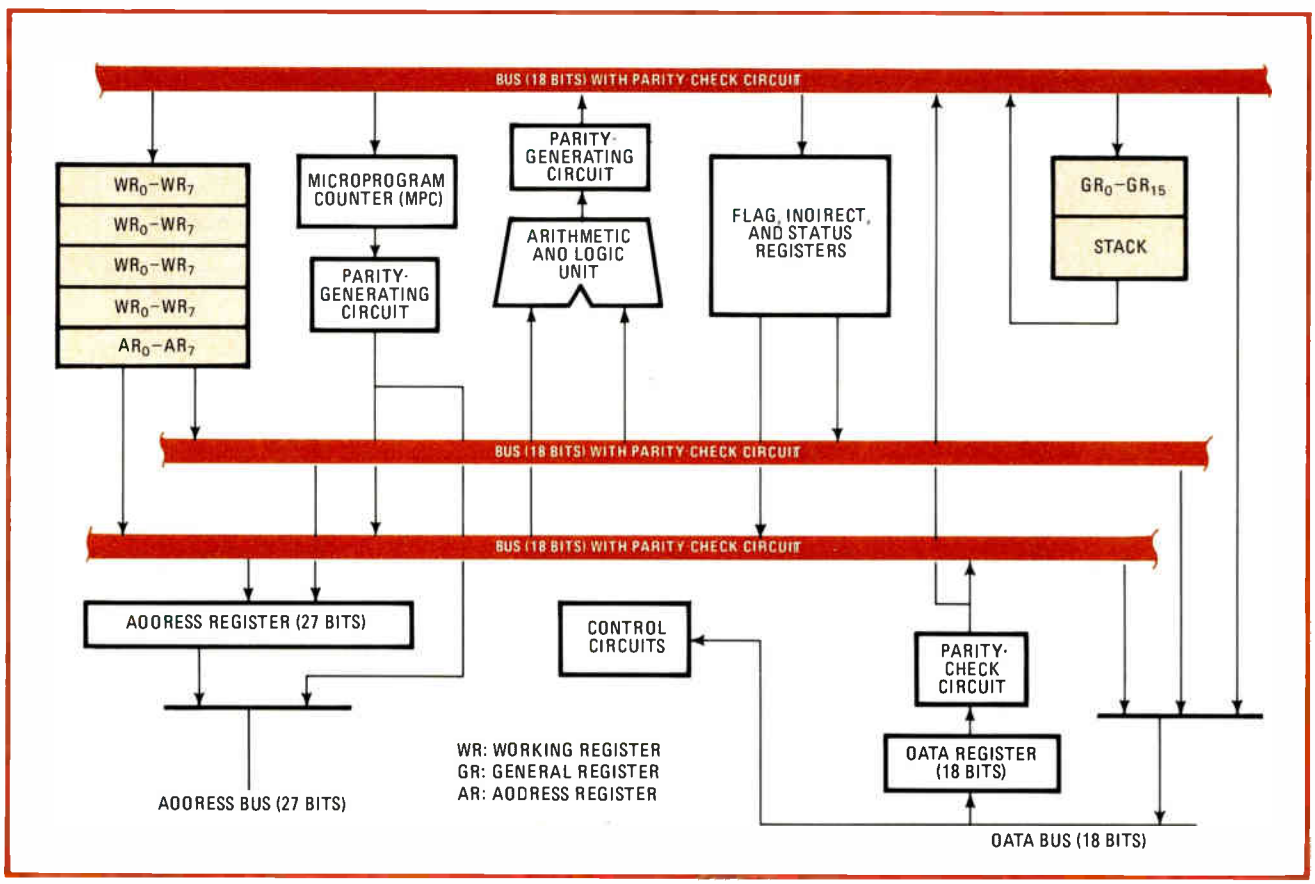
be reduced by supporting the most frequently used functions of the operating system through microprogramming and firmware.

The FSSP facilitates these functions by dividing storage into a control storage area and a main storage area. Figure 2 shows a typical example of how this storage scheme works. The control storage area contains an interpreter that emulates the architecture of the target machine, as well as microprogrammed routines for I/O control; the main storage area contains the target machine's operating system and user programs.

Microprogrammed architecture

The logical structure of the FSSP is designed for multiprocessing, especially in business environments. There are 117 microinstructions for binary arithmetic, logic operations, and shifting—all based on 16-bit data—and the shift instructions can shift from 1 to 16 bits in a single clock cycle. For accelerating the processing of business data of varying word lengths, there are also decimal arithmetic instructions, as well as decimal data-checking and -modification instructions.

The unit also has an ample set of data-transfer, I/O control, branch, and other instructions for fast and effi-



3. On-chip error detection. Each byte of data has a parity bit appended to it, making most of the data paths 18 bits wide. The FSSP also appends parity bits to its results, and whenever a parity error is detected, its source is logged and the offending operation retried.

cient microprogramming control. In addition, both the main and the control storage are accessed by a set of instructions that include an address-update function to streamline sequential accesses.

At the hardware level, four sets of 8-by-16-bit working registers furnish fast operating-system context switching. There are also 8 16-bit address registers, 16 16-bit general registers, a dedicated indirect register for address calculations, and other, more specialized registers—all arranged to facilitate the emulation of higher-level architectures. A functional branch instruction speeds emulation by quickly decoding instructions and commands. This instruction can be used with Unios or any other architecture.

Anticipatory control

High-speed operation is achieved through anticipatory control. Because the FSSP prefetches and predecodes microinstructions, most can be executed in a single machine cycle (400 nanoseconds). This extremely fast speed, coupled with the unit's interrupt-driven multiprocessing capability, enables most I/O control to be performed by microinstructions.

These instructions generate I/O control signals for up to 256 I/O ports, making it easy to add remote interfaces. Each signal transfers either 1 or 2 bytes of data, and a direct-memory-access circuit can be added when even higher transfer speeds are necessary.

The FSSP is designed to produce systems with high reliability and accordingly has a full range of error-detection functions not found elsewhere. On all the internal FSSP registers and buses, for example, 1 parity bit is attached to each byte of data, making most data paths 18 bits wide (Fig. 3).

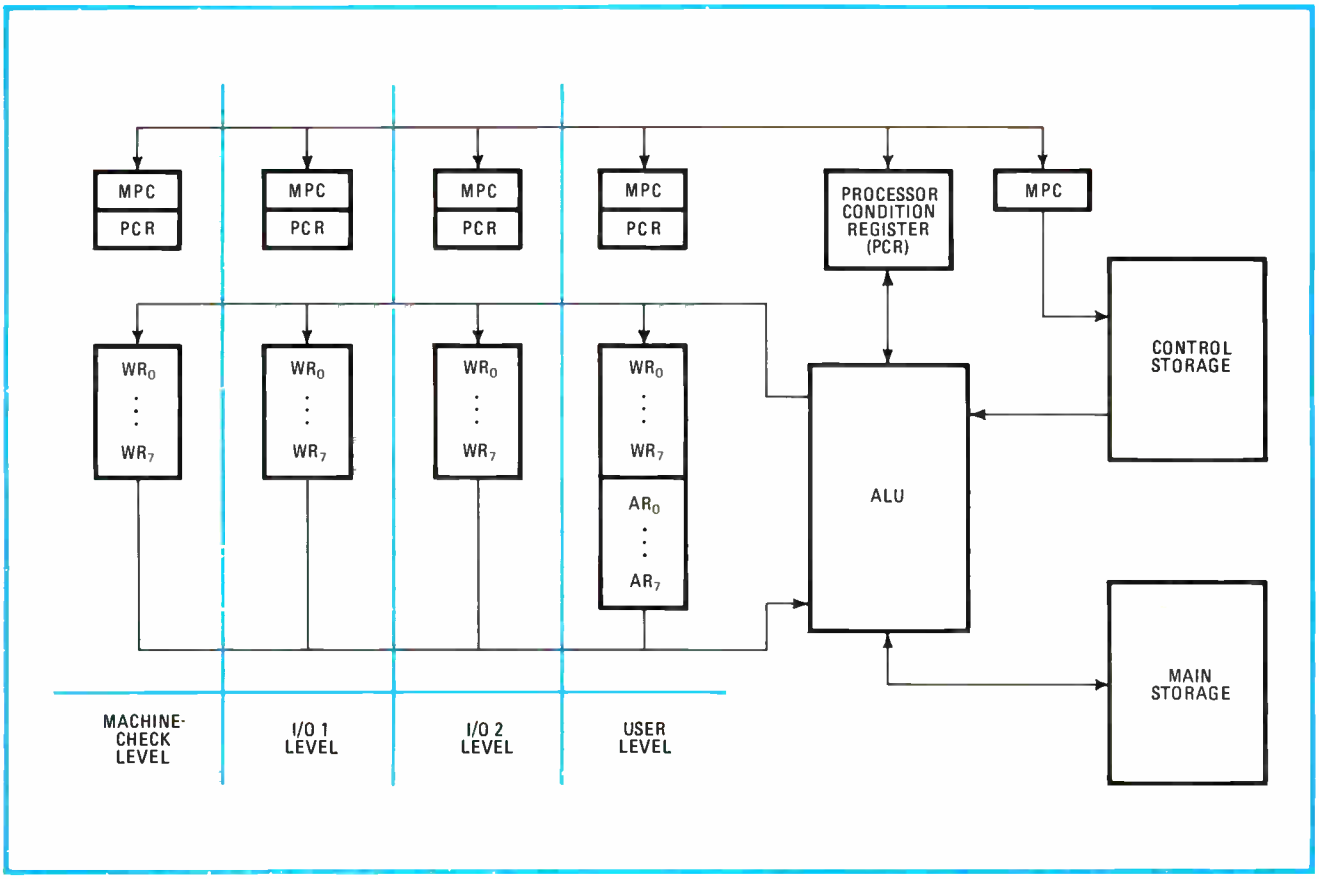
Achieving parity

The arithmetic and logic circuits use the parity method to check for errors without interrupting the data flow. The input-section circuits also check the parity of data coming on chip, making it possible to separate internal from external errors—an operation that is extremely difficult to effectively accomplish on conventional microprocessors.

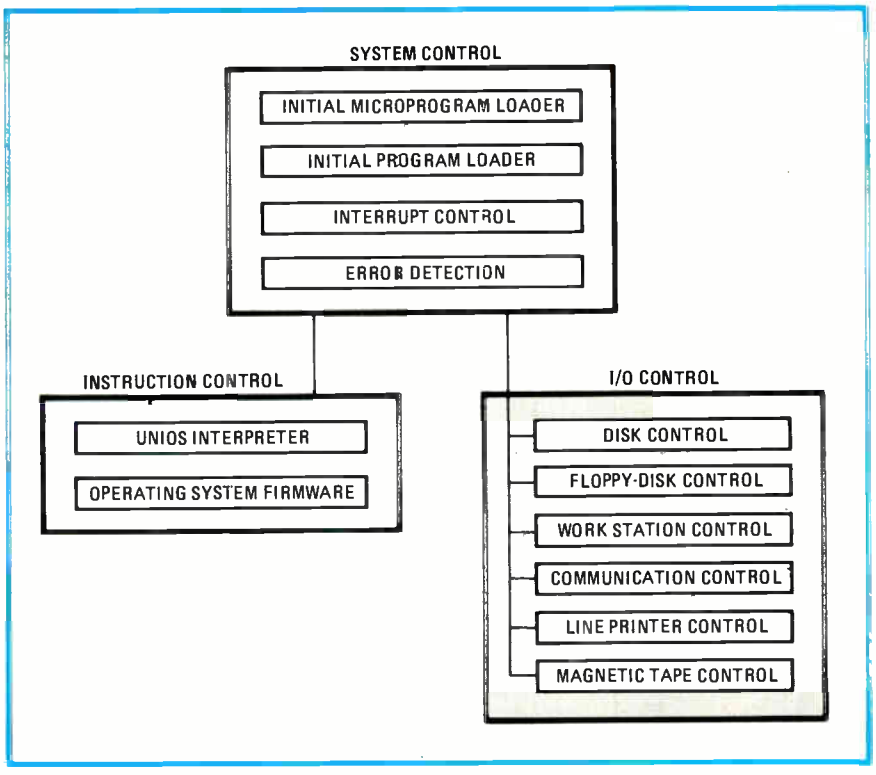
Backup registers behind all control registers give the machine-check level its own set of working registers. When an error occurs, the FSSP is designed to detect the source of the error, which is logged for later inspection, and then recovers by retrying the offending operation.

The FSSP has powerful multiprocessing functions that enable numerous I/O units to be processed simultaneously and in parallel with the execution of programs. A key factor in this capability is the chip's use of four operating levels, each of which has its own set of 8 16-bit working registers, a microprogram counter, and a area for saving condition codes (Fig. 4). No other microprocessor has such an extensive set of registers.

This duplication of register sets for each of the four levels of operation does consume die area, but the disad-



4. Multiple register sets. Four separate register sets and program counters on the FSSP eliminate the necessity for swapping values in and out of the FSSP when switching between the four operating levels. Switching is interrupt driven and is optimized for multiprocessing.



5. Firmware support. The Facom V-830 has extensive firmware support for system, instruction, and input/output control. The interpreter recognizes the Unios instruction set; other often-used functions such as disk control are also handled in firmware.

vantage is more than offset by the time saved during context switches. Specifically, in moving from one level of operation to another, an extremely frequent operation in multiuser environments, no time is wasted swapping register sets—an operation that can significantly slow down conventional processors.

Many computers have only two operating modes: a supervisory mode and a program mode. In contrast, the four mode levels of the FSSP are the machine check level (level 0), the I/O levels (1 and 2) and the normal user mode (level 3).

Switching between levels is done automatically when interrupts occur. These functions permit programs at each level to use the microprocessor as if they had independent possession of it, thereby achieving a high multiprocessing throughput not otherwise attainable.

Establishing an order

An order of processing priority is established among these levels, with level 0 as the highest and level 3 the lowest. Thus, tasks are automatically executed according to their degree of urgency, resulting in efficient multiprocessing. Since each level has its own working registers, program counter, and condition-code save area, there is no need to save either the registers or the condition codes when switching between levels.

The machine level answers two types of interrupts: those caused by hardware errors and those caused by program exceptions. I/O level 1 and I/O level 2 are reserved for interrupts from I/O devices, which are divided into two groups according to the time-critical nature of the peripheral. Slow devices like terminals and printers are assigned to the lower priority level, whereas higher-priority peripherals, such as disk and tape controllers, are assigned to level 1.

The FSSP has compiled a good service record in the Facom V series and Facom system 80. A representative example can be found in its use in the Facom V-830.

The functional components of the V-830 are a main memory capacity of 768-K bytes for storing the operating system and user's programs, all of which are written in the machine language of the emulated computer. A 192-K-byte control storage holds programs made up of FSSP microinstructions and their data.

The central processing card is the heart of the Facom V-830 and consists of the FSSP, plus storage and DMA control circuits. It uses microprograms held in the control store to execute Unios instructions, control I/O, convert virtual addresses, and execute DMA transfers over the high-speed bus. In addition, the V-830 has a disk file capacity of up to 464 megabytes and can support up to 16 work stations and 4 communication lines.

The central controller of this fairly large system is the FSSP along with the firmware residing in control storage to perform system, instruction, and I/O functions (Fig. 5). Under system control are two bootstrap programs for loading microprograms and user's programs, both initially from magnetic disk.

Another system firmware routine handles interrupt control. Yet another manages error detection whereby hardware status can be displayed and causes of machine checks are analyzed and reported to software.

The Unios interpreter, which emulates the Unios instruction set, is part of the instruction-control firmware, as shown. In addition, the operating-system firmware uses microprograms to carry out certain supervisory functions of the Unios control program. I/O control is also handled in firmware in order to efficiently execute the channel functions that control the I/O units. □

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Circle 187 on reader service card

Light pen generates plotter signals

by E. Chandan and Agarwal Anant, *Department of Electrical Engineering, Indian Institute of Technology, Madras, India*

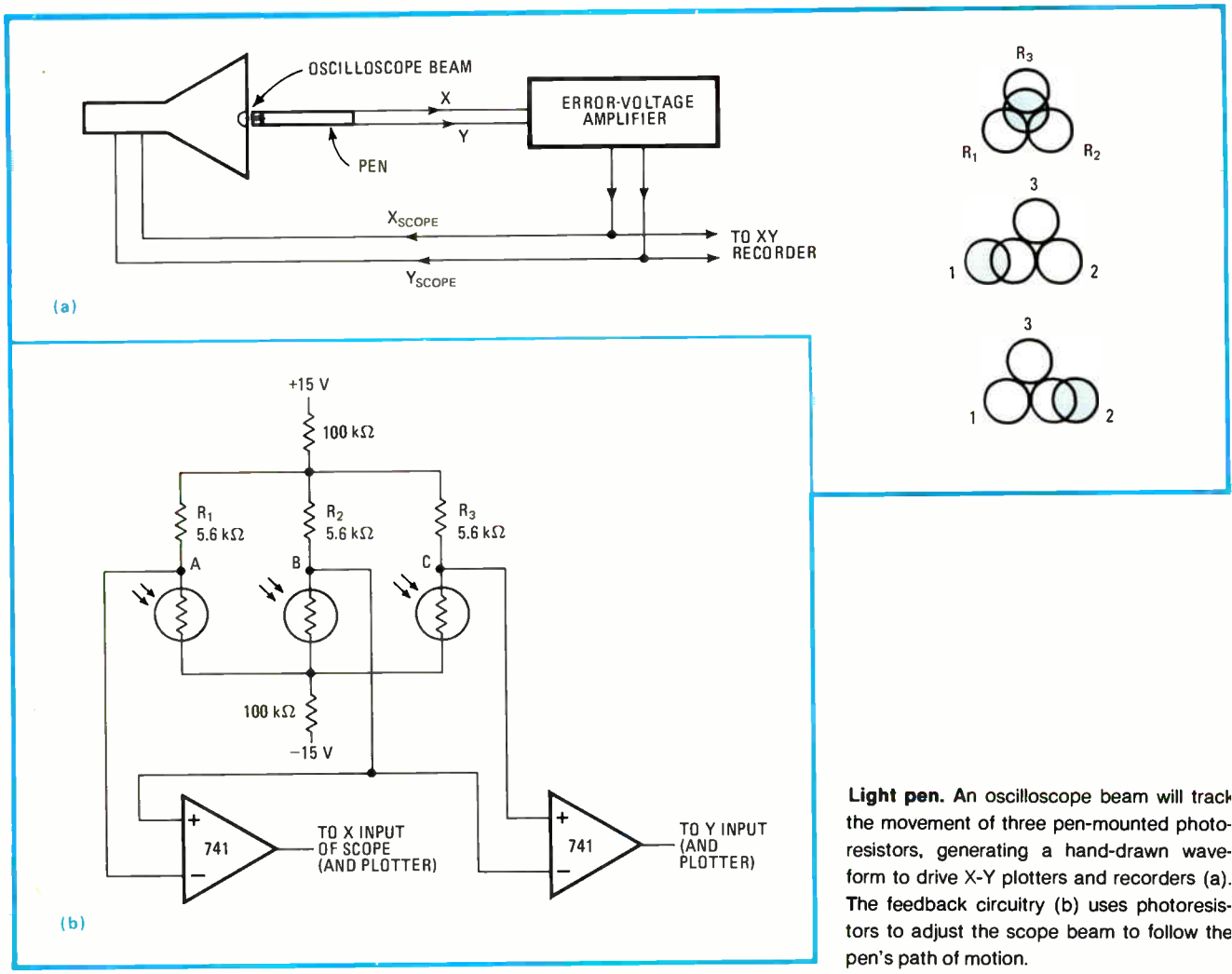
By tracing out the shape of any waveform and sending it to an X-Y plotter or other recording instrument, this photoresistive sensor, in conjunction with an oscilloscope, provides a convenient and inexpensive way to translate hand-drawn data and similar information to a remote location in real time. The sensor requires only three light-dependent resistors (LDRs) and two operational amplifiers. The scope supplies a pinpoint light source that follows the movement of the sensor and thereby generates the required X and Y signals to the plotter or recorder.

As shown in (a), the faces of three LDRs, each having a diameter of about 4 millimeters, are mounted on the tip of an ordinary pen so that their centers lie on the vertices of an equilateral triangle and in the same plane. The LDRs are then wired into the circuit whose schematic is shown in (b).

The pen is brought within a few millimeters of the scope and thus in proximity to the initially unswept scope trace, which is a spot of light on the screen when the scope is in the X-Y mode. The position of the LDRs with respect to the screen (R_3 at the top, R_1 and R_2 at the bottom) must remain fixed.

When the scope beam (shaded area) is in the center of the LDRs, their corresponding resistances are virtually equal, because approximately the same amount of light hits each device. Consequently, no error voltage (no X_{scope} or Y_{scope} signal) is generated, and the spot will not move with respect to the light pen.

If the pen is moved to the right or left or up or down, as shown, the resistances of the LDRs become unequal, an error voltage is generated, and the scope beam moves in a direction that minimizes the feedback voltage—toward the center of the LDRs. The spot thus follows the



Light pen. An oscilloscope beam will track the movement of three pen-mounted photoresistors, generating a hand-drawn waveform to drive X-Y plotters and recorders (a). The feedback circuitry (b) uses photoresistors to adjust the scope beam to follow the pen's path of motion.

pen and in so doing creates the X_{scope} and Y_{scope} signals used to drive the remote recorder or plotter. Should the pen be removed from the proximity of the screen, the beam spot returns to its original setting.

As the schematic shows, when the spot hits the center of the sensor, $R_1 \approx R_2 \approx R_3$, and so $V_A \approx V_B \approx V_C$. Thus, neither 741 op amp generates any appreciable X_{scope} or Y_{scope} signal and the spot remains fixed. For the second condition, $V_C > V_B > V_A$, and a large positive voltage is generated at X_{scope} to push the beam to the right, while a small Y_{scope} voltage pushes the beam slightly upward. For the last condition, $V_C > V_A > V_B$, and the beam is pushed left and slightly upward. □

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Computer notes

Pocket computer solves for LC resonance using Basic

by Cass R. Lewart
System Development Corp., Eatontown, N. J.

The pocket computers that were recently introduced by several manufacturers represent a new breed of calculator. A unit manufactured by Sharp Corp. and distributed by Radio Shack (catalog No. 26-3501), for example, executes a comprehensive set of Basic statements, thus allowing easy writing, editing, and debugging of programs. Here, a coil-resonance program illustrates some of the computer's strong and weak points as compared with an advanced programmable calculator.

To make programming it easier, the pocket computer has alphanumeric prompts, alphanumeric variables, and dimensioned variables. Programming in Basic also has the inherent advantage over reverse Polish notation (RPN) or arithmetic operating-system (AOS) notation of keeping the display register free—the display is not explicitly used by the computer for computation (except in the INPUT statement). Thus, a running program can be interrupted at any point, its variables reviewed or modified, and the program then restarted without affecting the computation process.

The program evaluates a resonant circuit having a lossless, single-layer airwound coil and a capacitor. The circuit is fully described by two equations—an approxi-

COIL RESONANCE PROGRAM

```
5:   "S"CLEAR:  USING"##.## ⌢ ": PRINT "COIL RESONANCE PROGRAM"
10:  "Z" Z=1:  PAUSE "COMPUTE":  END
15:  "C" AREAD C:  IF Z=0 GOTO 20
17:  Z=0:  C=1/(2πF)⌢ 2/L
20:  PRINT "CAPACITANCE=";C
25:  "L" AREAD L:  IF Z=0 GOTO 30
27:  Z=0:  L=1/(2πF)⌢ 2/C
30:  PRINT "INDUCTANCE=";L
35:  "F" AREAD F:  IF Z=0 GOTO 40
37:  Z=0:  F=1/2π/√(LC)
40:  PRINT "FREQUENCY=";F
45:  "D" AREAD D:  IF Z=0 GOTO 50
47:  Z=0:  D=(9L+√(81LL+40LANN* EXP-6))/NN* EXP6
50:  PRINT "DIAMETER=";D
55:  "N" AREAD N:  IF Z=0 GOTO 60
57:  Z=0:  GOSUB 100:  N=√(XL)/D
60:  PRINT "# TURNS=";N
65:  "A" AREAD A:  IF Z=0 GOTO 70
67:  Z=0:  A=((DN* EXP-3) ⌢ 2-18DL)/40L
70:  PRINT "LENGTH=";A
75:  "X" Z=0:  GOSUB 100
77:  L=NNDD/X:  GOTO 30
100:  X=(18D+40A)* EXP6:  RETURN
```

	Shift S	clear all variables, start computation
⟨value⟩	Shift F	enter frequency in hertz
Shift Z	Shift F	compute F from C and L
⟨value⟩	Shift C	enter capacitance in farads
Shift Z	Shift C	compute C from F and L
⟨value⟩	Shift L	enter coil inductance in henrys
Shift Z	Shift L	compute L from F and C
Shift Z	Shift X	compute L from A, D, and N
⟨value⟩	Shift A	enter coil length in inches
Shift Z	Shift A	compute A from L, D, and N
⟨value⟩	Shift D	enter coil diameter in inches
Shift Z	Shift D	compute D from L, A, and N
⟨value⟩	Shift N	enter number of turns
Shift Z	Shift N	compute N from L, A, and D

To review value of any parameter, key its name followed by ENTER; for example, to find the currently stored frequency, press F, then ENTER.

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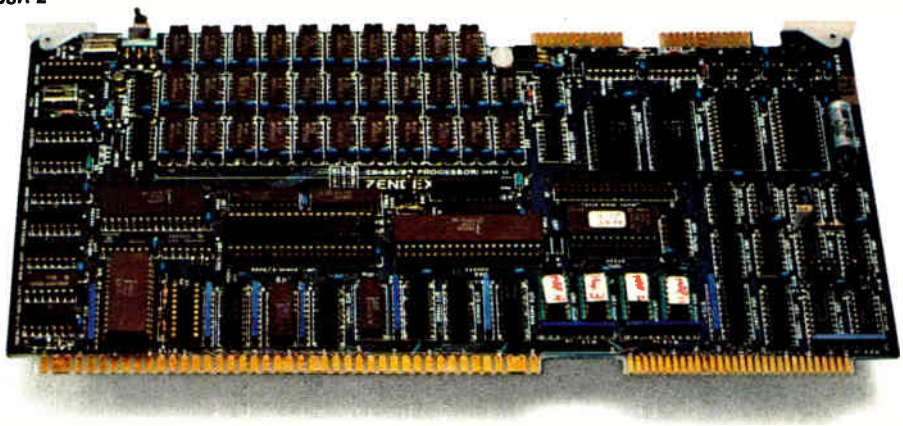

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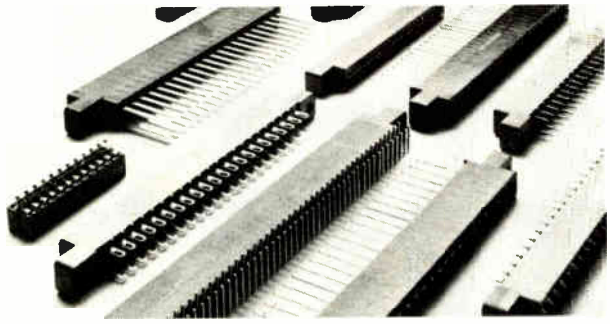

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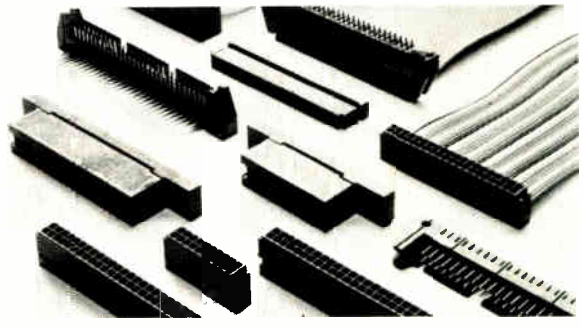

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LC RESONANCE EXAMPLES

A single-layer coil 1.5 in. long, 0.6 in. in diameter, with 14 turns, resonates with an unknown capacitor at 10 MHz. What parallel capacitor value is required to lower the resonant frequency to 9 MHz?

Key entry	Display	Remarks
Shift S	COIL RESONANCE PROGRAM	start, clear variables
Exp 7 Shift F	FREQUENCY= 1.00 E07	enter frequency
1.5 Shift A	LENGTH= 1.50 E00	enter coil length
0.6 Shift D	DIAMETER= 6.00 E-01	enter coil diameter
14 Shift N	# TURNS = 1.40 E01	enter number of turns
Shift Z Shift X	COMPUTE INDUCTANCE= 9.96 E-07	find L from A, D, and N
Shift Z Shift C	COMPUTE CAPACITANCE= 2.54 E-10	find C from F and L
T=C Enter	2.54 . . . E-10	save C temporarily
9 Exp 6 Shift F	FREQUENCY= 9.00 E06	enter new frequency
Shift Z Shift C	COMPUTE CAPACITANCE= 3.13 E-10	find new capacitor
C-T Enter	5.96 . . . E-11	an extra 60 pF is required

Instead of adding a capacitor, how many turns could be added to the coil?

Key entry	Display	Remarks
C=T Enter	2.54 . . . E-10	restore previous C
T=N Enter	14.	save old N temporarily
Shift Z Shift L	COMPUTE INDUCTANCE= 1.23 E-06	find new inductance
Shift Z Shift N	COMPUTE # TURNS= 1.55 E01	find number of turns equals 15.5
N-T Enter	1.55	add 1.5 turns

mation formula for the coil inductance together with the resonance equation of a resonant parallel or series LC circuit: $L = [(ND)^2 \times 10^{-6}]/(18D + 40A)$ and $(2\pi F)^2 LC = 1$, where F is the frequency in hertz, C is the capacitance in farads, L is the coil inductance in henrys, A is the coil length in inches, D is the coil diameter in inches, and N is the number of turns.

When running the program, the user either stores a parameter value or computes it by means of an appropriate linear or quadratic equation that can be derived from the above formulas.

For example, once the program on page 189 has been listed, the computer should be placed into the define (DEF) mode. The parameters F, C, L, A, D, or N may then be entered, computed, or reviewed in any order by pressing the appropriate keys, as designated in the table's lower portion. Then to review the value of any parameter, its name is keyed and followed by an enter statement.

Typical examples are illustrated above. Suppose a single-layer 14-turn coil 1.5 in. long and with a diameter of 0.6 in. resonates at 10 megahertz when paired with a capacitor of unknown value, and it is desired to lower that resonance to 9 MHz by adding in parallel another capacitor. By following the steps in the first of the examples, the program will indicate an additional 60 picofarads is required. Alternatively, the problem could have been solved by adding turns to the coil. The second of the examples indicates the coil would require an additional 1.5 turns.

This program was originally prepared for the Hewlett-Packard HP-67 calculator. For the unit, a 112-step program occupied half of the calculator's program memory and took many hours to write. Though it is simple to use, the calculator program is difficult to modify and also difficult to follow.

In contrast, the Basic program took less than an hour to write, occupies only 40% of a pocket computer's program memory, has good prompts, and is easy to follow and modify for other personal computers that can be programmed in Basic. Because of this and other programs, the Basic calculator has about 1.2 to 2 times the program capacity of the HP-67, but executes programs at speeds that are 20% slower.

The weak points of the hand-held Basic computer, as compared with a desktop or larger computer, are its lack of string-manipulation commands and DATA statements, which often lead to long and repetitive programs. However, it is possible to enter repetitive statements quickly into program memories by assigning a string of program text in the reserve mode to a single key.

Finally, although a hand-held computer can store programs and data on an external cassette recorder, the process is somewhat more inconvenient than the use of the magnetic strips of calculators. However, the unit's complementary-MOS memory retains programs and data even when the computer is turned off. □

Bibliography
C. Lewart, "Coil Resonance Program for HP67/97," Microwaves, December 1978, pp. 86-88.

Engineer's newsletter

How to evaluate software tools

Software tools—those aids to writing better programs—are all well and good, but how can you tell if one is better than another? **A framework for comparing software tools and a scheme for classifying them by their special features are given** in a new National Bureau of Standards publication, SP-500-74, "Features of Software Development Tools." Its taxonomy of tool features can be used to categorize currently available tools, standardize associated terminology, and ease the task of comparison and evaluation. The report is available for $1.75 from the Superintendent of Documents, U. S. Government Printing Office, Washington, D. C. 20402. Order it by stock number 003-003-02295-1. A pocket-sized guide to the taxonomy, publication LC-1127, is free from the Software Tools Project, Technology A265, NBS, Washington, D. C. 20234.

Converting the M-10 four-voice instrument into an orchestra

A battery-operated polyphonic keyboard instrument popular with engineers interested in electronic music, the Casio M-10 can simulate the piano, violin, flute, and organ and play up to eight pitches simultaneously. Appropriate modifications to the M-10's microprocessor, says Robin Whittle of 42 Yeneda St., North Balwyn, Australia 3104, can make the machine do even more tricks—**for example, offer 25 voices, a milder vibrato, and a 49-note keyboard rather than the present 32.** Whittle has written a thorough technical bulletin describing how to modify the instrument to add these and other features, some of which are already programmed into the main chip. He'll be glad to send you a copy of his 14-page memo for $3.00 in U. S. funds, to cover the cost of printing and mailing by air.

Get the word on the Z80 bus

The standard Z80 microprocessor bus board needs its pin functions and bus timing clearly defined so that designers can ensure the compatibility of other boards connected to it. Mostek Corp. is **offering a free user's manual** to make life easier for those responsible for these chores. The 50-page publication details the timing of the central processing unit's bus, memory read and write operations, input and output cycles, interrupts, request and acknowledgment cycles, and general timing specifications. For a copy, write to Mike Honea at 1215 W. Crosby Rd., Carrollton, Texas 75006, or call him at (214) 323-7202.

IEC offers help in comparing earth station receivers

There are two methods of measuring the figure of merit—the ratio of the antenna gain to the system noise temperature—of earth station receivers operating at 6 GHz for the uplink and 4 GHz for the downlink. One uses stars having known flux densities at the earth station and takes into account the errors introduced by various system parameters; the other, an indirect method, is based on the absolute measurement of the power into the antenna from a distant source, usually a satellite beacon, that radiates a known flux density. Both methods are complicated and, in practice, difficult to implement. Whichever you choose, the International Electrotechnical Commission has come to your rescue. Publication 510-3-2 is, in the words of the commission, **"a highly technical document," complete with how-to information** that goes so far as to include the characteristics of the radio stars used in the first method mentioned. It is available for 32 Swiss francs from the Information Officer, IEC, 1 Rue de Varembé, 1211 Geneva 20, Switzerland.

-Harvey J. Hindin

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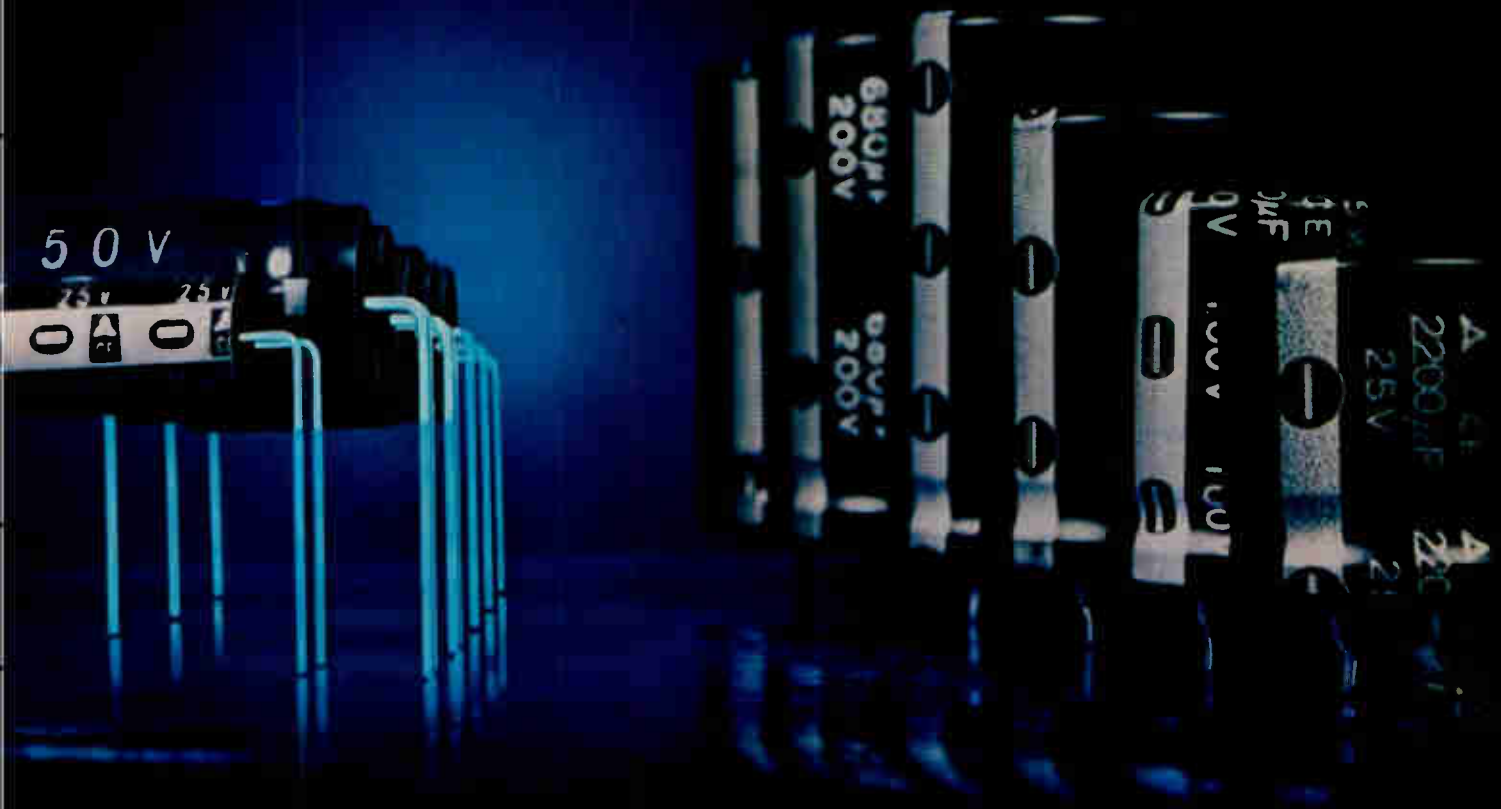

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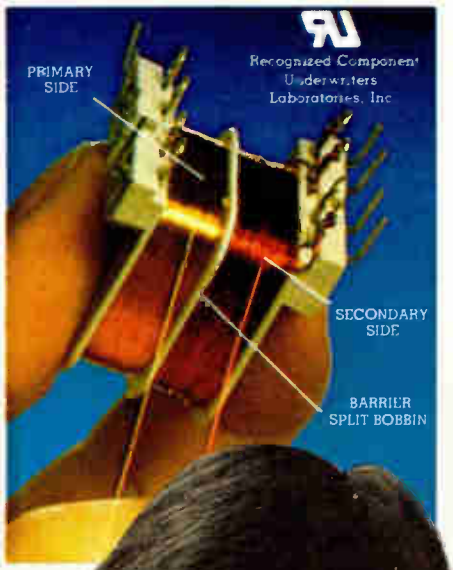

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Circle 196 on reader service card

68000 powers desktop computer

16-bit unit has 7-in. CRT for graphics, language in ROM, floppy-disk drive, soft keys, and 512-K-byte RAM limit

by Martin Marshall, West Coast Computers & Instruments Editor

In designing a software-compatible successor to the popular HP 9825A desktop computer, the 9826A, Hewlett-Packard has chosen the 8-MHz Motorola 68000 as a central processing unit [*Electronics*, March 27, 1980, p. 33]. At the same time, the company has also taken the wraps off some new options for the HP 9845 desktop line.

The 9826A has been benchmarked at two to five times the power of the 9825A, -B, or -T, depending upon the type of job run. That additional power makes its basic price of $8,950 compare favorably with the $8,600 selling price of the 9825T (with system software in read-only memory) and the $8,150 price of the 9825B. The price includes a ROM-based high-level language, either HP's enhanced Basic or HPL, and a Pascal option is planned. It also includes 64-K bytes of random-access memory; a double-sided, double-density 5¼-in. floppy-disk drive with a capacity of 256-K bytes; a built-in IEEE-488 interface; and a 7-in. 400-by-300-picture-element monochromatic cathode-ray tube.

The CRT displays 25 lines of 50 characters each, as well as graphics, with the character set comprising 256 5-by-7-dot characters, each in an 8-by-12-dot cell. The keyboard includes 10 programmable soft keys (5 keys with a shift) whose labeling can be displayed on the CRT.

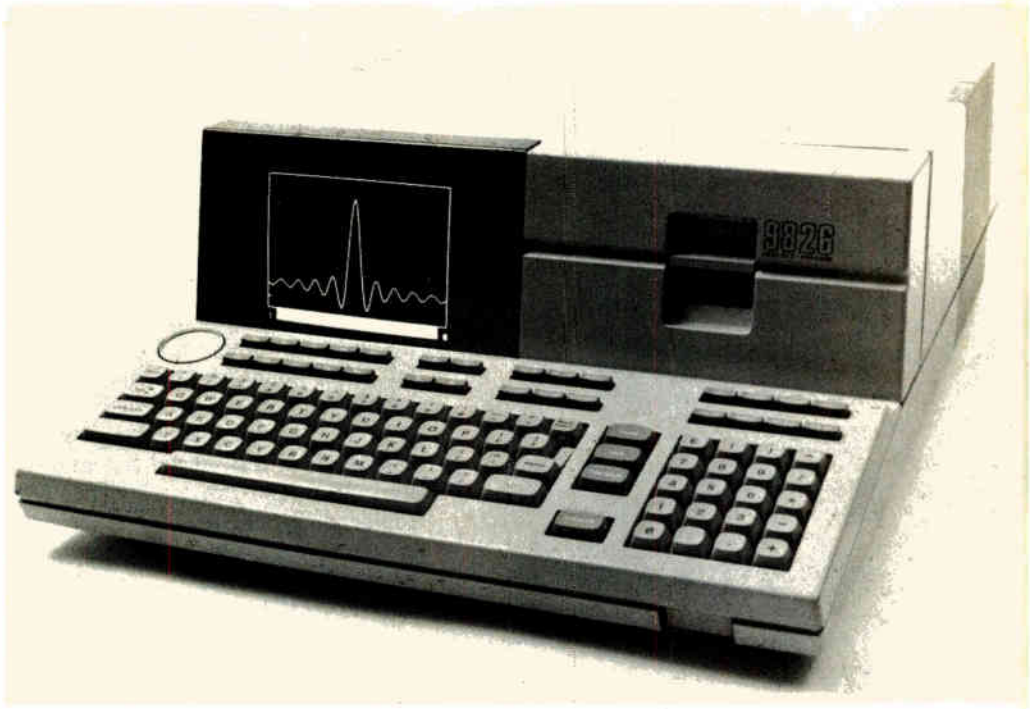
Other features include a real-time clock and a new data-communications interface that implements both an asynchronous protocol and HP's Distributed Systems Network link protocol. Four interface cards are optional: a general-purpose input/output card providing 16 bits of latched bidirectional data transfer, a binary-coded–decimal interface card, an RS-232-C serial interface card, and an extra IEEE-488 interface card allowing communication with up to 14 more IEEE-488–compatible devices.

Disk-based language. The main memory of the 9826A can be increased in increments of 64-K bytes from the standard 64-K bytes up to 512-K bytes at a cost of $1,000 per 64-K-byte board. HP also will make available versions of the 9826A with the programming language on floppy disk. These require 128-K bytes of RAM and cost $11,950 with Basic and $8,950 with HPL.

In addition, there are several new versions of the HP 9845 computer system, each made more powerful by the use of a microprogrammed bit-slice processor to replace the language-processing unit used on previous models. New options include a high-performance green CRT, soft keys, a light pen, and foreign-language printing. Main memory can range from 56-K bytes to 449-K bytes, with 187-K bytes used in the standard version.

The new standard color graphics version of the 9845 is the HP 9845C model 250, and the monochrome version is the HP 9845B model 250. With 187-K bytes of RAM, the former is priced at $43,500 and the latter at $28,000. Delivery on all 9845 and 9826A systems takes 18 to 20 weeks.

Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, Calif. 94304 [338]



Semiconductors

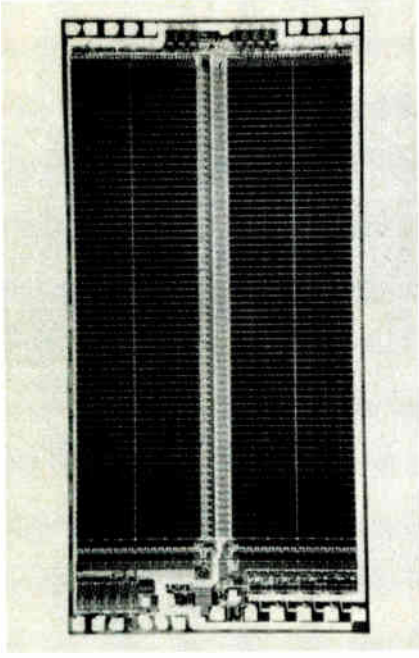
Static RAMs set MOS speed record

4-K-by-4-bit memory chips reduce package count in speed-critical applications

Inmos Corp. surprised memory manufacturers and users last year when it unveiled a 16-K static MOS random-access memory with a maximum chip-enable access time of 45 ns and a power dissipation of 660 mW [*Electronics*, Sept. 11, 1980, p. 117]. Organized as 16-K by 1 bit, the IMS1400 is ideally suited for deep storage arrays, replacing lower-density high-speed MOS and bipolar memories.

The IMS1400 has spawned two companion products, the IMS1420 and 21, arranged as 4-K by 4 bits. These chips are perfect for shallower memory systems, where the advantages of large-scale integration and reduced package count can be simultaneously enjoyed.

But shallower stores are not the only application for the new chips, points out Rahul Sud, a senior engineer who was instrumental in the design of the memories. Like the 1400 itself, the 1420 and 1421 chips will benefit bit-slice microprocessor systems, writable control stores, fast cache and buffer memories, and just about any other kind of speed-critical application.



Indeed, the 1420 and 1421 are direct upgrades for the 2148H and 2149H 1-K-by-4-bit fast MOS static RAMs that were pioneered by Intel Corp. Like the 2148, the IMS1420 provides a chip-enable function that can be used to place the device in a power-down mode, thereby reducing its power consumption to 100 mW.

Maximum access times. Whereas the 1420 has 45- and 55-ns chip-enable access times, the 1421 does away with the automatic power-down function to gain speed, like the 2149. The 1421 has its chip-enable signal internally tied off via a metal-mask option so that the device stays on. In place of a chip enable, that pin is used for output control, resulting in maximum chip-select access times of 30 and 40 ns.

Both new RAMs have kept the 20-pin dual-in-line package of the 1400 by multiplexing data-input and -output signals on four common pins. The by-4-bit parts have also retained a very low active-power dissipation of 500 mW, maximum, using "some tricks in I/O signal routing to accommodate the three additional sense amps," comments Sud. Memory cells in the new chips have also been compacted using 2.5-μm minimum tolerance instead of the 2.7-μm features that are on the 1400.

To bolster yields in the face of hard errors, the IMS1420 and 21 incorporate redundancy. The company looked at single-bit replacement, but the amount of switching circuitry and the number of polysilicon fuse elements would have become unwieldy. So if a 4-bit word contains a bad bit, the entire word gets replaced, using spare bits from 8 extra memory columns.

Sample quantities of the IMS1420 and the IMS1421 will become available in the second half of this year. By the fourth quarter, either memory chip will sell for less than $50 in quantities of 100 units or more.

Inmos Corp., P. O. Box 16000, Colorado Springs, Colo. 80935. Phone (303) 630-4000 [411]

C-MOS gate arrays use double-metal technology

The G90000 series is a family of high-speed, high-density complementary-MOS gate arrays using double-level-metal interconnection technology. The oxide-isolated silicon-gate C-MOS family consists of six members with counts of 1,160, 1,790, 2,240, 2,780, 3,500, and 5,100 cells per chip. The 5,100-cell part has a die size smaller than a 308-mil² single-level-metal product with 1,960 cells. Each cell can make a gate with up to three inputs.

The G90000 series offers both C-MOS- and TTL-level interface logic, plus a full low-power Schottky fan-out capability of 4-mA sink current at 125°C. Inverter delays are less than 3 ns with an internal fan-out of three at 5 V and over the commercial temperature range. Development of the customized circuits takes from 12 to 26 weeks, and the production phase about 6 weeks. Pricing is 9¢ per gate for small quantities, and averages about 1.5¢ per gate for quantities of 100,000 or more.

International Microcircuits Inc., 3350 Scott Blvd., Building 37, Santa Clara, Calif. 95051 [412]

Large portion of monochrome TV receiver is put on a chip

Motorola has introduced the Monomax chip, which contains all the signal-conditioning circuitry needed for a complete black and white television receiver. Sound intermediate-frequency and power stages and the tuning section are about all that need to be added.

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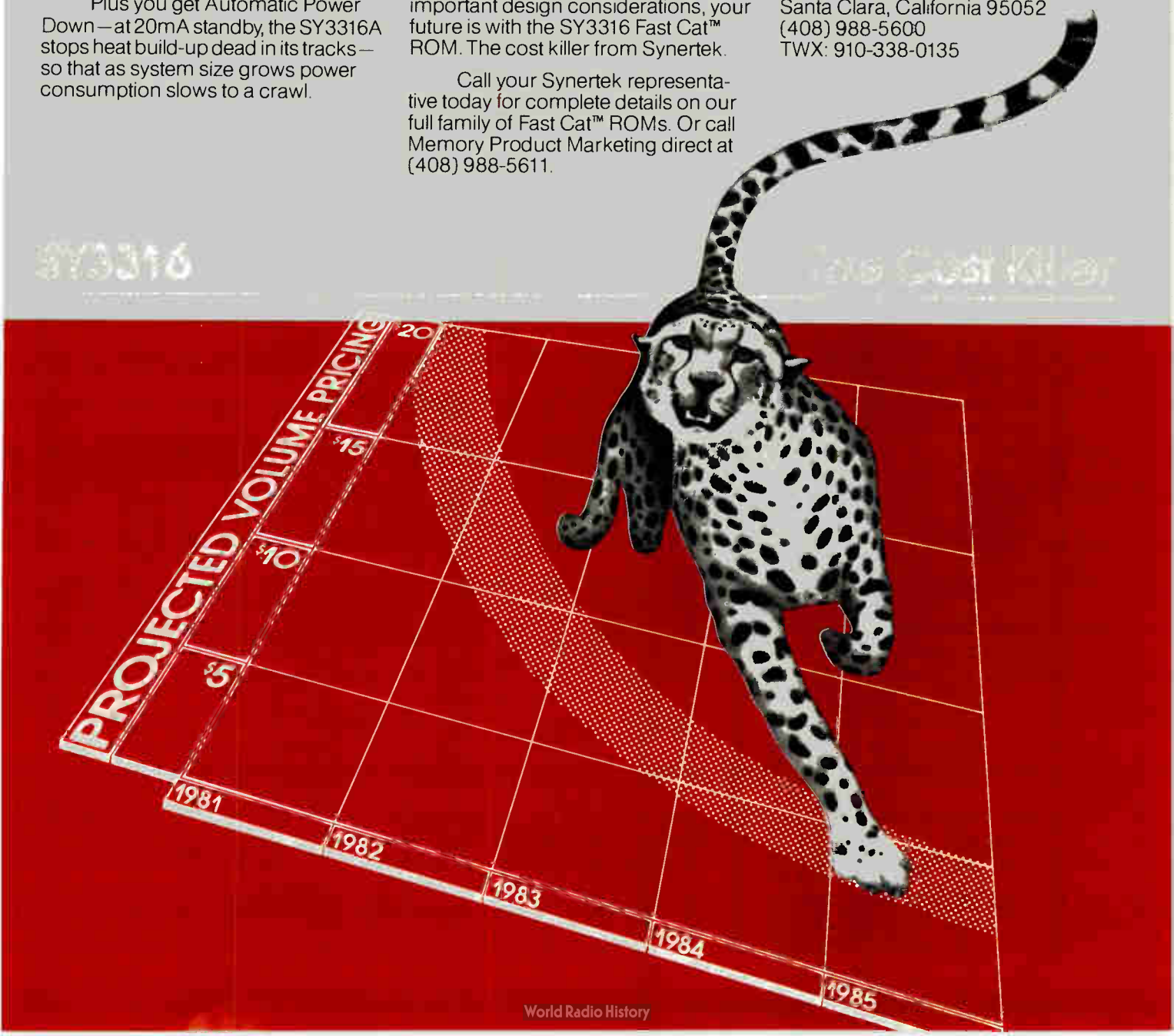

New products

video detector that is fully balanced, linearized, and filtered on chip to eliminate detector coils. Its synchronization-signal separator has on-chip noise filtering and canceling and its two-loop phase-locked–loop system needs only a raw feedback pulse for synchronization. The Monomax has an input sensitivity of 100 μV, an i-f bandwidth of 80 MHz, and a horizontal oscillator drift of less than 1.0 Hz/°C.

The chip sells for $6.82 in quantities of 100 to 999, $4.55 in lots of 1,000, $3.66 for 5,000, and $3.36 for 10,000.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036 [413]

Low-noise op amp slews at 2.8 V/μs, has 10-μV offset

The OP-27 operational amplifier offers designers a peak-to-peak noise of only 80 nV in the 0.1-to-10-Hz band and just 3 $nV/Hz^{1/2}$ at 1 kHz. It also features a low offset voltage of 10 μV, a slew rate of 2.8 V/μs, a gain bandwidth of 8 MHz, and a long-term drift of 0.2 μV per month. It has a noise corner frequency of 2.7 Hz, a maximum input offset voltage of 25 μV for A- and E-suffix devices, 0.2-μV/°C offset drift, a voltage gain of 1.8×10^6, common-mode and power-supply rejection ratios in excess of 120 dB. The OP-27 is available in eight-pin dual in-line packages and in eight-pin TO-99 cans. It is offered in versions for −55° to +125°C or −25° to +85°C operation and three electrical grades. Pricing varies from $5.50 to $50 for 100-piece quantities.

Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, Calif. 95050 [416]

8-pin PCM integrated circuit controls switching supplies

The NE/SE5561 switched-mode power-supply controller is an eight-pin integrated circuit that provides pulse-width-modulation control in dc power supplies, motor-controller in-

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Circle 201 on reader service card

New products

verters, and dc-dc converters. It has internal supply temperature compensation, a pulse-width modulator, sawtooth oscillator, overcurrent sense latch, and output stage. The chip provides cycle-by-cycle current limiting and double-pulse and low-supply-voltage protection. The extensive housekeeping functions of earlier versions have been eliminated to simplify use.

The 5561 SMPS is currently available in a miniature dual in-line N-type package and will be offered later this year in Signetics' microminiature small-outline D-type package and in a military-temperature-grade version in an FE-type Cerdip package. The 5561 has a supply requirement of +18 V, an output of 40 mA, and an output duty cycle of 98%. It will operate over the temperature range of 0° to +70°C in the N and D packages.

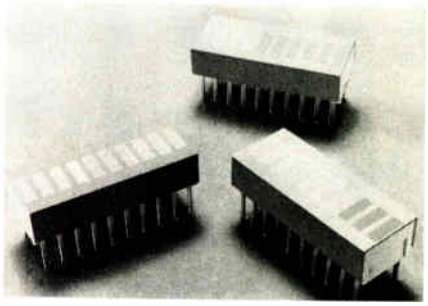
Available from stock, it costs 75¢ each in quantities of 100.

Signetics, 811 E. Arques Ave., P. O. Box 409, Sunnyvale, Calif. 94086. Phone (408) 739-7700 [414]

Bar-graph LEDs take on high ambient-light levels

The HDSP-48XX series of 10-element light-emitting-diode bar-graph arrays are used in systems with digital signals that are to be displayed in analog form. They are housed in standard dual in-line packages measuring 6.10 by 10.16 by 25.40 mm and feature an interlocking mechanism that facilitates end-stacking alignment.

The bar-graph arrays are available in standard red (the 4820), high-efficiency red (the 4830), and



yellow (the 4840). The latter two are useful where there are viewing problems due to high ambient light. All three have high segment-to-segment on-off contrast and segments measuring 1.52 by 5.08 mm.

In quantities of 1,000, the standard red display is priced at $2.25 in the U. S., the high-efficiency red at $2.75, and the yellow at $3.25.

Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [415]

Schottky process technology gives PROMs fast accessing

A new family of 4-K and 16-K programmable read-only memories offers fast access times as a result of advanced Schottky process technology employing highly reliable titanium-tungsten fuses. Initial test results indicate programming yields exceeding 95%. The 4-K family is available in both 512-by-8-bit and 1,024-by-4-bit versions with maximum address access times of 45 ns for the commercial versions, and 60 ns for the military parts.

The 4-K PROMs are available in 20- and 24-pin plastic or ceramic packages. The 20-pin, 512-by-8-bit device ranges from $8.60 in commercial-grade plastic (DM74S472/-473AN) to $14.35 for the DM54-S472/473AJ ceramic military part. The 1,024-by-4-bit plastic DM74-S572/573AN is $6.75, and $11.75 buys a military ceramic counterpart, the DM54S573/574A. The 24-pin commercial DM74S474/475A is $8.60, and the military DM54S-474/475A is $14.35.

The 16-K PROM is a 2,048-by-8-bit device having access times of 65 ns maximum for the commercial temperature range and 80 ns for the military range. Power dissipation is typically 600 mW. The plastic commercial version, DM87S190/191N, runs $28.25, and the DM77S190/-191J military version sells for $47.80. All prices are based on quantities of 100.

National Semiconductor, 2900 Semiconductor Drive, Santa Clara, Calif. 95051. Phone (408) 737-5000 [417]

Instruments

4½-digit meter joins family

Hand-held digital multimeter resolves 0.01 Ω and can characterize diodes

Data Precision Corp.'s model 945 digital multimeter is the firm's second portable 4½-digit DMM in less than a year, following hard on the heels of its model 255 [*Electronics*, Nov. 6, 1980, p. 169]. At 13 oz, the 945 is 8 oz lighter than the 255, and unlike the 255, it has a form factor that is common among hand-held DMMs. At 6.75 by 3.5 by 1.5 in., however, it displaces some 6½ in.^{3} more volume than the 255.

Both DMMs measure ac and dc current and voltage, as well as resistance. The 945, however, adds a 200-Ω full-scale range for 0.01-Ω resolution, plus the ability to characterize diodes and other components.

The diode-characterization feature uses the constant current sources in the 945 to help measure diode forward voltage drop at currents a decade apart from 100 nA to 1 mA, yielding a five-point curve. Active and passive components of other types may be characterized in a similar fashion.

The 945 takes 2.5 readings per second, registering them on its 0.43-in.-high liquid-crystal display, and indicates polarity automatically. Overload is indicated through a blinking display. Power is supplied by a 9-V alkaline battery that in normal use should last about 100 hours. When the battery weakens, the display reads "Lo bat." The unit can operate over a 0° to +40°C temperature range and in humidities as high as 80%.

The 945's specifications are comparable to those of the 255, and in a few cases, they compare favorably with the firm's 2480 benchtop DMM series. However, the new unit is aimed at low-frequency applications—typically below 1 kHz. Also, as is appropriate for a unit expected to ride in a tool kit, endure extremes of temperature, and generally lead a knock-about existence, some of its specifications are not as tight as those of its predecessors.

The 945 measures dc voltage over five ranges from 199.99 mV to 1,000.0 V full scale, with a resolution of from 10 μV to 100 mV. Long-term accuracy on its lower two ranges is typically ±(0.05% of input plus 1 or 2 counts). On the upper three ranges, the numbers are ±(0.07% of input plus one count).

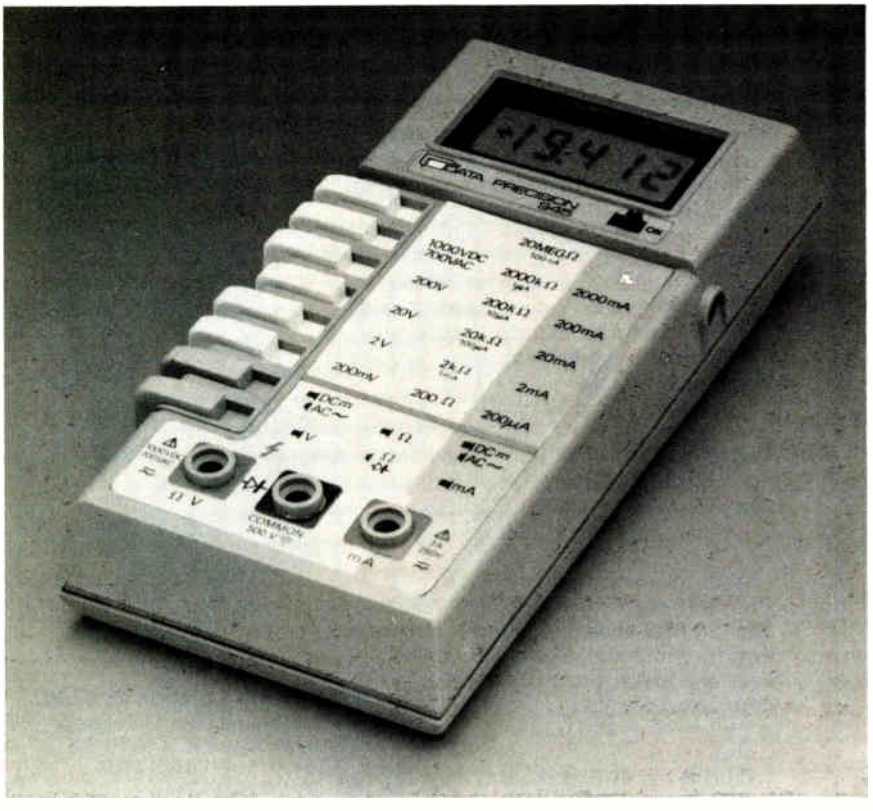
The 945's common-mode voltage rating is ±500 V dc or peak ac. Its common-mode rejection ratio is more than 120 dB at dc and exceeds 100 dB at 50 to 60 Hz. The normal-mode rejection ratio is more than 50 dB at 50 to 60 Hz; thus the 945's developers expect noise to be a minimal problem in dc-measurement situations.

The unit is capable of withstanding a full kilovolt of dc for 1 minute, even on its two lowest dc voltage ranges. Input impedance is 10 MΩ, in parallel with 100 pF.

Averaging. Ac voltage is measured over the same ranges, but the topmost range is limited to 700 V rather than 1,000. Accuracy varies with frequency and is highest in the 50-to-500-Hz region, ranging from ±(0.5% to 2.0% of input plus 3 counts). Ac measurement is average-sensing; the unit is not aimed at measurement of complex waveforms. Input-voltage maxima are 700 V rms (sine wave) on all ranges, 630 V dc on the two lowest ranges, and 1,000 V dc on the three upper ranges.

Resistance measurements are carried out over six ranges from 199.99 Ω to 19.999 MΩ full scale. Accuracy in the 200-Ω range is better than it might appear from its specifications; it is rated at ±(0.08% of full scale plus 10 counts) plus another 10 counts. Those extra counts are the result of fairly constant items such as contact resistance at the banana input plugs and lead resistance. Thus when the leads are shorted together, there will be a dependable offset of a few digits, and this number can be extracted from any measurement that requires maximum accuracy.

On other resistance ranges, accu-



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Circle 205 on reader service card

CA-006

New products

racy runs from ±(0.08% of full scale +2 counts) to ±(0.4% + 2 counts). Maximum fault voltage in the resistance mode is 250 V ac or dc.

Dc current is measured in five ranges from 199.99 μA to 1,999.9 mA full scale, for a resolution range of 10 nA to 100 μA. Long-term accuracy is typically ±(0.15% to 0.5% of input + 1 count).

The 945 can handle a maximum of 2 A and includes a 2-A, 250-V fuse. Nominal voltage burden is 200 mV full scale. Ac current ranges are the same as for dc; voltage burden and maximum current also are identical. Accuracy varies with frequency and is given as ±(1.2% to 0.5% of input plus 4 to 20 counts).

Standard equipment includes test leads, test-data certification, a certificate of conformance to standards established by the National Bureau of Standards, and a spare fuse. The price of the 945 in quantities of one to five is $265 each, with discounts available on larger quantities. Deliveries will begin late this month.

Data Precision Corp., a division of Analogic Corp., Electronics Avenue, Danvers, Mass. 01923. Phone (800) 343-8150 or, in Massachusetts, (800) 892-0528 [351]

Power-system recorders serve multiple purposes

Two recorders help reduce calculation work and reliance on costly single-purpose recorders in power survey applications. The Miniservo. III three-pen ac watt, volt-ampere–reactive, and demand integrator records combinations and integral measurements that are functions of two or more variables. It can record kilowatts; kilovolt-amperes reactive; kilowatt, kilovolt-ampere–reactive, and kilovolt-ampere demand; kilowatt and kilovolt-ampere–reactive hours; dc voltage and current; and power factor. Controls and jumpers select the parameters and assign pens to given variables.

The Miniservo III one-pen ac watt and volt-ampere–reactive recorder handles three-phase three- and four-wire; four-wire delta; and one-phase two- and three-wire measurements. Both use 115- or 230-V, 60-Hz power and have stepper-motor chart drives with speeds of 2, 5, 10, 15, 30, and 60 cm/h or cm/min.

The three-pen unit sells for $5,220, the other for $2,920. Delivery takes two or three weeks.

Esterline Angus Instrument Corp., P. O. Box 24000, Indianapolis, Ind. 46224. Phone (317) 244-7611 [357]

15-MHz portable scope has battery-pack option

Capable of operating from an ac line, external dc, or an optional internal battery pack, the model COS 3010-TW oscilloscope from Kikusui International Corp. has a bandwidth of dc to 15 MHz. Its normal sensitivity is 5 mV to 10 V/division in 11 steps, though that can be increased to 1 mV to 2 V/division with a 5× magnifier. Sweep time is 0.5 μs to 0.5 s/division. A 5× magnification will result in a sweep time of 0.1 μs/division.

Contained in a rugged compact aluminum housing to minimize external noise, the instrument measures 24.4 by 11.2 by 33.0 cm and weighs approximately 6 kg. It is modular in design and uses plug-in boards that can be changed easily in the event they become defective.

The model 3010 is available with two 10:1 probes, a plug for external dc power, a hood, and a shoulder bag and sells for $895. A nickel-cadmium rechargeable battery pack is available as a $100 option. The scope comes with a two-year warranty. Delivery is approximately 30 days after receipt of order.

Kikusui International Corp., a subsidiary of Kikusui Electronics Corp., 17121 South Central Avenue, Carson, Calif. 90746. Phone (213) 638-6107 [356]

Fast recorder uses CRT and fiber optics to expose paper

The 1808 high-resolution line-scan recorder uses ultraviolet light gener-

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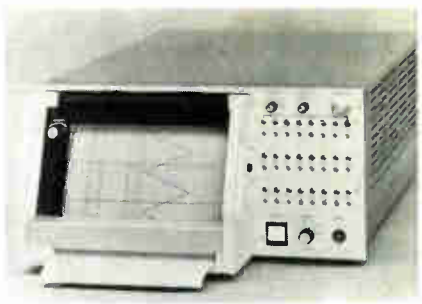


ated by a cathode-ray tube and directed by a fiber-optic faceplate to expose UV-sensitive paper moving at speeds of 5 to 500 mm/s. The recorder's modular design allows adaptation to specific requirements for such applications as multichannel analog recording, echocardiography, mapping, and video-image printout.

One of two available paper transports uses dry silver paper (3M type 8100 or equivalent) 6 or 8.5 in. wide and runs at 5 to 100 mm/s. The other uses direct-print oscillograph paper (Kodak 2022 or 1895) 6 or 8 in. wide, moving it at 5 to 500 mm/s. Time lines, grids, and a wide gray scale can be generated, and up to 24 analog input channels accommodated. The quiet-running 1808 is 8.75 in. high and can be rack-mounted. It sells for around $10,000, and delivery takes 90 days.

Honeywell Test Instruments Division, P. O. Box 5227, Denver, Colo. 80217. Phone (303) 771-0960 [353]

In-circuit digital tester contains expandable library

The Thalamus I dynamic in-circuit digital integrated-circuit tester, says its maker, can test most logic families—TTL, complementary-MOS, and emitter-coupled logic—as well as

microprocessors, memories, and peripheral devices. Testing is done at the full operating rate of the device under test (up to 5 MHz) and there is no need for programming by the user. The unit's self-contained library of device characteristics can be upgraded to cover new components and technologies; library data is called by keying in the generic part number of the device to be tested. Devices with from 14 to 40 pins are included in the digital tester's stored repertoire.

The 8085-based unit has a 40-character alphanumeric display to read out system mode, status, and responses to commands. A matrix of 40 light-emitting diodes monitors the activity of the pins of the DUT or shows which of them have failed in the fault-capture mode. The portable Thalamus I is intended for small or custom manufacturing facilities, repair depots, and field service; it is priced at about $35,000. Delivery is in 90 to 120 days.

Thalamus Electronics Inc., 1885 Sismet Rd., Unit 1, Mississauga, Ontario L4W 1W8, Canada [358]

3½-digit multimeter has 24 ranges, ½-in. LCD

The 3450 3½-digit hand-held multimeter has basic dc accuracy within 0.15% and costs $150. The 2-kΩ full-scale range has an audible tone output for continuity checking. The meter measures 3 by 5⅜ by 1⅜ in. and has a liquid-crystal display with digits ½ in. high. Its 9-V battery powers it typically for 500 hours; a low-battery annunciator on the display comes on when about 8 hours of battery life remain.

One rotating and one sliding switch select 0.2 to 1,000 V ac or dc full scale in five ranges, 2 to 2,000 mA ac or dc full scale in four ranges, or 200 Ω to 20 MΩ full scale in six ranges. The price covers clip leads, battery, manual, and one-year warranty. Carrying case, miniature-hook leads, and a clamp-on current sensor with shunt are optional.

Triplett Corp., One Triplett Dr., Bluffton, Ohio 45817. Phone (419) 358-5015 [360]

Microcomputers & systems

Module aids disk controller design

Small unit performs conversion from mfm to NRZ and back, plus address-mark functions

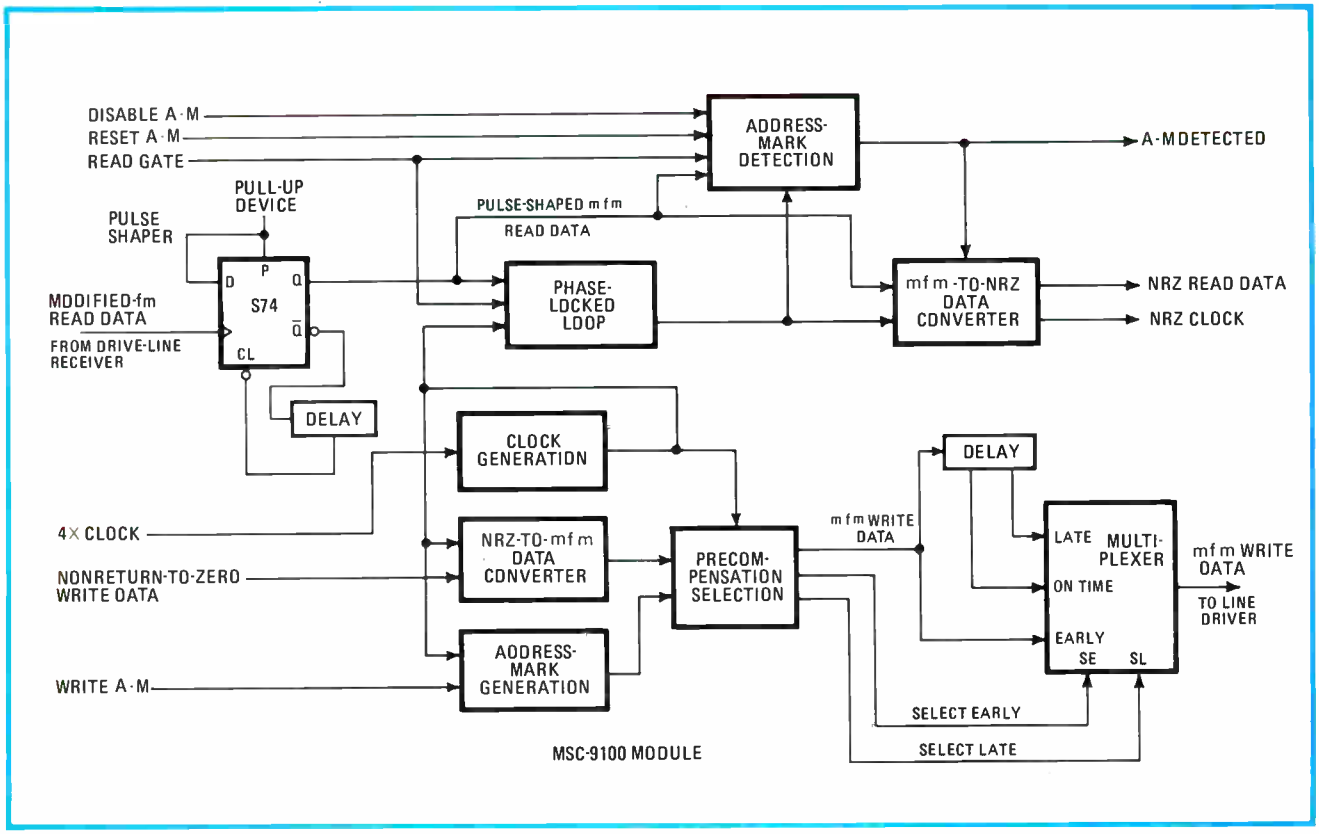
Although a great deal of effort has been put into the production of 5¼- and 8-in. Winchester disk drives, a similar effort has not been made in the design of their controllers. Controller board design often takes some six to nine months, and the result can cost more than the drive it is meant to control. The problems of controller board designers have been further exacerbated by the fact that, unlike IBM 3340-class drives and up the scale from there, the lower-cost units lack built-in data separators.

The functions of a data separator can be performed by a new module, the MSC-9100 from Microcomputer Systems Corp., with the aid of eight or fewer additional integrated circuits. The 9100 module contains such circuit blocks as a write-data converter, which puts modified-fm data in the nonreturn-to-zero (NRZ) format, and precompensation selection, which generates early, late, and on-time signals. It has an address-mark generation circuit, an address-mark detection circuit, and a read-data mfm-to-NRZ converter.

The 9100 lacks only the circuitry for a crystal clock, a read-data pulse-shaping circuit, a write-data precompensation delay circuit, and data-line drivers and receivers. It is designed to be used with the MSC-9000 module introduced last year [*Electronics*, March 24, 1981, p. 155]. The two modules, with the extra ICs mentioned, plus up to 12 more for the host interface, allow a designer to put together a controller less than 30 in.² in area. The Winchester drives it could serve include the Shugart Associates SA 1000 8-in. and the Seagate Technology ST 506 5¼-in. one, as well as others with compatible interfaces.

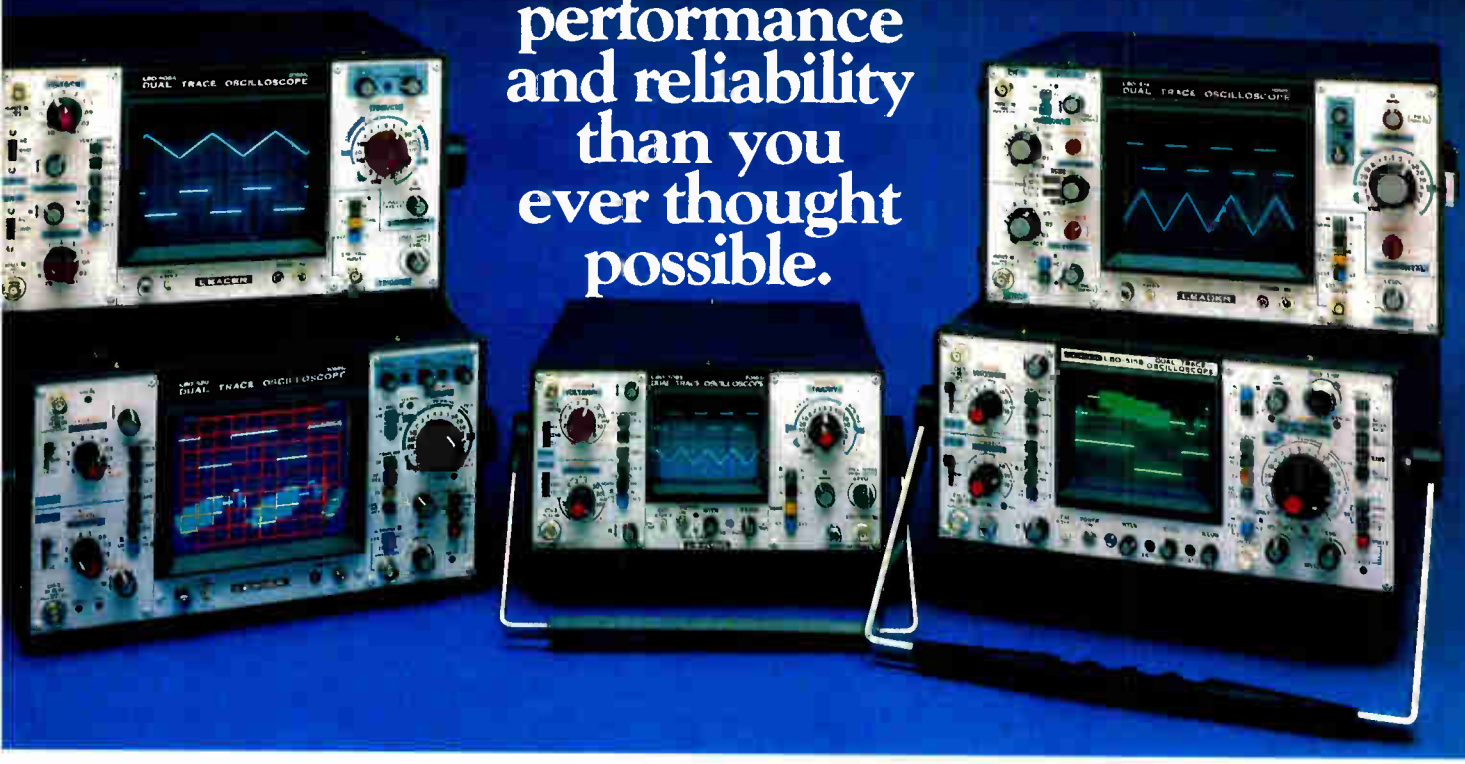
Quick-design centers. "What we are providing is a way to shorten design time, ensure repeatability, shrink the board, and lower costs," says MSC president Jim Toreson. He notes that part of the marketing strategy for the modules is to open up controller design centers at which MSC helps designers produce custom controller boards using the modules. "A person should be able to walk into one of these design centers and eight hours later walk out with a design," claims Toreson. MSC has already established one design center in Sunnyvale, Calif., and plans to open similar centers in Boston and Minnesota by year's end.

The MSC-9100 measures 3¼ by 3¼ in. Samples will be available this quarter, and volume production is scheduled by the end of the year. The price is expected to be under $100 in large quantities, making pos-



Data separator. Most of the functions of the data separator portion of a Winchester disk drive controller are handled by the MSC-9100 module from Microcomputer Systems Corp. About eight more ICs are needed for the delay circuits, multiplexer, line driver, and line receiver.

10 to 50 MHz oscilloscopes with more performance and reliability than you ever thought possible.



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50 MHz alternate time base–$1950.

LBO-517 gives you complex analysis capability with composite triggering

The LEADER LBO-517 with dome-mesh CRT displays bright, clearly defined traces at all sweep speeds and repetition rates.

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30 MHz delayed sweep–$1530.

LBO-515B is a dual trace oscilloscope using a 4-inch CRT with parallax-free internal graticule, 5 mV sensitivity, 120 ns signal delay, trigger hold-off, delayed sweep and x-y operation at full sensitivity.

35 MHz with signal delay–$1200.

The dual trace LBO-520A combines 10 ns rise time with 5 mV sensitivity and 120 ns signal delay lines. Has 5.6 kV PDA CRT with internal graticule.

20 MHz dual and single trace–$880, $625.

LBO-508A and LBO-507A have 17.5 ns rise time, X5 sweep magnifier, 10 mV/cm sensitivity and add/subtract modes.

10 MHz with 1 mV sensitivity–$695.

LBO-514 features both vertical and horizontal X5 magnifiers, 1 mV/cm sensitivity and sweep speeds to 0.1 µs/cm. (Single trace version, LBO-513, $535.)

20 MHz battery/ac portable–$975.

LBO-308S provides lab performance in field service applications. Dual trace, 2 mV sensitivity, 18 sweep divisions to 0.1 µs/div with X5 magnifier, and 3-inch rectangular, internal graticule CRT. Optional battery pack recharges during ac operation, $75.00.
LBO-308PL high performance version includes high intensity 10 kV CRT and signal delay lines. $1345.

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Circle 211 on reader service card

sible a $400 controller board.
Microcomputer Systems Corp., 432 Lakeside Dr., Sunnyvale, Calif. 94806. Phone (408) 733-4200 [371]

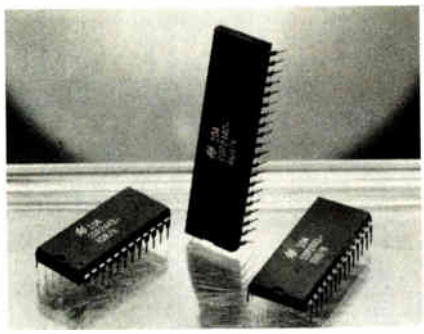
Multiuser system has 8-in. 10-megabyte Winchester drive

Altos Computer Systems has packaged its Z80-based single-board computer and direct-memory-access controller with a 10-megabyte, 8-in. Winchester disk drive for the small-business market. The ACS8000-10 system fits in a 19-in. rack and accommodates up to four users. It has 208-K bytes of random-access memory, six programmable serial ports, and an RS-432-C communications port. Network data rates of up to 800 kb/s are supported by the system.

Three types of back-up media are available for use with the 8000-10: single-sided (1-megabyte) or double-sided (2-megabyte) floppy-disk drives, or a 17.2-megabyte cassette-tape drive. Based on the CP/M and MP/M operating systems, the 8000-10 is compatible with a large body of applications software. Available now, with a single-sided or double-sided floppy-disk backup, it is priced at $8,500 or $9,500; with cassette backup the price is $10,990.
Altos Computer Systems, 2360 Bering Dr., San Jose, Calif. 95131. Phone (408) 946-6700 [375]

Two 4-bit microcontrollers work together on one chip

Two series of control-oriented processors are expanding National Semiconductor Corp.'s 4-bit microcomputer family. The COP2440 series represents a departure from the double-the-memory approach to microcontroller evolution: it contains two independent central processing units sharing read-only and random-access memory and input/output facilities. The two CPUs can work together, sharing data, or one CPU can off-load tasks to the other.



The COP440 series has single-CPU versions of the COP2440 series. Fabricated with n-channel silicon-gate technology, they provide a 4-μs instruction execution time. Features include multivectored interrupts from four selectable sources (plus restart), a four-level subroutine stack, a programmable time-base counter for real-time processing, an internal counter-register, and Microwire-compatible serial I/O. Versions in 40-, 28-, and 24-pin dual in-line packages will be available in the fourth quarter of 1981. In volume, COP2442 and COP440 microcontrollers are priced at under $5 and $4, respectively.
National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 737-5000 [373]

IEEE-488 interface card lets Apple control instruments

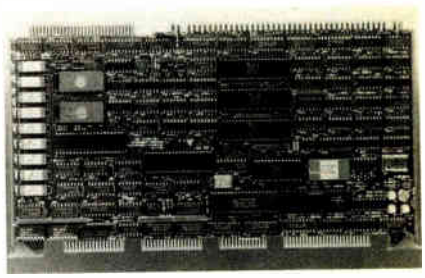
With an IEEE-488 interface card, over 1,400 instruments used in scientific and technical applications can be linked to and controlled by Apple II and Apple II Plus computers. The interface package includes a cable connecting the card to a standard IEEE-488 female connector. The Apple II accepts three such cards. This back-panel connector makes it possible to connect the bus shield to the Apple's case ground. A comprehensive manual gives detailed instructions for developing Basic programs to control the bus. The Apple IEEE-488 interface card can function as a controller or can interface with devices to be controlled by the IEEE-488 bus, the company says. The card is priced at less than $500 and is available from stock.
Apple Computer Inc., 10260 Bandley Dr., Cupertino, Calif. 95014. Phone (408) 996-1010 [376]

Small system supports five users with 5¼-in. Winchester

The new 5005 multishare system from Vector Graphic allows up to five workers to simultaneously perform word and data processing. The Z80-based system is configured with a 5-megabyte, 5¼-in. Winchester disk drive, a 630-K-byte floppy-disk drive, and a sophisticated error-correcting disk controller. The system can support up to five video display terminals and two printers, one with a serial interface, and another with a parallel interface. The basic system with one terminal runs $8,995; additional terminals are $1,895 each. The software provided includes the CP/M-2 operating system, Scope editor, Raid debugger, ZSM assembler, and Microsoft Basic 80. Among optional software are the Peachtree business accounting office software, the Memorite III word-processing software, and the ExecuPlan financial planning package. The first deliveries are slated for the end of June.
Vector Graphic Inc., 31364 Via Colinas, Westlake Village, Calif. 91362. Phone (213) 991-2302 [374]

Pascal development system for CP/M work is fast

The PDS-80 Pascal development system for CP/M applications has a cache memory system that increases execution speed by up to four times,



Our no-nonsense, low-cost circuit protector does double duty as an on-off switch, and sheds a little light on cost-cutting, too.

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Heinemann puts an end to fiddling with fuses, and to the ugly-red-button syndrome of conventional circuit protection. Now, add style as well as sensible protection when you design in our new Series TX—the circuit protector that looks good enough to stay up front, and doubles as an on-off switch.

All with no hardware, for quick installation in a single panel opening.

Think about it. It probably costs less than you're already paying for the ho-hum, fuss-and-bother of the old way. Miles less if you add in inventory hassle and production time.

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With current ratings from 2 to 20 amperes and your option of single-pole or two-pole configurations, Series TX from Heinemann cuts into your overheadaches by cutting straight into design complexity. Each pole in the two-pole TX can have a separate rating, so you can even protect an ac circuit and a dc circuit at the same time. And you stock only one component, install only one component.

Heinemann announces the end of ho-hum, high-hassle circuit protection.

Then, the optional light in the rocker has separate, isolated terminals. You can indicate power-on, or anything else—system-ready, hold, clear—any function you want.

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Circle 213 on reader service card 7387

New products

according to the manufacturer. The cache system makes use of the direct-memory-access and interrupt capabilities of Intersystems Series II disk controllers and memory boards to buffer whole tracks from the disks, reducing input/output.

The single-user S-100 system utilizes Intersystems Pascal/Z, a Z80 native code compiler generating reentrant object code that can be stored in read-only memory. Pascal/Z generates relocatable object modules permitting separate compilation; its programs run 5 to 10 times faster than identical code run under P-code interpreters, says the firm.

One of the three available mainframes for the PDS-80 has a front panel whose switches and displays allow the user to examine or change data in memory, set breakpoints, and single- or slow-step through programs, permitting both hardware and software development. Furnished with two 8-in. floppy-disk drives storing 2.4 megabytes, CP/M, Pascal/Z, and five utilities, the development system is priced at $7,995.

Ithaca Intersystems Inc., 1650 Hanshaw Rd., Ithaca. N. Y. 14850. Phone (607) 257-0190 [377]

Controller board doubles computer's disk capacity

A floppy-disk controller board compatible with the Heath 88/89 microcomputer allows users to double their 5¼-in. disk storage without adding drives by converting the Heath's hard-sectored drives to standard double-density soft-sectored formatting.

The FDC-88OH board runs under the CP/M 2.2 operating system and is capable of handling up to four Shugart-compatible 5¼- or 8-in. single- or double-sided floppy-disk drives simultaneously at either single or double density. The FDC-88OH, including 10-ft cable, programmable read-only memory containing zero-origin-conversion firmware, boot PROM with drive diagnostics, and manuals is priced at $695, with

delivery in approximately 30 days.
Controlled Data Recording Systems Inc., 7667 Vickers Street, Suite C, San Diego, Calif. 92111. Phone (714) 275-1272. [378]

Board interprets Tiny Basic, controls up to 128 slaves

The K-8073 board, based on National Semiconductor's INS8073 Tiny Basic microinterpreter central processing unit, is intended for engineers without software experience. The stand-alone computer communicates via an on-board RS-232-C connector at 110 to 4,800 b/s and has a modified STD-bus structure. It has a cassette tape port, 24 bidirectional input/output lines, a real-time clock, 1-K bytes of random-access memory, and an asynchronous receiver-transmitter for single-wire remote control of, or retrieval of data from, 128 slave devices. The card's price with development utility firmware is $388; delivery is from stock.
Transwave Corp., Cedar Valley, Road 1, Box 489, Vanderbilt, Pa. 15486 [379]

GenRad offers entry-level 8-bit development systems

A series of entry-level upgradable development systems supports work with the 8080, 8085, Z80, 6800, and 6802. The systems are upward-compatible with 2302 slave emulation systems and GenRad's cluster networks. A $17,950 package includes a cathode-ray tube, keyboard, the selected central-processing unit, 64-K bytes of static random-access memory, an in-circuit emulator and logic analyzer, a 1-megabyte dual-drive floppy-disk unit, and programmers for programmable read-only memory. Software includes an editor, macroassembler, linker, and debugger. Modules can upgrade the system to support 16-bit processors. A selection of cross compilers, Pascal, and S-Basic are offered.
GenRad, Development Systems Division, 5730 Buckingham Pkwy., Culver City, Calif. 90230. Phone (213) 641-7200 [380]

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Circle 216 on reader service card

Data acquisition

D-a converters are fast, cheap

Two digital-to-analog chips have maximum settling times of 250 and 350 nanoseconds

Aiming for the lead positions in the price-performance race among 12-bit monolithic digital-to-analog converters are the AD565A and AD566A from Analog Devices Inc. The AD565A, which typically settles to within ±½ least significant bit in 150 ns, outruns all the competition in this class, asserts David W. Kress, manager of new products marketing at the firm's Semiconductor division. The companion AD566A d-a converter has a typical settling time of 250 ns to ±½ LSB. The maximum settling times for the AD565A and AD566A are 250 and 350 ns, respectively.

"While their speeds will give these d-a converters applications in specialized areas like high-speed display drivers and fast analog-to-digital converters, their very low prices will make them strong in general-purpose applications as well," Kress maintains. In 100-unit lots, the AD565A's five models range from $15.95 to $95, and the AD566A's from $12.95 to $85. Processing to MIL STD 883B also is available, costing $115 for the AD565A and $99 for the AD566A.

The two converters accept TTL and 5-V complementary-MOS logic inputs. They come in both commercial models operating from 0° to +70°C, and in military-grade versions that operate from −55° to +125°C. High-end models in each temperature-range category have a maximum linearity error of ±¼ LSB and a differential nonlinearity of ±½ LSB maximum. Linearity error and differential nonlinearity in the lower-end models are a maximum of ±½ LSB and ±¾ LSB, respectively. All models are guaranteed to be monotonic over their full operating temperatures.

The AD565A has a typical full-scale gain-temperature coefficient of either 10 or 15 ppm/°C, depending on model; typical for the AD566A is either 2 or 7 ppm/°C. The AD565A operates off dual power-supply voltages from 11.4 to 16.5 V dc; its maximum power dissipation is 345 mW. The AD565A, which has the same power-supply–voltage requirements, dissipates a maximum of 300 mW.

Deliveries of the AD565A and AD566A are from stock.

Analog Devices Inc., Route 1 Industrial Park, P. O. Box 280, Norwood, Mass. 02062. Phone (617) 329-4700 [381]

16-bit hybrid a-d unit converts in 50 μs

The ADC72 16-bit hybrid analog-to-digital converter features a maximum linearity error of ±0.003% of full scale and a conversion time of 50 μs maximum. The TTL-compatible successive-approximation unit carries an internal clock, a comparator, reference, and laser-trimmed thin-film resistors. It can be programmed to have one of six input ranges. Four versions of the converter, which is housed in a 32-pin hermetic metal package, are available. Operating over the −25° to +85°C range, the ADC72AM has a maximum nonlinearity of ±0.006% of full scale and is priced at $219 in lots of 100; the ADC72BM, with a ±0.003% nonlinearity specification, is priced at $237 in quantities of 100. For operation from 0° to +70°C, the ADC72JM, with ±0.006% maximum nonlinearity, is priced at $184 in 100-unit lots, and the ADC72KM, with ±0.003% maximum nonlinearity is $213 in like quantities. For small quantities, delivery is from stock.

Burr-Brown Research Corp., P. O. Box 11400, Tucson, Ariz. 85734. [383]

Converter emits sine and cosine of digital input angle

The DTG5126 digital trigonometric (vector) generator, a 16-bit, four-quadrant converter, accepts a digital input of up to 16 bits (complementary-MOS– and TTL-compatible) and multiplies it with an analog voltage to generate the products of the analog-input voltage and both the sine and cosine of the digital input angle. Specifications include 2-arc-minute accuracy, a 0.03% radius accuracy, a 5-ppm/°C temperature coefficient of scale, and an offset drift of 25 μV/°C. The modular unit slews at 2.5 V/μs and has a step response (10 V or 90°) of 10 μs to within 0.1% of final value. It has industry-standard pinouts in its 12- and 14-bit modes. An internal reference is offered as an option (5 or 10 V dc); the analog interface is a buffer amplifier. The power supply requirements are ±15 V at ±30 mA. For lots of 1 to 9, the unit price is $345, with delivery in six weeks.

Natel Engineering Co., 8954 Mason Ave., Canoga Park, Calif. 91306 [386]

Acquisition system's modular design allows easy expansion

The Dual 77B, a complete turnkey data-acquisition, -logger, and -control system, consists of a computer with 64-K bytes of memory, dual floppy-disk drives, a 32-channel analog-to-digital converter, and 4-channel digital-to-analog converter outputs for control applications. The a-d channels may be expanded to several hundred inputs as needed. The d-a channels are also expandable for experiment or process control using

New products

plug-in modules. Other expansion modules include a fast printer, random-access memory, and disk storage. The 77B system has diagnostics, a CP/M operating system, and an extended Basic language. (Fortran, C, Pascal, and Forth are optional.) A complete system is available starting below $10,000. Delivery is from stock.

Dual Systems Control Corp., 1825 Eastshore Highway, Berkeley, Calif. 94710. Phone (415)549-3854 [387]

D-a converter attenuates signal in 1.5-dB steps

The AD7118 Logdac d-a converter attenuates analog signals in 1.5-dB steps under control of a 6-bit digital input code. Providing attenuation from 0 to 85.5 dB with guaranteed monotonicity, a total harmonic distortion of −85 dB, and intermodulation distortion of −79 dB, the AD7118 draws as little as 2.5 mW from a single +5- to +15-V power supply. It is available in a 14-pin plastic dual in-line package for operation over the 0 to +70°C temperature range (KN and LN grades) or a 14-pin ceramic dual in-line package for use over the −25° to +85°C range (BD and CD grades) and the −55°C to +125°C range (TD and UD grades). All ceramic versions available are processed to MIL-STD-883B. Pricing in units of 100 begins at $7.95 for plastic and at $10 for ceramic models, with delivery from stock.

Analog Devices, Rte. 1 Industrial Park, P. O. Box 280, Norwood, Mass. 02062. Phone (617)329-4700 [385]

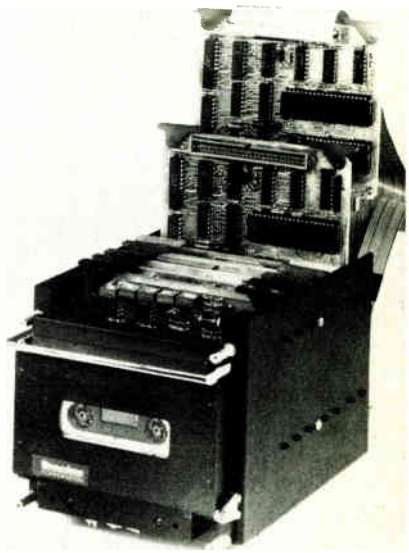
Real-time acquisition system offers 85 I/O-board options

Incorporating the ANDS5400 data-acquisition system with the ANDS7000 controller and software, the Focus 5000 Fortran-controllable universal system is an economical real-time data-acquisition system. Designed to meet the most stringent accuracy requirements for gathering, manipulating, and transmitting analog and digital data, it can accommodate over 1,000 input/output channels. It performs over 100,000 measurements/second, has an accuracy of up to 16 bits, and is very flexible: over 85 types of analog and digital I/O boards are provided. Other components of the Focus 5000 are a dual double-density floppy-disk drive, 12-in. cathode-ray tube, floating-point math package, and programmable I/O interface capable of direct memory access in the ANDS5400. Programmable in Fortran, the Focus system implements Analib, a sophisticated and flexible subroutine-calling package. The Focus 5000 is priced at $22,900 and delivery is within 60 days.

Analogic Corp., Audubon Road, Wakefield, Mass. 01880. Phone (617)246-0300 [388]

Acquisition system samples 8 analog inputs simultaneously

Based on the Z80 microprocessor, the M80/DAS data-acquisition, -processing, and -storage system accepts up to eight analog inputs with simultaneous sampling. The system uses one converter for each channel and multiplexes digitally to



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The future has arrived for automatic test equipment with the introduction of the new IE Series 4000... the ultimate computer-controlled test systems of the '80s. And they've arrived just in time, in view of the rapidly expanding complexity of electronic systems and circuits.

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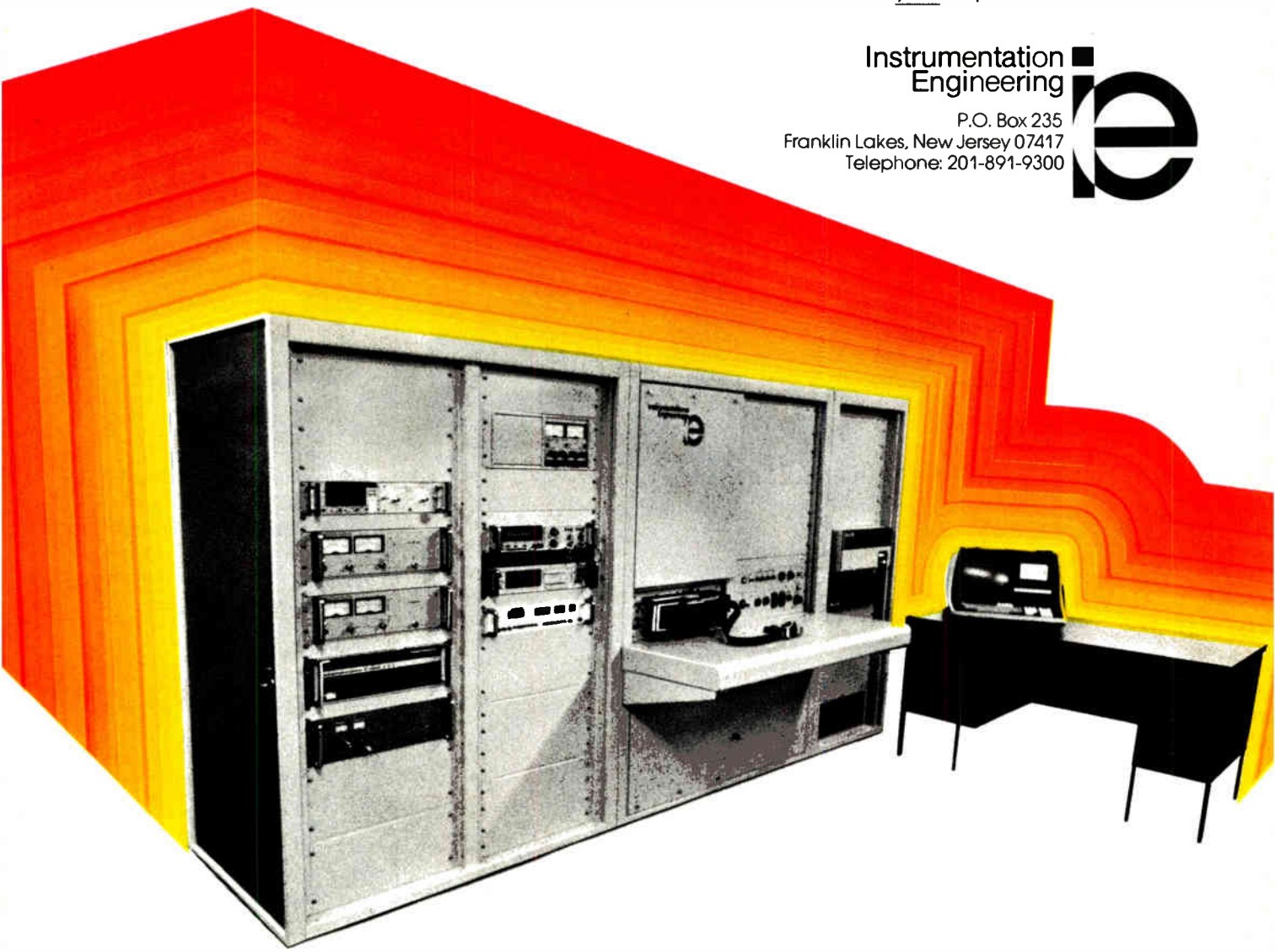


prevent degradation and skewing of data from analog multiplexing. The voltage inputs are differential with selectable ranges of ±500 mV to ±5 V; input impedance is greater than 20 MΩ. Conversion is done by the dual-slope technique to reduce 60-Hz pickup and guarantee monotonicity. Resolution is to 13 bits, including overrange indication. Storage is on Philips cassettes in ANSI/ECMA formatted tapes. Each unit runs $2,535 for eight-channel systems, and $2,190 for four-channel systems. Delivery is in four weeks.

Memodyne Corp., 220 Reservoir St., Needham Heights, Mass. 02194. Phone (617) 444-7000 [389]

Modular scalers count pulses at up to 100 MHz

A family of multichannel latching scalers allows flexible configuration of modular scaling systems. The scalers can count pulses at 100 MHz, transferring scaler values directly to a computer or storing them in local memory. Dead time of only 100 ns is obtained by latching the values in internal registers; inputs compatible with TTL and emitter-coupled logic allow operation with most pulse-generating instruments, such as discriminators.

The 8590 and 8591 each have eight 16-bit scalers with parallel latches; the 8591 has separate stops and the 8590 uses one common stop for all channels. The 8594 has four 32-bit scalers and a common stop. The 8591 is $1,900 and the others cost $1,650 each. Delivery is within eight weeks of receipt of order.

LeCroy Research Systems of California, 1806 Embarcadero Rd., Palo Alto, Calif. 94303. Phone (415) 856-1800 [344]

Two-chip d-a converter has 18-bit accuracy, resolution

The MP370 two-chip multiplying digital-to-analog converter achieves a 16-bit integral linearity (within ±0.0008%) and differential linearity within ±0.0004%. It provides 18-bit resolution and accuracy through dynamic laser trimming of resistors. The unit is compatible with both TTL and complementary-MOS and runs on a single 15-V supply, using less than 60 mW. It settles in 2 μs and has a scale-factor drift of ±1 ppm/°C.

The part's housing is a 28-pin metal package. The MP370B, for duty over military temperatures, is priced at $600 in lots of 25 to 99; in like quantities, the commercial MP370C runs $180. Delivery is in four weeks or from stock from any Micro Power Systems distributor.

Micro Power Systems Inc., 3100 Alfred St., Santa Clara, Calif. 95050 [345]

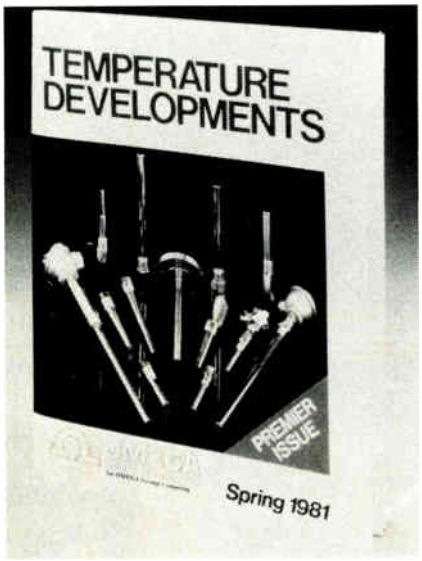
New literature

6809 microcomputer experiments. Programming and interfacing with the 6809 microcomputer are the subject of a 270-page book by Andrew C. Staugaard called "6809 Microcomputer Programming and Interfacing with Experiments." It stresses the 19 addressing modes needed to understand the software concepts that make the 6809 a powerful microprocessor and one that is particularly useful with high-level languages (Pascal, Fortran, Basic, and Cobol). The book, the third title in the Blacksburg Continuing Education series, is priced at $13.95 plus $1.00 shipping and handling; Visa and MasterCards are accepted. Order book No. 21798 from Group Technology Ltd., P. O. Box 87, Check, Va. 24072, or phone (703) 651-3153. Circle reader service number 421.

Electronic test equipment. Complete information on test instruments from North American Philips Corp. can be found in the 1981 Philips Test & Measuring Instruments Inc. 122-page catalog. It includes such new products as the PM3542 and PM3543 logic analyzers; the PM3264, a four-channel, 100-MHz oscilloscope; and the PM3310 digital storage oscilloscope, a 50-megahertz unit with 8-bit resolution. U. S. and foreign sales offices are also given. For more information (or the catalog), contact Philips Test & Measuring Instruments Inc., 85 McKee Dr., Mahwah, N. J. 07430, at (800) 631-7172. [422]

McFadden's activities. McFadden Newsletter is a new quarterly publication focusing on the activities of the company. It describes its products, their applications, and the use of force-control loading systems. Developments in process as well as notices of trade show exhibits and demonstration schedules are highlighted. The first volume features the McFadden autopilot tester, business jet control loader, and start/stop interlock controller. Free subscriptions are available from Sandra Barton, McFadden Electronics Co., 8956 Atlantic Ave., South Gate, Calif. 90280, at (213) 564-3958. [423]

Temperature developments. Temperature Developments is a quarterly publication in which Omega Engineering Inc. reports on its latest innovations in measuring and controlling temperature. Each issue will feature a technical article with photographs on the latest additions to Omega's product line. The first one highlights the use of thermowells and discusses such products as hand-held digital pyrometers for thermocouples, thermistors, and resistive



temperature detectors; solid-state relays for thermocouple controllers; retractable color-coded thermocouple cables; and high-temperature thermocouples. For a free copy, or to be placed on a complimentary mailing list, contact Omega Engineering Inc., 1 Omega Dr., Box 4047, Stamford, Conn. 06907. [424]

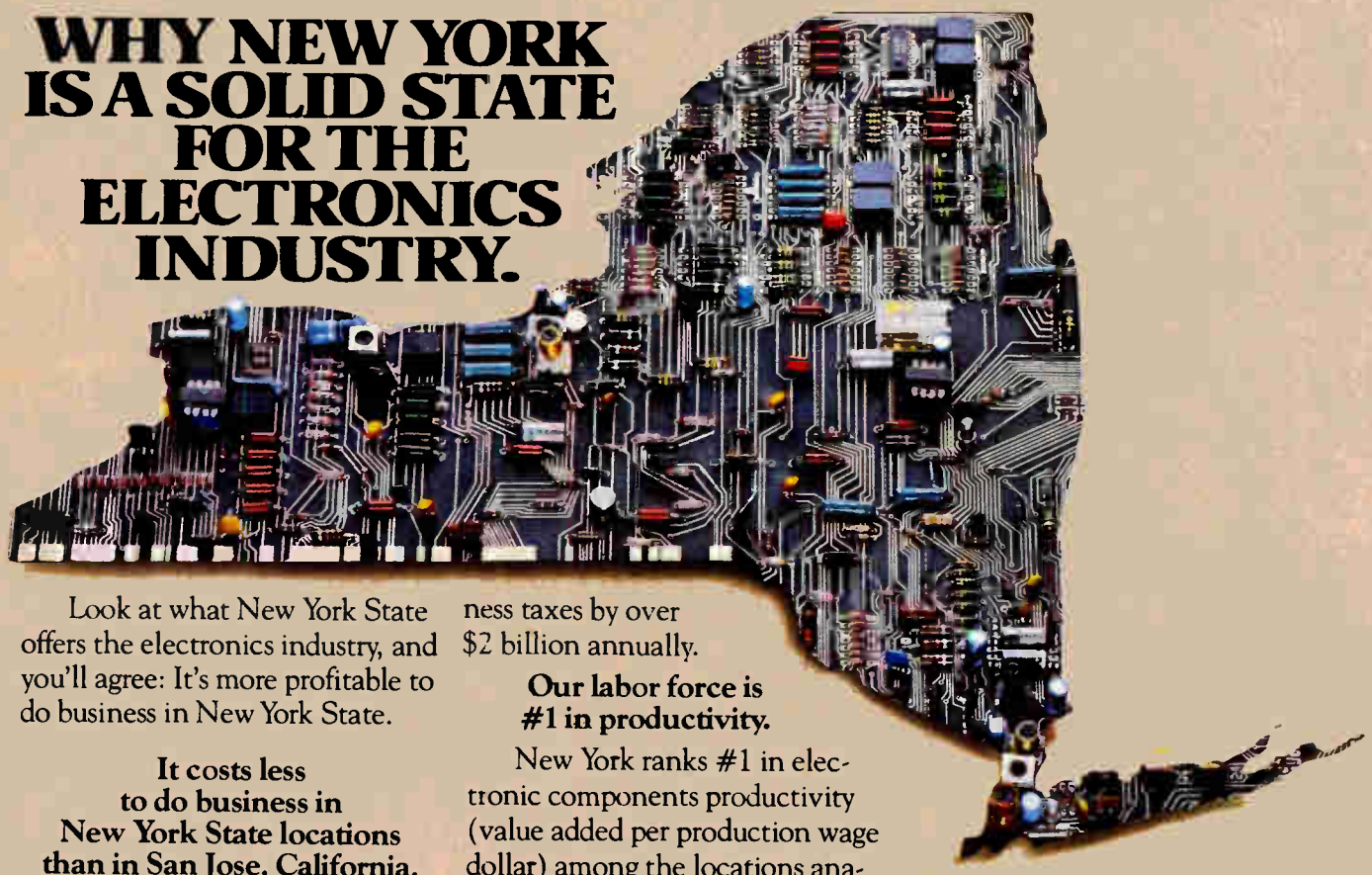
Crystal technology. A 16-page color catalog describes Piezo Crystal Co.'s product line. Included in the catalog is information on high-stability and double-rotated crystals for oscillators, mobile and hand-held communication devices, radar, telephones, television, telemetry, satellites, and other uses. Products cover the frequency range of 1 kHz to 250 MHz over a temperature range of −55° to +150°C. Also included are performance curves, a design guide, illustrations of typical holders, and a specification checklist for crystals and oscillators. For a copy, write to Piezo Crystal Co., 100 K Street, P. O. Box 619, Carlisle, Pa. 17013. [425]

Power transistor voltage ratings. "Power Transistor Voltage Ratings and RBSOA Curve" is the title of a 16-page application report discussing experiments that reveal how measured power-transistor voltage characteristics and the verified reverse-bias safe operating area relate to a device's high-voltage switching capability. Test experiments included in the report are the commutating switch test, unclamped inductive-

load–energy test, clamped inductive-test method, breakdown-voltage test, and the RBSOA test. Standard techniques for transistor voltage rating are also discussed. Report SCA-202 is available from Texas Instruments Inc., Central Literature Response Center, P. O. Box 202129, Dallas, Texas 75220. [426]

Semiconductor devices. Complete product descriptions and specifications on n- and p-channel devices and quad arrays are contained in the 270-page "VMOS Data Book." A 15-page cross-reference index to existing industry types available is provided and an explanation of Ferranti's latest power MOS field-effect-transistor process technology is given. The data book is fully illustrated with schematics, cross sections of various MOS FET structures, graphs, and package outlines. For additional information, contact Ferranti Electric Inc., Semiconductor Products, 87 Modular Ave., Commack, N. Y. 11725, at (516) 543-0200. [427]

WHY NEW YORK IS A SOLID STATE FOR THE ELECTRONICS INDUSTRY.



Look at what New York State offers the electronics industry, and you'll agree: It's more profitable to do business in New York State.

It costs less to do business in New York State locations than in San Jose, California. And we can prove it.

An independent study analyzed the four critical costs of taxes, wages, power and construction for a model new electronics firm. It showed that New York State offers locations where these costs are less than they are for choice electronics industry locations around the country.

For example, these costs would total $7.6 million annually in San Jose, versus only $6.4 million in, say, Brookhaven, New York.

New York has the best business advantages in America.

New York State is committed to a big, broad business-boosting program to create private sector jobs.

Our costs are lower because we have the best tax incentives and credits. We have on-the-job training and job incentive programs. Long-term, low-cost financing. And, we've cut personal and business taxes by over $2 billion annually.

Our labor force is #1 in productivity.

New York ranks #1 in electronic components productivity (value added per production wage dollar) among the locations analyzed. And in the past five years, New York's number of idle man-days due to work stoppages was half that of the national average.

We graduate more electronics engineers than any other state.

Thanks to universities like RPI and Cornell–and dozens of other fine colleges and universities–more electronics engineers are graduated each year in New York State than in any other state including California or Massachusetts. And since many of the largest electronics firms are already doing business here–GE, IBM, to name only a couple–our graduates are quickly turned into seasoned professionals.

When you look into New York, you'll love New York.

We have an abundance of electric power. Lots of affordable housing for your employees. And our 30 million acres include thousands of available plant sites. And some of the most magnificent outdoors and year-round recreation on the American continent.

Tell me more about why New York is a solid state for business. I am particularly interested in information on:

- ☐ Electronic Components
- ☐ Small Computers
- ☐ Semiconductors

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Circle 223 on reader service card

Now, Racal-Vadic has invisible dual and triple modems.

They're packaged inside TEXAS INSTRUMENTS' *Silent 700** 780 Series Data Terminals.

In the beginning...

When Texas Instruments designed the 780 Series of 120 character-per-second data terminals, Racal-Vadic was asked to solve a difficult engineering and packaging problem.

The requirement was for modems on a PC card that would operate full duplex at both 1200 & 300 bps; be compatible with Racal-Vadic's VA3400 and Bell 212A & 103 type modems; operate as a direct-connect modem or as an acoustic coupler; yet be small enough to fit inside TI's portable data terminals. An incredibly tough problem. But Racal-Vadic solved it.

Today...

Texas Instruments' Model 785 Portable Data Terminal includes a micro-processor controlled DUAL originate-only, acoustically coupled modem that operates at 1200 & 300 bps full duplex, and is compatible with Racal-Vadic's VA3400 & Bell's 103.

The modem for the TI Model 787 Portable Communications Data Terminal presented an even tougher challenge. The result is a full originate/answer TRIPLE modem that is direct-connect to the switched network (with an acoustic coupler option), and is compatible with Bell's 212A, 103, and Racal-Vadic's 3400 Series.

A truly universal modem packaged on a single PC board.

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Products Newsletter

Wafer flatness tester sorts automatically

Tencor Instruments of Mountain View, Calif., has built an automated version of its Flatgrade wafer and photomask flatness tester, adding a **cassette-to-cassette handling and sorting subsystem.** The new tester has software that can sort wafers on a pass/fail basis using several parameters, including focal-plane deviation limits and offset and percentage of usable area. The Flatgrade accepts wafers ranging in size from 3 to 5 in. and prompts the operator by way of a cathode-ray-tube display. The automated version, with RS-232-C interface, is priced at $81,900.

Houston Instrument offers six-pen plotter

A six-pen option is available for the DMP series of plotters from Houston Instrument of Austin, Texas. The option lets the user produce **graphs or charts in black, red, blue, green, violet, and orange** (brown is optional), completely under program control. This enhancement can also be retrofitted to any of the Hi Plot series of low-cost plotters. With the addition of the $395 six-pen option, the DMP series is the only line of multicolor plotters starting under $1,500. The user can install the option on any DMP-2, -3, or -4; DMP-5, -6, and -7 models must be returned to the factory for updating. The charge is $100 plus shipping.

Printer controllers interface non-IBM printers to IBM 3270

In an effort to broaden the IBM user's choice of printers, Agile Corp. of Sunnyvale, Calif., has introduced a printer controller that can interface non-IBM compatible printers with the IBM 3270 series equipment. Agile's model 5287 line of printer controllers **can handle Centronics parallel protocols, Diablo type 2 printers, and 19.2-kb/s RS-232-C serial printers** with a specifiable protocol. The $3,000 model 5287 plugs into an IBM 3274 or 3276 control unit and appears to these units as a category A device. It includes a 3,440-character buffer and uses EBCDIC or logical-unit-interface codes. A version of the 5287 for original-equipment manufacturers, the single-board 6287 ($1,000), is also available.

National hits stride in NSC800 production

National Semiconductor Corp. of Santa Clara, Calif., has begun volume production of its NSC800 family of microprocessors and support circuits, which are manufactured with National's double-polysilicon complementary-MOS process (P^2C-MOS). Executing the Z80 instruction set, the central processing unit dissipates only 50 mW at 5 V when operating at 2.5 MHz. The line includes the 2.5-MHz NSC800, priced at $134, and two slower versions, the NSC800-2 (2 MHz) and -1 (1 MHz) at $114 and $87, respectively. Pricing is for 100-piece quantities, and delivery is from stock to eight weeks. The firm has also begun volume production on several new small- and medium-scale integrated logic devices, designated the MM74PCXX/82PCXX series. In addition, it announced **a 28% drop in the prices of its medium-sized programmable array logic—the DMPAL16L8, -R8, and -R4—from $25 to $18.50 in hundreds.**

10-MHz 68000 offered by Motorola

Motorola Semiconductor Group of Austin, Texas, has introduced a 10-MHz MC68000L10. Designers requiring a 68000 faster than the current 8-MHz microprocessor will gain 25% in throughput with the 10-MHz version. The fast microprocessor **is the result of Motorola's program for yield enhancement.** Samples are now available for $449 each.

EE salaries average $39.9K

Electronics and aerospace engineers place in the middle in median salaries among engineering disciplines, according to results of the 15th National Compensation Survey conducted by the National Society of Professional Engineers. NSPE's breakdown for 15 branches of engineering ranks EEs and aerospace engineers eighth and seventh, with median earnings of $36,000 and $36,400, respectively. Their average salaries are $39,900 and $38,700, respectively.

Petroleum and mining engineers take home the biggest paychecks by far (see table). In terms of median income, safety engineers rank last, with environmental, pollution control, and sanitary engineers running a little bit ahead. The draft report being readied for printing by the NSPE (2029 K St., N. W., Washington, D. C.) lists salaries for all engineers by disciplines, industries, job functions, levels of education and experience, and geographic regions, as well as major cities.

Overall, inflation outpaced income gains for engineers last year. An annual median income of $35,000 represented an 11.4% increase in the 15 months since the preceding survey, whereas the Consumer Price Index rose 15.6% in the same period. During 1980 the median base salary increase was 9%.

Poor payers. When salaries are broken down by industrial and nonindustrial categories, instead of disciplines, the salary levels display a different pattern. Engineers working for electrical and electronic equipment makers rank seventh in 12 industry categories, with average and median salaries of $40,624 and $36,000, respectively, while engineers employed by aeronautical and aerospace equipment makers rank near the bottom of the list, with average and median salaries of $36,714 and $36,000, respectively. These industry categories could be misleading, however, because the NSPE figures cover all types of engineers employed in that industry.

Money paid by employers not in manufacturing to all engineers offers another measure for EEs. The average/median salaries for research organizations and laboratories, for example, are $40,460/$35,000, while the communications services pay $40,171/$36,400. As for colleges and universities, they pay $37,690/$36,246, or just about the same as the Federal government, including the armed forces, at $37,074/$35,365. State and local government engineering, however, pays much lower salaries, with average annual incomes hovering around $30,000.

The NSPE's breakdown for all engineers by job function is also of interest. As expected, executive and administrative assignments lead the average/median salary list at $51,269/$42,000. However, a design engineer is the lowest-paid at $32,507/$30,374. Not much better off are quality control, production, and maintenance engineers, at $33,775/$31,800. Research and development jobs are worth $36,451/$35,000, but sales or marketing positions are better paid at $44,368/$37,950.

Regional differences. Geographically, the NSPE data generated no surprises, showing that the highest median incomes for engineers are in the Northeast ($37,500) and on the West Coast ($37,033). As for metropolitan areas, Houston ranks first in median income, followed by New York City and the Los Angeles/Long Beach/San Diego area. A statistic of possible interest to manufacturers looking for potential plant sites shows that Memphis, Tenn., has the lowest median salary of all of the 29 population centers surveyed, followed by Columbus, Ohio; San Antonio, Texas; and Cleveland, Ohio.

As far as organization size goes, NSPE found no general trends. Pay differentials between small and large organizations were slight. Not surprisingly, the NSPE results show median salaries are higher for engineers with doctorates ($41,500) than for those with a bachelor's of science ($34,400).

The NSPE survey was designed, conducted and prepared by Steven Langer, managing consultant of Abbott, Langer & Associates, a Chicago-based consultant firm in personnel management and industrial psychology. The questionnaire, mailed to 66,789 NSPE members in January, produced a response of 19,297, or 29%, by the March 11 cut-off date. Of these, 17,993 were considered usable. Respondents were asked to report their annual base salary from their primary employer as of Jan. 1, plus additional cash income from the employer, excluding overtime pay. Secondary and part-time work was excluded. **-Ray Connolly**

TODAY'S SALARIES FOR U.S. ENGINEERS
(in thousands of dollars annually)

Branch of engineering	Average	Median
Aeronautical/aerospace	38.7	36.4
Agricultural	37.3	34.5
Architectural	45.1	37.0
Chemical	48.9	39.1
Civil	39.6	33.7
Cost/value	37.6	35.0
Electrical/electronic	39.9	36.0
Industrial	41.3	35.6
Manufacturing	42.6	37.0
Mechanical	42.8	36.6
Metallurgical/materials	38.9	35.0
Nuclear	41.1	38.0
Petroleum/mining	55.4	44.5
Safety	40.4	33.0
Environmental/pollution control	40.1	33.4
Job function (all engineering)		
Design	32.5	30.4
Executive/administrative	51.3	42.0
Quality/production/maintenance	33.8	31.8
Research/development	36.4	35.0
Sales/marketing	44.4	37.9
Teaching/training	35.0	33.3

Source: National Society of Professional Engineers

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ELECTRICAL ENGINEERS

The Cyclotron Institute at Texas A&M University is seeking engineers to participate in the design, construction, and operation of a super-conducting cyclotron to be used for basic and applied research in nuclear science.

Two positions are immediately available. One is for a creative electronics design engineer with a background and interest in digital data acquisition, computer interfacing, and digital control of analog devices. A knowledge of modern nuclear instruments and data-collection techniques would be useful. The other position requires an engineer who has an interest in the design and construction of precision high-voltage and high-current power supplies, control systems, and high-power radio-frequency systems. Experience with cyclotrons or other accelerators would be advantageous but is not required. The Cyclotron Institute is located on the main campus of Texas A&M University in College Station, Texas. The city and surrounding area offer attractive living conditions, a healthy economic environment, and near year-round outdoor recreational facilities. The University offers an attractive benefits program including educational opportunities.

The salary for these positions will be commensurate with qualifications and experience. Interested individuals should send complete resumes to:

D. H. Youngblood,
Director
Cyclotron Institute
Texas A&M University
College Station, Texas
77843

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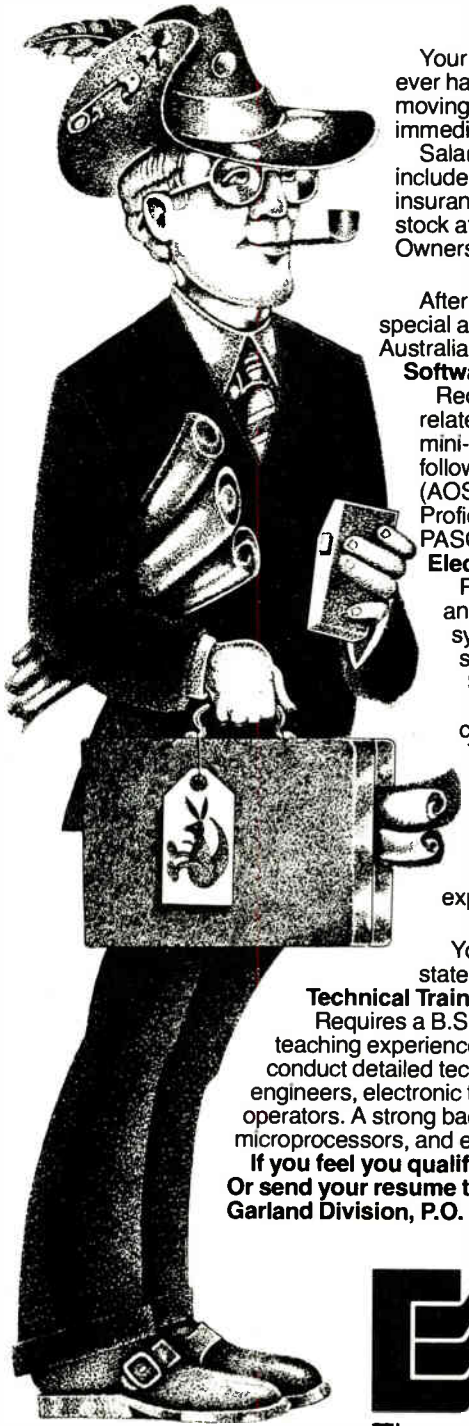

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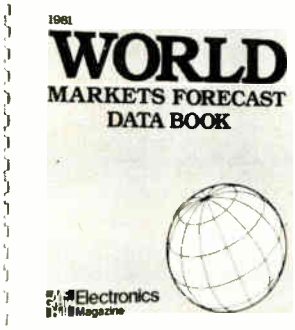

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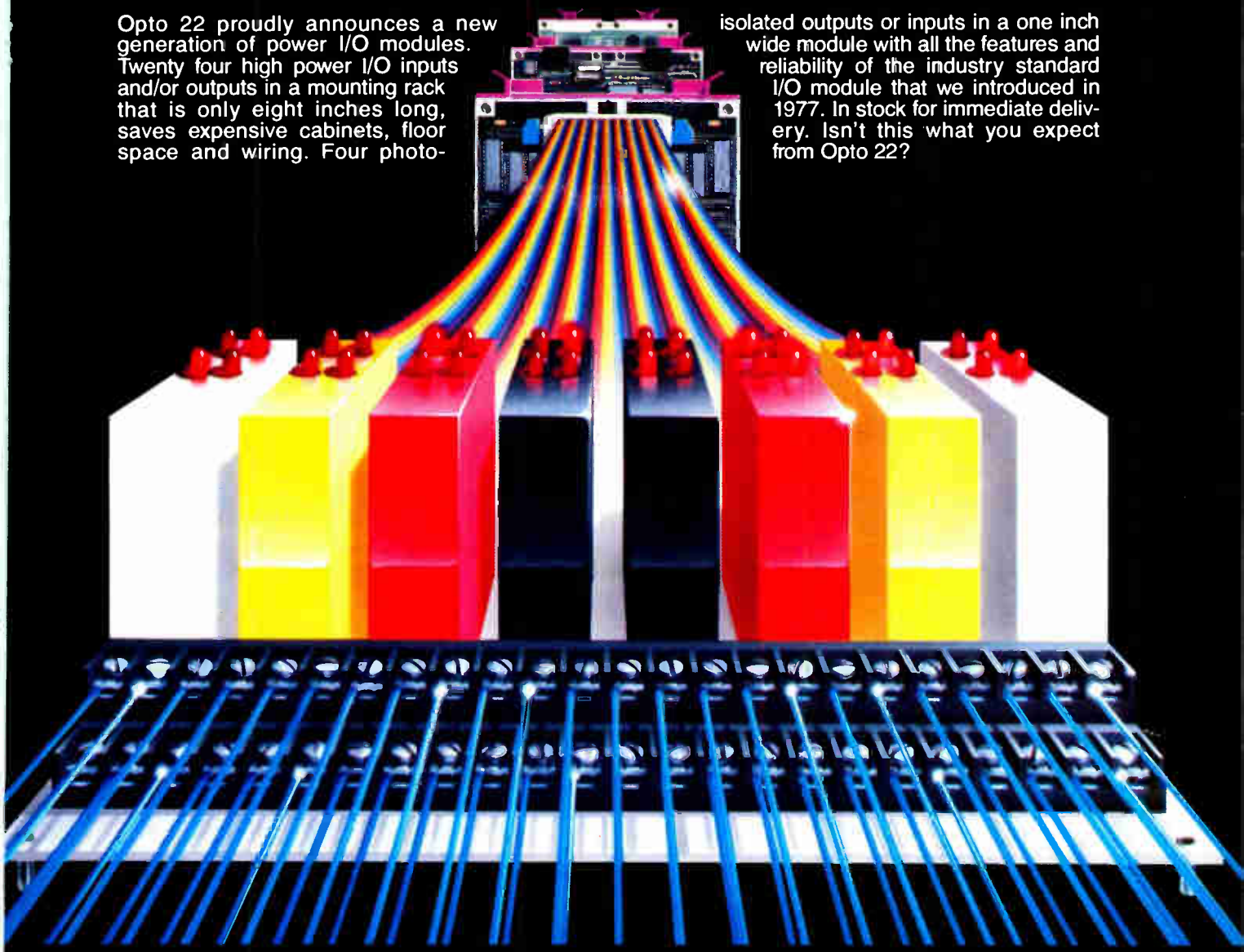

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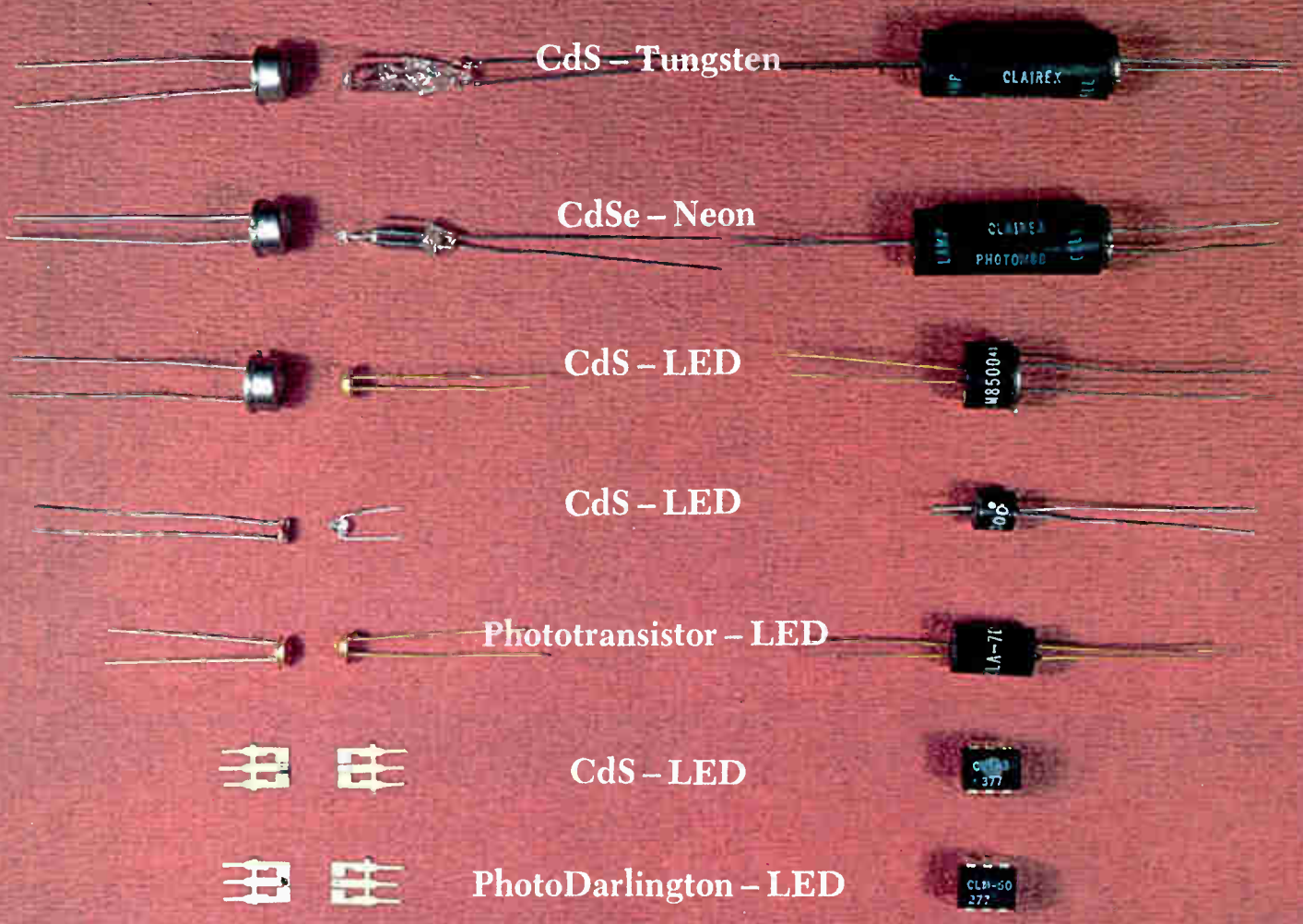

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