NOVEMBER 3, 1982

ELECTRONICA: EUROPEANS WONDER WHEN SLUMP WILL END/79

Test engineers focus on chip and functional testing/ 100

Work station consolidates VLSI design tasks/ 105

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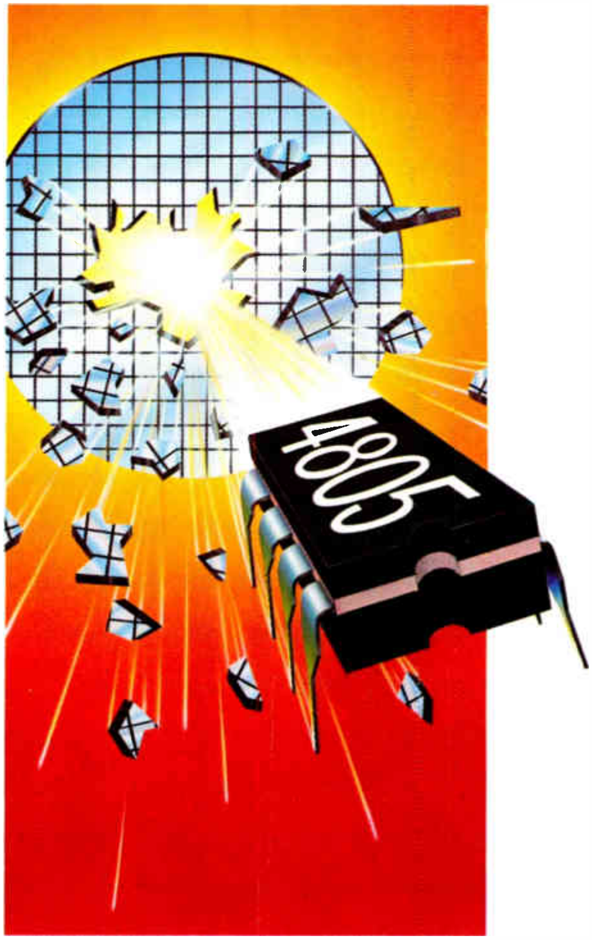

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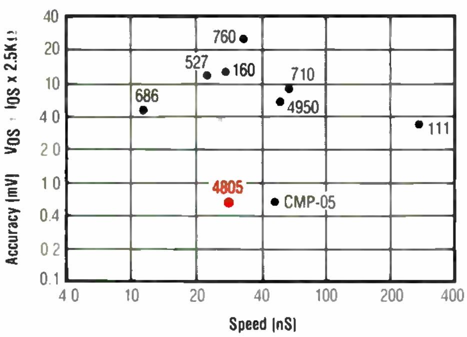

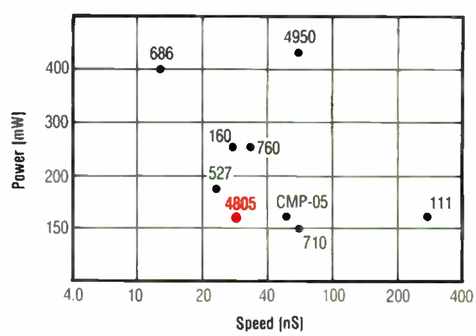

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Circle 900 on reader service card

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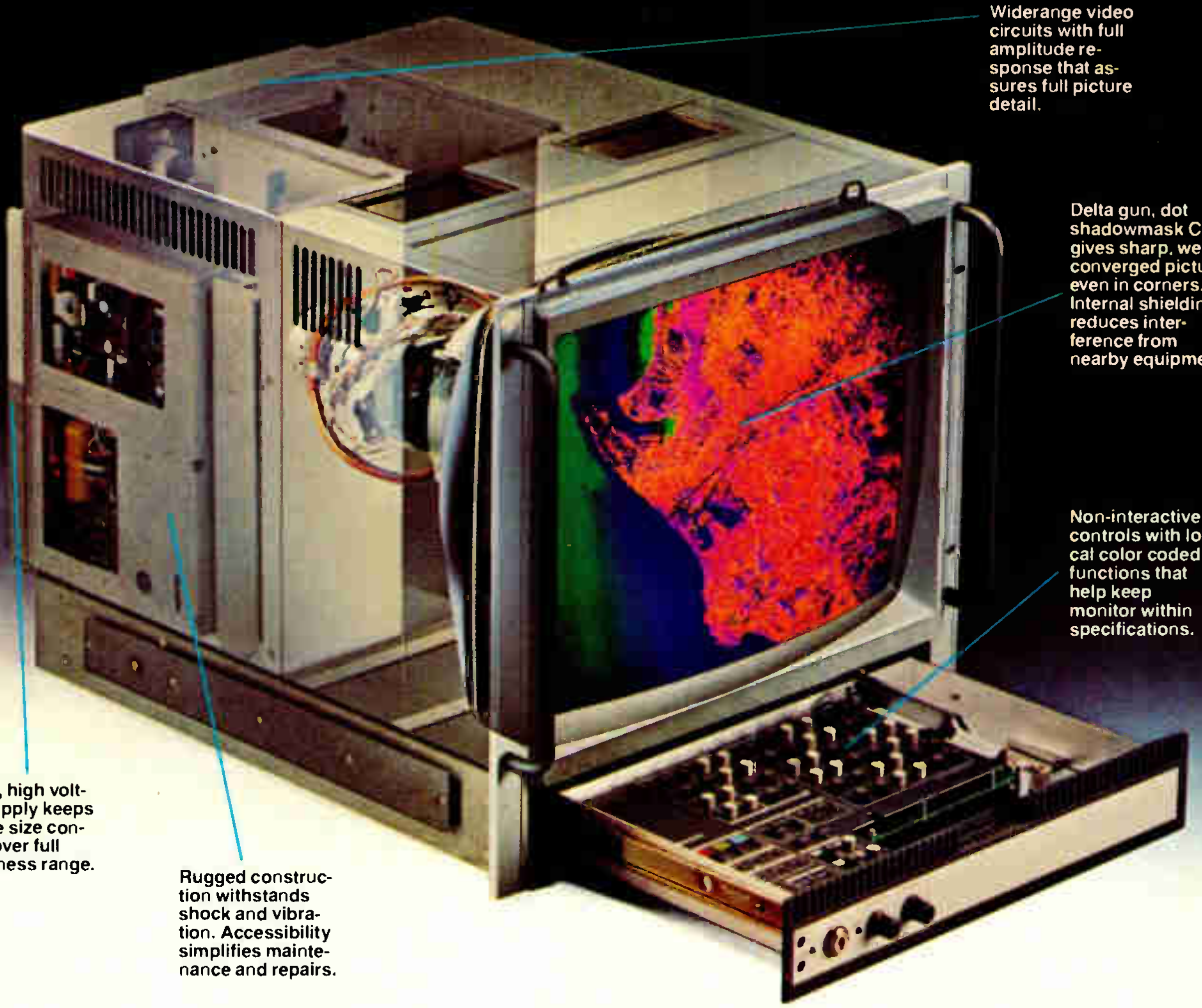

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Circle 174 For Literature

Circle 1 For Sales Contact

Electronics
The International Magazine of Electronic Technology and Business

Cover designed by Fred Sklenar.

The cover story

Fast custom logic meshes with advanced packaging in new computer, 93

In Honeywell's large DPS-88 mainframe, arrays of current-mode-logic large-scale integrated circuits have been automatically tape-bonded to multilayer ceramic substrates based on a copper thick-film system.

Major New Developments

Computer playground

The first visitors to Epcot Center at Disneyworld in Florida have been dazzled by the special effects. But few realize the huge amount of computing power needed to make everything work—displays, shows, communications, and even heat, light, and air conditioning. Here's a look behind the scenes, 86

Comprehensive work station

A stand-alone work station based on the 68000 microprocessor and high-resolution color graphics will support all phases of very large-scale integrated-circuit development, from logic synthesis through physical design, 105

Small-area network

Miniature local networks, which have started a new trend in home-electronics design, are also being aimed at small-business and industrial systems, 119

Low-profile floppy-disk drives

Half-height 5-½-in. floppy-disk drives arrive in force, some less than half height, some bigger than a megabyte, 131

Making circuits more testworthy

A new test program employs a grading system to discover whether and where a circuit needs more work to improve its testability—all prior to automatic test generation, 45

NEWSLETTERS

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SERVICES

Vol. 55, No. 22 • November 3, 1982

Electronics Review

Electronics International

Probing the News

Technical Articles

New Products

Electronics

Highlights

High-speed mainframe sports CML and micropackaging, 93

Current-mode logic, supplanting the usual emitter-coupled logic, is only the beginning of the technological departures in a fast new mainframe computer. Rather than using multilayer boards and dual in-line packages, the CML arrays are mounted face down by tape automated bonding onto a large multilayered ceramic module called a micropackage.

Cloudy outlook darkens the mood at Electronica, 79

As European exhibitors head for the Electronica show in Munich, they report few encouraging signs of business upturn. In fact, most say that 1983 will not mark the return to double-digit growth. The outlook does vary; British manufacturers, for example, report an end to their downturn.

Testing VLSI is the focus at Cherry Hill test conference, 100

With very large-scale integrated circuits turning up regularly in systems, on-chip and functional testing are in the spotlight at the 1983 International Test Conference. Other important topics include improved humidity testing for plastic-packaged parts and a way to combine signature analysis of ICs with level-sensitive scan design of the systems in which they appear.

Design station embraces all phases of VLSI design, 105

Bringing together the major design tools for very large-scale integrated circuits, a stand-alone work station can capture, simulate, and verify both logical and physical designs. The hierarchical organization of the design tasks means that data is iterated on all levels, regardless of the one on which it is entered.

Chip set provides a modem on a board, 111

Reducing the essential circuitry for a modem to a few chips gives designers of small systems a way to fit this valuable feature onto a single board cost-effectively. The mix of chips can be altered to suit the modem standard that the application will adopt.

Simpler networks suit smaller linkups, 119

By paring down the traditional local-network concept, two small-area nets meet the performance and cost demands in applications like a household or a small business. Using serial buses, they combine the best of network-access protocols and asynchronous data-link techniques.

Coming up . . .

Sizing up engineering work stations: a special report . . . achieving improved radiation resistance in MOS large-scale and very large-scale integrated circuits . . . a bit-mapped display brings high resolution to a microcomputer system.

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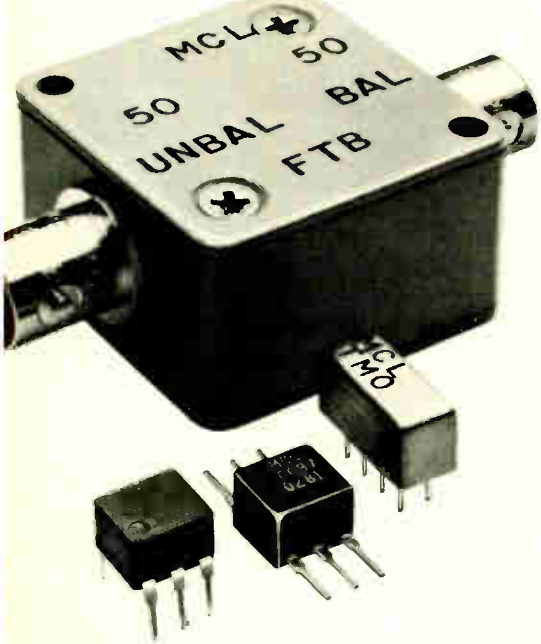

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C 59 REV. A

Circle 5 on reader service card

Publisher's letter

The jigsaw puzzle on our cover is art director Fred Sklenar's visualization of the complexities of putting bits and pieces of new technology in just the right places so that together they form a viable system—in this instance, the very large DPS 88 mainframe computer that Honeywell Information Systems announced in mid-October. Fred's mosaic, on another scale, also symbolizes the way our editors meshed their talents to assemble the two articles of our cover-story package on the innards of the DPS 88.

Tom Manuel, our computer and peripherals editor, got hold of the major pieces of the package in late July at the Siggraph computer-graphics meeting in Boston. There he persuaded a Honeywell public-relations man to have the firm's engineers write exclusive articles for us on the current-mode-logic (CML) technology developed for the chips in the central processing unit, the tape automated bonding (TAB) used to mount the chips on leadframes, and the micropackage devised to house them. With that early start, we were able to ready the package for this issue. Nicely enough, it comes right on the heels of the introduction of the DPS 88 machines, the speediest of which zips through 14 million processing instructions a second.

What Tom initiated, Rod Beresford and Jerry Lyman wrapped up. Rod, our solid-state expert, edited the CML piece that starts on page 93. Jerry, our packaging and production editor, melded the two articles on the packaging of the chips into the subsequent piece (p. 96).

Jerry also had a hand in another major article in the issue, a preview of the technology trends that will mark the Cherry Hill test conference in Philadelphia later this month (p. 100). Richard Comerford, our test and measurement editor, teamed with Jerry on this piece.

Software know-how is becoming an increasingly important tool in the arsenal of the electronics designer, and we've recognized this for some time with greater coverage of advances in software technology. But practical solutions to software engineering problems are just as important to our readers, so beginning with this issue we will regularly publish short programs addressed to engineering problems. These pieces will appear in the section formerly called Engineer's notebook, which we're converting into Software notebook. Engineer's notebook will be merged into the popular Designer's casebook, which continues to serve the practical hardware-design interests of our readers.

Ashok Bindra, our circuit design editor, is responsible for both these departments, and he continues to seek contributions of unique, practical hardware and software solutions to design problems. And he'll pay $75 for each one we publish. Submit ideas for either section to: Ashok Bindra, Circuit Design Editor, *Electronics*, 1221 Avenue of the Americas, New York, N. Y. 10020, or call him at (212) 997-2798.

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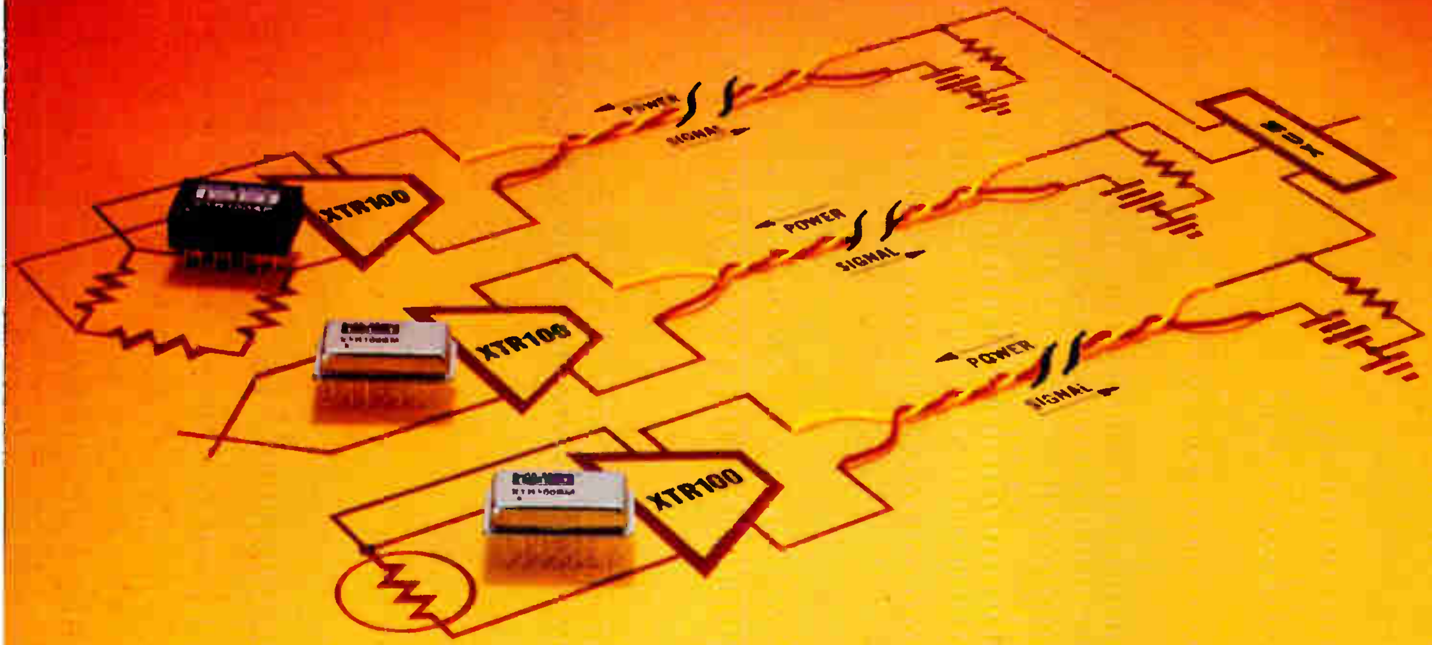

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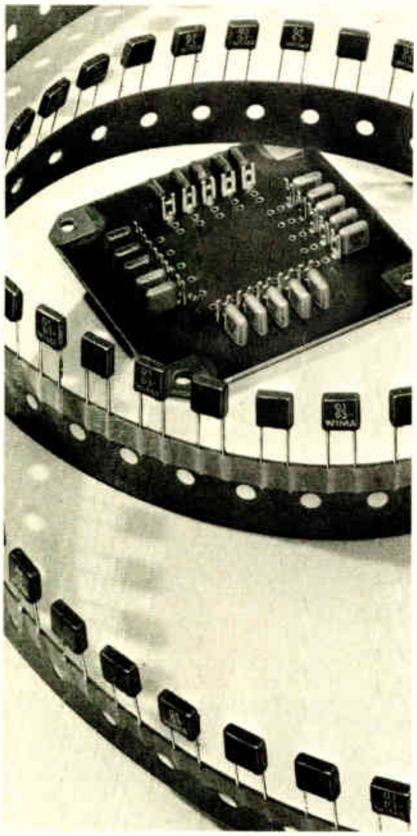


Readers' comments

Dielectric materialism

To the Editor: It is indeed unfortunate Mr. Benzing elected to omit polyimides from his dielectric comparisons ("Shrinking VLSI dimensions demand new interconnection materials," Aug. 25, p. 116). Variable results are not uncommon when significant departures from comfortable technology are attempted.

At present, one of the world's largest manufacturers of high-density dynamic random-access memories uses polyimides as an interlevel dielectric in those devices. Others are evaluating polyimide, as it appears to offer good step coverage, low defect density, stress and crack resistance, a low dielectric constant, and low cost.

Kenneth A. Rygler
Du Pont Co.
Wilmington, Del.

Night owls

To the Editor: As I live in suburban Boston and have attended evening graduate school at nearby Worcester Polytechnic Institute, I was intrigued by the Massachusetts Institute of Technology's recommendations for continuing education ["MIT calls for lifelong schooling for engineers," Oct. 6, p. 76]. However, I find it ironic that MIT is advocating lifelong education when they offer no evening college or professional courses like their crosstown rival, Northeastern University.

I hope they have recognized the need for professional and continuing education in some sort of attendable evening program as well.

Gregory L. Opp
Hudson, Mass.

Heated argument

To the Editor: Your research into the history of the use of liquid cooling for computers ["Supercomputers demand innovation in packaging and cooling," Sept. 22, p. 136] was all wet, to say the least. The CDC 6600 circa 1969, IBM 370/168 circa 1974, and IBM 3033 circa 1979 (reported by you as air-cooled) are a few examples of the application of liquid cooling prior to the time you reported as the earliest use.

Such blatant errors in areas about which I have some knowledge always make me wonder how accurate your remaining facts are.

David W. Morris
Cupertino, Calif.

■ **Author Jerry Lyman replies:** *Today, liquid cooling has come to mean a fully conductive method where integrated-circuit packages are in intimate contact with a liquid-cooled plate or bar. The earlier systems cited used a hybrid of liquid cooling and some other heat dissipation method at best. In the 6600, the cooling system is similar to that of the Cray-1, where heat flows through a passive copper plate that contacts two stabilized cold sources; in the two IBM computers, chilled air blown across circuit boards is recooled by heat exchangers.*

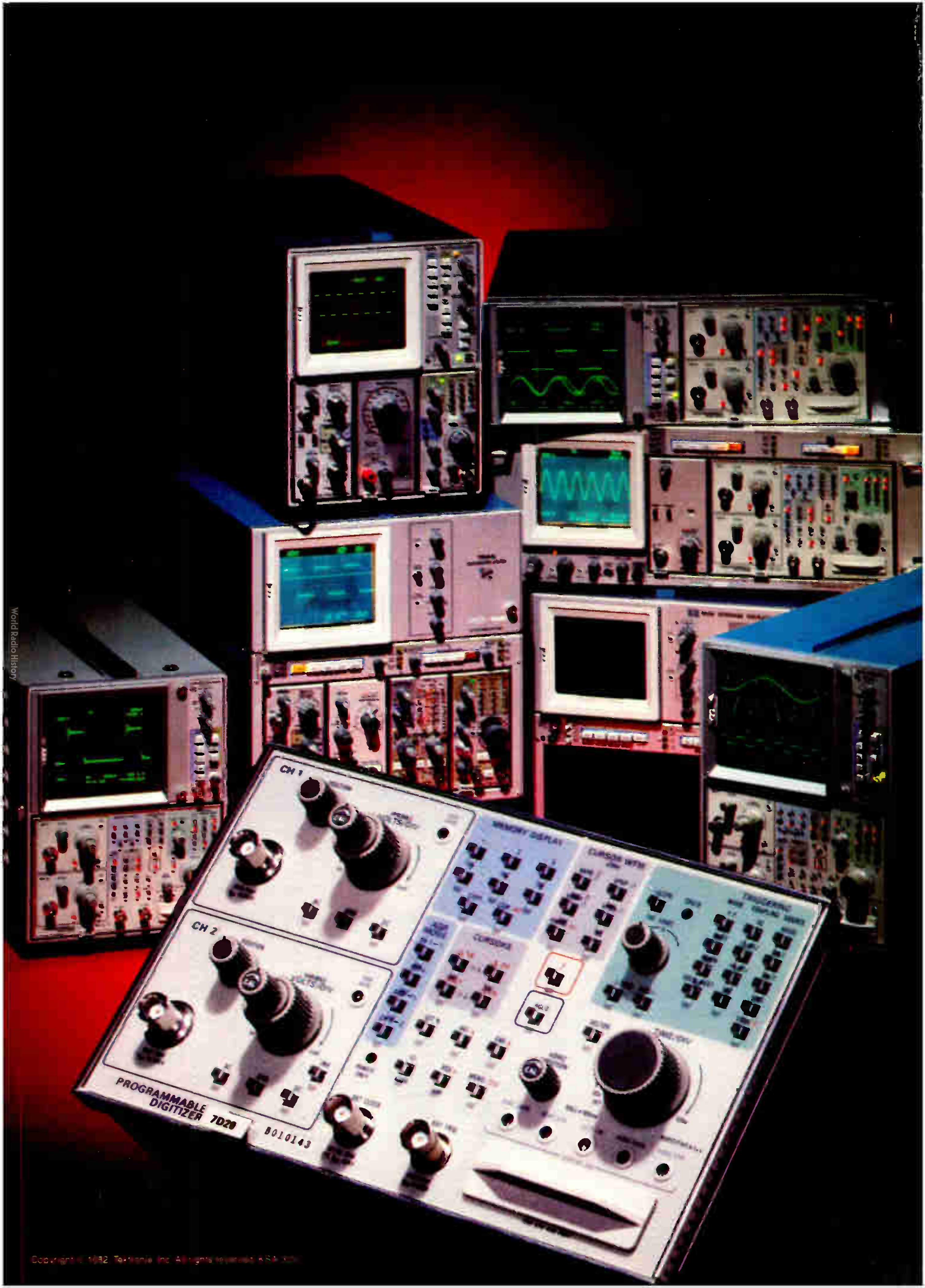
Litigated to the eyeballs

To the Editor: In the In my opinion column of Oct. 6 ["The U. S. neglects human capital," p. 24], Mr. Tanaka stated that Japan, with about half the U. S. population, graduates 22,000 electrical and electronics engineers each year, whereas U. S. colleges and universities graduated fewer than 19,000 such engineers last year. He might have added that, in contrast, the U. S. also graduates 30,000 lawyers a year, while Japan has a total of 30,000 lawyers.

David S. Walker
Great Neck, N. Y.

Corrections

In the News update item of Sept. 22 on Cameca's high-resolution X-ray source photolithography system, with the exception of the 0.1-µm resolution and the 0.02-µm alignment accuracy, the Thomson-CSF subsidiary mistakenly supplied information referring to the ARW 610 ultraviolet-light source system. Development of the X-ray system is now complete, but no orders for it have yet been received. Also, the subject of "Stand-alone 16-bit emulator acts as a minicomputer terminal" (Sept. 8, p. 222)—the 9516S—is a Gould Millennium product and does not come from the company's Biomation operation.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Circle 11 for Literature

Editorial

The U. S. must not rely on luck

Last month marked the twenty-fifth anniversary of the launching of Sputnik by the Soviet Union, as has been noted in these pages, and with it has come an orgy of regrets and recriminations over the slippage in technological leadership of the U. S. versus the USSR. And indeed, those who remember the national convulsions we experienced when those first non-American beeps from space were heard are understandably tempted to liken those days to the present situation.

It is impossible not to note the decline in emphasis in mathematics and science in our secondary schools, the reduction in the number of skilled teachers in these subjects, and the growing difficulty in funding our educational resources. The fact that other nations—our competitors—are turning out many more graduates equipped for the highly technological future has been pointed out *ad nauseam*. And the evidence is there to see that we are no longer alone, nor even significantly dominant, in many areas.

Apparently there is something in the American psyche that lets us make assumptions about our superiority until something happens to rudely awaken us to the fact that our assumptions are false. Finding this situation unacceptable, we then proceed to expend the energy and the money needed to restore us to our accustomed place at the top of the heap. Witness Pearl Harbor, which galvanized us into a massive war effort that resulted in undisputed world dominance, and the aforementioned Sputnik.

Now we are faced with a new challenge, no less threatening yet more subtle than the previous ones. The previous situations evoked clarion calls to action, because all of us could see clearly our own stake in the outcome of the contest. It is hard to arouse national passions over the problems of an industry that has experienced 20% growth rates in the past (like the semiconductor industry until recently), and it is tough to galvanize support for massive infusions of funds for education when thousands of manufacturing workers cannot find employment. Yet, continued failure to come to grips with the realities of the technological revolution can doom the U. S. to second-rateness and economic decline.

Up to now we have been relatively lucky in following our historic bent through cycles of apathy and energetic problem solving. Let us hope that for this new national emergency, our arousal will not be too late.

The cost of the Pentagon's year-end bonanza

A commitment to spend more than $3 billion in a single day is worth more than passing mention, especially when more than a third of that—some $1,042,570,000—goes for electronic products and engineering. That was the outlay promised by the Department of Defense and its military services when they awarded 182 contracts on Sept. 30, the final day of fiscal 1982.

Emptying the till at year's end is the inevitable result of the Government's use-it-or-lose-it rule, under which uncommitted funds must be returned to the Treasury. Understanding such behavior is a key to understanding high-technology economics in America. With much of its available capital tied up in military programs, it is no wonder that industry finds it increasingly difficult to remain competitive in growing global markets for other electronic products. Disproportionate outlays for guns threaten the industry's commercial bread and butter.

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Circle 13 on reader service card

People

Not-so-humble typewriter profits Xerox's Jackson

In the scramble to find the so-called office of the future, it may be all too easy to overlook the electric typewriter. New microelectronic chips and modular, upgradable designs are giving an additional boost to this most familiar of office products.

Such is clearly the case with Xerox Corp.'s year-old Memorywriter line, maintains William C. Jackson, president of the company's Office Products division and former head of its typewriter effort. In fact, Xerox's typewriter business is now so brisk that it is opening new production lines in Fremont, Calif., and Lille, France, that will supplement the main plant output in Addison, Texas.

Contender. Don't overlook the typewriter in the office of future, cautions Xerox's William Jackson.

When the Memorywriter line made its debut in November 1981, Xerox's Dallas-based Office Products division had a goal of taking 9% to 10% of the market in a year. "I would not be surprised if we don't end up doubling our objectives," states a confident Jackson, 50, who was promoted to his current position last summer after the office products operation was split into two units. One, called Office Systems division in Palo Alto, Calif., was given responsibility for Xerox's Star information system and Ethernet local-networking services. Jackson's lot retained responsibility for stand-alone products, like typewriters, facsimile machines, word processors, and personal computers.

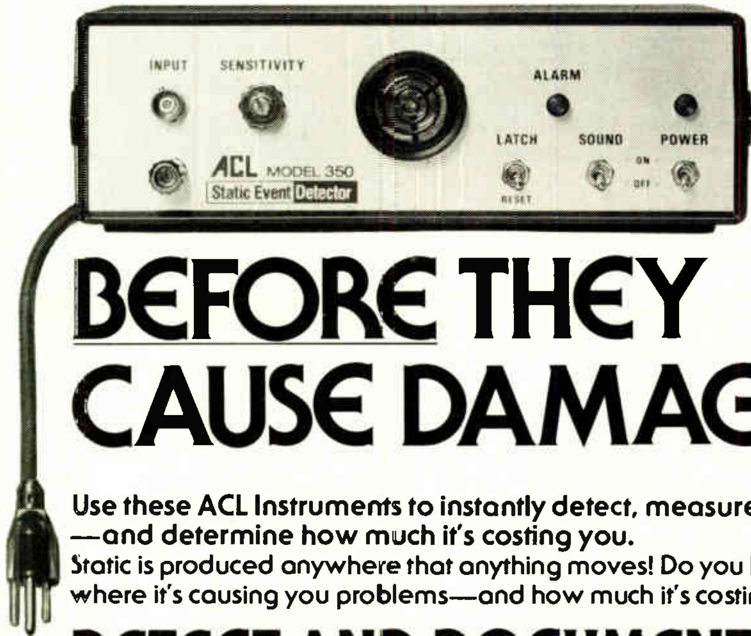
Jackson, who joined Xerox in 1978, rejects reports that the Office Products division has been a big money-loser during its eight-year existence. He says the division actually acts as a product planning and manufacturing arm for other Xerox sales and marketing organizations. "We develop, manufacture, and plan products for worldwide consumption, and yet they are sold by someone else," he notes. "For that reason, we cannot be looked at in the classic profit-loss sense."

Of all of his products, none has taken off as quickly as the Memorywriter. "Typewriters are well-known, nonconcept sells, and when you approach it with a modular, upgradable product with functions and communications capabilities, it is an added boost," he states. The native of Southern California credits Xerox's encroachment on IBM Corp.'s traditional typewriter territory to "staying current" with microelectronics and offering a great number of increments in cost and features. Slated next year are new models that will move the line into the $7,000 range.

Towne, at 39, is Microsoft's old man as well as president

When Jim Towne took over as president of the Microsoft Corp. last summer, he quickly became known as The Suit to the young programmers who had made the company a leading producer of software for microcomputers. Towne had left a position as vice president of staid Tektronix Inc.'s Instruments division to take charge of a company started only a few years ago by a pair of computer whizzes barely out of school. A self-described "straight arrow" with the requisite wife, two

Locate Your Static Problems



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Use these ACL Instruments to instantly detect, measure, and document static —and determine how much it's costing you.

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The sophisticated ACL 350 continuously monitors for static discharge, or the presence of potentially harmful static charges. Compact, with simple controls, the ACL 350 is ideal for use in clean rooms, and "static free" environments, at assembly work stations and for process control. And, it's compatible with other environmental monitoring equipment.

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Once you're set up to detect static with the ACL 350, you can focus precisely on "where" and "how much" with the hand-held ACL 300. The highly accurate ACL 300 answers three basic questions:

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2. How much static?
3. What is the polarity of the charge?

The ACL 300 features:

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People

New world. Jim Towne finds himself the leader of a group of young software jocks.

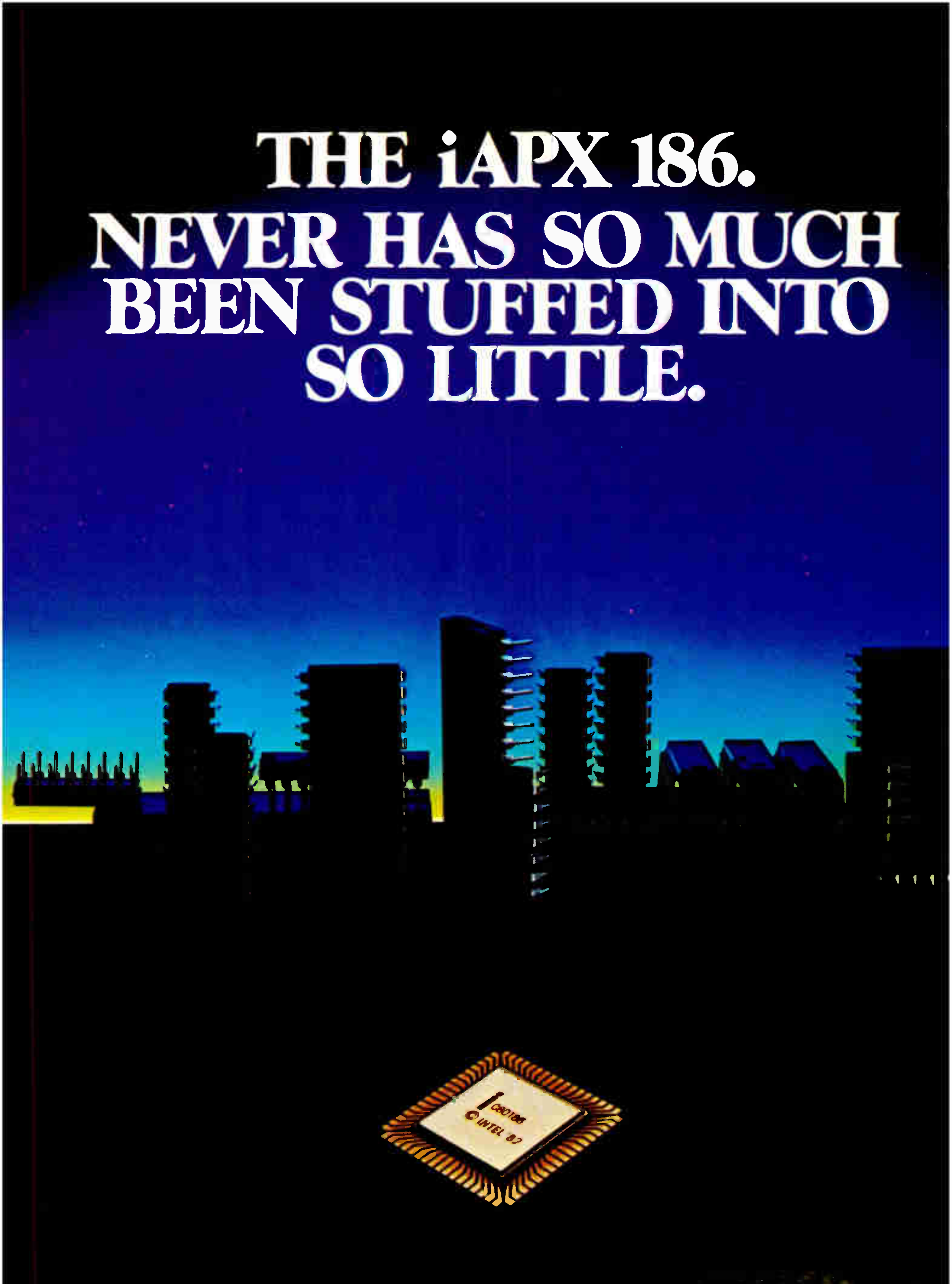
children, three dogs, and active civic life in his native Portland, Ore., he found himself in a new role as leader of a band of young and freewheeling software jocks.

Microsoft markets system and application software for Apple, IBM, Tandy, and CP/M-based microcomputers. It has doubled in sales every year for the past six and projects revenues of $30 million for 1982. In the process it has reached the point where the process of doing business is as important as the development of business products.

"Microsoft wasn't looking for someone to manage software and products, but someone to allow Bill Gates [the 26-year-old cofounder with Paul Allen, 28] the time to provide leadership to the technical people," Towne says. "My job here is to enable. I'm here to bring order and discipline—not heavy-handed power, but to determine who does what and how it is to be done. That's what the company needs to grow."

Although he still winces at being thought of as "the old man" at 39, Towne seems to have adjusted to the relaxed Microsoft work process. "At Tektronix," where, Towne makes clear, he was not looking for another job, "I almost resented the way the senior executives would talk about 'the good old days,' because I never got to see them." Towne recalls. "At Microsoft, *these* are the good old days." □

ANNOUNCING THE BIGGEST LITTLE BREAKTHROUGHS IN 16-BIT TECHNOLOGY.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BEEN STUFFED INTO
SO LITTLE.
C80186
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Introducing the biggest, little thing in 16-bit technology today.

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Perfected through HMOS III technology, the 186 is a remarkable microprocessor that handily integrates 15-20 LSI chips.

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There isn't another processor around with as high a level of integration. The 186 brings together almost all the functions of a CPU board.

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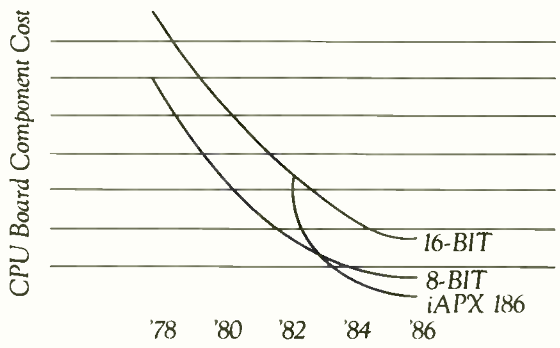
You get an enhanced 8086-2 CPU. A programmable, dual-channel DMA controller. Three timer counters. A programmable interrupt controller. Memory and peripheral chip select logic. A clock generator. A local bus controller. And a programmable wait state generator.

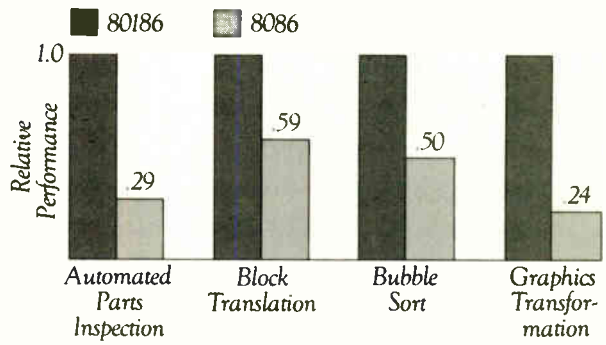
Incredibly, the 186 does all this in production volume for just $30. Or in hundred unit quantities for $50. That's less than half the cost of the chips it replaces.

Which means if you've been settling for less performance to save money, now you can't afford not to step up to 16-bits.

A comparison of CPU board component costs shows that 16-bit performance can be purchased at 8-bit prices with the help of the 80186.



Benchmark results measuring the standard (5 MHz) 8086 vs. the standard (8 MHz) 80186 show an overall performance increase of approximately 2.0.



Worried about software? Don't be. Because its software is totally compatible with Intel's iAPX 86, 88 family, the 186 is immediately supported by the largest base of 16-bit software in the industry.

Now, if that data doesn't make you move your cursor, listen to this. The standard 8 MHz 186 has twice the performance of the 5 MHz 8086.

As a matter of fact, there's only one other chip in the world faster than the 186.

You'll read about it on the next two pages.

The Intel iAPX 186. It's no big thing. Just a minor miracle.

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AND OUR iAPX 286. ITS PERFORMANCE IS OVERPOWERING.

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Anywhere.

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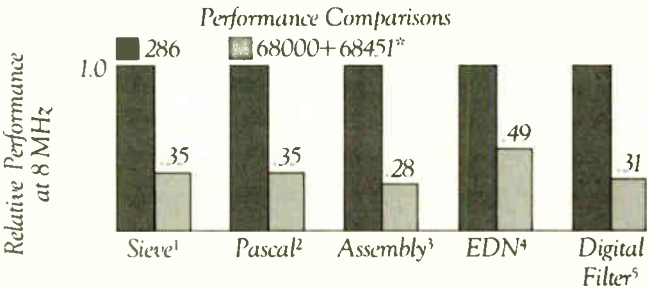
It gives you three times the performance of what you thought was the fastest chip in the market.

To add more power to the punch, this one has been designed from the beginning to include memory management and protection on chip.

Which means you can design these sophisticated capabilities into your system without the cost, complexity or performance degradation of external hardware.

If 16 Megabytes of physical memory isn't enough, there's a virtual memory capacity of 1 gigabyte per user.

The 286 has been optimized to handle advanced operating systems such as the UNIX* and iRMX™ OS. It also provides new instructions for languages such as Pascal, BASIC, FORTRAN, C and ADA.



*Performance adjusted to reflect indicated system configuration. Details available from Intel. [1] "A High Level Language Benchmark." Byte, Sept., 1981. [2] "A Performance Evaluation of the Intel iAPX 432," Computer Architecture News, June 1982. [3] "16 Bit Microprocessor Benchmark Report," Intel Corporation, 1981. [4] "16 Bit Microprocessor Benchmarks," EDN, Sept., 1981. [5] "Digital Filter Implementation on 16 Bit Microprocessors," IEEE MICRO, Feb., 1981.

And to simplify sophisticated system development even further, there's an integration of performance-critical functions. Such as task switching, interrupt handling and O.S. call, among other things.

A couple more hard facts about software. The 286 is compatible with the iAPX 86, 88. So not only will you have the hottest CPU on the market, but also immediate access to a huge software base.

System Comparisons

	iAPX 286 System	68000 + 68451* System	Advantages of Integrated Memory Management & Protection
Typical System (16 Users)	1 CPU	1 CPU 1-4 MMU's 2 Transceivers 1 MMU Selector	Less Board Space
Wait States Required 8 MHz	0 W.S.	2 W.S.	Higher Performance
Task Switch Overhead	22 µS	>120 µS	Faster Response
Max. BUS Bandwidth at 8 MHz	8 MB/Sec	2.67 MB/Sec	Higher Throughput

*Based on published data sheets.

On the hardware side, the iAPX 286 is a well integrated 16-bit family. It delivers full performance at the systems level, through support circuits like the 8207 DRAM controller and the 80287 floating point numerics processor.

All this allows the Intel 286 to give the ultimate in command performance.

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652 (653—DC version)—High power switching relay. 25-40 amps. High immunity to transients. 1500 VRMs optical isolation. 3.8 to 32VDC @ 10mA control range. Logic compatible. Meets MIL-R-28750/10 and MIL-STD-704.

The widening fiber-optic gap

by William J. Hudson
vice president, Connector & Electronic Products Group, AMP Inc., Harrisburg, Pa.

American engineers and scientists have been leaders in fiber-optic research and development. Though their inventive contributions should not be minimized, technology centers in other countries, specifically in West Europe and the Far East, have been concentrating on taking existing technology—with their governments' assistance—improving it, applying it, and producing fiber-optic systems for a broad spectrum of applications.

Unlike France, Canada, and Japan, the U.S. has no experiments under way to connect cities with fiber-optic data links—only plans for wiring up a few buildings with fiber optics this year and next. No industrial plants with complex fiber-optic data networks exist in this country, whereas overseas, both to the east and west, whole-house systems are now in place at numerous locations.

Further, although many U.S. data-processing equipment manufacturers are hotly engaged in fiber-optic network and short-run–link research at every level, no commitment to production has been made. With the exception of a few highly specialized military applications whose technology transfer value is essentially nil, the U.S. government is not engaged in active support of fiber-optic development or implementation. There are no research grants or grants for system installations. The crux of the problem is that the U.S. is primarily dependent on the private sector for development and application of this new technology, and activity that does exist in the private sector is centered around development rather than practical experience through field applications.

Lagging. The U.S. is still perfecting systems that the Japanese and the Europeans already have in service. We continue to work with prototypes that much of the industrialized world already has in production. Why?

Some of the answers may lie in a basic reluctance by potential users to accept the new technology, in a technological inertia, or in the lack of support by the Government. But perhaps the most obvious reason for the general inactivity in fiber optics in the U.S. is, as always, money—the bottom line.

Just about the time fiber-optic users were ready to take the risk of moving into fiber-optic systems, the current severe economic downturn caused them to pull back and reduce risk factors. No original-equipment manufacturer wants to invest substantial sums on new design, tooling, or marketing if it can be avoided.

Afraid of risk. Related to economic concerns is the natural tendency to wait for someone else to be first. With capital costs at an all-time high, manufacturers are reluctant to earmark large sums for a technology that is not yet entirely mature. They would rather let someone else take the risks than themselves commit to a nonstandardized technology that has the potential of changing and leaving them with incompatible products.

The slowdown in the economy has retarded U.S. development in fiber optics by at least two years, putting the rest of the world at least four to five years ahead of us in telecommunications as well as short-run–link applications. The same is true for the development of emitters and detectors. In addition, the lack of spending in fiber-optic communications for research and development as well as applications has resulted in a slowing of expected price reductions as production volume increases.

And there is another important factor to consider. While the Japanese and Europeans are gradually increasing their use of fiber optics and putting in place increasing numbers of complex systems, they are also building production capacity. Both the French and the Japanese have forthrightly stated their world market goals, and in both cases they expect to export half of their production. They are gaining vast practical knowledge in the field about handling the surprises that occur when a design moves from the laboratory to the real world. The experience in developing the peripherals that make for a smooth operating system—the need for which will invariably arise with new systems—will be the province of the early starters.

Electronics *will periodically invite the expression of outside views on this page concerning issues of importance to the electronics industries.*

Meetings

15th Annual Symposium, International Society for Hybrid Microelectronics (P. O. Box 3255, Montgomery, Ala. 36109), MGM Grand Hotel, Reno, Nev., Nov. 15–17.

Annual Conference of the International Electronics Packaging Society, (P. O. Box 333, Glen Ellyn, Ill. 60137), Sheraton Harbor Island Hotel, San Diego, Nov. 15–17.

Fall Conference on Industrial Electronics, IEEE (P. P. Fasang, Siemens Corp., P. O. Box 5476, Cherry Hill, N. J. 08034), Hyatt Rickeys Hotel, Palo Alto, Calif., Nov. 15–19.

Cherry Hill '82—International Test Conference, IEEE (Doris Thomas, P. O. Box 371, Cedar Knolls, N. J. 07927), Franklin Plaza Hotel, Philadelphia, Nov. 16–18.

Comdex/Fall '82—4th National Conference and Exposition for Independent Sales Organizations, The Interface Group (160 Speen St., P. O. Box 927, Framingham, Mass. 01701), Las Vegas Convention Center, Nov. 29–Dec. 2.

Globecom '82, IEEE (Liang Li, Gould SEL, 6901 West Sunrise Blvd., P. O. Box 9148, Fort Lauderdale, Fla. 33310), Sheraton Bal Harbour Hotel, Miami, Fla., Nov. 29–Dec. 2.

Midcon/82 High-Technology Electronics Exhibition and Convention, Electronic Conventions Inc. (999 North Sepulveda Blvd., El Segundo, Calif. 90245), Dallas Convention Center, Nov. 30–Dec. 2.

Applied Superconductivity Conference, IEEE (Martin Lubell, Oak Ridge National Laboatories, Building 9204-1, MS-14, P. O. Y., Oak Ridge, Tenn. 37830), Hyatt Regency Hotel, Knoxville, Tenn., Nov. 30–Dec. 3.

Semicon Japan '82, Semicon Japan Secretariat (4-8-19 Akasaka, Minato-ku, Tokyo 107 or Semiconductor Equipment and Materials Institute, 625 Ellis St., Suite 212, Mountain View, Calif. 94043), Tokyo International Fair Grounds, Dec. 2–4.

Plan '82—Position Location and Navigation Symposium, IEEE (Edward Yannuzzi, Code 30, Naval Air Development Center, Warminster, Pa. 18974), Golden Nugget Hotel, Atlantic City, N. J., Dec. 6–9.

Real-Time-Systems Symposium, IEEE (Earl Swartzlander, TRW, 7702 Governor Dr., Huntsville, Ala. 35805), Hyatt Airport Hotel, Los Angeles, Calif., Dec. 7–9.

21st Conference on Decision and Control, IEEE (A. H. Levis, 35-410/LIDS, MIT, Cambridge, Mass. 02139), Holiday Inn, Orlando, Fla., Dec. 8–10.

International Electron Devices Meeting, IEEE (Melissa M. Widerkehr, Courtesy Associates Inc., 1629 K St., N. W., Suite 700, Washington, D. C. 20006), San Francisco Hilton and Tower, Dec. 13–15.

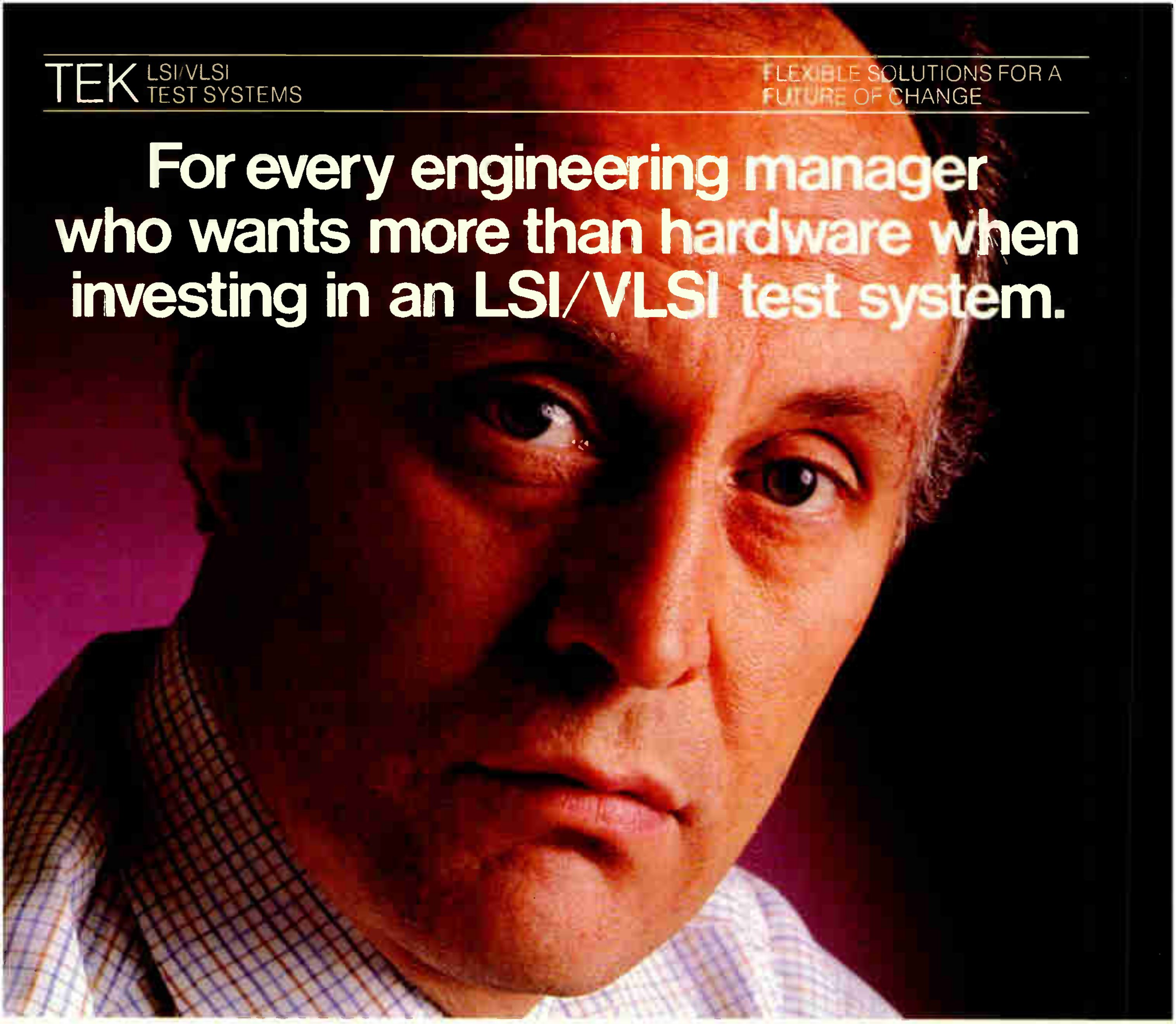
Lasers '82—5th International Conference on Lasers and Applications, Society for Optical and Quantum Electronics (P. O. Box 245, McLean, Va. 22101), Hyatt Regency Hotel, New Orleans, La., Dec. 13–17.

Space Electronics Conference, EIA (Frank A. Mitchell, EIA, 2001 Eye St., N. W., Washington, D. C. 20006), Hyatt Hotel, Los Angeles, Jan. 25–27, 1983.

Seminars

Thin-film for hybrids training course, Materials Research Corp. (Rosemary McPhillips, MRC, Orangeburg, N. Y. 10962), Santa Clara Marriott Hotel, Calif., Dec. 7–9.

Modern Spectral Analysis, Columbia Inn, Columbia, Md., Jan. 10–14, 1983 and Sheraton-Crest Inn, Austin, Texas, Feb. 7–11; **Peripheral Array Processors,** Columbia Inn, Columbia, Md., Jan. 18–21. Both are sponsored by Continuing Education Institute, 5410 Leaf Treader Way, Columbia, Md. 21044.



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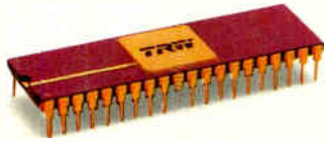

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Circle 31 on reader service card

News update

■ The most visible product of the public-relations campaign begun three years ago by the Institute of Electrical and Electronics Engineers [*Electronics*, Nov. 8, 1979, p. 92] may prove to be the "dial-an-engineer" program for the nation's press that gets under way by the end of this year. The object is to make it easier for the press to report on scientific—and electronics—subjects by providing cooperative experts to answer questions.

To this end, the IEEE has prepared a directory of some 400 knowledgeable members of the institute's technical societies that lists their areas of expertise and telephone numbers. The hope is that more, and clearer, technical news will filter down to the public.

Somewhat behind the scenes but so far of more significance, according to IEEE general manager Eric Herz, is the way the organization has jockeyed itself into a position of influence in the nation's capital. Helped by Pender McCarter, the IEEE's one-man information staff in Washington, D. C., the IEEE was a "large contributor, maybe even a leader" in getting Congress to revise the Individual Retirement Account legislation last year, Herz says. The new setup lets individuals, including the working engineer, establish their own pension plans, protecting those who could lose pension rights as they move from company to company.

That's it. These are the main developments from the heightened public-relations effort, which saw the PR budget jump from $46,000 to $200,000 between 1978 and 1979. The budget, which includes functions previously performed by other IEEE departments, has stayed near this level. A sizable chunk of it had gone toward hiring a PR director, Joseph J. Codispoti, and retaining heavy-hitting New York PR firm Ruder, Finn & Rotman Inc. (formerly Ruder & Finn). But Codispoti left in September of last year, and no successor has yet been named in order to "make budget," says Herz. Nor are there plans to replace or rehire Ruder, Finn, dropped at year-end 1980. **-Marilyn A. Harris**

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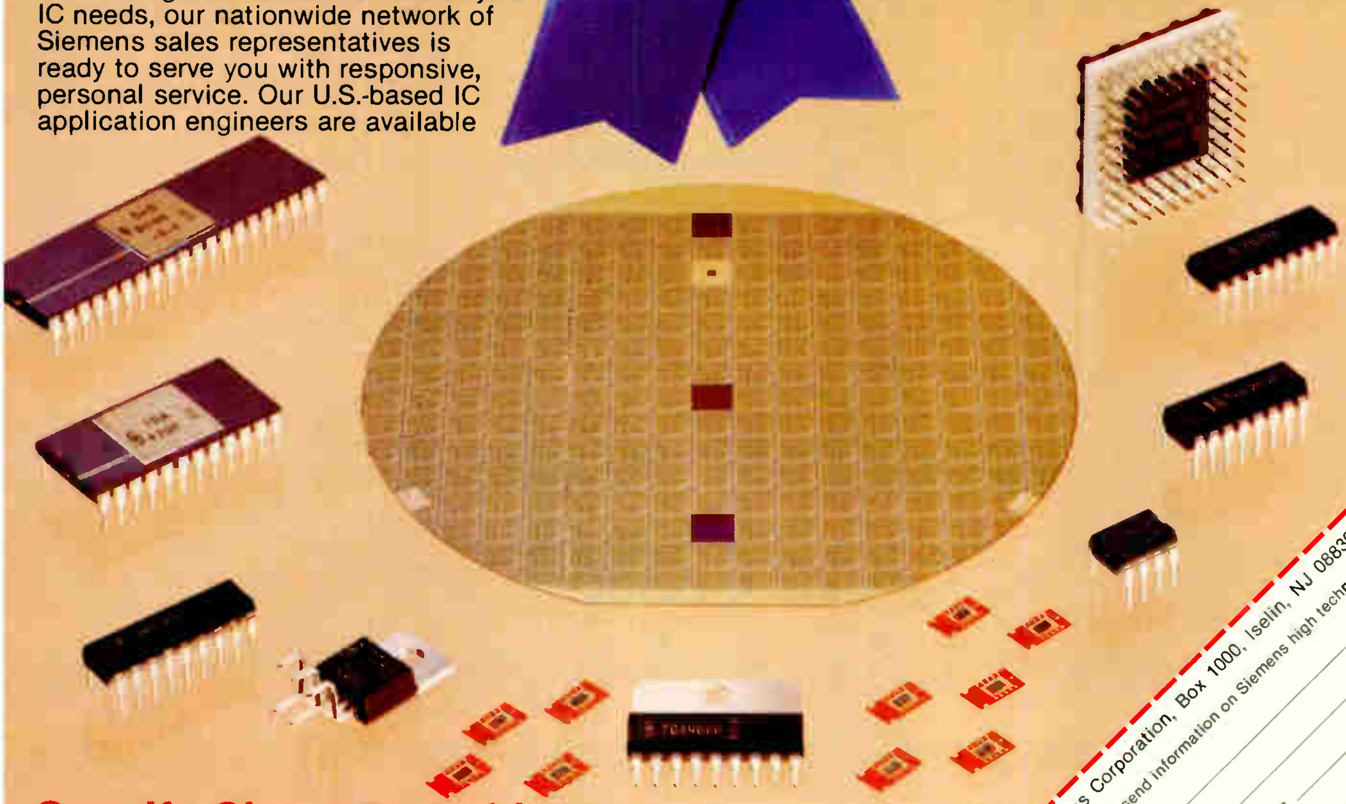

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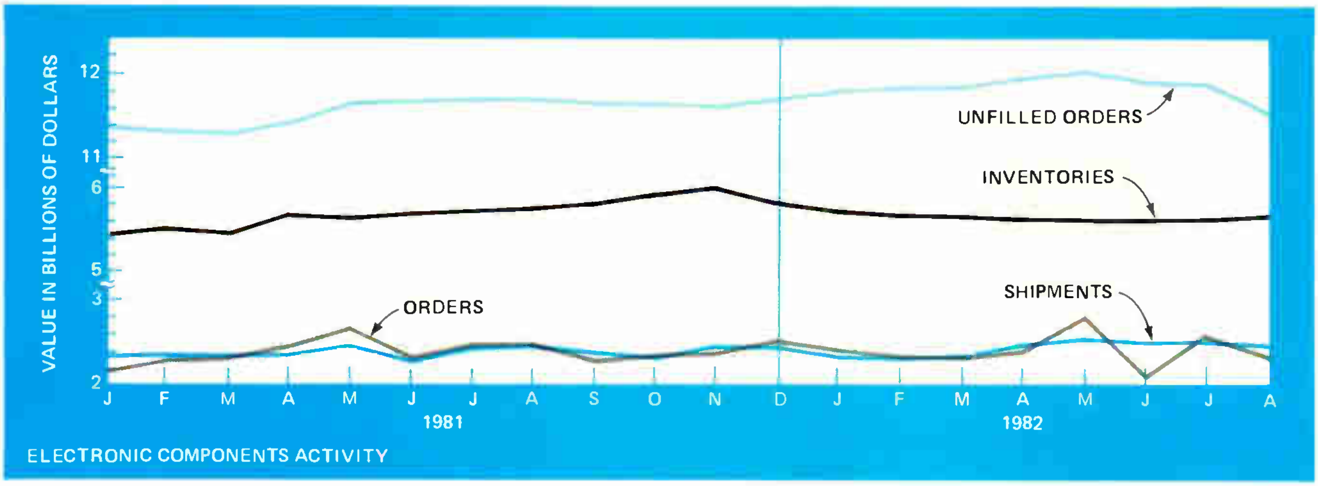
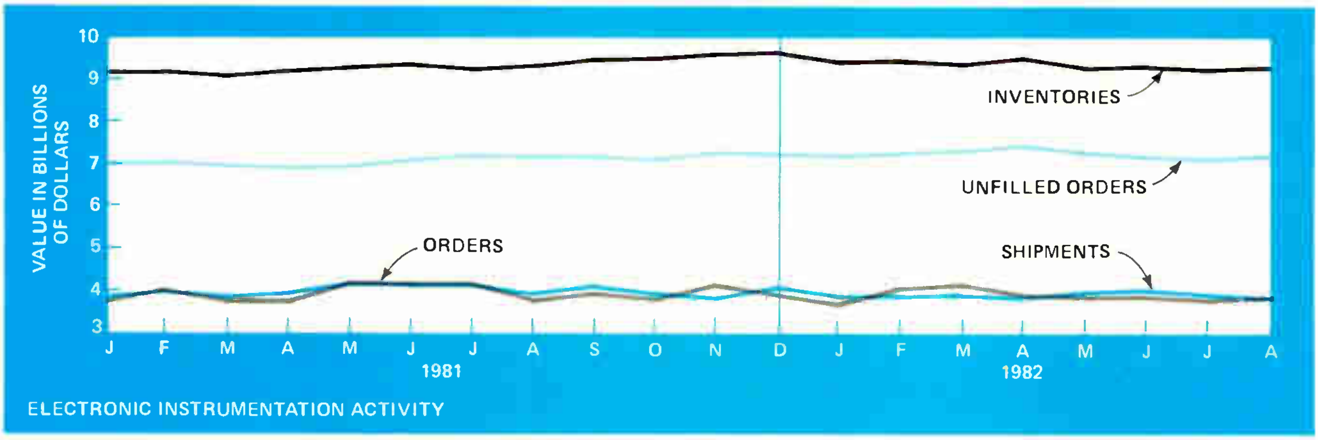
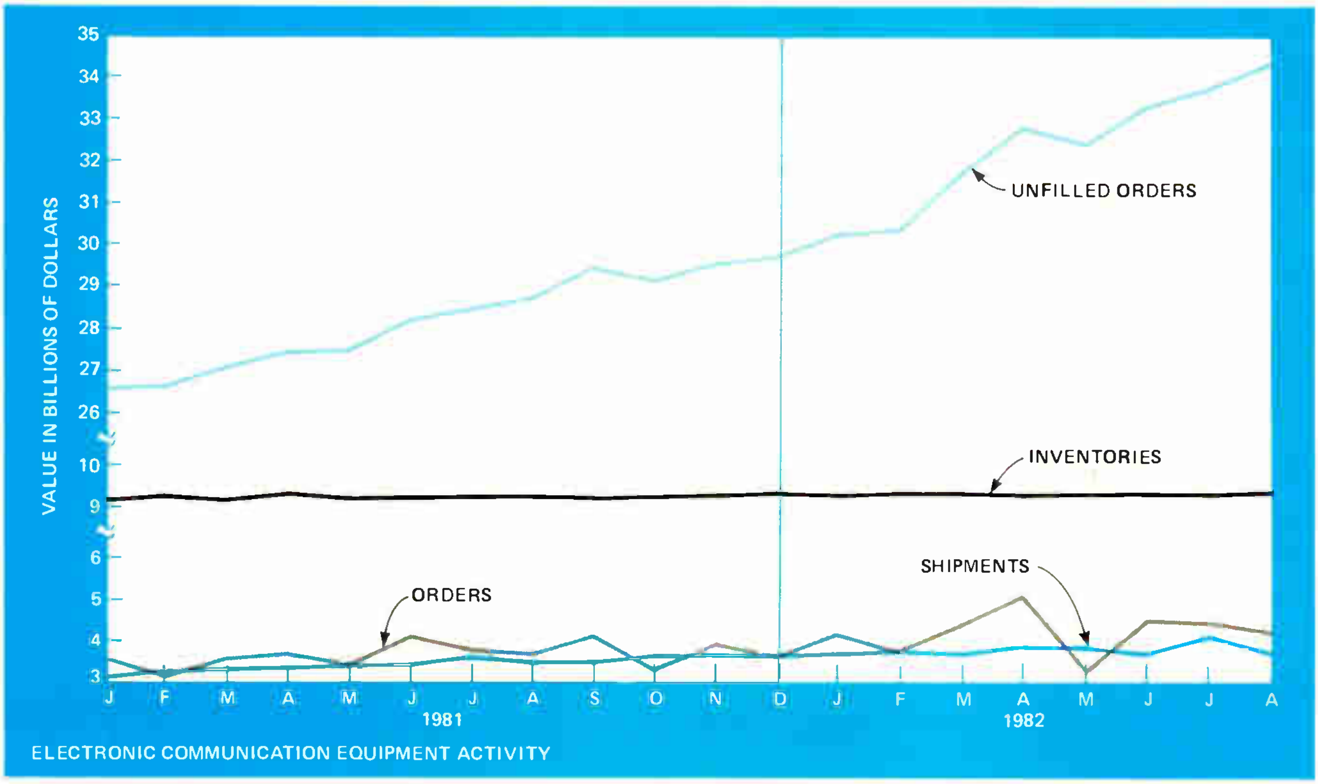
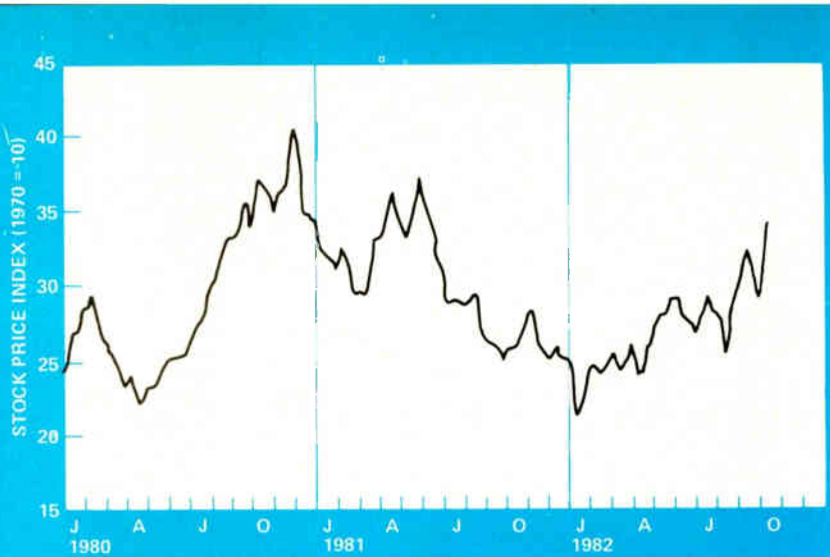






Business activity



TRENDS IN SEMICONDUCTOR AND COMPONENTS STOCKS
SOURCE: STANDARD & POOR'S CORP.

A rosy forecast of improving shipments in the semiconductor industry for 1982–85 has run afoul of volatile business conditions worldwide. According to the semiconductor trade statistics program (STSP), an effort sponsored by the Semiconductor Industry Association and the European Electronic Component Association, worldwide semiconductor shipments by U. S. and European manufacturers will grow 6% to $9.8 billion this year from $9.3 billion last year. In 1983, shipments are expected to grow another 18% to $11.6 billion, followed by a 21% rise in 1984 to $14.1 billion and a 23% gain in 1985 to $17.3 billion. However, the study was conducted in mid-August, and since previous estimates by the STSP have not always been borne out, the forecast rates of growth are not accepted by all industry analysts, nor even by the SIA.

Speaking on behalf of the trade group, National Semiconductor Corp. president Charles E. Sporck says, "The next few months look less optimistic than what this forecast says. I expect that the industry will remain flat for a minimum of six more months." A growth rate of less than 2% is more likely for this year, he said, with 1983 shipments increasing 14%. However, he sees 1984 shipments soaring about 32% and agrees with the STSP rate of growth for 1985.

A spate of orders in the second quarter of this year gave rise to a sense that the semiconductor industry was on the road to recovery, according to leading industry analysts. However, that optimism has since waned as orders have fallen once again to depressed levels. "The happy thoughts of spring have disappeared," notes Stanley Balter, an industry analyst with Herzfeld & Stern. "I see no sign, based on talks with users and suppliers, that there is any improvement. There seems to be a very low level of confidence that a sustainable upturn is within sight."

"We're looking for order recovery around year-end," reports Michael Krasko of Merrill Lynch, Pierce, Fenner & Smith Inc. Buying will be by distributors, he says, with original-equipment manufacturers starting to come in by mid-1983. However, a major problem facing the industry is pricing, according to Balter and to James Barlage of Smith Barney, Harris Upham & Co. "Pressure will continue on pricing," Barlage notes, because "excess capacity is not being absorbed by unit shipments." Balter points out that industry also has a substantial "nascent capacity, which could be brought up relatively quickly" and which would "keep prices unsatisfactory."

Semiconductor shipments could total between 4% and 6% this year, the analysts believe, and growth in 1983 could range between 10% to 20%. Though forecasting farther into the future would be "futile," as one observer put it, the analysts see major growth potential for the industry. "The semiconductor industry is poised for unprecedented growth in the next decade," Krasko says. Or, as Sporck puts it, "If we can hang on until the shipment curve takes off, then we will return to financial attractiveness."

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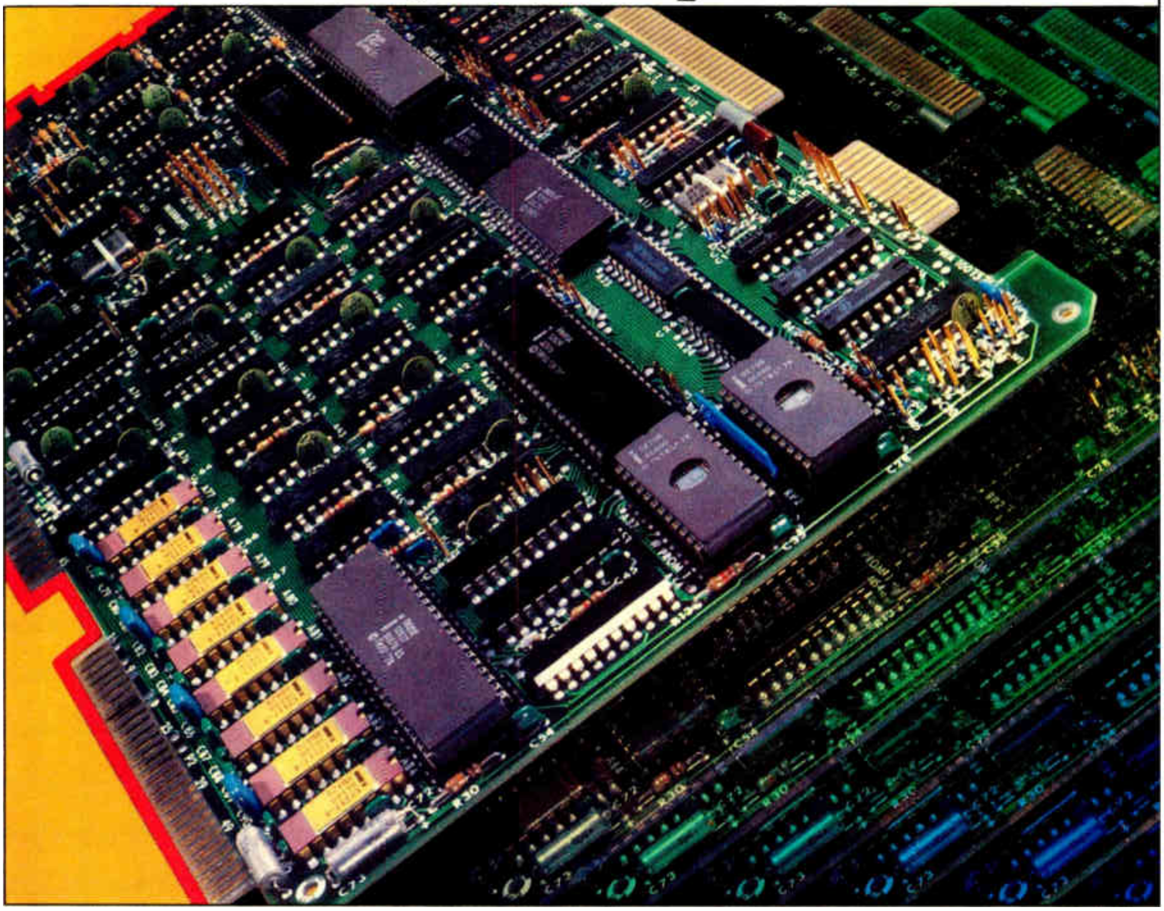

Electronics newsletter

Sperry enters office market . . .

The Sperry-Univac division of Sperry Corp. **has entered the office-automation market** with an integrated system called Sperrylink that initially will be sold to users of medium- to large-scale Sperry mainframe computers. **It includes a new Z80-based work station that can do CP/M-based personal computing** and stand-alone word processing, communications processing with mail and file services to connect small groups of what Sperry calls desk stations, and other services.

. . . with Northern net to be used by Sperry and DEC

At the same time, Northern Telecom Inc.'s Business Communication Systems operation in Richardson, Texas, has announced two agreements, one with Sperry and one with Digital Equipment Corp., designed to make Northern's SL-1 computerized private branch exchange compatible with Sperrylink and with DEC computers, **in effect making SL-1 the local network for such equipment.** Sperry has established a test site for the voice and data network at its Salt Lake City communications and terminal headquarters. DEC's first step will be to test the compatibility of its office products with Northern's equipment. The separate accords signal Northern's intention to aggressively seek more backers of its office-communications system; to that end it will make available interface specifications in an attempt to encourage design of compatible systems.

Frequency allocations, satellite slots cause international clash

As expected, a confrontation has emerged at the International Telecommunications Union plenipotentiary conference in Nairobi between the developed and the developing member states. By obtaining five seats more on the administrative council, Third World countries are attempting to dominate the meeting in a bid to secure a future place for themselves in the allocation of slots in the radio-frequency spectrum and in geostationary satellite orbits for telecommunications. Western nations, on the other hand, are seeking to safeguard their positions, **with the U. S. jockeying for support for such things as military radar space in the radio-wave spectrum** against countries seeking bands for TV and radio broadcasting. The U. S. is expected to take a tough stance at the meeting, with some delegation officials talking about reaching agreements outside ITU.

Antijam system gets 6-dB boost from a signal

The Naval Air Systems Command in Washington, D. C., has received a final contract report on a novel antijamming technique that improves communications performance as much as fourfold. Andrew J. Viterbi, president of M-A/COM Linkabit of San Diego, Calif., says the new technique, developed for coded frequency-hopping systems, allows digital communications systems to **overcome four times as much jamming power without increasing their own transmitting strength.** The Linkabit technique utilizes a signal-power–threshold formula to achieve greater reliability in identifying digital signals that have been subjected to interference.

Laser trimmer makes 200,000 cuts an hour

Automated laser trim systems for thick-film hybrid circuits will move to new productivity levels with the CLS-37 from Chicago Laser Systems Inc. Set for prototype demonstration at the International Society for Hybrid Microelectronics' meeting Nov. 15–17 in Reno, Nev., the system's ability to perform more than 200,000 passive trims per hour is nearly double the capability of current systems, the company says. **One secret of its speed is**

Electronics newsletter

a closed-loop beam-positioning system that offers better mirror control than the open-loop system in the Chicago firm's five-year-old CLS-33. Mirror-settling time, for example, drops from 25 ms to below 5 ms. A new Z80B-based controller, plus software enhancements, capitalizes on the faster beam-positioning system. Final pricing is expected to come in somewhat higher than for the earlier model, which typically sells for around $150,000. Delivery should start in the first quarter of next year.

Rockwell unveils first five parts in C-MOS effort

First production parts in Rockwell International Corp.'s new R65C00 complementary-MOS family will bow this month, with its Electronic Devices division offering five chips. **Three microprocessors are led by the R65C02—a pin-compatible C-MOS version of Rockwell's 8-bit 6502.** Two peripheral support chips make up the rest of this initial development with more to follow next year, according to the Newport Beach, Calif., division. Rockwell says it is on schedule in a strong move into C-MOS devices, announced earlier this year [*Electronics*, June 30, p. 54].

NCR microcomputer is Multibus-compatible

Departing from a computer-system philosophy that stressed proprietary peripherals and software, NCR Corp. was set this week to unveil the first in a series of products that will **rely more heavily on industry standards for compatibility with a broader range of equipment.** The initial version of the Dayton, Ohio, company's 68000-based microcomputer features a Unix 3 operating system and IEEE-796 (Multibus) compatibility. Called the Tower 1632, the multiuser, multitasking central processing unit is aimed at original-equipment manufacturers, but may be sold with peripherals as a replacement for the company's current low-end minicomputer products. Billed as a microcomputer with the performance of a mini, the Tower 1632 in its maximum configuration can house up to 2 megabytes of main memory and handle up to 1 gigabyte of mass storage.

Lasar test software adds timing check

Teradyne Inc. is adding a checkout for signal-propagation times to its Lasar software, which permits the engineer to simulate a design before building hardware. Up to now the system from the Boston, Mass., firm has been limited to checking out logic states. Lasar Version 6 is scheduled to be demonstrated later this month at the 1982 International Test Conference in Philadelphia. **It is outfitted with a special language for detailed timing characterization of board operations at both the gate and the chip levels.** Another package simulates application and propagation of dynamic test patterns for a board model and performs real-time analysis of timing patterns that could flag design or testability violations in a model. The primary license fee for Version 6 is $225,000; a secondary license goes for $75,000, with deliveries to start in June 1983.

Addenda

The first international meeting on **the use of lasers in microelectronic processing and device diagnostics** will be part of this week's Materials Research Society meeting in Boston. . . . Frank T. Cary, chairman of IBM Corp., referring to alleged thefts of proprietary information by Hitachi Ltd., warns **against rationalizing acceptance of such behavior because "everyone does it."** He spoke at a dinner at which he received the American Electronics Association's 1982 Medal of Achievement.

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The monolithic 7 bit parallel (flash) CMOS A/D converter operates at a sampling rate of 10 MHz while drawing only 150 mW of power. If the sampling rate drops to 1 MHz, the power drain of the Telmos TM 1070 may be reduced to 20 mW.

The actual operating current may be set from 15 mA down to less than 0.5 mA by adjusting one external bias resistor (excluding power in 4K ladder resistor).

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Overrange and underrange status lines indicate whether the input signal is above or below the input range of the converter. Nominal input voltage range is -3.2V to +3.2V.

Simple Interface

The TM 1070 may be simply interfaced to TTL, ECL, CMOS logic with output data lines driven by N-channel open drain MOS FETS and with the digital ground independent of the analog ground.

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- 10 MHz sampling rate
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- Open drain drivers
- Floating digital ground
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- High input impedance
- 4K ladder resistance

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Circle 43 on reader service card

pends on a set of algorithms similar to ones used in chess programs, like so-called alpha-beta pruning and minimum-maximum searches. Min-max techniques "look ahead" to determine the shortest and best testing path through the network maze; pruning is employed to weed out paths that need not be explored. "Min-max and other techniques are well understood in programs for game playing, but I'm afraid they are not so well understood in ATG because they have not been used here," says Kirkland, who used to write chess programs.

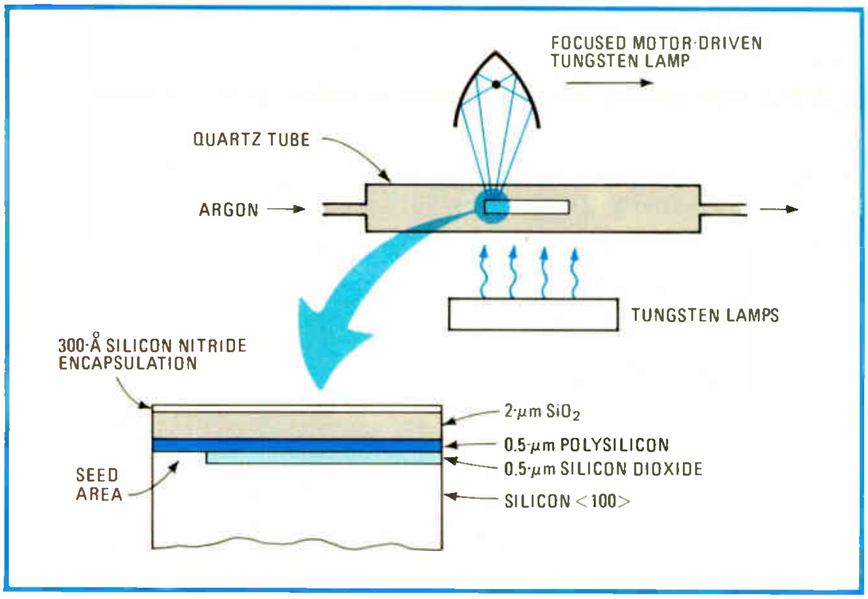
Fast grade. Coptr has been optimized for speed. Typically, the grading program can cover a complex board—like a central processing unit for a 16-bit minicomputer—in less than two minutes. Coptr can also examine circuits at several levels, including the basic gate level and higher levels of description, as an engineer might view layouts.

The ATG leg of the package, however, spends a little more time in the network, making decisions on testing paths based on clues left behind by Coptr. With its nine-valued algorithms, the program can more accurately examine and produce test patterns on highly sequential elements, such as counters and shift registers. (Tegas' current ATG capability uses five-valued algorithms.)

Production

Lamps are hot for silicon-on-insulator

With their superior packing densities and potential for high speed, integrated circuits made of silicon deposited on an insulating substrate may prove ideal for very large-scale integration. However, a major obstacle to the technology has been how to melt the deposited polysilicon so it recrystallizes into the single-crystal layer in which devices can be fabricated. Lasers, electron beams, and graphite strip heaters [*Electronics*, June 2, p. 45] have all been applied to this purpose.



Hot light. Tungsten lamps below the silicon-on-insulator wafer and a moving lamp focused from above melt a zone that moves across the polysilicon, creating a single-crystal layer.

Now, however, bright incoherent light from tungsten or halogen lamps is emerging with promise as a fast, low-cost means for achieving the crystallization. At a recent workshop on silicon-on-sapphire and silicon-on-insulator technology [*Electronics*, Oct. 6, p. 41], Bell Laboratories, Murray Hill, N. J., and Centre National d'Etudes des Télécommunications (CNET) in Meylan, France, reported similar experimental techniques for recrystallization with incoherent-light sources.

Tungsten. The Bell process uses the heat from tungsten lamps to recrystallize the silicon. Wafers are processed with a 0.5-micrometer layer of silicon dioxide thermally grown atop a silicon substrate. A 0.5-μm film of polysilicon is deposited on the silicon dioxide to create a seed area where the polysilicon contacts the bulk single-crystal silicon, as shown in the diagram. The polysilicon is encapsulated by a 2-μm-thick layer of silicon dioxide and a 300-angstrom layer of silicon nitride.

The wafer is placed in a rectangular quartz tube flushed with argon to ensure an uncontaminated environment, explains Avid Kamgar, a member of the technical staff at Bell Labs. Light from six tungsten lamps heats the wafer from below to a temperature of approximately 1,200°C. Additional heating to bring the wafer to the 1,750°C melting point of silicon comes from a motor-driven tungsten lamp 2 inches above the wafer, whose light is precisely focused in a line by two elliptical polished-aluminum reflectors. The moving-line heater begins melting at the seed area and moves across the wafer surface at approximately 0.5 millimeter per second. The entire wafer surface is melted and reformed as single-crystal silicon.

The CNET technique differs chiefly in its use of halogen lamps instead of the tungsten-filament type employed by Bell. Also, CNET has recrystallized somewhat smaller areas.

Kamgar reports the creation of a single-crystal layer on 3-in.-diameter wafers and is currently working on extending the process to 4-in. ones. Neither CNET nor Bell reports the fabrication of devices at this point. "We are in the process now of fabricating various test circuits in these films, but it is too early to report results," says Kamgar.

Fewer problems. She claims that the incoherent-light technique is cleaner than the one using graphite strip heaters, which may contaminate the silicon with silicon carbide. Laser and electron-beam methods, she notes, are more costly and take longer than heating with the lamp light. Kamgar feels that her technique will eventually prove superior in handling larger wafer sizes.

Looks good. Another researcher in the field, Lubek Jastrzebski, a member of the technical staff at RCA Laboratories in Princeton, N. J., points out that the tungsten lamp promises higher throughput than laser-based systems because the laser's beam is so narrowly focused. For the laser to heat wider areas, power must be increased, but this produces another problem: at sufficiently high powers, the beam is hotter at its center than on its fringes. This creates uneven heating patterns and surface temperatures.

At the Massachusetts Institute of Technology's Lincoln Laboratory in Lexington, Mass., John C. C. Fan, assistant group leader of the electron materials group, describes the incoherent-light approach as "very interesting," but he is not ready to concede its superiority. He notes, for instance, that his lab has been successful in controlling contamination from graphite heaters and has actually fabricated devices and circuits.

"It's another way to skin the cat," he says of the incoherent-light technique, "but it will take another year or two before people can make a determination as to which is really the best." And Fan adds that "we may well find that there are users for all these techniques depending on the particular device structures that are involved." **-Norman Alster**

Magnetoencephalograms: a new brain check

Medical researchers continually look for new ways to diagnose disorders deep inside the human body "noninvasively," that is, without resorting to surgical procedures that insert sensors. One of the latest of such techniques is the magnetoencephalogram, which can pinpoint disorders within the brain, something the widely used electroencephalograms cannot do.

At the University of California at Los Angeles, for example, doctors are using squid-generated magnetoencephalograms (MEGs) to locate the sources of epileptic discharges deep within the brain. Such MEGs yield precise information on the location and depth of the paroxysmal activity that often precedes and predicts epileptic attacks. The noninvasive MEG offers the hope of supplanting the arduous and risky procedure of implanting electrodes inside the cerebral cortex of an anesthetized patient to obtain electroencephalograms, which chart the brain's electrical signals.

Dr. Jerome Engel Jr., professor of neurology at UCLA, estimates that as many as 100,000 epileptic candidates for surgery could eventually benefit from these noninvasive MEGs. 'We are looking at patients with focal (partial) epilepsy who may require surgery. Between seizures, an area within the cortex of a focal epileptic may produce localized paroxysmal transients, called interictal spikes," explains Dr. Engel. "In most cases, the interictal spikes indicate the source of the general seizure."

The hypersensitive squid can distinguish between the brain's normal magnetic fields of 10^{-13} tesla and the magnetic fields produced by the interictal spikes, which are of the order of 10^{-12} tesla. Having mapped the patient's cortical magnetic fields through a series of 20 to 40 MEG readings, surgeons can then target the appropriate area without exploratory electrode implantation inside the skull. Already, MEG readings of six focal epileptics have accurately established the location, depth, polarity, and orientation of currents within the discharging areas.

Eventually, MEGs may also prove useful in assessing epileptic drug treatment programs, notes Dr. Engel, since recent research indicates that successful therapy provokes changes in the shape and field of the spikes generated. Other members of the UCLA team are Dr. William Sutherling, Jackson Beatty, and Daniel S. Barth. **-N. A.**

Research and development

Squids search out brain dysfunctions

Up until now, superconducting quantum interference devices (squids), whose Josephson junctions can detect and measure very weak magnetic fields with great accuracy, have not found much use outside research laboratories. But new dc versions of squids that improve response by an order of magnitude may yet propel these little-known components out into the real world.

SHE Corp., a San Diego firm that has fabricated squids since its start in 1970, is now readying commercial versions of the dc type. They can measure magnetic fields down to levels so low—two hundreths of a billionth of the earth's field—that medical researchers think they can use them as sensors in magnetometers to pinpoint problems within the human brain (see "Magnetoencephalograms: a new brain check"). Says Eugene Hirschkoff, the firm's senior vice president, "The odds are great you'll see [dc-squid magnetometer] systems in all major hospitals by the end of the decade." Commercial models, the first of their kind, Hirschkoff says, will be out next April; the basic dc-squid detector will sell for $14,000 or so. Complete magnetometer systems built around squids are also in development.

The dc squid measures fields down to 10^{-15} tesla, some 10 times better than its predecessors, radio-frequency squids. These earlier versions were based on a single superconducting Josephson junction, which is formed by separating two layers of superconducting material by a very thin layer of insulation. The junction acts as the controlling link in a niobium-ring secondary loop of a tank circuit excited by a 20-megahertz oscillator. As the external magnetic field changes, the superconductivity of the controlling link is altered. This allows the secondary loop to absorb energy from the tank circuit, lowering its Q. Very low-level fields can be measured by monitoring the Q and feeding calibrated current into the squid to null the external field.

The noise levels, and hence the sensitivity, of rf squids drop as their operating frequency rises, explains

Duane Crum, vice president for marketing. To get the 10× improvement of the dc squid, SHE boosted the frequency. However, rather than using a higher-frequency oscillator, it relied on the fact that a Josephson junction develops superconducting alternating currents at gigahertz frequencies when a small dc voltage is applied across it. To take advantage of the effect in the dc squid, SHE beats the frequencies of two junctions that are in a ring about 1 millimeter in diameter on a substrate about 0.5 by 0.5 mm. The squid is at 4 to 6 Kelvin, a temperature obtained by a liquid-helium bath or a closed-cycle refrigerator.

Along with the much higher sensitivity, another improvement in the squids is their increased reliability. Early versions of the Josephson junction used in the rf squid were made by machining tiny rings of niobium. The firm has since graduated to standard semiconductor processes, using thin-film techniques to lay down the niobium rings and the proprietary insulator that make up the junction. "We haven't had a single failure with rf squids since we started using thin-film processing two years, ago," says William Black, SHE's president. **-Arthur Erikson**

Education

Plato takes aim at small computers

In development for some 20 years with not a penny of profit to show, the Plato computer-based instruction system from Control Data Corp. is being hitched onto a new star. It is hooking up with the fastest growing segment of the computer industry—low-cost microcomputers.

Last month, the Minneapolis-based company announced plans to supply packages of elementary- and secondary-level Plato courses to run on the Apple II Plus, the 99/4A from Texas Instruments Inc., and the Atari 800. Supplied on 5¼-inch floppy disks, the packages will sell for $45 for the first course and $35 for each additional one.

Small fry. Control Data Corp. is converting its Plato educational-course software for use on microcomputers like the Apple II Plus machine shown in the photograph.

"We realize our microcomputer [the Control Data 110 introduced last year for $4,995 and up] won't compete in every segment of the market," explains Thomas W. Miller, CDC vice president for business development. But by adapting existing Plato-based courses to run as stand-alone packages on lower-cost machines, CDC hopes to cash in.

Indeed, the potential is there, notes Egil Juliussen, chairman of Future Computing Inc., a Richardson, Texas, consulting firm. He projects that sales of educational software for use on personal computers at home and in schools will surge from about $50 million this year to nearly $800 million in 1987. Likewise, on the hardware side, personal-computer sales into educational markets are expected to jump to about $1 billion by 1985, up from only $180 million in 1982, says Kenneth T. Lim, a research analyst at Dataquest Inc., Cupertino, Calif.

Catching up. Until last year, the delivery of Plato instructional material was limited to centralized systems employing CDC mainframe computers and dedicated time-shared Plato terminals, an approach that has failed to earn passing marks from most educators because of its relatively high cost. As a result, the firm derives only about 12% of its Plato revenues from the academic market, the remainder coming from vocational and industrial training. Total sales in 1981 were about $90 million, and profitability is not expected before 1984.

Time is of the essence in the Plato push, CDC's Miller notes, since a number of new competitors, including traditional textbook publishers, are moving into the microcomputer-based course-publishing business. In addition, the company wants to move quickly to head off a perceived backlash among academic users with recently purchased microcomputer hardware who have found the existing course offerings for the units to be inadequate.

Miller will not predict how quickly the company will adapt its Plato library of 8,000 hours of programs for stand-alone microcomputer use. But during the first half of next year, he promises, CDC will "add substantially" to the nine academic packages, which include physics, foreign-language vocabularies, elementary numbers, and computer literacy, being released for the Apple, Atari, and TI units.

New approach. CDC's drive to apply its Plato software to microcomputers is only one of several steps taken by the firm recently in an effort to broaden the Plato delivery base. Last May, for example, the company announced a separate agreement with TI by which the Dallas-based company will manufacture and distribute a broad range of 99/4A-compatible Plato software beginning early next year. In addition, CDC made Plato available for the first time as an application on a general-purpose computer with the introduction of its Cyber 170 series 800 mainframe earlier this year [*Electronics*, May 5, p. 40].

Overall, CDC has sunk some $900 million into its educational projects over the last 20 years. Plato represents "a sizable portion," the firm says. **-Wesley R. Iversen**

Gallium arsenide

GaAs symposium struts useful stuff

Stressing the commercialization of the high-speed technology, the 1982 Gallium Arsenide Integrated Circuit Symposium gets under way next week, Nov. 9–11, in New Orleans. Two sessions on ICs and a third on fabrication technology highlight the technical program that has been put together by the Institute of Electrical and Electronics Engineers. Those will be joined by presentations on optoelectronics, materials, analog circuits, and power ICs.

Sessions 1 and 5 on digital ICs, chaired by R. E. Lundgren of Hughes Research Laboratories, Malibu, and D. K. Kinell, Lockheed Missiles and Space Co., Sunnyvale, both in California, show that researchers are nearing mastery of medium-scale integration of GaAs.

Among the first real applications of the material could be cache memories for fast computers. Along those lines, a 1-K static random-access memory using both depletion- and enhancement-mode devices will be discussed by the Musashino Electrical Communication Laboratory of the Nippon Telegraph & Telephone Public Corp. Another company adding enhancement-mode transistors to its capabilities, Texas Instruments Inc., will report on the status of memory technology at its Central Research Laboratory in Dallas.

Several firms have realized that, as with silicon, gate-array designs will be well suited to the low-volume orders likely for actual GaAs products, at least early on. TI, for one, has chosen to make bipolar arrays based on heterojunction transistors in integrated-injection-logic gates. Lockheed will describe a 320-gate array made with Schottky-diode, field-effect-transistor logic.

Two from Tek. Instrumentation applications are also high on the list of priorities for GaAs developers. High-speed sampling and switching will be reported in two papers from Tektronix Inc., Beaverton, Ore. One details a three-gate metal-semiconductor FET switch that is employed in a sample-and-hold circuit; the other paper discusses an 8-bit multiplexer and demultiplexer.

Engineers testing the fastest silicon ICs will also be turning to GaAs. Hewlett-Packard Laboratories, Palo Alto, Calif., will give details on a bit-stream generator and a recurrence-relationship test chip that operate at 2 gigabits a second.

Session 7, IC fabrication technology, chaired by R. A. Murphy of the Massachusetts Institute of Technology, Cambridge, has Rockwell International Corp., Thousand Oaks, Calif., reporting on the manufacturing problems and yields of GaAs chips. Also in that session, Bell Laboratories, Murray Hill, N. J., will tell of a self-aligned 1-micrometer-gate FET that switches in under 30 picoseconds. **-Roderic Beresford**

CP/M-based disks supply application notes

With the ever-increasing complexity of integrated-circuit products, explaining how they work and, more importantly, how to use them is also becoming an arduous task. National Semiconductor Corp. is taking a unique route in getting applications information to designers: it is putting it—accompanied by step-by-step, fill-in-the-blanks forms—on 8-inch single-density disks compatible with CP/M, the operating system of many popular 8-bit personal computers and development systems.

According to Bob Nelson, memory applications engineer for the Santa Clara, Calif., firm, "Today's devices have gotten so complex that the number of different ways a part can be used is becoming too great to document on paper in the traditional way." Called ACT (for applications for computer terminals), the new applications-note disks will sell for $95 each. All the designer needs is a computer that runs CP/M.

The first in the ACT series—called, naturally enough, ACT-1—deals with designing memory systems around National's DP8400 error-correction chip. This chip is used in large memory systems to ensure the integrity of the data. It catches and flags errors in memory or it can catch, flag, and correct errors in memory on the fly. In addition, the chip can be configured in hundreds of ways, depending on the memory size, address codes, and word length.

ACT-1 defines every usable single-bit error code and selects and stores on disk the most efficient code for any number of error locations. It also lets the designer print out any defined code and the proper IC pin interconnections for implementing it.

"If this definition process could be performed manually at all, it would take many man-years," says Nelson, the architect of the DP8400 and creator of ACT-1. "This program is the first of its kind—engineering software designed by engineers for engineers." Subsequent ACT packages will aid designers working with National's speech-synthesis parts, programmable logic arrays, gate arrays, active filters, and power supplies. **-Stephen W. Fields**

Solid state

Gate arrays attract well-heeled entry

After two years of well-funded preparation, Fairchild Camera & Instrument Corp.'s gate-array operation is ready to meet the public as a full-fledged division of the company. Fairchild's parent Schlumberger Ltd. footed the bill—estimated by observers to exceed $20 million—for the development of computer-aided design tools, a design service center, and products that include 1.25-micrometer-geometry emitter-coupled logic arrays. Now the new division must make money in a market for high-speed gate arrays that is dominated by Motorola Inc.'s Macrocell line.

Based in Milpitas, Calif., the Gate Array division is headed by general manager Ed Caldwell, who reports to Jean Boucau, the executive vice president and general manager of Fairchild's LSI Products Group.

In place. "We now have about 60 people in Milpitas," says marketing manager Martin Harding, "and expect to grow to over 100 in the next two to three years." A second design center in Reading, England, duplicating the Milpitas facilities, will be opened in January 1983. Harding expects Fairchild will probably add one more center, on the East Coast of the U. S.

The Milpitas operation keeps three Digital Equipment Corp. VAX 11/780 computers and a Floating Point Systems array processor busy running design software, which is a mix of commercially available and proprietary programs. A program for test-vector generation is in development at Fairchild to provide input tapes for Sentry-format automatic testers. Customers sign up for training with the CAD system for about $2,000 and then contract for specific production runs.

"In time we'll favor a work-station approach," says Harding. Like other gate-array vendors, Fairchild is evaluating current engineering work stations, in the hope of selecting one or more as standard tools for remote design work. **-Roderic Beresford**

Military

EIA cranks down earlier forecasts

If the Electronic Industries Association is on the mark with the latest version of its respected 10-year forecast on U. S. defense spending, growth will not be nearly as steep as predicted by the Reagan Administration. The new forecast (adjusted for yearly inflation of about 6%)

News briefs

Navy resumes funding of ELF

ELF is back, and GTE/Sylvania Systems Group again has got the Naval Electronic Systems Command contract. The $5.25 million award to the Waltham, Mass., organization calls for a full-scale development model of the extremely low-frequency system for communicating with submerged submarines. Now pegged to cost $231 million, ELF will include new receivers for the U. S. missile-carrying submarine fleet. Using a 28-mile underground antenna grid already in place, the Clam Lake, Wis., site will be upgraded to operational status by 1985 to serve the Atlantic submarine fleet. The Pacific will be covered by a 56-mile antenna to be installed above ground at Sawyer Air Force Base in Michigan. First known as Sanguine, then in 1977 as Seafarer, the controversial ELF program stalled when local residents protested, calling it a radiation hazard. The Navy expects to avoid protests by putting new construction on public lands and in state forests.

Programmable calculator a question at TI . . .

Five months after unveiling its new high-end programmable calculator, Texas Instruments Inc. is still trying to decide whether to market the TI-88 [*Electronics*, June 2, p. 42], originally scheduled for availability in the third quarter. Consumer electronics officials in Lubbock, Texas, continue to wrestle with the fact that sales of keystroke-programmable calculators have been severely depressed by pocket computers, which feature alphanumeric keyboards and Basic programming.

. . . as business overall advances

Meanwhile, corporate leaders in Dallas say third-quarter consumer and semiconductor sales continued to show improvements over last year, as TI's net income rose 36% to $36.9 million. Its government electronics business was strong, but distributed-computer, metallurgical-material, electrical-control, and geophysical-seismic activities all slumped in the period. "Third-quarter orders for semiconductors remain above year-ago levels, but were down from the second quarter when distributor orders were at peak," the company reports. Sales of MOS 64-K dynamic random-access memories grew, but bipolar products suffered a drop in demand and price, it says.

16-bit digital audio recorder sells for $5,000

A professional-quality digital audio recorder that sells for $5,000, a fifth the price of today's models, is in the works at dbx Inc., Newton, Mass. The model 700 Digital Audio Processor achieves a dynamic range of more than 110 decibels by employing an improved delta-modulation analog-to-digital processing technology that is inherently cheaper to implement than the linear pulse-code modulation used in present 16-bit recorders, according to dbx. In tests at recording studios, the model 700 has proven itself the equal of $25,000 instruments, with good frequency response and low distortion, the company says. Its 110-dB dynamic range, in fact, exceeds the 90 dB of linear PCM recorders. The recorder was announced at the Audio Engineering Society convention in late October at Anaheim, Calif.; volume deliveries are to start next May.

Solid-state power amps a first for RCA Satcom

The first commercial communications satellite to use all-solid-state power amplifiers was set for launch from Cape Canaveral, Fla., at the end of October. When orbited and operating, the Advanced RCA Satcom will be sold to Alaska's long-lines carrier, Alascom Inc., to provide intra- and interstate services. Operating in C band, the satellite contains 28 gallium arsenide amplifiers putting out 8.5 watts each in a redundant configuration for 24 operating channels, according to Jack A. Frohbieter, director of satellite programs for RCA Astro-Electronics, Princeton, N. J. Each of four electronic power conditioners containing two dc-to-dc power converters supplies power on 8.5-, 3.5-, and −3.0-V buses.

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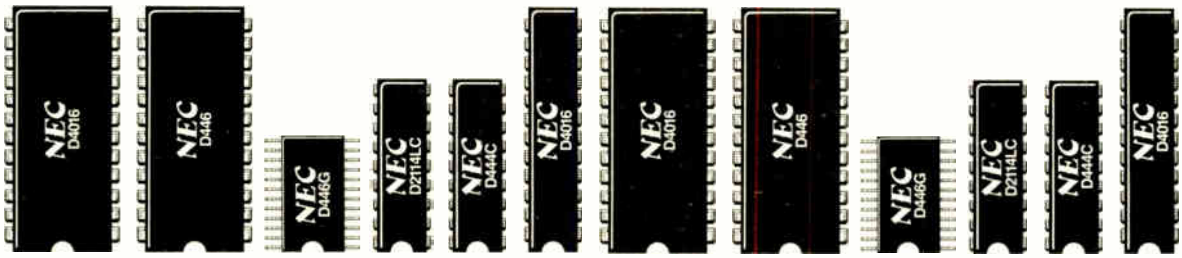

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looks for spending to increase annually through 1992 at 4% to 5%, rather than the Administration's 7%.

The cause of the shortfall is a simple one, William A. Heuslein of Grumman Aerospace Corp., Bethpage, N. Y., told the EIA's fall symposium on the defense electronics market late last month in Los Angeles. "There are not enough dollars to do all the jobs," he explained.

Along with Wesley S. Sherman of GTE Products Corp., Arlington, Va., he presented the predictions, which are compiled from many Government and industry sources by an EIA committee. The forecast is valued by industry planners because it is considered more accurate than Government projections.

Crunch next year. Heuslein pinpoints fiscal year 1984, beginning next October, as the period when the spending crunch will hit and predicts major programs will be canceled due to fierce competition for funding. He did not offer specific examples, but uncertainties about the MX missile caused the forecast on missile spending growth to be cranked down to a 5.5% annual rate from 9.1% in the 1982–91 forecast, it was noted at the meeting.

Although any such cutbacks would eventually affect the electronics industries, for the time being military electronics is projected at a solid 6.5% growth rate, with steadily increasing percentages of total Department of Defense research, development, test, and evaluation outlays. For fiscal 1982, total electronics RDT&E stands at $29.3 billion, or 34.3% of the category's total.

In fiscal 1983, the value should grow to $37.2 billion, or 35.1%, according to the forecast. These figures are consistent with earlier DOD forecasts [*Electronics*, Feb. 24, p. 89]. By 1992, the figures should rise to $65.2 billion and 42.1% of total RDT&E spending.

One category maintaining strong annual increases is space equipment, reflecting numerous programs to develop and deploy military gear in what has been the bailiwick of the National Aeronautics and Space Administration. Annual growth is put at 8.9%, little down from 9.3% in the previous forecast.

Electronics content will grow only slightly in the space field, from 67% to 69.5% in 1987, but total spending looks to take off for the period. It is $4.3 billion in 1982, going to $7.6 billion in 1987, as the Reagan Administration moves to create a new space weapons capability [*Electronics*, July 14, p. 70].

The EIA projections take issue with some other Administration assumptions, those replacing manpower with investments in technology. The reason: the military "always opts for men rather than equipment," notes GTE's Sherman. Also, the EIA expects the Air Force will get only 40 wings of fighter aircraft, rather than 44, and the Navy, 14 carriers instead of the 16 it wants—both anticipated compromises with Congress. **-Larry Waller**

Personal computers

School picks IBM to design work station

International Business Machines Corp. emerged as the successful bidder last month in a joint venture with Carnegie-Mellon University to develop an advanced personal computing network at the school. The deal is typical of a trend among technically oriented colleges and universities to require students to have their own personal computers [*Electronics*, Oct. 20, p. 50]. But this deal goes beyond those announced by other schools. Integrated into a network, the stations will offer capabilities far beyond those of personal computers currently on the market. And there will be more than one work station per student so students can access stations around campus.

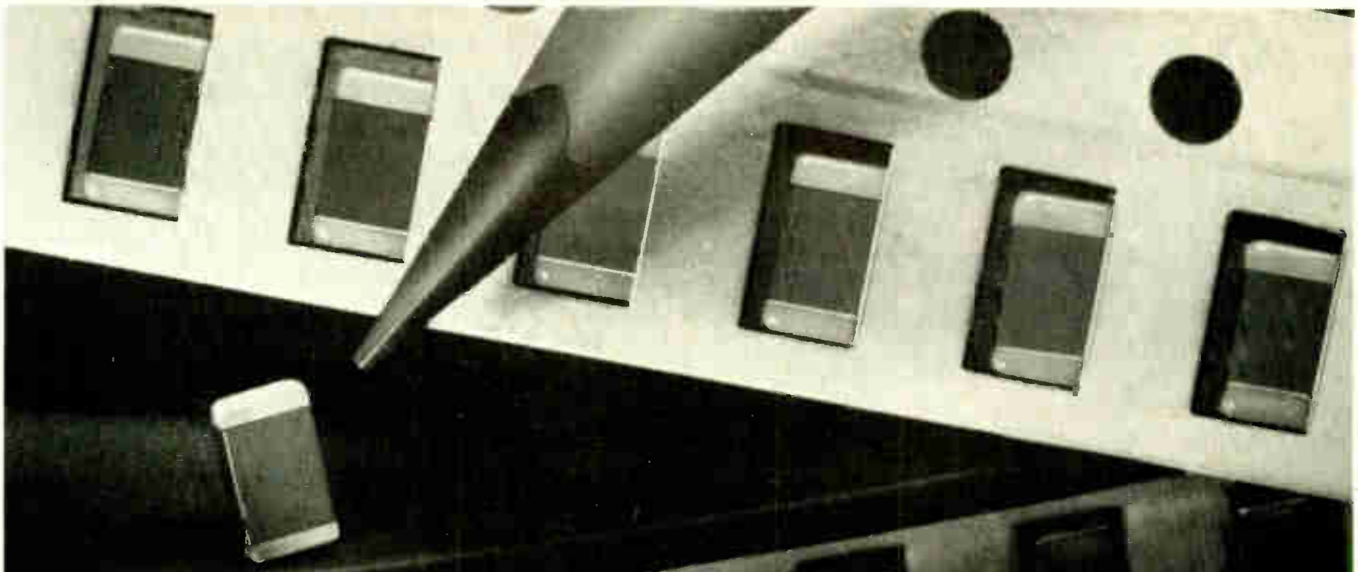
As expected, the school chose a 32-bit work station with a virtual addressing range of up to 1 billion characters, an execution speed of up to 1 million instructions per second, 500 kilobytes to 1 megabyte of main memory, and a high-resolution bit-mapped graphics display with both graphics tablet and keyboard input. A work station with such capabilities would likely sell in the $20,000 range on the open market today. However, the IBM unit is expected to cost about $6,000 by late 1985 when the university plans to begin installing the units on campus, says Douglas Van Houweling, Carnegie-Mellon vice provost for computing and planning.

Carnegie-Mellon eventually plans to hook up between 7,500 and 8,000 work stations on its Pittsburgh campus. In the interim, the university is evaluating several work stations, including one built by IBM's Instruments division around a 16-bit Motorola 68000 processor and a bit-mapped graphics display.

From IBM. Under terms of the joint venture, IBM will develop all hardware for the project and will provide staff members to work with Carnegie-Mellon personnel at an Information Technology Center to be established on the campus to develop the network software. In all, the Armonk, N. Y.-based company expects to spend about $20 million during the three-year development period and in return will own all patents and copyrights.

According to Keith A. Slack, IBM program manager for the project, the company currently favors a local-network scheme for the system that is consistent with the baseband token-passing access-control approach that IBM has presented to the 802 standards committee of the Institute of Electrical and Electronics Engineers. Texas Instruments Inc. has announced joint plans with IBM to develop interface chips using n-channel MOS and low-power Schottky technologies [*Electronics*, Sept. 22, p. 41].

The Carnegie-Mellon setup is also expected to rely on a totally new operating-system environment that will be optimized for distributed personal computers. Among its proposed features will be the use of central file servers, instead of built-in disk storage located at each work station. This setup will enable system users to access files from any work station. **-Wesley R. Iversen**



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Washington newsletter

First DBS service set for 1986 using RCA satellites

The first pay-television service transmitted through direct broadcast satellite (DBS) technology is set to begin in early 1986. That is when Satellite Television Corp. plans to launch two satellites, one a spare, to serve the eastern U. S. They will be built by RCA Corp.'s Astro-Electronics division of Princeton, N. J. Satellite Television, a subsidiary of Communications Satellite Corp., awarded RCA a contract worth more than $100 million for the two satellites—**with options for four more to serve the rest of the country.** The satellites will carry three traveling-wave-tube amplifiers with 200-W minimum outputs for each channel, plus three spares. The amplifiers, said to be 20 to 40 times more powerful than those on conventional satellites, will be coupled to advanced shaped-beam antennas to permit home reception by rooftop antennas with diameters as small as 2 ft. The satellites will use the 17.3-to-17.8-GHz band for the uplink and broadcast at 12.2 to 12.7 GHz. The Federal Communications Commission, which granted Satellite Television's application at the end of September, indicates it will act on the remaining eight DBS proposals soon.

EIA unit formed for personal computers and video games . . .

A new computer division formed by the Electronic Industries Association's Consumer Electronics Group expects to expand its membership by up to 25 companies in the personal-computer and video-game business. EIA/CEG has 70 members now, including about 15 makers of personal computers and games. The new division, chaired by Casio Inc.'s John McDonald, also expects to develop a data base on U. S. sales of personal computers and video games, with public dissemination beginning about 1984. International Business Machines Corp.'s Personal Computer operation, which exhibits at EIA/CEG shows, is targeted for a membership pitch by the new division.

. . . no EIA vote on trade stance; January briefing set

Senior Government and industry trade analysts will brief the Electronic Industries Association's board of governors on international-trade issues when it meets in Phoenix, Jan. 19–23. The briefing was set up in Los Angeles at the board's meeting last month, says EIA president Peter McCloskey. Contrary to an earlier report on that meeting [*Electronics*, Oct. 20, p. 67], the governors did not vote on controversial trade-policy proposals by the EIA's International Business Council. **The council had urged the governing board to call for stiff and retroactive Government penalties against imports from Japan,** relief for damages for U. S. manufacturers, and the opening of Japan's domestic markets, as well as for changes in rules of other countries that constrain U. S. investment there.

Cellular approval still under appeal

Insiders at the Federal Communications Commission believe its conditional approval of the nation's first cellular mobile telephone system may be blocked in court. Awarded to a Chicago subsidiary of the American Telephone & Telegraph Co., the approval calls for early 1984 start-up. However, the October award to Advanced Mobile Phone Service Inc. **is subject to a Federal appeals court ruling on the FCC's earlier decision** to set aside one of the two cellular channels in each of the top 30 markets for local phone companies [*Electronics*, June 16, p. 47].

The high price of defense

Students of congressional inaction who thought the military appropriations process this year came as close to paralysis as possible are in for another lesson come January. That is when President Reagan is expected to unveil his fiscal 1984 Department of Defense budget request with outlays of more than $242 billion—nearly 13% more than the request for fiscal 1983, which began in October.

A growing body of Senate and House members, including Republicans and fiscal conservatives of every stripe, stand ready to slash that level of spending on the grounds that the nation cannot afford it. Moreover, they are convinced that the country's industrial base, severely weakened by recession, could not absorb the funds even if the military were to get them. It is an argument that was advanced a year ago [*Electronics*, Sept. 22, 1981, p. 56], although the chorus is larger and louder now.

California's conclusions

Industry's acknowledgment of slowing growth in the military electronics market is contained in the latest forecast presented in Los Angeles last month by the Electronic Industries Association's Government division (see p. 50).

Perhaps more interesting for Capitol Hill is the less well-publicized conclusion earlier this year by State of California economists that, despite that state's commanding lead in military contract awards, the Reagan military budget plan through 1986 would leave California a net employment loser. Titled "The Effect of Increased Military Spending in California," the study by the Office of Economic Policy, Planning, and Research concludes that, dollar for dollar, military increases create far fewer jobs than nonmilitary market growth.

California's electronics companies will be especially hard-pressed to find people with the particular skills required to fill their military obligations, the report notes. Though engineers and skilled technicians are available as a consequence of the recession, a recovery in the domestic economy coupled to military spending increases "will result in a bidding up of wage costs, reducing the ability of civilian firms to compete in world markets," the economists contend. To those engineers and employers who say that they would welcome such problems of abundance, congressional analysts point out that the California study is examining the impact of military spending over a five-year span.

Another concern in the state that captured 19.3% of direct military expenditures in 1980 is the concentration of that business in only 10 counties. Just under 57% of the total goes to companies in three counties, with Los Angeles taking nearly one third, followed by San Diego's 13.2% and Santa Clara's 11.5%. If that historical distribution pattern is followed in the proposed Reagan budgets, increases in costs of living and services would make the region even less appealing to employers and employees alike. These, say the Californians, are some of the perverse results of their analysis.

Too many jobs

The problem of finding talented electronics specialists to serve both the military and the world's civilian markets—assuming the latter's recovery—is not peculiar to the West Coast. The dramatic nature of the problem is, however, well illustrated there.

For example, if California maintains only its historical share of military spending—and the effects of such proposed massive projects as the MX and Trident missiles and the B-1 and Stealth aircraft are excluded—the study estimates that jobs will triple between 1982 and 1983 in such fields as communications equipment, computers, components, and scientific instruments. Through 1986 the multiplier for new jobs in those technologies is closer to 10. In terms of electrical engineers alone, the California share of the Reagan military budget will create 12,695 new jobs, says the study, although the state will probably graduate only 11,500.

Economic priorities

The recession seems certain to skew those numbers. Also, some in industry and the Federal government say the figures were skewed at the start, a distortion that at least one Reaganomics advocate attributes to the influence of Gov. Jerry Brown.

The point of the exercise now, however, is not whose numbers are most credible. It is whether the national economy—and the electronic technologies at its forefront—can afford to be further unbalanced by unrealistic military demands. Federal deficits of more than $150 billion annually deserve higher priority, for they are proving to be the greatest threat to national security. **-Ray Connolly**

How Texas Instruments and Mitel team up for the last word in communications.

An advanced work station now ties together virtually all forms of modern communications with word and data processing. In one compact package.

Developed by the Mitel Corporation, with a strong assist from Texas Instruments, the desk-top station offers outstanding communications capabilities to the general office.

TI helped make the station possible by supplying early samples of its new TMS4416 64K DRAM, organized 16K x 4. The ByFour™ organization provided highly efficient memory utilization and essential space savings.

Turn the page to see how 16K x 4 memory organization can result in more efficiency and space savings for you. ▶

TI's new memory

With four times the bandwidth of 64K x 1 dynamic random access memories (DRAMs), and four times the memory density of 16K DRAMs, TI's new TMS4416 16K x 4 DRAM opens enormous new design opportunities.

The ByFour organization — the first of its kind — allowed engineers of Mitel Corporation to achieve dramatic board space savings in their new Integrated Communications System (ICS).* While it increased system efficiency and reliability.

The Mitel Integrated Communications System consists of the SX-2000,* Mitel's newest, most sophisticated digital PABX. And its companion SUPERSET 7* work station, which combines communication functions including telephone, electronic mail, word processing, data processing, and local computing power into one totally integrated communications package unlike anything else on the market.

The multi-functional SUPERSET 7 allows people to simultaneously access and share voice, text, and image information through a friendly, compact work station.

ByFour organization cuts parts count

Memory for the data terminal's high-resolution graphics posed problems for Mitel's engineers.

To combine many types of communication into one streamlined work station, Mitel needed to put the memory and microprocessor on one PC board. But 16K DRAMs would require two boards to provide the necessary memory. And 64K x 1 DRAMs would not be cost effective: 75% of the memory would be unused.

When a TI sales engineer heard of Mitel's problem, he told the company about a new TI product: The TMS4416 16K x 4 DRAM. TI made early samples available for system design.

The TMS4416 proved to be the key to solving Mitel's memory problem. Only 16 TMS4416s provided the needed video display memory — a four-to-one parts reduction over 16K DRAMs. And a 50%

◀ **A single board** containing TI's new TMS4416 16K x 4 DRAMs allowed Mitel to meet size constraints yet provide required memory density in the design of an advanced, compact communications work station (prototype board shown).

16K x 4 DRAM organization cuts space by 50%* in Mitel system.

TI's new TMS4416 16K x 4 DRAM uses advanced design concepts developed for TI's pacesetting TMS4164 64K DRAM. For example, square array architecture results in less power dissipation, lower junction temperatures, greater reliability, and lower cost.

space savings that allowed Mitel to incorporate more functionality into the SUPERSET 7.

ByFour organization utilizes memory efficiently

The 16K x 4 organization provided excellent utilization of the memory.

The TMS4416 interfaces efficiently with the 16-bit processor used in the SUPERSET 7 work station. It allows the processor to access four bits of information at one time—as opposed to one bit at a time in 64K x 1 DRAMs.

Using the TMS4416 gave Mitel other benefits: Improved resolution. Significant cost reductions. Power savings—only one 5-V supply required. Improved reliability—fewer parts and interconnects.

Other TI products enhance system versatility

Mitel uses many other TI semiconductors in its ICS system. Main memory of the SX-2000 consists entirely of TMS4164 64K DRAMs.

In addition, Mitel employs TI's TMS5220A speech synthesis modules in its telephone operation. The speech analysis took place at the TI Regional Technology Center (RTC) in Chicago. At the RTC, Mitel personnel worked with TI engineers to verbalize all the variables that confront the user of a telephone.

ByFour organization right for many applications

Although new, the TMS4416 is already proving itself in the Mitel equipment. And, because of its high bandwidth, it is finding more uses. Rapidly.

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For details on the TMS4416 (16K x 4) and the TMS4164 (64K x 1), now available in the industry's first high-density, plastic chip carrier, check numbers 1 and 2 on the coupon.

TMS4416 16K x 4 64K DRAM

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY, WRITE CYCLE (MIN)
TMS4416-15	150 ns	80 ns	260 ns	360 ns
TMS4416-20	200 ns	120 ns	330 ns	440 ns
TMS4416-25	250 ns	150 ns	410 ns	560 ns

TMS4164 64K x 1 64K DRAM

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY, WRITE CYCLE (MIN)
TMS4164-15	150 ns	100 ns	260 ns	285 ns
TMS4164-20	200 ns	135 ns	330 ns	345 ns
TMS4164-25	250 ns	165 ns	410 ns	455 ns

New TI DRAM controller slashes design time

TI's new TMS4500A DRAM controller allows you to get the speed, density, and power-saving features of DRAMs in any size system. Big or small.

Cuts part count

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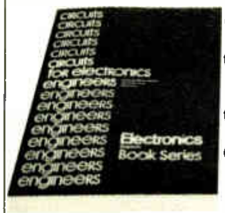

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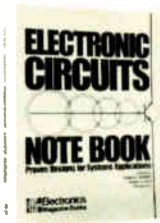

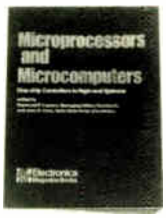

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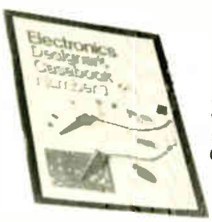

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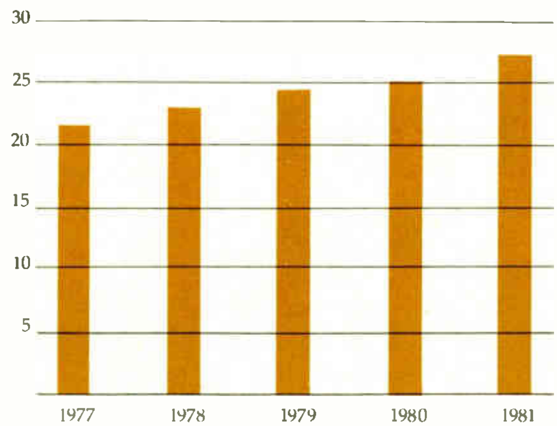

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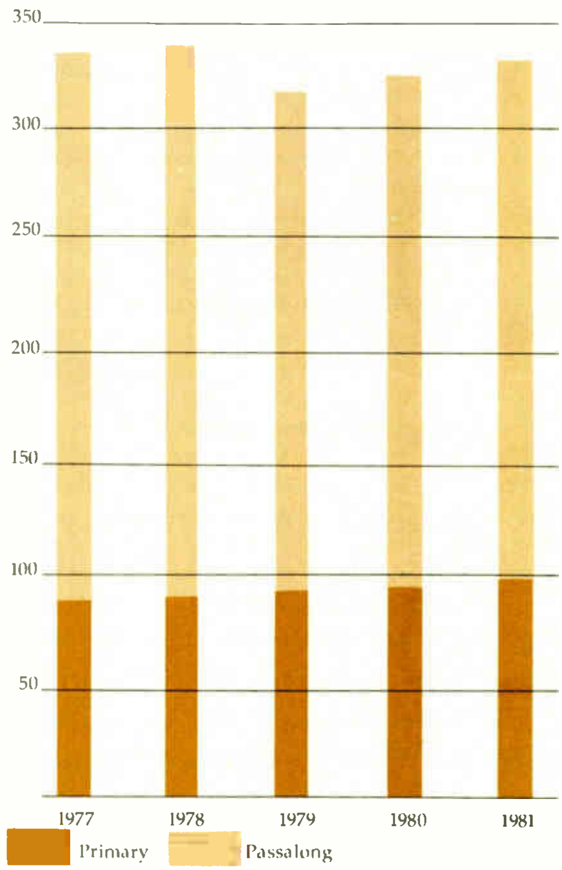

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International newsletter

Danish system uses multiple microprocessors to hit 4.8 MIPS

Watch for a high-performance multiple-microprocessor system from Danish Data Electronics A/S, Copenhagen, to appear under the colors of U. S. and European original-equipment makers. **The new Unimax can run from two to eight Motorola 68000s on a common 32-bit bus** to achieve a performance of 4.8 MIPS, or about twice that of the most powerful VAX, says the company. That level of performance will support up to 128 terminals with a generous 1 megabyte of memory per user. To leave the main bus free for interprocessor communication and input/output, each processor has its own local memory bus. Tying it all together is a new concurrent-processing operating system written in the C language and based on Bell Laboratories' Unix concepts. The company will be showing off Unimax at next week's Europe 82 OEM computer show in Amsterdam.

Semicustom chips set a subnanosecond pace

Now anybody with a logic design, a pocketful of money, and 10 weeks can order ultrafast semicustom logic suitable for jobs ranging from state-of-the-art test equipment to supercomputers. The fastest gate arrays on the market from Japan is the claim for 100K-compatible emitter-coupled-logic gate arrays just announced by Nippon Electric Co. **Loaded propagation delay for the internal gates is only 0.5 ns for a 300-gate chip and 0.7 ns for 1,200- and 2,000-gate chips.** Load conditions include a fanout of three with 2-mm leads for the smallest chip, 3-mm leads for the two larger chips. When 90% of the gates are used, the devices require 3 to 6 W to fuel their high speed, but heat sinks attached to the ceramic-brazed packages allow them to be mounted on boards on ½-in. centers. Price of the 300-gate part is $11,000 for design and $18.50 per chip in lots of 1,000.

Japanese firms enter 128-K E-PROM race

Fujitsu Ltd. has become the second firm, after Intel, to announce a 128-K erasable programmable read-only memory, but two other Japanese firms will follow soon. Fujitsu also is announcing an intelligent programming method that can program each byte in as little as 2 ms, rather than the 50 ms that is standard with most MOS E-PROMs. Intel has a similar scheme, except that minimum programming time is 5 ms/byte. **Major E-PROM programmer manufacturers indicate they will incorporate the Fujitsu and Intel schemes by software control in their upcoming models.** Fujitsu will start sales of 250- and 300-ns parts in December and will be followed in January by Nippon Electric Co., which will market 128-K E-PROMs rated at 200, 250, 300, and 450 ns. Hitachi will follow later in the first quarter with its own 128-K E-PROMs.

Broadcast digital code automatically turns on home video recorders

A broadcast technique in which a digital code is transmitted before the start of a TV program to turn on a programmed video recorder will see first use in January by several West German regional stations. The Storage Television System, developed by Hildesheim-based Blaupunkt-Werke GmbH [*Electronics*, Feb. 10, 1981, p. 80], uses a code that identifies the program. **At the receiver end, a decoder compares the code with the contents of a memory** in which the viewer has previously entered codes for the desired programs. When they match, the video recorder is switched on. Eventually, viewers will be able to pick their TV fare from a guide in which programs are identified by a bar code that can be entered into the decoder's memory by scanning with a light pen.

International newsletter

Pocket TV set uses thin-film FET switches

Sanyo Electric Co. expects to start sales of a pocket TV set with either a 3- or 4-in. liquid-crystal display by the end of next year. Prototype sets of both these sizes, shown at the Japan Electronics Show in Tokyo, feature an amorphous thin-film field-effect-transistor switch under each picture element of the twisted-nematic reflected LCD. **On the 3-in. display, there are 120 by 160 pixels; on the 4-in., 220 by 240 pixels.** This is the second TV with transistor switching of individual pixels of an LCD matrix to be announced in Japan. The first, by Suwa Seikosha, is built on a single-crystal silicon substrate using conventional MOS transistor switches.

Miniature laser weighs 70 grams

A laser claimed by its developer, Siemens AG, Munich, to be the most compact helium-neon type operating in the basic transverse electromagnetic mode, measures 146 mm long and 25 cm in diameter. **The LGR 7647 requires 3.5 mA and 1 kV to produce an output of 0.5 mW.** Its small size and low weight of 70 g makes the laser especially suitable in mobile equipment like hand-held scanners, aiming devices on rifles, and portable industrial measuring systems. It will be introduced at the Nov. 9–13 Electronica show in Munich and is scheduled to go into volume production in mid-November.

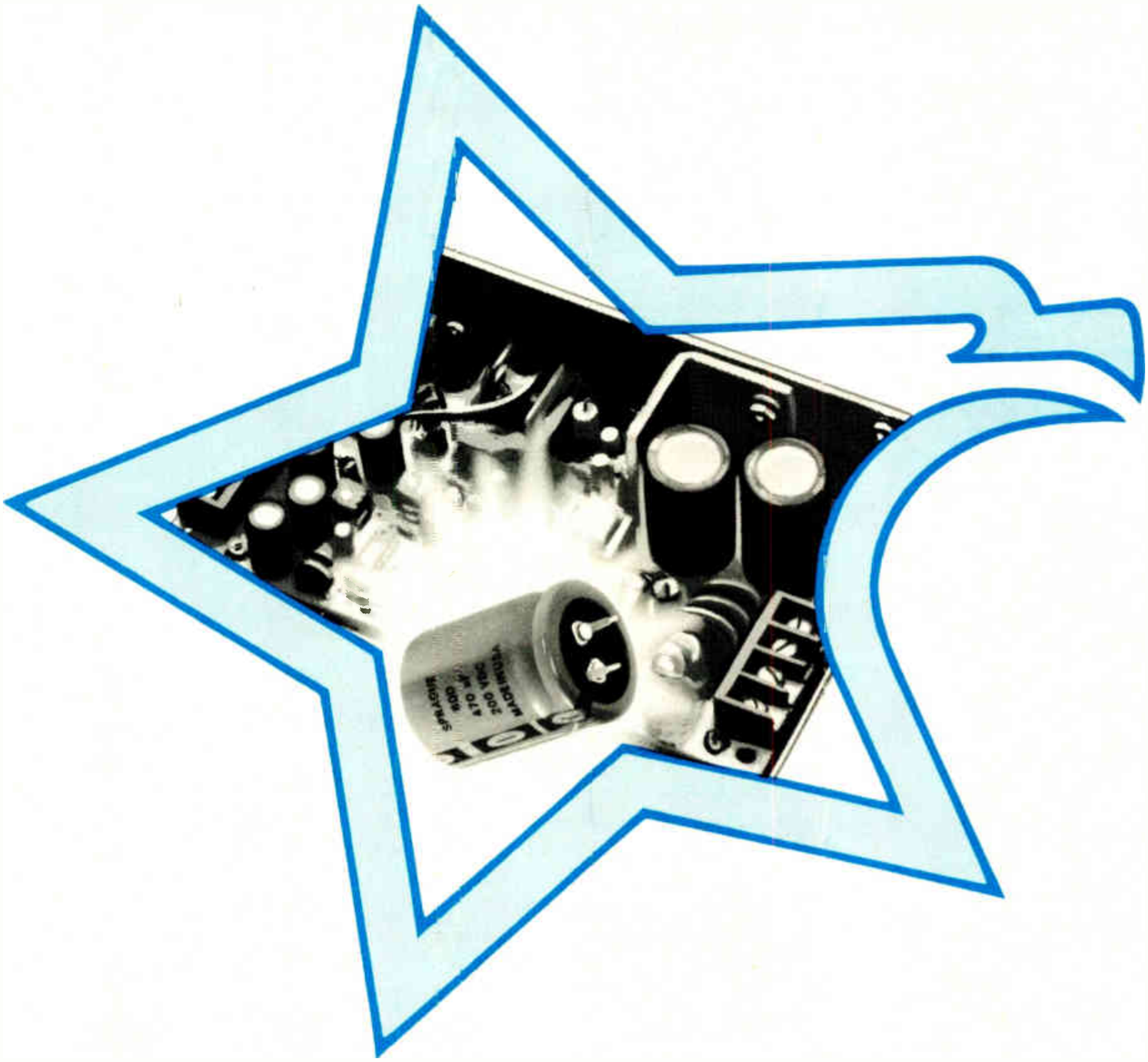
Thomson uses GaAs for PLA organization

Preparing the way for gallium arsenide in very large-scale integrated circuits, engineers at the Central Research Laboratory of Thomson-CSF in the Paris suburb of Corbeville have developed a GaAs programmable logic array using low-power normally-on metal-semiconductor field-effect transistors. Based on the multilevel logic capability of the buffered-FET logic approach, the PLA **features a NOR-wired OR organization.** Standard PLAs have a NOR-NOR organization, which, translated into buffered-FET logic, would have been slower and consumed more power than the Thomson design. Using a single-clocked master-slave frequency divider as a test vehicle, the PLA version showed propagation delays 50% longer than those achieved by an optimized random-logic version. However, it was designed in a much shorter time and with an active layer 30% smaller than the hand layout. The PLAs will be presented at the GaAs IC symposium in New Orleans next week (see p. 49).

Hitachi to sell solid-state video cameras in Europe

Japanese consumer-electronics makers are beating their European competition in the race to start selling video cameras with solid-state image sensors on the Continent. A newly developed MOS sensor will enable Hitachi Ltd. to be selling a $1,200 video camera with such an imager in PAL-standard countries—especially West Germany—by the end of the year. Sales will start in Secam-standard countries soon after that, when the firm completes the design of camera circuits for the French system. **The 8.5-by-10-mm imager has 374 picture elements horizontally by 577 vertically** in the 6.6-by-8.8-mm area of a 2/3-in. vidicon target. The remainder of the chip is taken up by peripheral circuits and bonding pads. Horizontal resolution is improved to 350 lines, compared with 280 lines for the same-sized NTSC-standard devices, which have 384 elements horizontally by 485 vertically. The higher resolution is attained by staggering the pixels along alternate horizontal lines by half their pitch and by signal processing.

AN AMERICAN-MADE POWER SUPPLY CAPACITOR THAT'S A SNAP TO PUT ON BOARD



New Sprague Type 80D Aluminum Electrolytics are competitively priced and designed for easy installation.

These new 'lytics are ideal for use as input and output filter capacitors in switched-mode power supplies and other industrial and commercial applications. They feature snap-lock terminals to assure secure mounting on printed wiring boards with low-cost solder assembly.

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For detailed technical data, write for Engineering Bulletin 3156 to Technical Literature Service, Sprague Electric Co., 35 *Marshall St., North Adams, Mass. 01247.*

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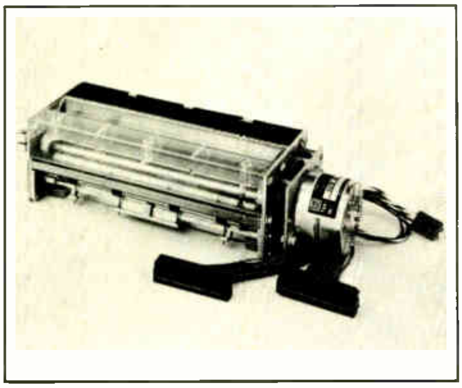

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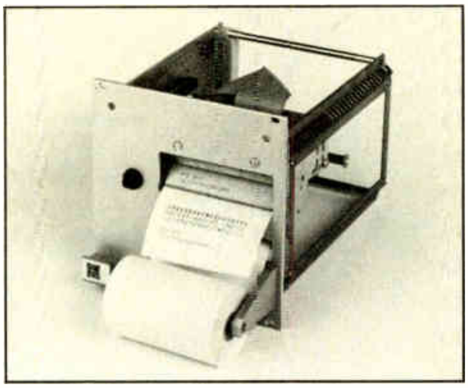

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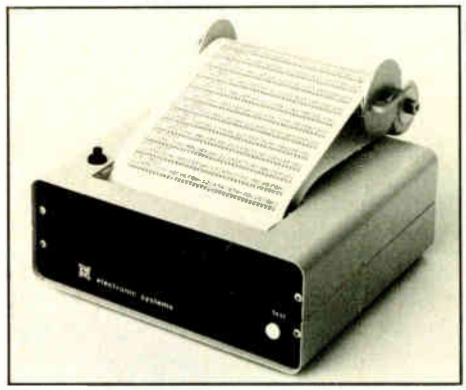

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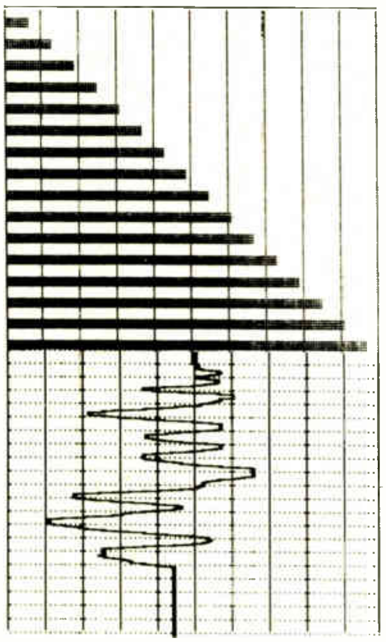

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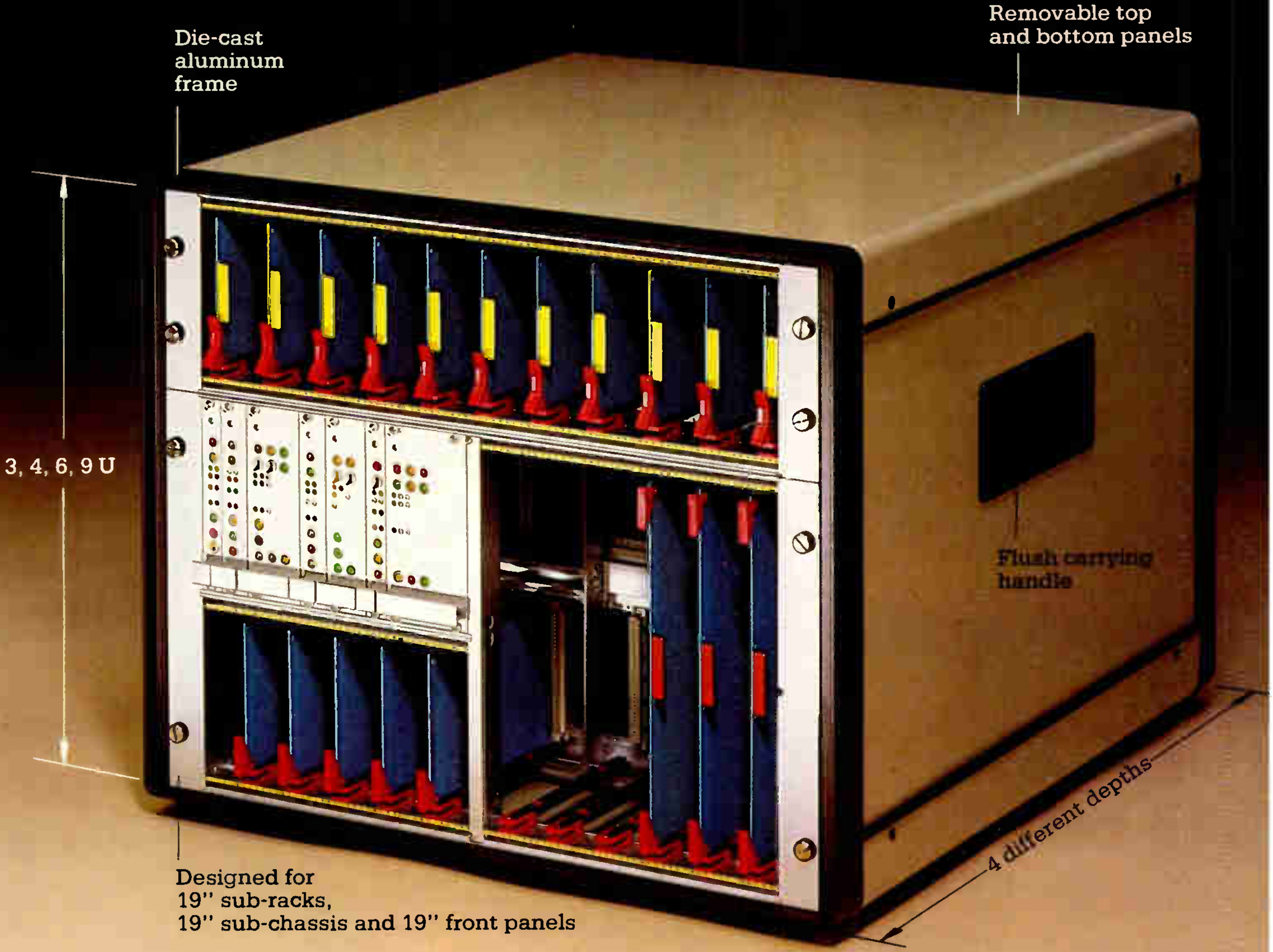

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Microprocessor does multitasking in real time

by John Gosch, Frankfurt bureau manager

Performance is enhanced using a 16-by-16-bit instruction cache for up to 16 program instructions

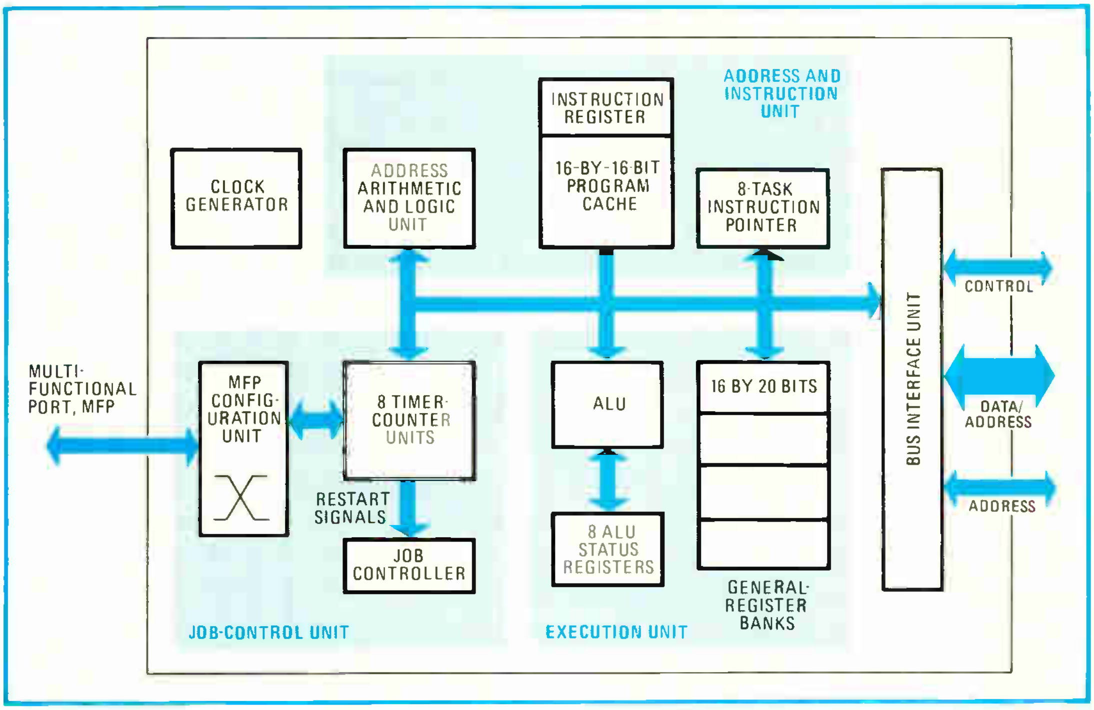
A new approach to microprocessor design that incorporates such essential parts of a real-time operating system as the task scheduler has led to a 16-bit microprocessor with true on-chip multitasking support. Developed at West Germany's Siemens AG, the SAB 80199 processor is particularly suited to applications with extremely critical time related demands—high-speed printers are a particularly good example.

Thus far, 16-bit microprocessor support of real-time operating systems has been accomplished by expanding the instruction set with special instructions or by integrating special parts of such systems into an external read-only memory. The goal of this "software on silicon" approach is primarily to increase system performance, but there is no real improvement in system response time. This drawback makes such a processor rather slow at doing real-time tasks.

The SAB 80199 gets around this software shortcoming by implementing essential parts of a real-time operating system in on-chip hardware. "The big advantage is that functions like task changes or prioritization of different tasks can be executed extremely fast, which is important in handling critical real-time tasks," says Bernd Huber, sales and marketing manager for microprocessors, memories, and gate arrays in the company's Munich-based Components Group.

Multitasker. To be discussed at the Nov. 9–11 International Microelectronics Congress in Munich, held concurrently with the Electronica exhibition, the 80199 can handle up to eight tasks in quasi-parallel fashion. Thus it can provide real-time multitasking support.

To do this, it has complete on-chip context storage, with eight instruction pointers, eight status registers, four banks of 16-by-20-bit general registers, each bank dedicated to two tasks, and eight dedicated input/output spaces for the eight tasks. Therefore, there is no need to save and reload the old and the new task contexts—so long as no more than eight tasks at a time are vying for execution.



Supportive. The SAB 80199 has complete on-chip context storage, with eight instruction pointers, eight status registers, four banks of 16-by-20-bit general registers and dedicated input/output spaces for eight tasks.

Switching a task context typically is performed in 1 microsecond. The system response time is at least one order of magnitude better than that of the best software-driven real-time multitasking microcomputer on the market today, Huber says.

In contrast to other operating systems, a task change is possible after each instruction and adds no time penalty. The built-in scheduler provides a predefined priority: task 0 has the highest priority and is privileged and intended for the operating program.

Tasks self-sufficient. For flexible interrupt handling, the 80199 provides up to eight pins for external task-restart requests and eight 20-bit timer-counter circuits for delayed external or internal timer-counter–controlled restart requests. Each task can mask its own restart request and control its multifunction input/output port's pin and its timer-counter.

To raise processing performance, the 80199 features a 16-by-16-bit instruction cache, which makes it the first microprocessor with such a cache on chip. The instruction cache is a high-speed first-in, first-out storage unit for up to 16 program instructions.

For short program loops, it needs to fetch instructions from the external program memory only once, placing them in the cache. The execution time for a typical move instruction is 0.5 μs using the cache. It is 1 μs when the instruction is fetched externally.

Bus-compatible with Intel Corp.'s 8086 and 8088 processors, the 80199 has a 1-megabyte address space and sports an instruction cycle time of 0.5 μs. It uses a 20-megahertz clock. The device is based on Siemens' Mymos (for micrometer MOS) technology with 3-μm channel lengths, which is compatible with Intel's high-performance H-MOS.

The 80199 microprocessor was designed for applications in which available processors are too slow to fulfill the demands of real-time processing. Besides high-speed printers, systems in which it can be put to use advantageously are automotive engine controls, process-control and telecommunications gear, and data-transmission systems.

The 80199 can also be used to realize functions that are presently implemented with special hardware. Thus it is possible to run a high-level data-link communications protocol with a transmission speed of up to 500 kilobits a second, using two of the eight tasks that the Siemens processor can handle simultaneously. This leads to a significant reduction of chips in cost-sensitive applications like terminal printers.

Samples will be available during the second quarter of next year. Development support will follow during the third quarter, Huber says.

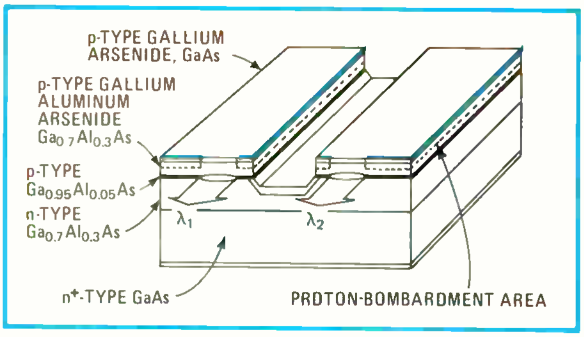
France

Integrating two multiplexed optical sources allows direct coupling to single fiber

Optical transmission systems using wavelength multiplexing currently consist of two separate optical sources transmitting at different wavelengths, connected by an optical multiplexer. In order to simplify this configuration and thus render it cheaper and more reliable, engineers at the Centre National d'Etudes des Télécommunications in the Paris suburb of Bagneux have been studying the possibility of a monolithic device that integrates both optical sources and that can be coupled directly to a single fiber.

So far, they have developed a structure composed of a gallium-aluminium-arsenide laser and a GaAs laser transmitting at 0.885 and 0.85 micrometer, respectively, at low threshold currents.

They have run trials of the structure, with the lasers 25 and 10 μm apart. Reducing the distance to 10 μm makes it possible to couple the structure to a 50-μm multimode fiber with a loss of 3 decibels.



Groovy. Laser structure consists of a GaAlAs/GaAs double heterostructure with two active layers of different composition, two proton-bombarded stripes, and an engraved groove.

The basic architecture consists of a GaAlAs/GaAs double heterostructure with two active layers of different composition, two 10-μm stripes realized by proton bombardment, a groove engraved down to the active layer between the stripes, and the usual metallic contacts on the p-type layer and the substrate.

Varying the composition of the layers in the double heterostructure is achieved by two successive epitaxial growths. After the growing of a GaAs active layer, selective chemical etching through a dielectric mask leaves 30-μm bands every 400 μm. A double heterostructure with a GaAlAs active layer is grown in these bands, with the dielectric mask protecting the rest of the surface.

Double function. After removal of the mask, a groove is chemically etched between the two double heterostructures. Then proton bombardment both defines the two 10-μm-wide laser stripes and electrically and optically isolates the lasers from each other.

Because the bombarded regions are not subjected to thermal treatment after implantation, their absorption level is at least 10 times higher than the nonbombarded regions. Therefore, optical interaction between lasers is minimized even though they are close together. When

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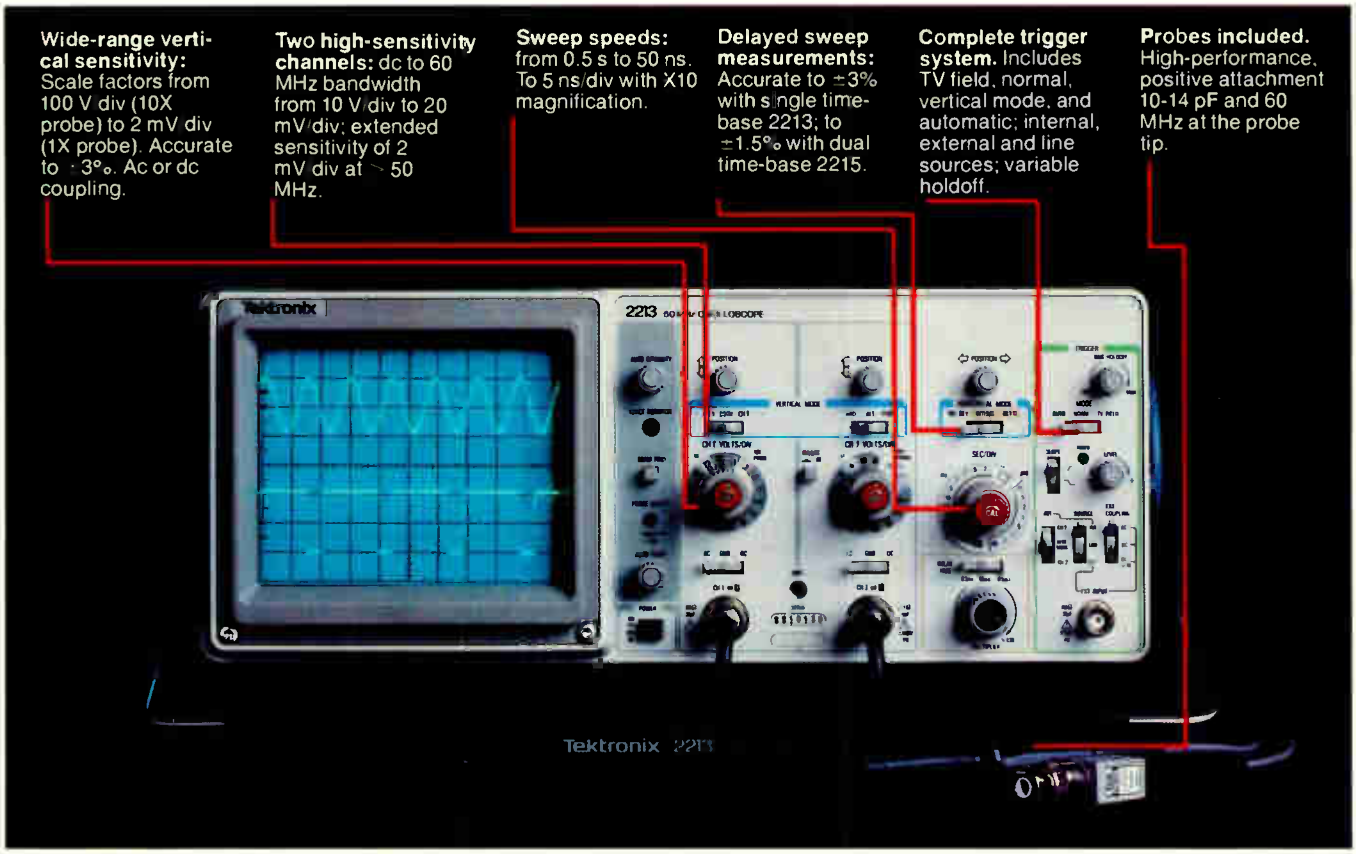

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produced in this manner, the laser with the GaAs active layer operates at a pulsed lasing threshold of 65 milliamperes, while the one with the GaAlAs active layer has a threshold of 45 mA. The lasers function in the fundamental transverse mode, and they are capable of simultaneously emitting a power of 7 milliwatts per face. The 350-angstrom difference in wavelength between the lasers is large enough so that the spectra emitted by them do not measurably overlap.

The structure is, however, not without its problems. At low speeds and low modulation, CNET engineers have noticed a 16-dB crosstalk effect that rises with the amplitude of the current variation of the GaAlAs laser. This effect could cause some undesirable heating in the other laser, so the engineers plan to reduce it by working with higher-frequency modulations.

But the first problem CNET will tackle is the kind of photodetector that would be appropriate for the negative-feedback circuit for each laser. Proximity of the two lasers makes this a potential stumbling block, so the next step will be a structure integrating a negative-feedback photodiode. After that, trials at 1.3 and 1.5 μm are in the offing. **-Robert Gallagher**

Great Britain

Digital signal-processing system does 5 million 16-bit multiplications per second

Question: when are a spectrum analyzer, a vocoder that digitizes voice at very low data rates, and a radio receiver one and the same instrument? Answer: when the digital processing unit on which all three are based has been programmed to emulate each in turn.

This technological sleight-of-hand, by Racal Electronics PLC, requires a digital signal processor fast enough to handle all three types of analog signals in real time. In this case, the processor is a seven-board unit built around a TRW 1010 multiplier chip.

A fast performer. Over 100 times faster than a 16-bit Motorola 68000 microprocessor, for example, the Racal digital processing unit crunches its way through 5 million 16-bit multiplication and accumulation operations per second. Alternatively, it can perform a 256-point fast Fourier transform in 10 milliseconds, compared with 1.4 seconds for a 16-bit microprocessor.

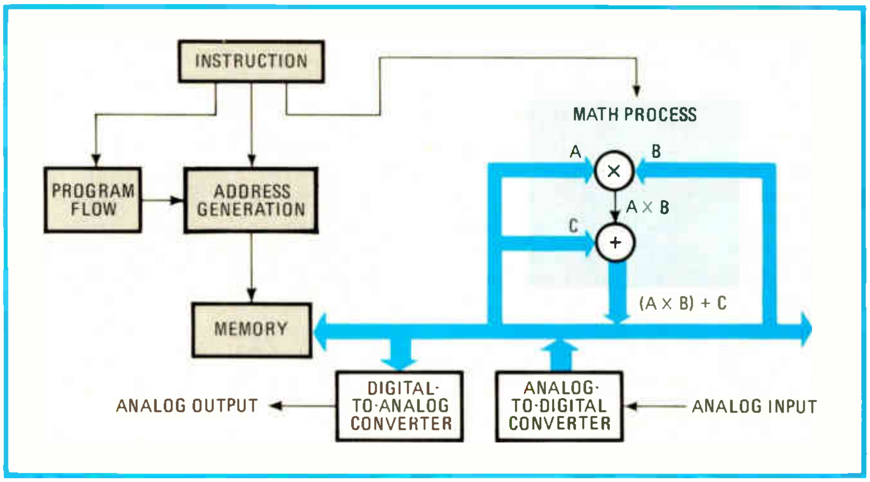
To be sure, the TRW chip on which it was based is now getting a little long in the tooth, and now coming onto the market are single-chip digital signal processors with a similar level of performance, such as Texas Instruments' TMS 320 or Nippon Electric Co.'s Micro PD-720. But the difference, says John Alexander, research director at Racal Research Ltd. in Reading, Berks., is that these single-chip solutions have only now become available and are in short supply, whereas the Racal processor already has been designed into production equipment.

For starters, it has been teamed with one of Racal's high-frequency receivers—the RA 1792. It assists the operator in spectrum surveillance tasks by displaying the frequency spectrum under surveillance, with control facilities to examine it in large gulps or in fine detail.

That said, Alexander's group could be among the first to use these new single-chip high-performance processors. "When we started four years ago, there was nothing available, so we had to develop our own architecture," he says. "Now these second-generation chips are just coming into view. With the help of chips like this, Racal wants to get its seven-card processor down to just a single card—that could create a raft of new equipment possibilities."

Software a key. The group appreciated early the technology's potential impact on equipment design. "For the manufacturer," says Alexander, "there's the possibility of evolving a family of products from a single hardware development by software changes alone. For the military user—assuredly Racal's first customer—logistics problems could be greatly simplified if an equipment's function can be changed by changing the software."

Racal's processor can perform all the usual signal-processing functions, such as attenuation, amplification, filtering, frequency changing, modulation and demodulation, spectral estimation, statistical analysis, and so on. In some applications, of course, use of the techniques would be like "taking a sledgehammer to crack a nut," notes Alexander. He



Well-fed. The design of Racal's digital signal processor involves supplying the multiplier accumulator with its multiplicands and transferring the accumulated products to memory.

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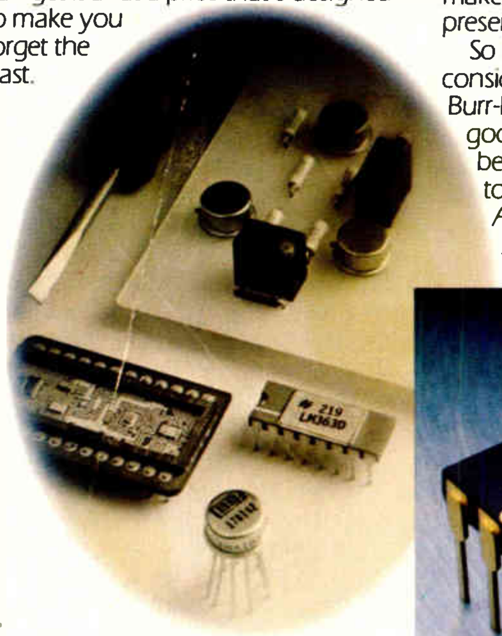

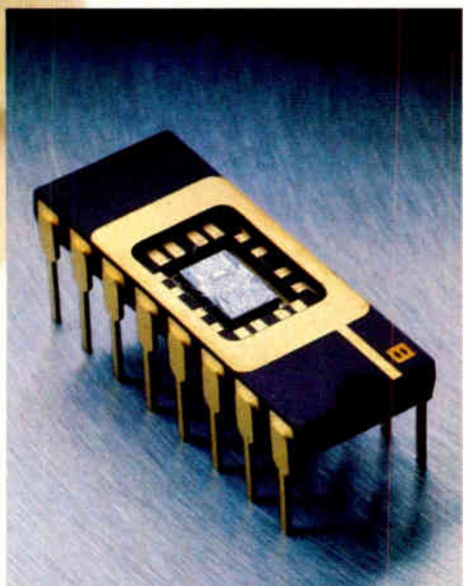

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Circle 75 on reader service card

Keeping the data pipeline full

Basic to Racal's digital processing unit is the TRW 1010 16-bit multiplier, which can multiply two 16-bit numbers in a single 200-nanosecond cycle. Racal's design task was to extract the maximum performance from the chip by keeping it well stocked up with data. This involved the use of look-up tables to speed computation, as well as heavy pipelining with each instruction divided into three parts—program flow, address generation, and mathematical process—each independently executed on special-purpose hardware. The overall architecture is relatively simple, with a common bus to fetch operands and return results to memory and with two product-term registers to feed the multiplier. Now occupying seven 5-by-7-inch printed-circuit cards, the processor has already been through three design iterations. The next objective is to reduce it to a single card by using large-scale integration on some of the surrounding chips. -K. S.

adds, "You have to combine a lot of functions at once to make the technology viable. For example, in low-bit-rate voice signaling, about 2.4 kilobits per second, the processor could emulate a modem and the encryption unit; it could execute the data projection codes and could perform the voice coding, or vocoding, function as well." -Kevin Smith

Japan

Terminal runs downloaded program, acts as a personal computer in second mode

Combining roles, Hitachi Ltd.'s Personal Terminal can operate as a mainframe terminal or a personal computer simply by swapping operating systems from a built-in disk drive. As a terminal, it will run mainframe programs written in Cobol and thus is a powerful tool for highly distributed processing.

For the terminal function, the 16-bit 8086-based system uses Hitachi's Business Terminal Operating System, which is compatible with the firm's mainframes. It features Host Cobol for the downloading of programs developed on a mainframe and then parceled out to terminals.

The unit has only execution routines—it has no compiler, so it cannot develop programs. Hitachi says that equipping the terminal only with Host Cobol enables a large company to maintain control of programs used. A user may, of course, purchase a Cobol compiler to run in the personal-computer mode, but it would not operate on the mainframe.

The system also features Hitachi's Data Entry Record Format Descriptor, a simplified language with an RPG-like flavor for developing programs for data entry. Moreover, it has dual job capability—it can perform both batch processing and interactive processing simultaneously, or it can do on-line processing, including accessing a central computer, and local processing.

In the personal-computer mode, the system uses Microsoft's MS-DOS operating system. Extended Basic is offered by Hitachi, although, of course, any language compatible with MS-DOS can be used. Also offered are a number of service programs, including a text editor and a file-conversion program.

Conversion bridge. The last-named program forms a bridge between the two modes. It will convert files even if the file format or character representation is different. In the terminal mode, EBCDIC is used for compatibility with mainframes, while in the personal mode, the usual ASCII code is used. Conversion time for a 100-kilobyte file is a very reasonable two or three minutes.

In its simplest configuration, the terminal has 60-K bytes of user memory. Nozomu Shimamoto, chief of the Engineering division's marketing department, says that this amount is sufficient because jobs requiring larger amounts of memory can be performed more efficiently on the host.

There are, in fact, 256-K bytes of main memory, but 128-K bytes are used by the terminal operating system and another 60-K bytes by its firmware, including device drivers and task control. As an option, another 60-K bytes are available for dual job operation. The remaining 4-K-byte blocks are used for tables.

The MS-DOS only requires 64-K bytes, however. So in the personal-computer mode, there are 192-K bytes of user memory.

Options available. The smallest practical system includes a 12-inch black and white cathode-ray tube, two built-in 1-megabyte floppy-disk drives, a 150-character-per-second dot-matrix printer for alphanumerics or the Japanese kana syllabary, and Host Cobol. The list price is $3,600 in Japan, but there are many options, starting with the extra memory for dual-job operation. Others include a color CRT and 180-K bytes of memory for a 720-by-540-dot, seven-color graphics display.

The system can be ordered with a 9.8-megabyte, 5-in. hard disk in one of the floppy-disk slots. Additional floppies can be added externally, but at present the hard disk must be installed at the factory. Other options include readers of bar codes, identification cards, and optical characters, plus several printers.

These printers include a nine-by-seven-dot alphanumeric matrix printer and a 24-by-24-dot kanji (Chinese character) printer, which fit under the terminal and so occupy no desk space. Single sheets of paper are fed through the front, so though they are obviously not suited to applications requiring high throughput, Hitachi says they are especially useful in applications requiring multiple preprinted forms, which would be difficult to implement with roll-paper feed. -Charles Cohen

sector. Telecommunications in particular failed to materialize as a boom market. At Thomson-CSF in Paris, there is even some surprise at the weakness of ICs. "At the moment, discrete components are stonger than ICs. It's usually the other way around," says Jean Caillot, the company's commercial director for components and tubes.

Even if he agrees that the market is generally weak, Caillot takes some comfort in the relative position of the French market. "Compared with other European countries, we are not doing that badly at all, particularly when you look at Germany," he argues.

Hope in Albion. For the British, there is some hope as the nose-diving UK economy has leveled off. Among the more promising signs, the big electronics companies—among them GEC, Plessey, Ferranti, and Racal—have been reporting good results. And even ICL Ltd., which was almost shipwrecked, is now expected to become profitable before too long.

For components, there is an upturn on the way. Mike Young, chief of market research at Texas Instruments Ltd., says, "We expect a small dollar growth for the semiconductor market for Europe as a whole." But he adds, "The UK economy is booming with quite a strong growth in dollars and an enormous growth in pounds sterling."

Sector by sector, telecommunications is perhaps strongest. British Telecom is accelerating its modernization and a host of new companies is lining up to enter the liberalized terminal equipment market. And consumer spending has plummeted, which has helped parts of the consumer electronics market. For example, homebound Britons have turned to television, with more than 2.5 million color sets to be sold this year. And video-cassette recorder sales are exceeding expectations: sales this year could reach 1.8 million units compared with last year's total of just under a million.

However, the instrument market is flat, says Colin Gaskell, managing director of Marconi Instruments Ltd. Still, Marconi's program of 20 new products in as many months has meant good growth, which may make Gaskell's view overly pessimistic. For example, at Hewlett-Packard, product marketing manager Ian Allardice expects 8% to 10% dollar growth in the UK market in the year ahead; meanwhile, Marconi's Roy Lester, who heads test-equipment marketing, reports a major business upturn in the last few months.

Half-full. In Italy, perhaps the most important asset is a more sunny way of looking at things. "I'd say we are in a stable recession," chuckles Mauro Taraborrelli, manager of the semiconductor division of the Italian subsidiary of ITT. "Probably our most serious problem is a constant rise in the cost of labor, about 20% a year, coupled with low per-capita productivity."

Despite this somber background, Taraborrelli is cautiously optimistic about the Italian electronic industry's chances for 1983. "This year our book-to-bill ratio was above 1 from January to July," he says. "Taken as a whole, this year will be flat. But in 1983 we could see a growth in the electronics market of as much as 25% to 30% in lire." That, though, translates into just about 5% in dollar-based real terms, allowing for continuing decline of the lira against the dollar.

Common for Western European countries is that some products will be doing much better than the average for semiconductor components. In West Germany, for example, sales of memories should grow about 20% and those of microprocessors even better than that next year, according to Bernd Huber, sales and marketing manager for these product groups at Siemens AG. Huber forecasts the same growth for Western Europe as a whole and thinks it can be sustained at least through 1986.

Devices that interface microelectronics with the outside world are also in for above-average hikes. German marketing officials predict annual growth of at least 20% and see Western Europe consuming well over $200 million worth of such components in 1985. During the second half of this decade, some 20% of all sensors sold will be for mass applications in, for example, household appliances and automobiles, the experts say.

Much the same can be said for gate arrays, although the timing for a real applications breakthrough is a controversial subject. UK-based Mackintosh International Ltd., a specialized market-research firm, pegs the world's noncaptive gate-array market in 1986 at $1.2 billion, a ninefold increase over the 1981 level. Needless to say, such growth will come at the expense of standard ICs. □

Two pessimistic views of Europe

As executives of worldwide component firms, Fritz A. Lohmann, a director at Philips GmbH, and Gernot J. Oswald, marketing director for integrated circuits at Siemens AG, are inclined to take a global view of their specialties, and some of their assessments may be disquieting to the Europeans. Lohmann, who is also head of Hamburg-based Valvo GmbH, the West German components-producing subsidiary of the giant Dutch firm, regards the per capita consumption of microelectronic devices as an important indicator. He puts this year's consumption in the U. S. at $16.80 per person and sees it rising to $32.40 in 1986. For Japan, the 1982 per-capita figure is $17.60, going up to $34.40 in 1986. Western Europe checks in at a meager $4.80 for this year, doubling to $9.60 by 1986.

For his specialty—integrated circuits—Oswald also sees Western Europe slipping at the expense of the U. S., Japan, and Southeast Asia. One reason, he says, is that Europe lacks significant production of personal computers, electronic games, and video recorders—all items that gobble up ICs. Taking a look at Western Europe alone, the Siemens executive sees West Germany, although still the continent's biggest single IC consumer, losing ground to France and the UK. The reason: insufficient awareness on the part of the German public of the importance of electronic technologies. **-John Gosch**

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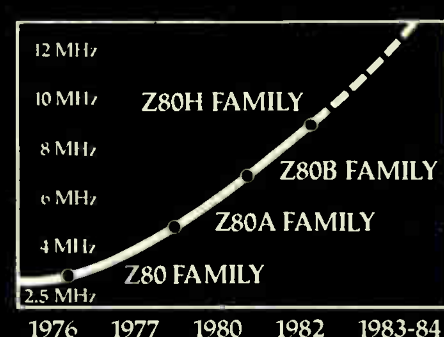

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Now evidence of success is starting to show up. First, Motorola says that it is pleased with initial second-sourcer Signetics' processor production and that Mostek is "coming along nicely." Second, the peripheral parts that Motorola needs to challenge Intel are beginning to see daylight.

Peripherals, in fact, are now a top-priority item at Rockwell. The division already has brought out three devices of its own for delivery before year-end, most notably an ambitious multiprotocol communications controller. A chip with the density of very large-scale integrated circuits, it supports all major protocols, including synchronous data-link control, X.25 bisynchronous, and RS-232-C. In addition to a local-network and a floppy-disk controller, Rockwell plans several more each year.

Perfect blend. Signetics' Meyer calls the planning process a high point. Besides getting together frequently to agree on new products and specifications, the partners have added a new wrinkle: a voice in what specific features Motorola's soon-to-be-announced processors should have. "We get a vote in what they are doing—they may have 51% and we may have 49%, but we still have the 49%," Meyer says.

For Motorola's part, it acknowledges "taking greater pains to ensure that second sources can actually produce" says Jack W. Browne Jr., 68000 marketing applications manager. "The customer base tends to demand a little more accuracy than perhaps five years ago," he adds, which is one reason the partners keep in close touch. Not only does this prevent process missteps—one area where Motorola rides tight herd—but it produces another advantage mentioned frequently by everyone. "It cuts down on duplication and allows each company to pursue its own strength," says one engineer.

Motorola has strung out its alternative pacts over nearly three years, signing Rockwell in 1979. Japan's Hitachi Ltd. and France's Thomson-CSF came aboard in early 1980, with Signetics and Mostek following. All initially built 68000 processors, but emphasis on peripherals grew: it culminated in the Mostek-Signetics announcements in March 1982.

The relationship with Hitachi is ticklish, industry observers say, particularly in the view of U. S. customers. Motorola says only that it treats all partners equally and that Hitachi is performing well, with samples of peripherals now beginning to ship. However, other sources say that Hitachi is slow to keep other second sources informed. Sources add that Thomson was slow getting up to speed, but now is nearing the product phase.

Intel dealing. If the Motorola agreement is blazing a trail, what about competitors, particularly Intel? Even this Santa Clara, Calif., frontrunner gives signs of hearkening to the same needs, as indicated by its 10-year pact for the iAPX86 family with neighboring Advanced Micro Devices Inc. in Sunnyvale. Similar to the Motorola deal, it involves all updates on masks and test tapes along with design information. Says Dick Koeltl, AMD marketing manager for MOS microprocessors and peripherals, "It's far more than just agreeing with a spec; you have to build and test the parts as well." No details have yet been announced on specific parts.

On the boards at National Semiconductor Corp., Santa Clara, Calif., is a similar contract that calls for Fairchild Camera & Instrument Corp., Mountain View, Calif., to build and support its NS 16032 processor and peripherals. Gil Amelio, general manager of Fairchild's Microprocessor division, shuns the "second-source" term. "It's a partnership in a particular business area. This is not just a change of words—it's a change in attitude as well."

Though initial successes are heartening, Motorola thinks six to eight more months must pass before its partnerships fully prove themselves. But others such as Rockwell's Cotterman see grander vistas. "This could be a way for U.S. firms to meet the Japanese challenge," he believes, since this type of cooperation is possible without violating antitrust statutes. □

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Companies

Tektronix prepared for the upturn

Advanced new production lines and thorough reorganization are put in place as firm faces lower profits

by Stephen W. Fields, San Francisco regional bureau manager

There are two chief ways to ride out a recession such as the current U. S. downturn: a company might cut back severely on capital investment, research and development, and expansion. Or it might beef up its production lines and accelerate product development in order to position itself for the anticipated upturn. In Beaverton, Ore., however, the management of Tektronix Inc. has taken the latter method even further.

In an effort to "get back to the string of consecutive yearly increases in earnings that we enjoyed for 10 years from 1971 through 1980, the company is undergoing a major overhaul," says William Walker, chief operating officer of the world's leading oscilloscope maker. The reorganization began several years ago. Tektronix is now divided into three groups, and it has made major plant investments intended to support the production of advanced new products.

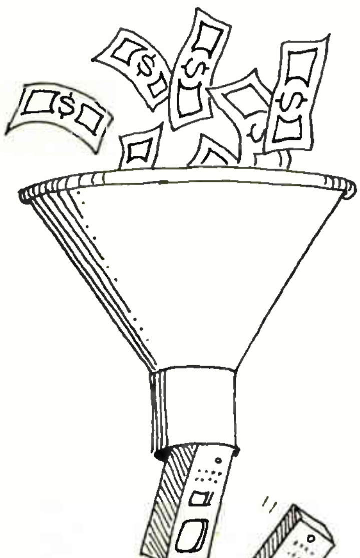
Fiscal 1982 (ending May 31) showed a 12% increase for sales to about $1.2 billion. But after-tax return on sales dropped from 7.5% to 6.6%. "The first three quarters of fiscal 1982 looked very good," says president Earl Wantland, "but then we saw a slow deceleration and then a drop in May [1982] resulting in a weekly order rate below fiscal 1981 levels."

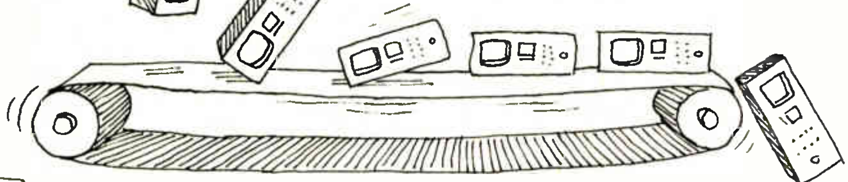
Even with the lower earnings, Tektronix has been putting about 10% of sales into capital investment. However, the firm has cut back in other areas, including reducing all expense budgets by 6%, phasing out temporary workers, and laying off 68 employees (out of 23,000 worldwide) from product divisions and central administrative functions. It anticipates more layoffs as it adjusts production schedules to the reduced level of orders.

For the past three years the firm has made large investments in facilities and equipment. Last year, the largest expenditures were made in its new Clark County (Washington) manufacturing plant that is just coming on line for portable oscilloscopes. The plant is outfitted with the latest in computer-aided-design and semiconductor-production equipment. In addition, the facility has a printed-circuit–board section that is due to open in January; an automated high-volume CRT line, which is coming on stream; and a high-volume hybrid-IC assembly line that has just started up.

Toehold. All this is aimed at making Tektronix more productive. A good example is the 2200 series scope. As John Gragg, portable-scope marketing manager, explains it, "Tektronix has not been a high-volume, low-cost manufacturer and does not sell through distributors. But companies like Philips, Matsushita, Trio, and Hitachi [all of which make low-end portable scopes] are. If we let them establish a market base at the low end, they could move up, cutting into our market share. And since market share and profits are interrelated, we don't want this to happen."

Tektronix' answer was a portable-scope line in the 60-megahertz, $1,200-to-$1,450 range—the 2200 series—with a lower manufacturing, as well as a lower selling, price. It employs single-board construction with 90% less internal cabling and 65% fewer parts than the units it replaces—and no fan. "It's simpler and more reliable than the scopes it replaces [the T900 and the 455],"





says Gragg. This is an important marketing consideration because "it's difficult to support a $1,200 product when a sales or service visit costs from $190 to $230."

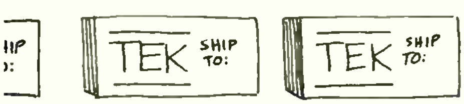
Changing markets. To enable it to react quickly to changing markets like low-cost scopes, technologies, and business conditions, the company has been organized into three groups. These are the Communications and International Group, the Design Automation and Information Display Group, and the Instrumentation and Technology Group.

The Communications and International Group, headed by Larry Mayhew until he left Tektronix last month to become president of Data I/O in Redmond, Wash., has the most employees. It contains the service operations, international marketing and sales, distribution, procurement, and the four business units that are associated with the communications division, among them the Grass Valley group, which makes switchers for TV studios and production houses.

Design Automation and Information Displays is managed by vice president Larry Sutter. The Information Displays half builds graphic terminals; Design Automation builds logic analyzers such as the DAS 9100 and the new color DAS.

The Instrumentation and Technology Group, headed by vice president Wim Velsink, is most representative of what Tektronix' business looked like in the 1960s. It contains the oscilloscope business units and the general-purpose modular instruments. But it also contains the Technology Center, responsible for the automated CRT line, semiconductor design, wafer fabrication, and hybrid assembly, along with advanced research. And it is the group that has been spending the most money—all of the new facilities come under it.

The overall situation at Tektronix is best summarized by Wantland: "Right now we have plenty of capacity. Unfortunately the future didn't arrive on time. But with these investments, we will be ready for the upturn when it comes." □



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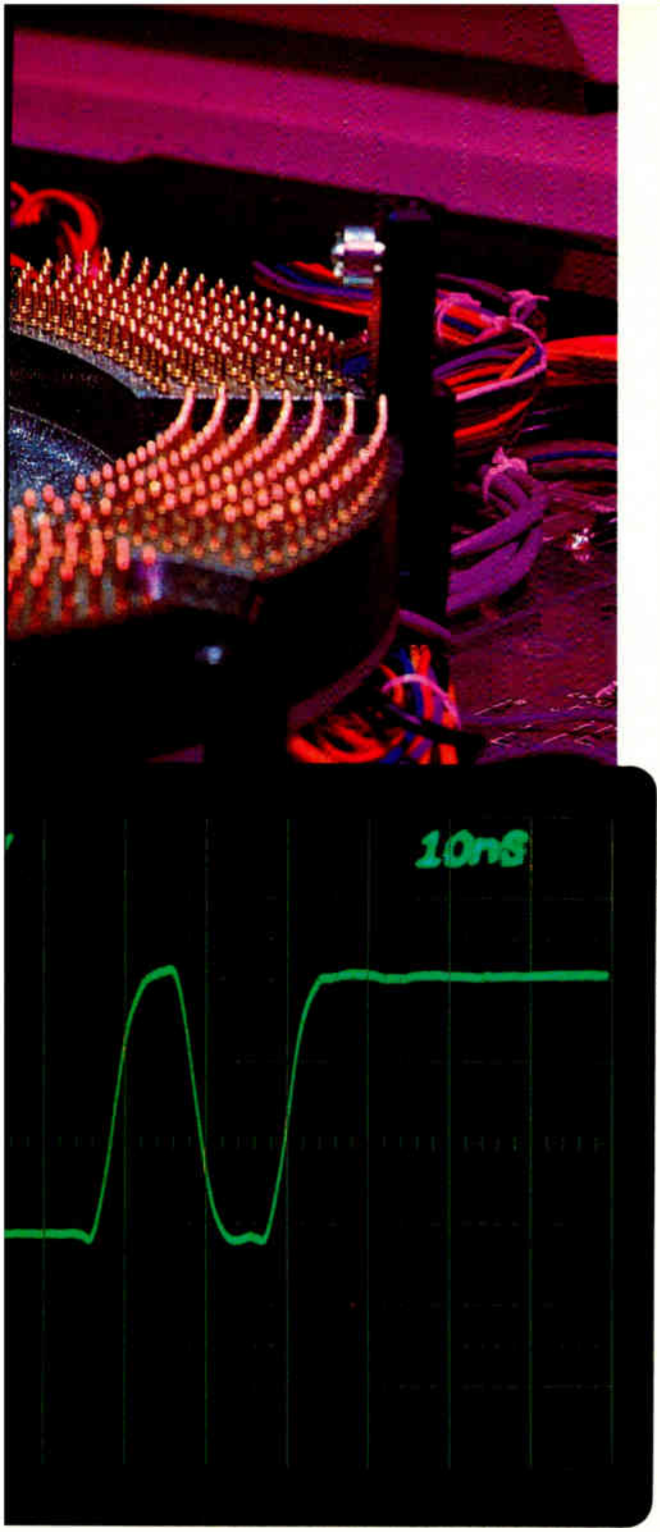

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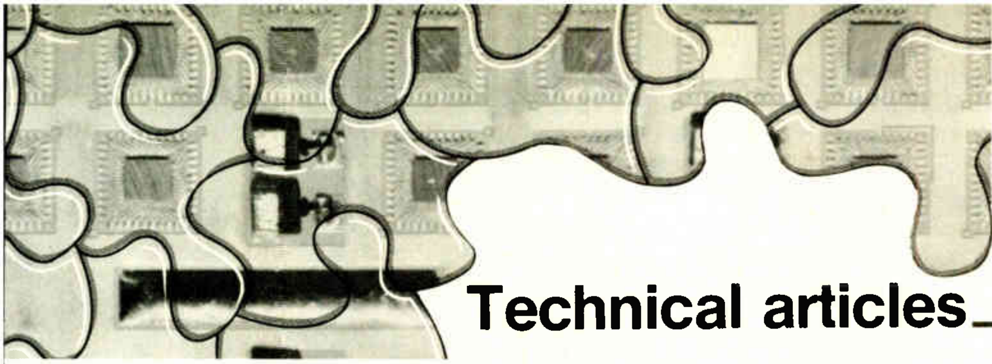


Technical articles

CML and flip TAB join forces in the DPS 88's micropackages

Honeywell's new DPS 88 computer marks a distinct advance from its DPS 8. The DPS 8 was an air-cooled mainframe based on TTL and Schottky TTL housed in ceramic dual in-line packages, which were mounted on multilayer printed-circuit boards. The DPS 88, on the other hand, is based on high-speed current-mode logic. These large-scale integrated circuits are tape-bonded face down to a large multilayer ceramic substrate, called a micropackage, which in turn is mounted to a multilayer pc board. Each micropackage is individually water-cooled.

The following two articles by Honeywell engineers will describe in depth some of the innovative technology that was developed to create this high-speed mainframe.

In the first, Dale Buhanan discusses state-of-the-art CML technology and compares it to emitter-coupled logic and TTL. The article shows why CML is superior in its proper environment and why environment plays an important part in its performance.

In the later article, C. H. McIver describes the details of the facedown tape automated bonding of the CML chips and the fabrication of the multilayer thick-film ceramic micropackage. Particular attention is paid to the special copper-thick-film conductor system. **-Jerry Lyman**
Packaging & Production Editor

Part 1

CML scraps emitter follower for ECL speed, lower power

by Dale Buhanan
Honeywell Information Systems Inc., Phoenix, Ariz.

☐ Driven by the manifold advantages of more highly integrated systems, mainframe-computer designers have strayed from the path of traditional packaging technology. One tack the DPS 88 designers have taken, packing scores of bare integrated circuits close together on a ceramic substrate, thrusts the chip designer as well into a foreign environment. The much-reduced interconnection capacitance of such a micropackage does away with the need for the power of emitter-coupled logic's emitter-follower driver and opens the door to current-mode logic, its lower-powered and slightly faster cousin. The simplicity of the logic gate, its speed in the basic logic functions achieved with a single gate delay, and the relatively low gate power combine to give CML a clear advantage over ECL in large-scale ICs in a micropackage carrier.

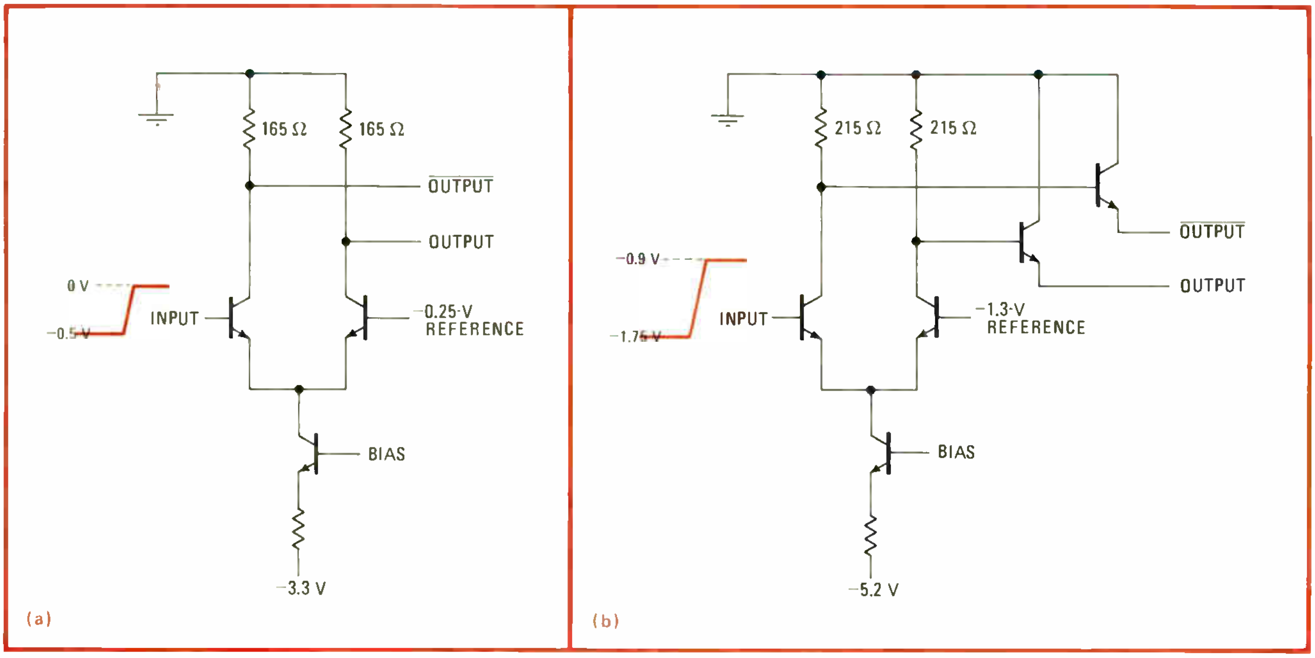
From the earliest days of bipolar technology, circuit designers noted that current switches are faster than their voltage counterparts. A logic family based on steering currents without altering their values, then, seems intrinsically faster than one based on voltage-switching techniques, such as TTL, that actually turn currents on and off. With some tradeoffs, that has indeed proven true with ECL and CML.

Both varieties use a differential pair for the major switch, which behaves like an operational amplifier driven completely to the supply voltage in each direction. Circuit diagrams of the basic gates look similar (Fig. 1), but they differ subtly in operation.

The reference voltages represent the center point of the logic swing. In ECL, with a −1.29-volt reference and a nominal collector voltage swing of 0.85 V, the collector-base junction on the signal-input side goes to 0 V under worst-case conditions. On the reference side, that junction always remains reverse-biased by 0.44 V. Thus, the transistors never saturate, speeding switching. However, the emitter follower is always on, increasing power consumption. The use of the emitter-follower output dictates the ECL operating levels. Rather than rising all the way to 0 V, as in CML, the ECL high level stays a diode drop below to drive the emitter-follower output stage.

In contrast, CML employs a reference voltage of 0.25 V and a signal swing of 0.5 V. The collector-base junction of the input transistor then becomes forward-biased by 0.5 V at most, a condition termed soft saturation because negligible forward injection across the junction takes place. With little excess charge stored in the base in soft saturation, switching speed remains comparable with that of ECL. At the same time, an off transistor cuts off completely, keeping power consumption of the basic switch to a minimum. Furthermore, the additional power of ECL's emitter-follower driver is eliminated.

The single differential pair of a CML gate drives the following gates directly from either collector—both true and complement outputs are available with nearly equal



1. Cousins. The basic current-mode logic gate (a) differs from the emitter-coupled version (b) in not including an emitter-follower driver. Also, the 0.5-volt logic swing of CML takes transistors into soft saturation, slightly turning on the base-collector junction.

speed. A typical 3-micrometer-geometry gate switches in 0.7 nanosecond. Gate delays are essentially a single transistor delay because most logic functions are implemented with a single differential pair as the primary switch. As in ECL, series gating generates the most useful logic functions with a single logic-gate delay, as in the exclusive-OR gate shown in Fig. 2. The 3.3-V supply is the minimum voltage that supports the series-gating logic structure, so CML's power consumption is at an absolute minimum, without sacrificing any speed.

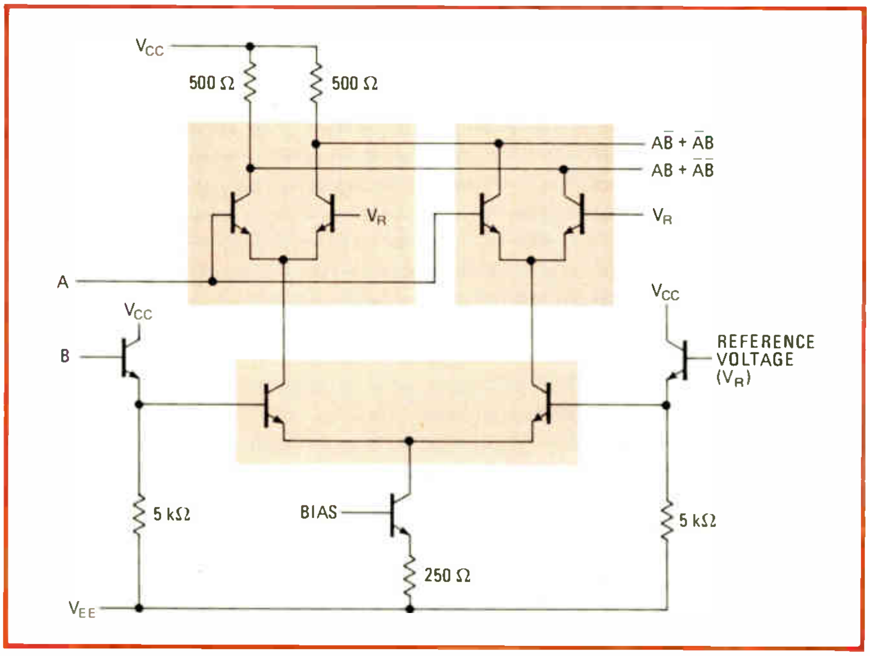
The temperature dependence of the CML operating point limited its use in the past. As temperature increases, the forward current across the collector-base junction increases, preventing CML operation above about 85°C. In effect, therefore, the soft-saturation region moves to lower collector-base voltages, slowing the circuits.

In the present generation of CML intended for very large-scale integration, currents are set on chip by a voltage- and temperature-compensated reference regulator, so that the current and the corresponding logic swing will stay below the collector-base saturation voltage (Fig. 3). Reliable operation at up to 110°C has been achieved.

Although those advantages and problems of CML have been known for some time, yet another set of constraints has kept ECL in the fore. The transmission medium and typical distances between gates in past systems heavily favored ECL, which is a load-terminated circuit, over CML, which is a source-terminated circuit.

To see this difference and the tradeoffs involved, assume a typical system configuration of the past decade: small-scale ICs on printed-circuit boards. The basic logic functions are housed individually in dual in-line packages mounted on copper-clad glass-epoxy circuit boards having nominal trace impedances of 50 to 100 ohms; up to several inches separates packages, and several ICs are connected along the printed transmission line.

When a CML gate drives such a network, the voltage

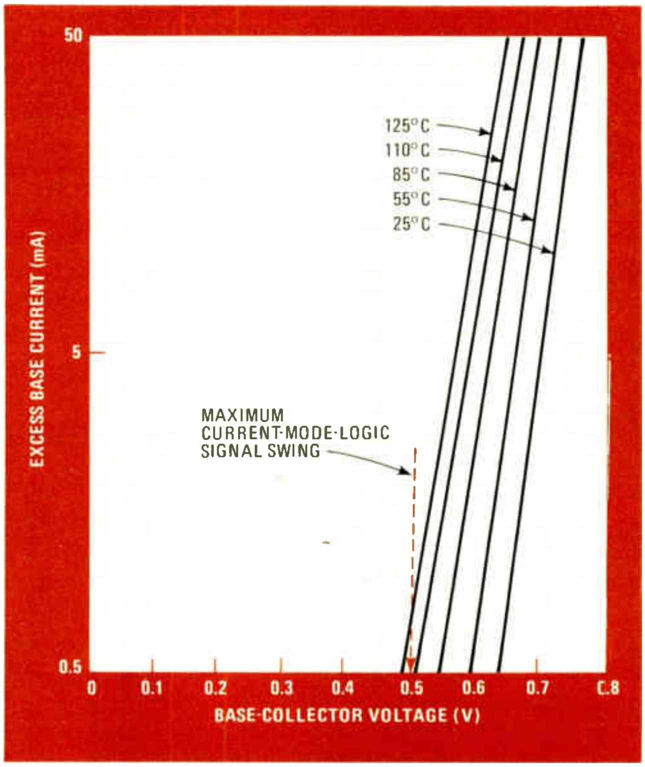


2. Series gating. CML, like ECL, economizes on transistors in the basic logic functions, as in this exclusive-OR gate. The B input switches the lower transistor pair, steering current to one of the two upper differential pairs that are switched by A.

division between the collector resistor of the gate and the characteristic impedance of the transmission line propagates a wave of voltage lower than the logic threshold down the line. Gates tapping off the line do not switch as the wavefront passes, because the voltage level is below threshold. When the wavefront reaches the far end of the line, it reflects off the high-impedance termination (the base input of another CML gate), bringing the voltage level up to full amplitude. As the reflected wave returns, the full-amplitude signal switches the stub-connected gates (Fig. 4). Gates close to the driver see almost twice the transmission delay, since the wavefront travels twice as far. Whatever delay the fast current-mode-logic gate saves, the doubled medium delay loses.

Source termination—the CML driver's collector resistor—is simply a poor solution for driving a line with distributed loading and has prevented CML from entering the market for standard logic parts. ECL's low-impedance emitter-follower output is a good solution: with the low-impedance output, voltage division with the line impedance is a minor effect, and a nearly full-amplitude wave propagates down the line, switching all the gates on the first pass. At the final load, the line terminates in its characteristic impedance, preventing reflections. Unfortunately, considerable power is consumed for this driving capability, more than is used in the gate itself.

In addition, even with the increased power consumption, transmission delays still account for roughly 50% of the overall delay. Clearly, those typical configurations of the past do not represent the ultimate solution for large systems.

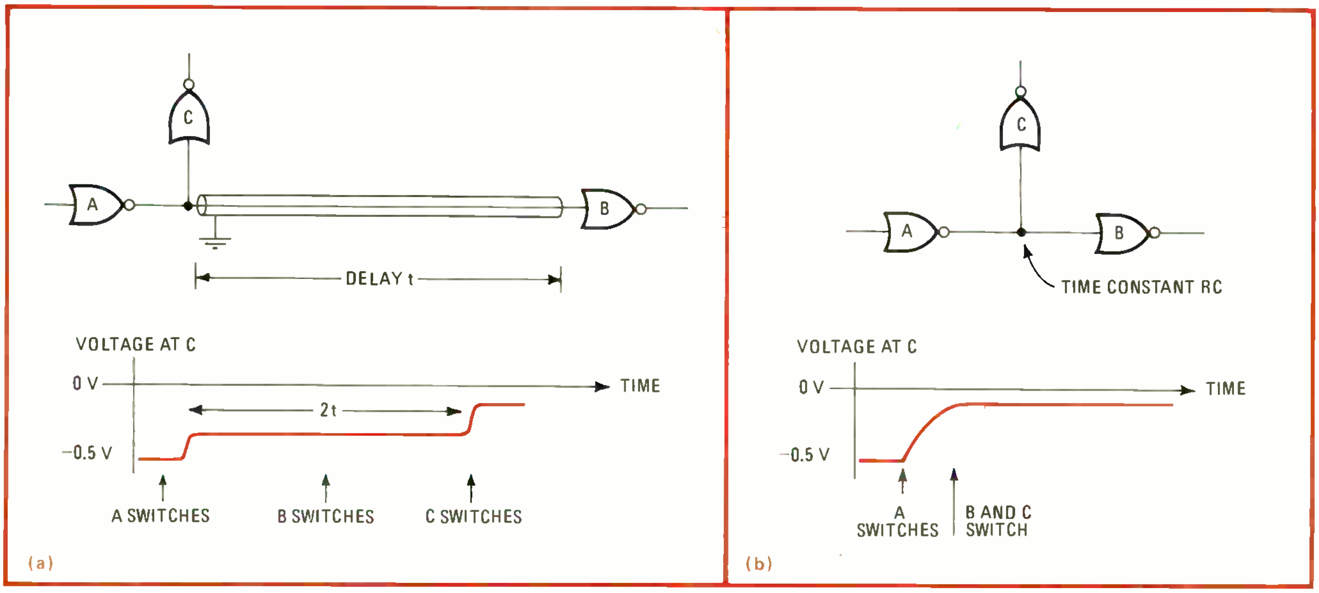


3. Soft. Excess base current to a forward-biased collector-base junction increases with temperature. To allow CML circuits to operate at high temperatures, the reference-voltage generator keeps the logic swing below the diode turn-on voltage.

The CML environment

With the advent of VLSI technology, a great many gates can be put on a single chip, where no significant transmission delay is encountered. In a micropackage, 50 to 100 CML chips can be mounted on a single substrate close together. In this case, the wires between chips are short enough that they behave as simple RC loads, rather than as the distributed load of a transmission line. In this environment, CML comes into its own.

CML's low 0.5-V logic swing means that load capacitances are charged more rapidly. Chips on a single substrate are at close to the same temperature, so that operating points differ little, maintaining noise margins. A CML gate may be readily modified to provide a



4. Termination. Switching a distributed load from the collector resistor of a current-mode logic gate in effect doubles the transmission delay (a). For the simple RC loading on chips or within a micropackage, CML has adequate drive capability (b).

low-impedance emitter-follower output, so that an ECL-like line-driving capability is available where needed.

Anticipating a large investment in CML as a logic family requires some attention to the process technology and expected yield of the chips. Since CML's supply voltage is only 3.3 V, lower breakdown voltages may be tolerated in the substrate. Heavily doped low-resistivity starting material is more impervious to impurity contamination, boosting yields.

Other factors also increase the yield of CML chips. CML ties driving collectors directly to receiving bases. Collector resistors are a low 100 Ω, so that emitter-base junction leakage currents cause negligible voltage drops in them. As a result, greater process variations are tolerated. Overall, the small number of devices per gate, plus recent advances in processing technology allowing two and three levels of metal wiring, help keep chip area manageable. CML depends on a correct ratio of emitter to collector resistance, but not on either's absolute value—another margin for error that helps yield. □

Part 2

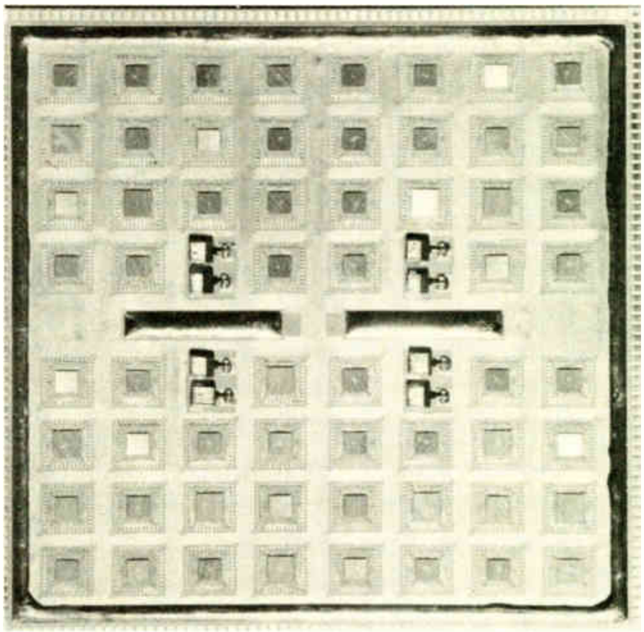
Flip TAB, copper thick films create the micropackage

by Chandler H. McIver
Honeywell Information Systems Inc., Phoenix, Ariz.

□ The multilayer board and dual in-line package that had been the pick of Honeywell's packaging designers for previous computers could not quite cut the mustard when it came to accommodating the extraordinary interconnection density, performance, and heat dissipation of the current-mode logic arrays of the DPS 88 mainframe computer. So, to unleash the high switching speeds of the arrays, a new multichip package was created. Called a micropackage, it consists of a large multilayered ceramic module with the CML large-scale integrated circuits bonded face down to copper thick-film conductors on the substrate in the method known as flip TAB, or tape automated bonding. These packages, in turn, are then mounted on a multilayered motherboard to achieve a high chip-packaging density with minimal wiring lengths.

At 80 millimeters on a side and with five layers, the micropackage shown in Fig. 1 carries up to 110 chips and has 240 input/output pads. One such package is the equivalent of two 12-by-12-inch multilayer printed-circuit boards and their associated hardware. It is fully up to the job of housing the dense wiring needed for the matrix of chips, with no degradation in performance, and of dissipating the high power generated by the large number of chips.

The dual keys to the success of the new package are its large-scale employment of the flip-TAB technique and the optimum electrical and thermal design of the large thick-film hybrid assemblies. Because the advantages of the micropackage *in toto* could not have been realized without a suitable IC package, the second level of packaging—comprising the chip and its beam-tape leads—merits first scrutiny.



1. Micropackage. Honeywell developed this micropackage for the subnanosecond logic of its new DPS 88 computer. The 80-by-80-mm multilayer ceramic substrate holds an average of 60 chips and replaces two 12-by-12-inch multilayer boards loaded with DIPs.

Facedown TAB

The TAB technique has gradually gained industrywide acceptance for assembling DIPs and hybrids because of its reliability and built-in chip-handling ability, plus the opportunity it presents for testing chips on tape. In conventional faceup TAB, specially bumped chips are mass-bonded to the inner leads of patterns, which have been etched from a thin layer of copper laminated on an insulating film. In a hybrid application, a chip and its copper interconnection are first excised from a frame of tape; then, with the chip facing up, its back side is epoxy-bonded to a ceramic substrate and its outer tape leads bonded or reflow-soldered to conductors on the substrate.

However, the current faceup TAB assembly invited improvement, for in certain circumstances it unduly stressed inner-lead bonds. Investigations into alternative TAB structures led to the development of facedown, or flip, TAB. The newcomer avoided the stresses that stemmed from faceup TAB and indicated its use would reduce TAB assembly cost and hoist the overall reliability of the final product.

The secret of flip-TAB assembly is its elimination of the risky lead-forming procedure, with a savings in substrate real estate as an added benefit. With flip TAB, chip thickness is not critical, and no back metalization is needed. Compared with the earlier solder-reflow method of forming outer-lead bonds, flip TAB is more easily automated. The use of an epoxy die attachment acts to encapsulate the inner lead bonds, strengthening them and preventing the mechanical contact of leads with die edges, which are vulnerable to short circuits due to thermal and mechanical stress.

The process is relatively unencumbered by accessory materials. No flux is required for certain outer-bond material systems, such as tinned copper leads bonded to gold thick-film pads on ceramic substrates. And in metal systems where pretinning of outer-lead bond pads is required, as with the copper conductors of pc boards, the usual solder dam for strict height control of the solder is also unnecessary. As a further advantage to flip TAB, it is possible to stack one chip on top of another if needed, and the whole structure may be bonded to pc boards.

But the technique has its down side as well. Only a limited number of chip replacements can be made at each site, for example, although in certain instances, such as in pretinned outer-lead bonding pads, a large number of repetitive repair operations can be performed at a given site by reapplying solder.

Another disadvantage is that an assembly attached by the epoxy-die method can only dissipate so much heat. It is adequate for the current generation of chips using the flip-TAB assembly method, as in the hybrid that was shown in Fig. 1, but with higher-powered chips (1.5 watts and up), an assembly consisting of epoxy die attachments on a substrate would not be able to handle the heat generated for many multilayer ceramic assemblies. With pc boards, however, it is possible to rig up heat sinks to take care of the problem.

In the flip-TAB process, a chip that has been mass-bonded to the inner leads of a chip pattern on tape is placed, active surface down, onto a substrate where an epoxy preform has been placed on the die's bonding pad. All the leads extending from this chip are then bonded simultaneously to their respective bonding pads by thermocompression bonding or reflow soldering. A step-by-step description follows.

After inner leads are bonded to the tape, chips can be supplied in one of two forms—on reels of tape or on individual frames of tape mounted in 2-by-2-in. slide carriers suitable for automatic handling. The leaded chips are automatically excised from the tape with lead lengths 3 to 5 mils longer than the maximum spread of the outer-lead bond sites on the substrate. These chips are then placed active side down onto already positioned B-stage epoxy material approximately 3 to 5 mils thick, which is held at 120°C. For the large multichip hybrids involved in the DPS 88, all chips are placed on the substrate within a 20-minute time frame.

After a partial curing of the epoxy, thermocompression bonds are made for all outer-lead bonds of each individual die. Figure 2 presents a simplified drawing of the thermode, die, and substrate positions during a typical outer-lead bonding operation involving flip-TAB chips on a multilayer ceramic substrate with thick-film conductors.

Flip-TAB procedures can be used in either individual IC packages or on hybrid structures with a variety of metalizations. The relatively low overall processing temperature and built-in stress relief suit the technique to both pc boards and ceramic substrates or chip-carriers. On the former, chips have been successfully placed onto boards coated with tin-lead solder using flip-TAB techniques; ceramic substrates accepts metalization of the common thick- or thin-film materials.

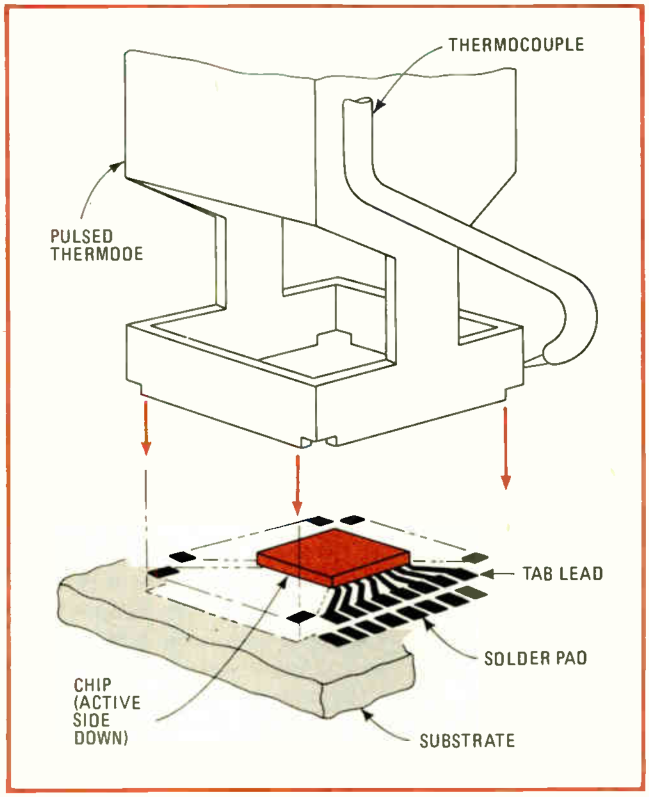
When chips are being tested after the inner-lead bonds have been formed, a three-layer beam tape made of 35-mm polyimide tape laminated with epoxy to 1-ounce copper foils acts as an insulator and support to prevent the chips from short-circuiting. After testing, the chips are readied for reflow soldering by electroless immersion-plating the etched lead frames with a tin coating to a thickness of 0.5 to 1 micrometer.

The epoxy that attaches the chip to the ceramic is electrically insulating yet thermally conductive in order to ensure mechanical integrity and dissipate heat. It can be applied with a dispenser, screen-printed, or laid down as a preform.

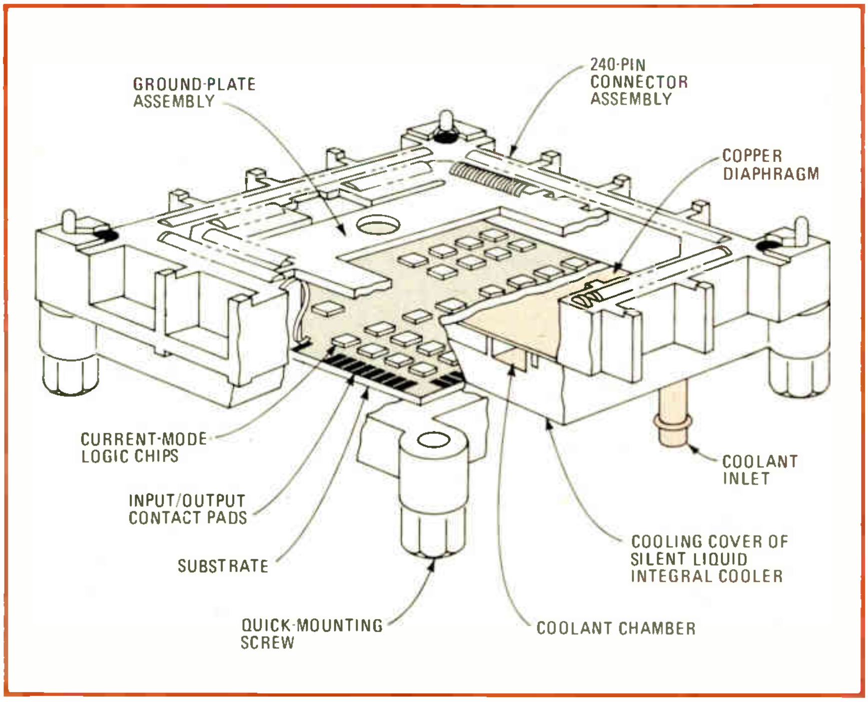
Pit stops

In a multichip hybrid configuration as complex as the DPS 88's, easy-to-follow procedures are paramount for repairing individual open connections or removing and replacing chips. Using TAB bonding to gold thick films on a ceramic substrate as an example, the following steps illustrate the procedure. With modifications, they apply to copper thick films as well.

A modified pulse-tip bonder with a solid-capillary bonding tip is needed to repair individual open bonds. The process is simple: the lifted lead is captured between the bonding capillary and the outer-bond pad, and a



2. Face down. CML chips are mounted in a patented tape-automated-bonding process onto the multichip-carrier substrate with their active faces down. Flip-TAB mounting protects the face of the chip and ensures accurate alignment with the outer-lead bonding pads.



3. Silent cooling. A simplified drawing shows the structure of Honeywell's silent liquid integral cooler, which houses the micropackage and makes a dry greaseless contact with it. A faulty micropackage can be replaced in about 6 minutes without shutting down the computer.

bond is made. If the tin on the lead or pad appears oxidized, a small gold-tin preform may be put down to aid the bonding operation.

To replace a chip, on the other hand, its outer-lead bonds must be cut. A hot-air gun heats the chip, softening the epoxy beneath it so it can be pried loose. Next, a new chip with an epoxy preform is applied, partially cured, and the chip thermocompression-bonded to the outer-bond sites using TAB equipment. In this operation, the remains of the old leads at the outer-bond sites need not be cleaned or removed—the leads of the new chip can be bonded right over the old ones, creating in effect a tin-to-tin bond. But such a bond has a lower pull strength (35 to 40 grams) than a totally new bond. For optimum reliability, the old leads can be removed by cutting them horizontally at the pad and re-exposing the gold thick film. The pull strength of a bond made to the film will be a much-improved 85 to 90 g.

Heated up

The key criterion of the reliability of flip-TAB outer-lead bonding for assembling chips in hybrids was analyzed in terms of both the maximum power dissipation of a bonded chip and the final metallurgical composition of the outer-lead bonds. The thermal analysis was made on a worst-case situation; that is, assuming heat was dissipated only through the leads, not through the epoxy. A 10°C temperature difference was assumed between the hybrid substrate and the ambient air, and the power-dissipation capacity of the bonded chip expressed in watts. Under these conditions, an 80-by-80-by-10-mil chip with 14 copper leads spaced evenly around the edge of the chip was able to dissipate 500 milliwatts of power, a figure large enough to permit flip TAB to be used with most logic chips.

To assess the compatibility of materials, plus long-term reliability, the metallurgical interactions at the outer-lead bond sites were characterized. The setup tested involved tinned, cold-rolled copper leads bonded to gold thick-film pads on alumina substrates.

Because the critical factor in alloy formation and elemental distribution is the soundness of the outer-bond sites, bond strength and mode of failure were determined by pulling leads on a universal bond tester. The results were more than satisfactory: typical pull breaking load was found to be around 100 g, with failure occurring at the point of pull.

The examination continued. Chips with sound outer-bond sites were then taken in the as-bonded and as-aged conditions, sectioned, and examined under a scanning electron microscope. In conjunction with this testing, energy dispersive analyses by X ray determined the tin content in the gold. It was found that in no case did the tin content exceed 29% by weight, implying that the outer-lead bond that was formed consisted of alloys near the gold-tin eutectic region and exhibited good electrical and mechanical properties.

Great expectations

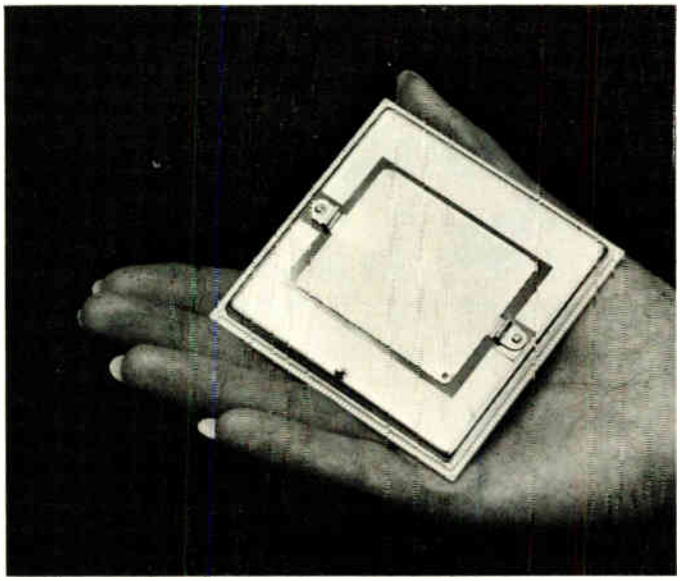
All tests to date have exceeded expectations and, what's more, indicate that there are in fact additional applications for flip-TAB processing in packaging electronic assemblies. The TAB technique's chief selling points are its compliant nature, coupled with the high bonding strengths and the increase in environmental and mechanical protection for the IC.

The bare CML chip and its tape "package" compose the first two levels of interconnection of the DPS 88. The third level is the 80-mm-square multilayer ceramic substrate to which the chips are attached by flip TAB.

A computer-aided-design study set up to maximize logic and bit density without sacrificing the producibility of the product defined an ideal ceramic structure as having two internal logic layers, each of which containing 4-mil (100-μm) lines on 10-mil (250-μm) centers, plus three internal power planes. A typical substrate has the equivalent of 15 meters of wiring.

The conductors of the logic layers are perpendicular to each other. The first layer contains the so-called X lines, and the second holds the Y lines. They are separated by a dielectric that typically has more than 2,400 vias, each 200 μm square, interconnecting the X and Y lines. Its dielectric constant is 7.6. The Y lines are, in turn, separated from the power structure by another dielectric. After this layer come the third, fourth, and fifth metal layers, each carrying a specific voltage, represented by V_{cc}, V_{ref}, and ground, respectively. With this structure, the characteristic impedance of the signal layers is 35 ohms. Eight patterns are available to accommodate various combinations of chip sizes and lead counts.

As for power, the full complement of chips for a micropackage requires a maximum power of 60 W, which is distributed in parallel paths directly from power planes to the chip pads with a maximum voltage drop of 1 millivolt. The main thermal path taken by heat from the chips is through the chip leads and the epoxy die attachment, then through the ceramic layer to the back of the substrate. The thermal conductivity of the multilayer ceramic substrate has been determined to be approximately 0.00172 W/mm²/°C. A copper diaphragm physically contacts the back of the substrate to water-cool a total of 60 W by means of a setup known as a silent liquid integral cooler (Fig. 3).



4. Lidded. The lid of the micropackage seals the substrate, supplies primary power to the substrate, and provides mechanical protection for the chips. The lid is soldered to the seal ring of the substrate, and a ground is supplied through the seal ring.

Copper thick films

All conductor layers are made of screen-printed thick-film copper with a resistivity of 3 milliohms per square. Metalization for all five layers is accomplished by first running an angular squeegee across a screen-emulsion mask, forcing both the paste through the mask and the mask against the substrate and thereby defining the pattern desired. The metalized substrate is then dried and fired at 850°C in a nitrogen atmosphere.

In a sequence repeated for every dielectric layer, the desired pattern is defined by coating a negative-acting liquid photoresist on the thick-film material of the dielectric, whereupon it is dried and then exposed to ultraviolet light through a photomask. The unexposed photoresist and unwanted dielectric materials are removed when the thick film is fired in the burnout step.

The multilayer substrate is screen-printed with a solid layer of dielectric and fired. The application of a low-viscosity paste minimizes the chance of pinholes—the paste's thickness is a function of the screen's mesh and wire diameter. As a precaution, the copper dielectric should be fired in nitrogen to protect the copper from oxidation. Neither the dielectric's physical and electrical properties nor its surface topography are adversely affected by either the photopatterning process or subsequent firing.

To ensure a high process yield, the substrates are tested with a specially designed capacitance tester at the metal layers. The finished substrates must also pass isolation testing of 10^8 Ω at 100 V. After testing, the I/O pads are gold-plated.

The micropackage lid of Fig. 4 fulfills three functions: first, it provides a hermetic seal to the micropackage substrate; second, it supplies primary power to the surface of the substrate; and last, it serves to mechanically protect the components bonded to the micropackage surface.

To meet a stringent hermeticity standard, the lid was designed as a single piece, a cold-drawn dish with the sealing edge ground flat to within 0.1 mm. The flat edge is soldered to the seal ring of the substrate to form the seal. The major ground for the micropackage is supplied through the seal ring and subsequently through the lid by two glass-to-metal hermetic feed-throughs, to which the voltage is distributed by fully annealed copper contact strips. Annealing ensures that no stress is transmitted to the feed-through from the contact strip. An internal contact strip distributes the voltage potential across the micropackage surface by contacting the third metal layer with several contact finders.

Thin films of Du Pont's Kapton placed between the contact strips and lid insulates them. The entire lid is assembled into a single unit and tested for hermeticity. For extra insurance, all joining is performed with 10/90 tin-lead solder whose melting range of 275° to 300°C is well above the 183°C melting point of the eutectic solder that attaches the lid to the substrate.

After testing, the lid is attached to the micropackage by pretinning the seal ring and the V_{cc} touchdown points with eutectic solder and heating the micropackage and lid at a controlled cycle until all edges of the lid have wetted. The unit is then cooled and removed from the heater. After the attachment process has been finished, the complete micropackage is further subjected to tests for hermeticity and functionality.

The setup stands up under capable multiple rework cycles and engineering changes. Access to the surface of the multilayer substrate can be had by elevating the temperature of the entire package above the liquidus temperature of the alloy sealing the lid and then lifting the lid assembly off the seal ring. Before resealing the micropackage, the solder on the substrate's seal ring is flattened to make good thermal contact with the lid during the reflow-heating process.

The proven hermeticity of the micropackage assembly, combined with silicon nitride passivation of its chips, make for a highly reliable microelectronic package that can be replaced in the field. □

On-chip and functional testing spearhead attack on VLSI systems

Also noteworthy at 1982's International Test Conference will be humidity tests, diagnosability, and a self-scan plus chip-test pair

by Jerry Lyman, *Packaging & Production Editor,*
and Richard W. Comerford, *Test, Measurement & Control Editor*

☐ Accelerated testing of plastic-packaged devices and a Schottky TTL test bar are just two of the unusual subjects being aired at this year's International Test Conference in Philadelphia. Less esoteric, perhaps, but equally instructional are the many fine papers on some of the deficiencies of in-circuit testing, leading in session 18 to a refocusing on the role of functional testing. The user is the ultimate beneficiary, for the papers presented here point in unison to greater product reliability.

Meanwhile, dominating many other sessions are the techniques of self-testing and level-sensitive scan design (LSSD). One particularly interesting paper discusses the advantages of combining the two.

Plastic under pressure

With more and more large- and very large-scale integrated devices like 16-K and 64-K random-access memory chips appearing in plastic packages, it becomes increasingly important to test their resistance to the combined effects of temperature and humidity. At present, pressure cooker and 85/85 (exposure to 85°C at 85% relative humidity) are the standard evaluation techniques, largely because of their simplicity, reliability, and reproducibility. The primary failure mechanisms uncovered by pressure-cooker testing are chemical corrosion and threshold shifts, whereas 85/85 testing pinpoints vulnerability to electrolytic corrosion.

Improvements in device processing and passivation and in plastic encapsulants and molding techniques have made plastic-packaged devices much more reliable, prolonging 85/85 testing times to an excessive 1,000 or 2,000 hours.

In session 11, a paper by Eugene Gottlieb of Burroughs Corp., Piscataway, N. J., describes a sequential procedure in which pressure cooking for 16 to 24 hours to expel moisture from a die is followed by an 85/85 procedure lasting 40 to 100 h. Called pressure cooker plus temperature humidity, or PCTH, this technique dramatically reduces the time it takes the moisture to reach the die surface, thus shortening testing time. It has been applied mostly to MOS RAMs but should also be applicable to other MOS and to bipolar plastic-packaged parts.

At Burroughs, the PCTH method detects a wide range of processing and packaging problems, including incorrect post molding, shear- and form-produced cracking, stress-induced cracking of the passivation layer and low phosphorus content in it, and prior incorrect storage of plastic molding material.

To develop its vendors' confidence in the method, Burroughs recently correlated its PCTH results with those of one of its major vendors. Both subjected four separate lots of 108 or 110 packaged integrated circuits to a 96-h PCTH at 125°C and a 24-h PCTH at 130°C, while Burroughs also did direct 85/85 testing for 2,000 h. As the table shows for two lots, correlation is excellent.

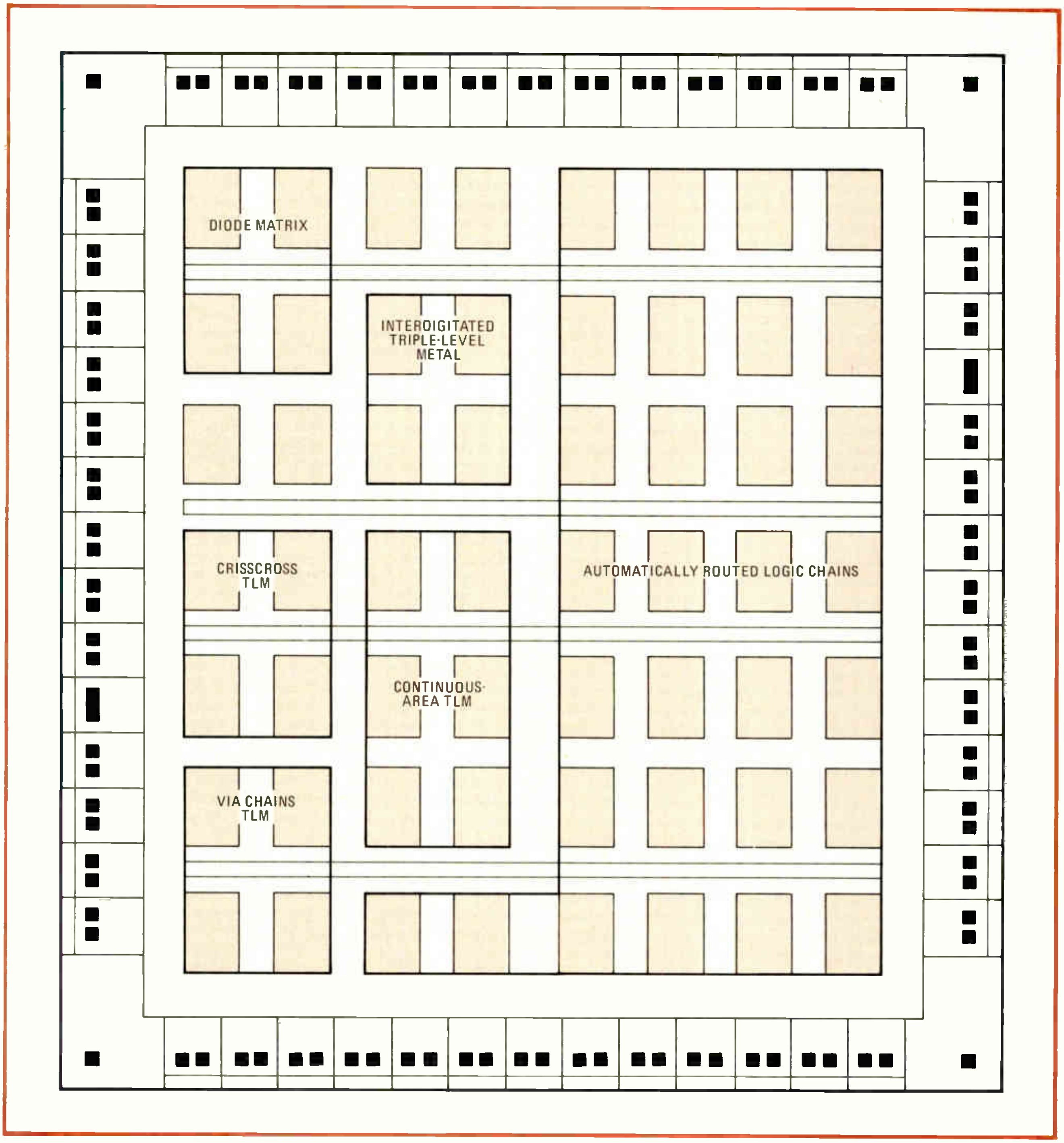
COMPARISON OF USER'S AND VENDOR'S PRESSURE-COOKER PLUS TEMPERATURE HUMIDITY (PCTH) TESTS

Test condition	Failures in lot 1		Failures in lot 2	
	Burroughs (108 parts)	Vendor (110 parts)	Burroughs (108 parts)	Vendor (110 parts)
125°C 96 h	0	0	0	1
130°C, 24 h	3	3	2	2
85/85, 50 h	0	–	0	–

Test bar

Test engineers normally glean their reliability statistics from long-term testing of packaged chips. However, IC manufacturers have long tracked the reliability of their processed wafers by means of test bars or chips with which various system and process parameters can be monitored. In his paper in session 11, Joel Le Blanc of Texas Instruments Inc. in Houston describes a test chip that monitors aspects of reliability unique to a wafer composed of Schottky TTL gate arrays (Fig. 1). Designed for TI's TAT008, a gate array consisting of 1,008 gates and 104 buffers, the test bar introduces the absolute worst-case condition for any given routing setup. The four major reliability areas addressed by it concern the internal gates, advanced-Schottky and Schottky diodes, triple-level metal (TLM), and input/output buffers.

Maximum fan-in–fanout conditions create the highest internal gate-current density, while minimum fan-in–fanout conditions serve as the low-current control. These internal gate-current conditions are developed through the use of logic chains where each stage has either a maximum or a minimum logic number. The heavily loaded chain consists of gates linked in series and



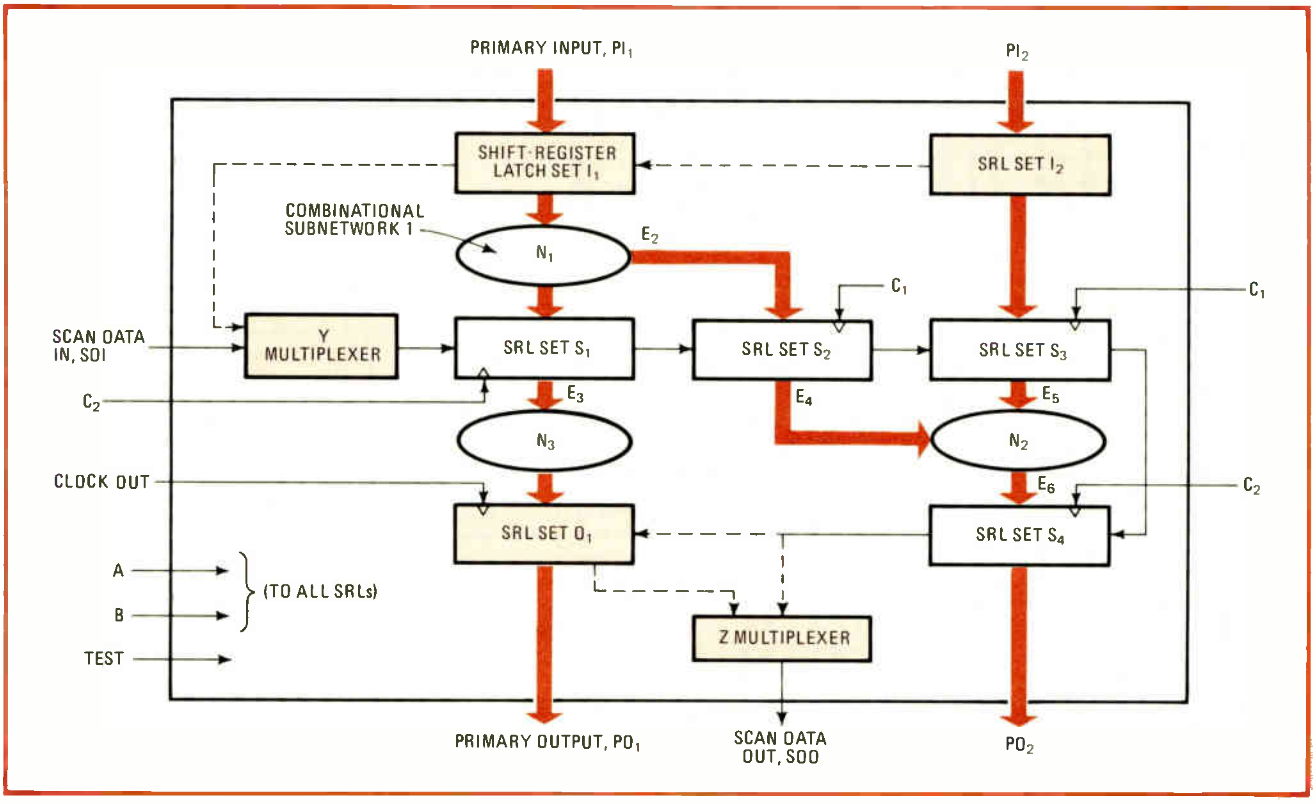
1. Test bar. A test bar for checking a TI TAT008 gate array is shown in simplified form. Each colored area tests one aspect of chip reliability. For example, the triple-level metal areas test for various failure mechanisms in the TLM interconnection.

each with a fan-in of 8 and a fanout of 4. The lightly loaded chain consists of a series of gates, each with a fan-in and fanout of 1. Controlling these gate chains independently makes it possible to separate similar logic-current densities. Comparison of individual gate-chain failure rates during reliability testing can thus be related back to the internal gate-current densities.

As for the advanced-Schottky and Schottky diodes, their reliability is checked by a matrix of 360 individually addressable elements consisting of 288 advanced-Schottky and 72 Schottky diodes. This section of the test bar permits monitoring of the devices' stability in both the forward and reverse voltage directions.

Interlayer via chains and multiple patterns of metal help to assess the reliability of a TLM interconnection system used on each gate array. The on-chip TLM structures are all designed to simulate worst-case routing and biased to worst-case operating-current densities. During reliability testing, four types of structures are employed: a crisscross metal structure, a continuous-area TLM, an interdigitated TLM, and multilevel via chains.

These TLM structures overlie diffusion areas of gate



2. LSSD self-test. With the addition of the circuitry shown in color, a digital network with level-sensitive scan design (LSSD) gains an on-board pseudorandom-pattern generator. Output responses are analyzed in either an external or on-board digital signature analyzer.

transistors as well as channel-routing areas where such diffusion is absent. With their aid, various failure mechanisms such as metal-to-metal shorting or opening, high via resistance, and dielectric pinholes can all easily be detected.

To check I/O buffer reliability, combinations of I/O structures are used to create high current density in the I/O power-distribution network. With all these output buffers simultaneously being switched low, maximum I/O power-bus transients are created along with large instantaneous power surges.

Self-test plus level-sensitive scan

Level-sensitive scan design (LSSD), a technique in heavy use at IBM [*Electronics*, Nov. 8, 1979, p. 116], has simplified LSI testing in two major ways. It makes a chip's internal circuitry more able to be controlled, and hence observed, and it can transform sequential circuits into combinational circuits. Because each shift-register latch in the LSSD circuit can become a control or observation point, how easy or hard it is to control and observe the circuitry no longer depends on the number of pins in the package. Furthermore, because the latches themselves are part of the internal circuit, they can be used to break feedback paths in a sequential circuit, enabling the paths to be tested combinationally.

Basically, LSSD testing is a matter of shifting test data into the shift-register latches, applying test vectors to the primary inputs to the chip, clocking the system clocks, and scanning the data out of the latches for comparison with known-good test vectors.

A disadvantage with LSSD, however, is that test generation is a heavy burden. Designers either have to go through a cycle of test generation and fault simulation that is largely manual, or else an LSSD test generator has to be developed to automate the procedure. In either case, the end product is a sizable set of test and response vectors that has to be catalogued and stored. Even then, to apply the vectors to the chip and collect the responses, elaborate LSI testers are needed. Moreover, the testing is time-consuming because the vectors have to be serially shifted in and the responses shifted out. As the density of chips increases, so, too, does the test-generation effort.

In his paper in session 14, Donald Komonytsky of Storage Technology Corp., Louisville, Colo., proposes an LSI test using LSSD and self-testing that combines the best features of both. Briefly, the advantages of self-testing are that test vectors are generated speedily and automatically inside the chip; neither test nor response vectors need to be stored externally; and testing can proceed much faster than is normally possible with LSI testers. No expensive testers are needed, and with proper partitioning, self-test efforts can be made largely independent of chip density. The disadvantage of self-testing is that it demands extra resources in terms of design time and chip area.

Komonytsky proposes instead that some of the shift-register latches that are inside a chip be linked into a linear feedback shift register that can generate pseudorandom test patterns to stimulate the chip logic (Fig. 2). In this method, all the latches normally inside the chip are used in the self-test, and extra ones are added to the input and output pins of the chip. Test vectors generated internally are pseudorandom. At this point, either an external signature analyzer gathers the responses from the chip or the signature is computed internally. Aside from the latches that are added to the I/O pins, additional chip area for self-testing is minimal. In the nonself-test mode, the self-test circuits inside the chip are transparent to both the system operation and normal LSSD functions.

The technique is easily applied to any chip that has been designed to the LSSD discipline and uses a minimum of real estate. There is one proviso—the extra latches on input and output pins must be integrated with the I/O buffers normally present on a gate array. Apart from these latches, the amount of extra digital logic required is trivial, consisting of some two input multiplexers and approximately a dozen exclusive-OR gates.

The author concludes by saying that it is to be expected that LSSD self-testing ability will become increasingly cost-effective as the density of digital ICs increases and the effort of test generation grows even greater. The reason is that circuit complexity and silicon area do not grow nearly as fast as circuit density, given that the shift registers internal to LSSD are already part of the chip.

Though techniques such as built-in testability may be the way in which boards and chips will be designed in the future, it will take significant retraining of the engineering force before the approach becomes commonplace, as was the case for signature analysis. Thus T. Jackson, P. Vais, and K. Schwerbrock of Zehntel Inc. in Walnut Creek, Calif., make a good case in session 18 for using an in-circuit tester as a means of letting an on-board microprocessor check its board out.

In Zehntel's scheme, the in-circuit tester presents a test program to a microprocessor and then serves to monitor results. Since the microprocessor actually runs at speed, the test is performed dynamically and timing-related errors can be found. The explanation in the paper uses an 8085A processor as an example.

In general, in-circuit testing has received too much attention in the past year, to the point where some facilities were coming to believe that it was the only type of automatic test equipment needed. This year, the conference is setting the record straight.

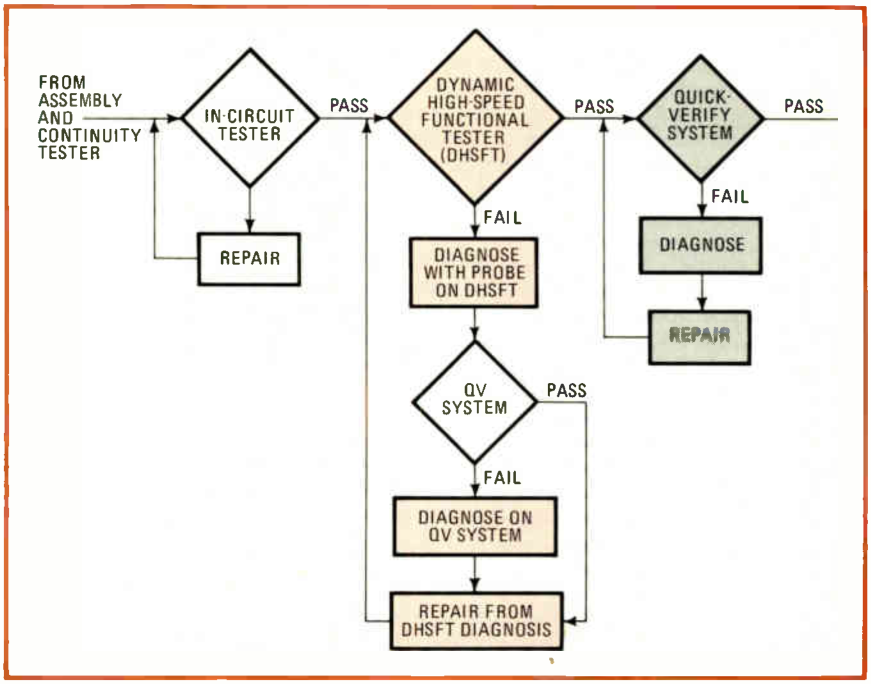
A balance in board testing

For example, GenRad Inc.'s Matthew Fichtenbaum will frankly present some of the problems that the Board Test division in Concord, Mass., has found to be significant challenges to in-circuit testers, along with some of the solutions that have been developed. And, in session 11, Louis Sobotka of American Telephone & Telegraph Co. in Parsippany, N. J., reveals data on the adverse effects backdriving can have on digital ICs during in-circuit testing—he notes that "at present, device specifications do not assure the suitability of devices for this test approach."

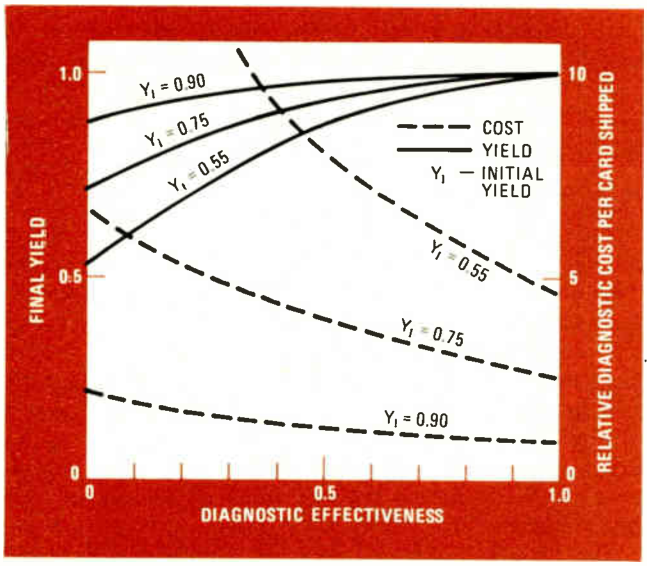
One company where functional testing has regained its rightful place on the production floor is Digital Equipment Corp. in Maynard, Mass. Jack Arabian, the company's well-known test guru, and Dennis Hebert will present the result of a study performed with the aid of other DEC personnel and Roman Sobon and Al Esser of Instrumentation Engineering Inc., Franklin Lakes, N. J.

The study was undertaken to see if ATE, in the form of a dynamic, high-speed functional tester, or DHSFT, could reduce the cost and time involved in diagnosing faulty boards, or modules. The DHSFT was compared with the test method currently used by DEC and many other companies, called a Quick Verify (QV) system. Sometimes known as a golden system, this is a known-good system of the type in which the board that is tested will actually be used.

The means of making the comparison while at the same time keeping production flowing is seen in Fig. 3, and the diagnostic software used on the DHSFT was modeled after that of the QV system. After some 850



3. With the flow. To investigate the efficacy of a dynamic, high-speed functional tester, DEC ran a functional test in parallel with a "golden," or quick-verify, system test as shown above. The functional tester won the competition hands down.



4. Diagnostic diagnosis. IBM investigators have shown that as the efficiency of a diagnostic regime increases, not only does the yield increase in direct proportion, but the actual cost of diagnosis for boards that are eventually shipped also goes down.

modules were checked, it was found that 92% of all failures encountered at this stage were caught by the functional tester, whereas only 44% were found by the QV system. Further, the 56% pinpointed by the functional tester alone, which uses a guided probe to speed diagnosis, were in every sense real failures that would have caused system-level test or field failures.

The system setup used by DEC also argues powerfully for combined in-circuit and functional testers. The same point will undoubtedly be made by Teradyne Inc., Boston, Mass., which will also be unveiling in session 8 a vastly improved version of Lasar test-generation software. Further, DEC has also undertaken and implemented an automated process for the generation of test software, an implementation that DEC's Hookuong Wong and David Florcik will discuss in session 2, the second one on board testing.

Pragmatic testing

Lest the advances of the last year bedazzle the conference's attendees, Peter Solecky and Frank Hsu of International Business Machines Corp.'s General Technology division in Endicott, N. Y., will close session 22 with an assessment of present board-diagnosis capability.

After defining the relationship between diagnostic efficiency, yield, and cost (Fig. 4), the two engineers critique guided probing and fault dictionaries. The probes, they note, though requiring only "modestly sophisticated software" to be effective, are a time-consuming approach—about 10 minutes on a complex card. And though fault dictionaries can improve test time, they are computer-intensive and require detailed gate models that are seldom available.

Solecky and Hsu therefore propose a discipline called design for diagnosability. It resembles structured design-for-testability techniques but adds the requirement that test points be so placed that failures causing the same type of fault can be easily distinguished. Also advocated is intelligent diagnosis—studying defect-occurrence statistics to speed diagnosis—and correlation between diagnostic results and process improvements.

These proposals tie in well with the theme of session 12—namely, use of test data analysis to close the production loop. Whereas a good deal has been presented so far on the various technical aspects of local networks, this session takes a very pragmatic look at real, on-line systems that are being used for both IC and board manufacturing operations.

For instance, IBM's East Fishkill, N. Y., operation uses what it calls MCMDATS, an acronym for multichip-module data-analysis tracking systems. According to R. Burgess, E. Pignetti, and J. Pitti of the corporation's General Technology division, the system delivers all the information considered essential to diagnostic procedures and personnel—and ultimately to keeping rework-ing cycles to a minimum.

The modules handled by the system are the 35- and 50-millimeter-square cards used in the 4300 processor. They have up to nine logic and/or array chips (approximately 6,000 logic circuits) and are tested using LSSD patterns. The tracking system resides on an IBM 370/168 host with a display terminal, print station, and 3330 MOD II disk drive, and has a time-sharing option operating under the MVS operating system.

The basic function of the system is to keep track of modules as they go through the rework process. When a module fails, an entry is made automatically in the active on-line data base and is kept there until the module has been successfully reworked, retested, and inspected. After this is done, the file is transferred to an archival data base.

On line, all failing modules are diagnosed by the system's MCM automatic diagnostics, which uses the tester's results, part numbers also provided by the tester, and part history. The history includes all electrical and visual-inspection failures and failing signature data (electrical net, I/O pad address, pattern number, and more). The information is used to determine whether earlier repairs were made properly and is passed along to rework along with visual inspection data. The system information is also made available to manufacturing engineering and to design engineering as well, for trend analysis. According to the authors, MCMDATS has become, "a vital tool" used now in IBM's French facility at Essonnes, as well as in East Fishkill.

But where IBM uses a custom system, General Electric Co.'s industrial control department in Charlottesville, Va., has put to use a commercial system—GenRad's Tracs. According to the paper to be presented by Paul Littlejohn of GE and Bruce MacAloney of GenRad, the system substantially reduced test time and costs for the 150,000 boards handled yearly in this operation.

The effectiveness of these local-network production systems is further brought to bear in papers from NCR Corp., Wichita, Kan., which employs test systems from different vendors, and from British Telecom Factories, Birmingham, UK, which employs both custom and commercial ATE along with remote data processing. With such systems in place, the next round of factory automation—the use of robots—is ready to begin. □

VLSI development system spans all phases of IC design

Stand-alone 32-bit computer captures, simulates, and verifies both logical and physical designs of very large-scale integrated circuits

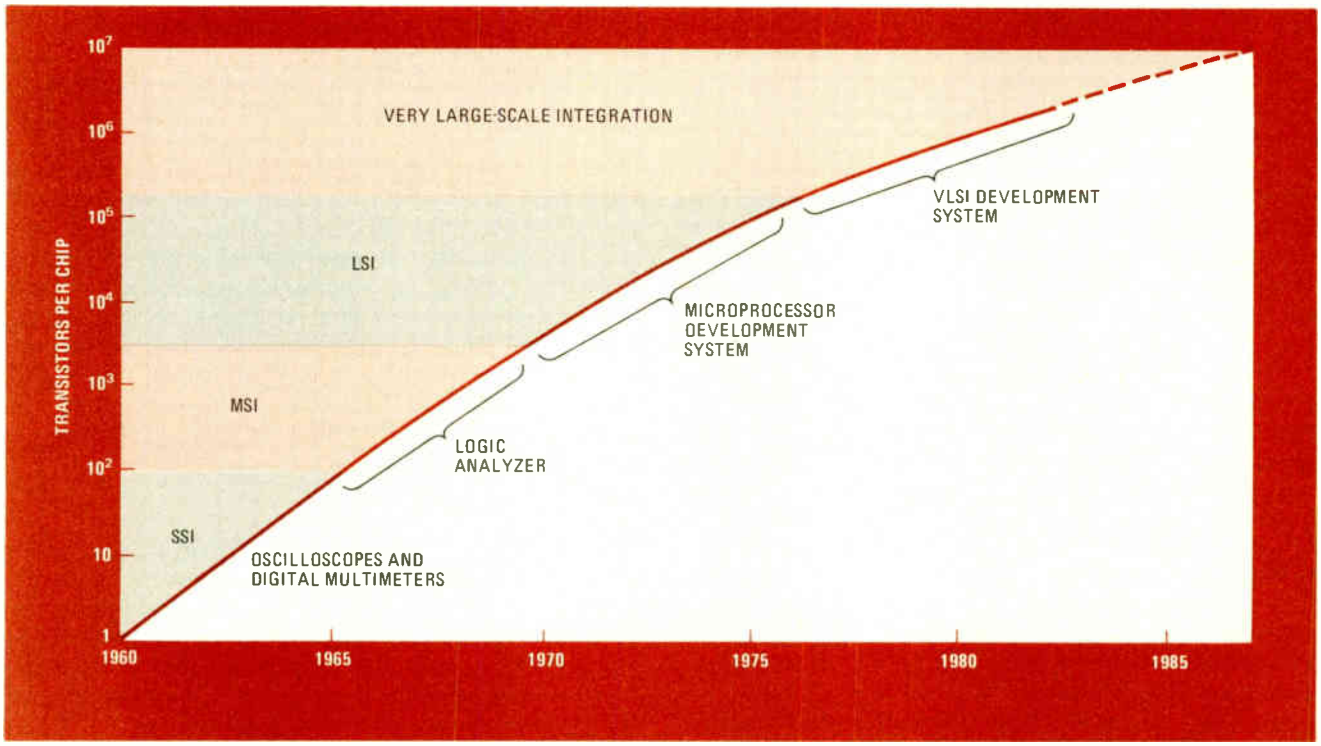
by Gene Chao, Chong C. Lee, and Terry Smith, *Metheus Corp., Hillsboro, Ore.*

☐ Out of the jumble of diverse and unstandardized software aiding the design of integrated circuits, the would-be custom-chip creator must put together a tool set. Work stations now on the market take on a piece of the job of developing very large-scale ICs: some lay out masks; others capture logic designs; assorted software packages simulate, place, and route circuits, check masks, and verify logic schematics. A stand-alone system spanning all these phases promises simpler, more accurate, and more productive designing.

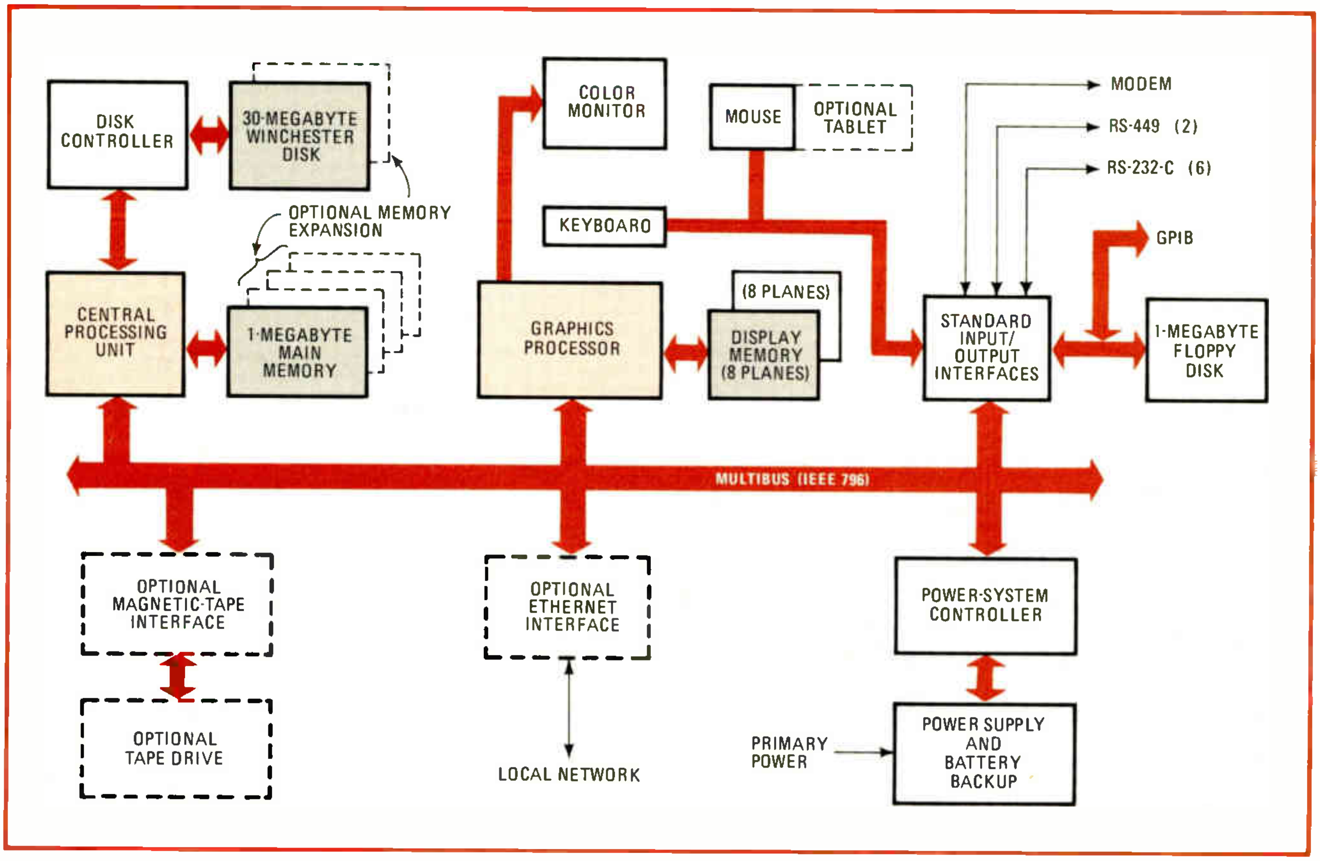
The λ750 work station provides access to a well-documented full set of integrated VLSI design tools, combined with facilities for project management and data-base control. Design information is therefore entered just once, eliminating a major source of errors. The hierarchical methodology of the programs eliminates redundant calculations, because a detail change at any level is iterated at all levels. This approach speeds execution and brings all the development tools to a highly interactive environment. Enhancing designers' productivity may stimulate innovation in custom VLSI designs, as well as providing a means of coping with the complexity of the chips.

Since the invention of the planar transistor in 1959, the complexity of electronics systems has increased as rapidly as has the level of integration in components. Two decades ago, products based on discrete components and resistor-transistor logic gates typically comprised a thousand devices. Today, 16- and 32-bit microcomputers and 64- and 256-K random-access memories reach users in systems containing upwards of 100 million transistors.

The skills to design such products have evolved concurrently. From a heavy reliance on logic and circuit design 20 years ago, through the acquisition of expertise in software and architecture development in the last decade, the electrical engineer's set of skills continues to



1. Future tool. Design aids evolve in step with chip complexity. A development system for very large-scale integrated circuits reflects the broad technology base supporting single-chip systems, from process technology to computer architecture.



2. Stand-alone design. The λ750 work station puts a 32-bit computer at the IC designer's desk. The Multibus-based system employs three 68000 microprocessors—two in the CPU and a third as a display-list manager for the bit-slice graphics processor.

expand. Now these skills extend downward to familiarity with IC process and device details and upward to knowledge of complete computer systems. Thus they encompass the broad technology base that will feed custom VLSI development in the future.

Three major benefits accrue from implementing all or part of a design directly in silicon, rather than in general-purpose ICs at the same or lower levels of integration. Custom chips reduce the chip count, and with it, board-space, cooling, and power requirements, package size, and product cost. At the same time, reliability improves and proprietary features are less likely to become public. Custom ICs represent about 30% of present semiconductor designs; according to market-research firm Dataquest, that figure could reach 50% by 1990.

To reap those advantages, three design approaches have emerged. Gate arrays mainly replace TTL implementations, although not always with identical circuit performance. Standard-cell designs can replace TTL circuits with an equivalent architecture or can create new systems from previously defined circuit elements. A fully custom approach typically suits completely new designs.

Although turnaround times, development costs, and performance measures more or less sharply differentiate those design approaches, the cost of fabrication and the complexity of design methods are limiting factors in all three cases. The IC designer has had to assemble all his or her tools: the major components are a host computer and graphics hardware to capture and manipulate design data and a wealth of software to verify designs.

As a result, custom IC design has been available primarily to companies with in-house design groups supported by chip-fabrication facilities. However, the growth of independent silicon foundries is enhancing the environment for user-designed parts.

Fully exploiting such services depends on access to appropriate design tools. That need spurred the creation of the λ750 VLSI development system.

Such a system represents the next logical step in a progression of tools that has accompanied the increasing complexity of electronics products (Fig. 1). Oscilloscopes and digital multimeters helped develop products based on discrete devices and small-scale ICs. System designs using medium-scale ICs called for logic analyzers. Large-scale ICs and microprocessor-based designs promoted the evolution of the microprocessor development system and related computerized design aids. New developments in computer hardware and in software tools are spawning a new generation of VLSI chips.

The design environment

Among these developments are advanced microprocessor chips readily available at reasonable cost, with capabilities, including virtual memory, that match the minicomputers of the recent past. In addition, 64-K dynamic RAMs can be had for very low cost and together with recent advances in hard-disk technology expand the memory capacity of small design systems.

Color-graphics technology reaches high performance with high-speed processors and bit-mapped rasterscanned displays. Communication among computer users benefits from the development of local networks and the standardization of system buses. Standard buses also make a variety of off-the-shelf peripheral controllers readily available.

Building on such advances, the λ750 is a complete single-user VLSI design system. This stand-alone work station supports a full complement of design tools, and its Unix operating system provides for a design- and software-development environment, as well as virtual-memory operation and data communications according to the Ethernet protocol.

Everything from design expression and logic analysis up to mask design and verification is handled at the work station. The tools for physical design are flexible enough to support fully custom, as well as standard-cell, approaches, and the software supporting logic design and analysis can be used to design gate arrays and board-level systems.

The λ750 employs a multiprocessor architecture (Fig. 2). The central processing unit is two 12-megahertz 68000 processors, configured as a main processor executing system and application software and as a real-time processor managing the main memory and disk input/output operations.

The hierarchical design methodology makes efficient use of local storage. Recent VLSI designs, such as the reduced-instruction-set computer at the University of California, Berkeley, indicate that 5 to 10 megabytes of local storage suffices to handle designs of up to roughly 50,000 transistors. Exceeding this requirement, the standard λ750 includes a 30-megabyte Winchester hard-disk drive and a 1-megabyte floppy-disk drive.

The display system suits a highly interactive design process. Its controller manages multiple windows, independent color maps for overlays, and real-time panning. A bipolar bit-slice processor manipulates graphics and a 12-MHz 68000 acts as a display list manager and preprocessor.

Display memory is configured as 16-bit planes of 1,024-by-1,024 picture elements each. The planes are split into two sets of 8 bits, each with independent color maps so that logic schematics and physical layouts may be simultaneously displayed.

In conjunction with the advances in semiconductor technology making possible the necessary computing power in a work station, recent software advances add to the foundation for a stand-alone VLSI development system. Software generally has progressed from batch-oriented processing to interactive interfaces and from disjointed tools to integrated systems. The last several years have further seen the widespread acceptance of operating systems, such as Bell Laboratories' Unix, that are tailored to the development environment.

Boosting productivity

Such an operating system boosts productivity with a hierarchical file system and a wide selection of development tools and utilities. Dynamic menus and multiple display windows for interactive control of two or more processes executing in parallel ease the interface with the operator. Furthermore, data-base management finds good use in the engineering environment, automating file-status tracking and updating.

As indicated in the table, the software resources for VLSI development include tools for both logical and physical design and for project management. Additional tools connect the results of logical and physical designs.

Logic design—the expression, or capture, and validation of the designer's intent—benefits from a top-down strategy emphasizing the hierarchical structures of the system. The progress is from the block level to intermediate and lower stages, such as the gate and transistor levels.

At each level, text and graphics editors document the design while schematic and symbol-creation editors form the logic and circuit schematics. When the symbol-creation editor is used for block-, gate-, or transis-

COMPLETE GENERIC TOOL SET FOR VLSI DESIGN

Tools	Purpose
LOGIC DESIGN	
Network description language	formal description of architecture
Schematic editors	logic design and data capture
Symbol library	cell schematics
Schematic plotter	checking
Register-transfer-level simulator	high-level simulation
Logic simulator	gate- and transistor-level verification
Circuit simulator	timing verification
Netlist comparator	crosschecking logic and layout
PHYSICAL DESIGN	
Layout editor	physical design capture
Layout plotter	checking
Placement and routing program	circuit interconnection
Function generators	automatic layout of programmable logic arrays, read-only memories
Design-rule checker	layout verification
Circuit extractor	geometric-to-electrical translation
Electrical-rule checker	verification of extracted circuits
Cell library	standard circuit layouts
Format translators	interface to other programs and mask-making systems
DESIGN MANAGEMENT	
Text and drawing editors	documentation
Test aids	test patterns and analyses
Data-base manager	project control

Profile of a VLSI development system

Building on recent advances in data-processing hardware and software development for very large-scale integrated-circuit design, the λ750 development system integrates an entire custom-IC design facility in a stand-alone work station (see photograph). The 32-bit computer is based on two Motorola 68000 microprocessors operating at 12 megahertz, one as a host and the other as a memory management and input/output coprocessor. High-resolution graphics are handled by a bipolar bit-slice processor and a third 68000 serving as a preprocessor.

The system runs Bell Laboratories' Unix operating system with the Berkeley extensions. User software development is supported in C and Fortran 77, with Pascal as an option. Proprietary software, along with some standard packages like the Spice circuit simulator, provide facilities for all phases of a hierarchical IC design. First shipments are scheduled for April 1983.

Schematic and symbol-creation editors capture logic designs; logic and circuit simulators verify them. A graphical layout editor captures physical designs directly or draws from standard n-channel MOS cells supplied with the system or others obtained from foundry services. A synthesizer of programmable logic arrays and an interactive router complement the layout editor. A design-rule checker, a circuit extractor, and a network-listing comparison program are all standard λ750 offerings.

A local 1-megabyte memory supports these tools, and three additional slots anticipate expansions up to 4 megabytes. The system supports virtual memory operation with secondary storage on a 30-megabyte 5¼-in. Winchester hard-disk drive and a 1-megabyte floppy-disk drive. A second 30-megabyte Winchester is available as an option.

In addition to fully supporting the Ethernet standard for high-speed data communications, the work station includes a 300-bit-per-second autodial modem for remote diagnostics and intersystem communication. Six RS-232-C serial interfaces are provided for peripheral devices, interconnection to other computers, or alphanumeric terminals. Also, two RS-449 high-speed serial interfaces and an IEEE-488 interface are provided for future peripherals or host-computer interface. The λ750 has a 13-slot backplane on Intel Corp.'s Multibus standard (IEEE 796). Standard boards are 12 by 12 inches, double the height of typical Multibus boards. The single-unit price of the machine has been set at $78,000.

The power system's microprocessor controls system start-up, shutdown, battery charging, and battery operation. The controller also monitors system voltages and operating temperature, performing automatic margin tests for field-service engineers. A battery-backup system powers the work station for 1 minute during a power failure, and the controller then completes a readout of main memory onto disk and conducts an orderly shutdown.

The λ750's 19-in. color monitor displays 1,024 by 768 picture elements with a 38-hertz interlaced scan. At any one time, 512 colors can be displayed from a palette of 8.4 million possible shades. As an option, the display controller can be configured to operate with 24 bits per pixel, rather than 16.

tor-level representations, the program links the graphical representation to sets of electrical parameters. The schematic editor fully supports a hierarchical design style, and its network-listing output feeds the logic and circuit simulators and the net-list comparison program that run locally.

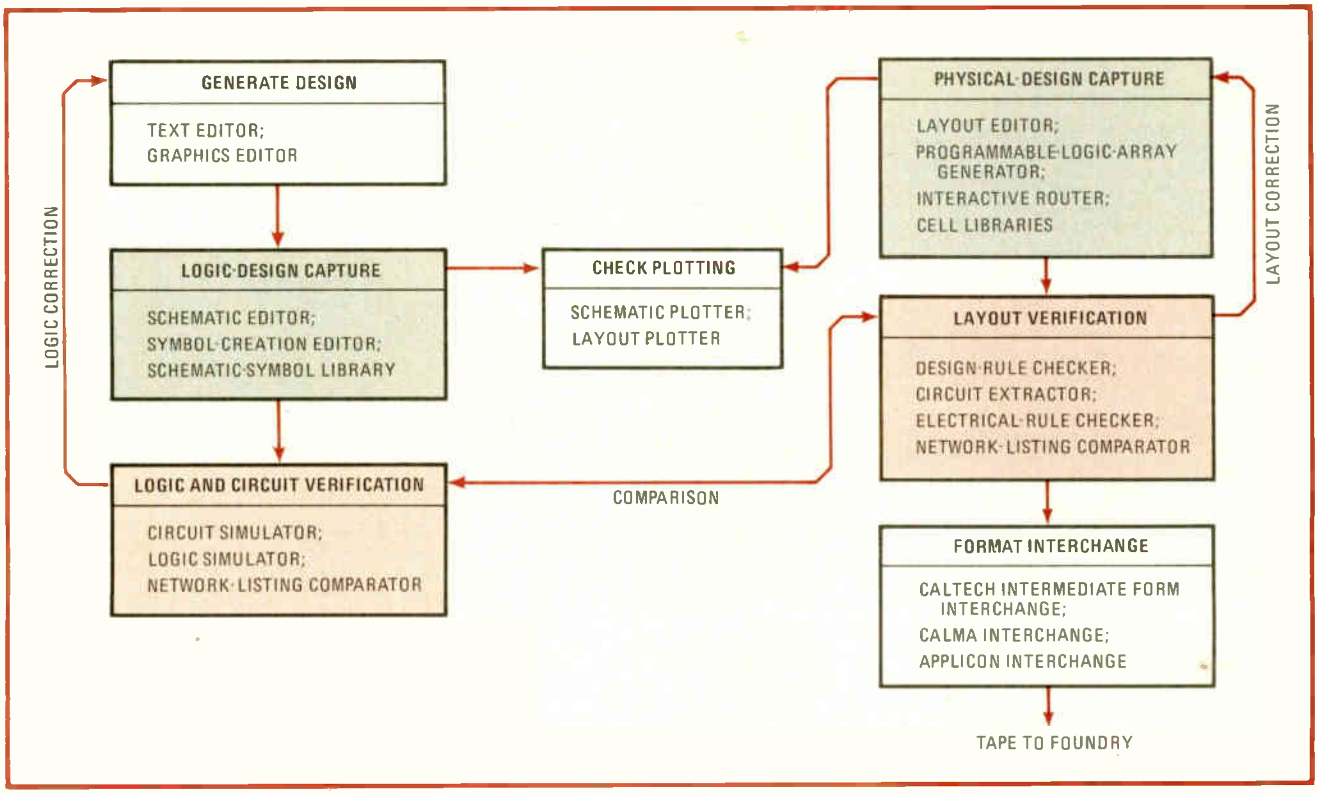
Logic and circuit simulators verify the logic design. The λ750's event-driven logic-level simulator accepts inputs from a schematic net-list output or one extracted from the physical layout. The simulator handles transistor-, gate-, or register-transfer-level simulations.

The circuit simulator that analyzes the analog behavior of the design in terms of nodes and associated voltages is Spice, developed at the University of California at Berkeley and widely used in the industry. Spice is a general-purpose circuit simulator, performing nonlinear dc, transient, and linear ac analyses. Again, a net list derived from either a schematic or a physical design serves as input to the program.

Both the logic and circuit simulators take advantage of the system's graphics capabilities to display their results. The logic simulator overlays its results on the schematic diagram, indicating logic states at selected nodes dynamically as the simulator steps forward under user command. The circuit simulator produces fully annotated analog or digital waveforms.

From a verified logic design, the user progresses to a physical implementation—graphical layouts for mask generation. Tools for physical layout fall into two categories: those for expression, where the designer generates the layout, and those for synthesis, where the computer generates a layout from user specifications. A given chip may well involve both types.

The major tool for the capture of the physical VLSI



3. Design flow. The complete integrated-circuit design process is supported on the work station, from logic-design capture through mask specifications. A hierarchical methodology speeds execution of checking and comparing programs.

design is the graphical-layout editor, analogous to the schematic editor for logic design. The layout editor also incorporates an interactive router for wiring up cells drawn from a hierarchical library consisting of standard n-channel MOS circuits supplied with the λ750, as well as special cells developed by individual designers. A hierarchical library holds instances of particular cells, often nested within other cells.

Going both ways

Library-based hierarchical design typically proceeds downward from a top-level architectural specification. The physical implementation, however, generally starts with the most primitive cells and builds upwards. The layout editor allows editing of nested cells in the complete context in which they are used, or it permits selective suppression of the internal structure of nested cells.

Furthermore, this editor displays multiple independent views of a design data base simultaneously. A typical application using the interactive router is cell interconnection. In such a case, the user can view a large area of the chip, including two distant points that must be interconnected, with the endpoints displayed separately at higher magnification. A later release of the system will include a full placement and routing program to further automate the process handled interactively in the initial version.

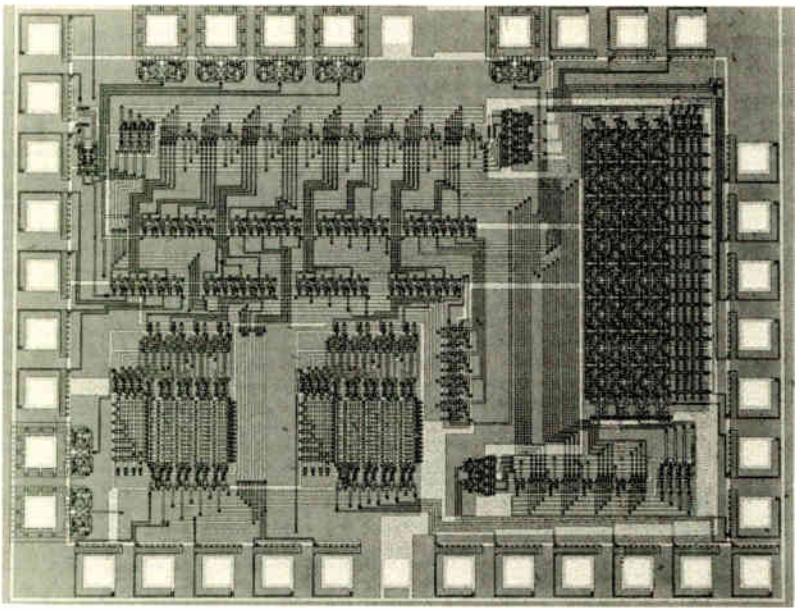
Complementing the physical layout editor, synthesis tools speed up the design by automating all or part of the layout process. A synthesizer for programmable logic arrays creates a physical layout from either a set of Boolean equations or a truth table. The design can be automatically optimized before the layout is fixed, for example, by eliminating redundant entries in the truth table. The PLA generator also synthesizes finite-state machines, in which some of the outputs are fed back into the array as inputs. Closely related to the PLA generator, a read-only-memory synthesizer generates a memory array of specified dimensions, including input and output pads and other interface circuitry.

Following the generation of a physical design, rule checkers verify its correctness against the process specifications. The net-list comparator checks it against the logical design previously verified.

Checking design rules

The design-rule checker works directly on the physical layout produced by the graphical layout editor. It is compatible with any MOS fabrication process, as technology constraints are configured by the user through a proprietary design-rule compiler. For example, any silicon foundry can supply the user with the rules for a given process. These rules from the input to the compiler, which translates them into the format employed by the design-rule checker. The checker uses a fast and accurate algorithm based on locating the corners of the shapes constituting the layout. Any violations of the rules are displayed directly on the graphical layout.

Once the design rules have been satisfied with a geometrically correct layout, a circuit extractor provides the key interface to the other verification tools. It translates the physical layout into an equivalent electrical circuit specified as a net list. Then an electrical-rules



4. Results. This 135-by-110-mil program source-address chip was designed on the λ750 in four weeks from an existing board-level architecture. Memory cells, multiplexers, and registers were built from scratch; a 4-bit adder was synthesized by the programmable-logic-array generator.

checker analyzes the gross electrical parameters of the transistors derived by the extractor. Unrecognizable or incorrectly connected elements are flagged, as are violations of electrical rules, such as those limiting threshold-voltage drops and setting ratios of pull-up–to–pull-down transistor areas.

The extractor's output also feeds the net-list comparator and the logic and circuit simulators. The net-list comparator crosschecks logical and physical circuit representations or compares two versions of logical or physical designs. Thus a physical design modified to meet geometric or electrical rules is resimulated and reverified, ensuring that a fully checked physical layout corresponding to a verified logic design is used to generate the masks for manufacture.

The λ750 will translate physical design data to several popular interface formats: the CIF intermediate form devised by the California Institute of Technology and those for the Calma and Applicon interchanges. Of course, there are also facilities for plotting logic schematics and physical layouts on a variety of printers and plotters.

The unit in action

Figure 3 diagrams a typical VLSI design process showing the λ750 tools that support each activity. An example of the process is afforded by a program source-address chip designed by Richard Blewett of Floating Point Systems and Myron White of Metheus.

The PSA chip directly replaces 14 MSI TTL chips that constitute the program source-address function in the FPS 100 processor, a pipelined array for high-speed floating-point arithmetic. It generates a 4-bit address used to fetch the next executable program instruction from the program source memory. The chips may be connected in parallel to form an address of any desired length.

Seven addresses are calculated on every 250-microsecond clock period; one of the seven is selected for output by the current instruction. The 135-by-110-mil chip (Fig. 4) has 37 I/O pins, including ground and power supply lines, and contains about 2,000 transistors.

The VLSI replacement for the program source-address function is a test vehicle that could cut the board count in the FPS 100, resulting in a smaller system that is cheaper to produce and package and uses less power than the TTL version. The possible alternatives to a fully custom design were a standard IC and a gate-array implementation.

The best way

The function of the PSA chip resembles that of Advanced Micro Devices' 2910 bit-slice microsequencer. However, use of the AMD chip would have required revisions to the FPS 100 microprogramming and modifications to the existing interface circuits, an alternative judged unacceptable.

The design was also not suitable for a gate-array implementation, due to the requirements for a 4-by-16-bit memory array on the chip. At eight gates per bit, a gate-array implementation would have wasted a large area of 512 gates just for the memory. Thus the custom approach was selected for economy of function in a design that preserved the original architecture of the product.

With the architecture specified from the FPS 100 design, the designers used a graphical layout editor, a PLA generator, a circuit extractor, an electrical-rules checker, and a switch-level simulator to produce the finished mask layouts. For this TTL-replacement project, a mix of design styles was applied. Memory cells, multiplexers, and registers were designed from scratch. In the production version of the λ750, these elements will be available from the cell library. The PLA generator was used to lay out the 4-bit adder circuitry. Library cells were used only for the I/O pads.

The two designers required just four weeks to complete the design. Fabrication was handled by a silicon foundry, and at this point the resulting chip is currently undergoing testing. □

Small-area networks fit jobs too small for local nets

Serial-data buses trim local network costs down to small-network, single-system, and even circuit-board size

by Alex Goldberger and Cecil Kaplinsky, *Signetics Corp., Sunnyvale, Calif.,*
and A. P. M. M. Moelands, *NV Philips Elcoma Group, Eindhoven, the Netherlands*

☐ Although LAN, the acronym for local-area network, is almost a household word, what is truly needed in a home is a SAN—a small-area network, with scaled-down performance and cost. SANs are also needed in small businesses, plants, laboratories, schools, and even in large companies. In the latter, they can feed interdepartmental data through data-highway local networks while handling the local-traffic load within smaller business units.

There is also a demand for more flexible methods of interconnecting microcomputers, control devices, displays, and other components within individual consumer electronic systems, automobiles, small instrumentation and control systems, industrial robots, and the like. Furthermore, it may soon be necessary to fit networks onto printed-circuit boards to link chip subsystems, since very large-scale integration and distributed processing are converging trends in system design.

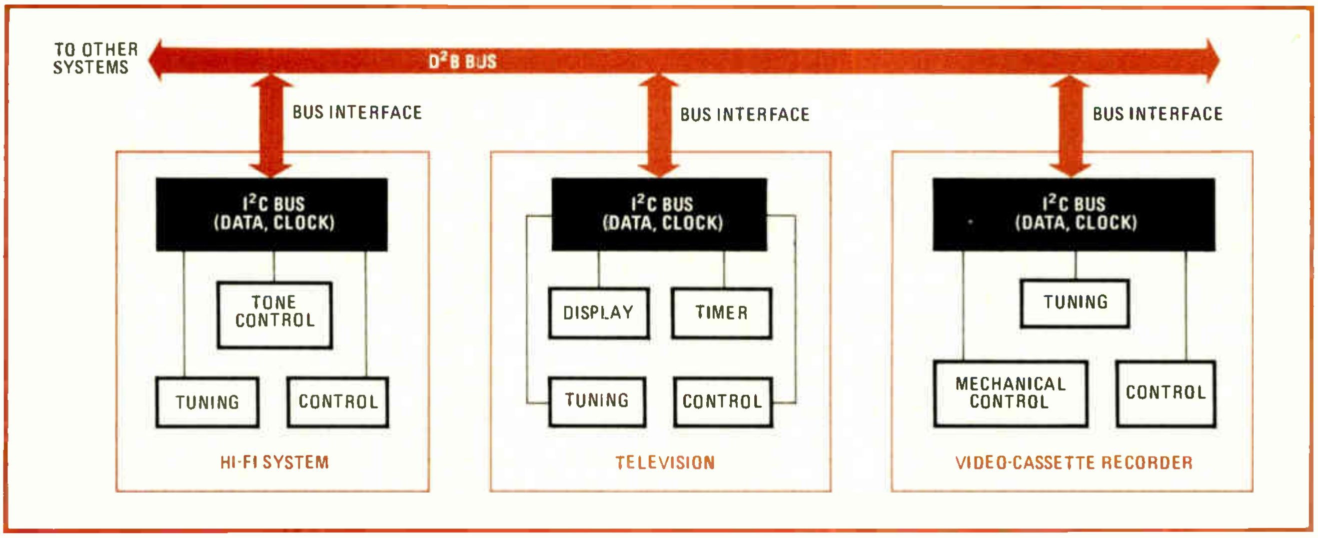
For such applications, two types of serial-data buses have been developed by NV Philips. Instead of competing with conventional local networks, the buses are designed to complement them, much as one-chip microcomputers complement high-performance microprocessors. Both have all the basic functions of modern local networks: a shared, two-way data channel, random access, arbitration, distributed control, and modular construction. Yet they also integrate some of the properties of traditional asynchronous data links to simplify control units and cut costs (see "Something old, something new in local networks," p. 121).

The 10-meter-long I^2C bus interconnects integrated-circuit assemblies in small, modular systems, such as microcomputer-controlled entertainment systems and personal computers. Several consumer-electronics manufacturers have already developed products that are based on this bus.

The 150-m D^2B bus has a more powerful protocol and high noise immunity. It can connect up to 50 packaged systems in domestic and other digital processing and control networks or a like number of subsystems and devices in such self-contained systems as automobiles, industrial apparatus, and instrumentation. Furthermore, the D^2B bus will soon be linking I^2C systems in domestic digital networks (Fig. 1). Its standardization is now being considered by Cenelec, the European consumer electronics manufacturers organization.

Low-cost control

Both buses operate at data rates from around 100 to 10,000 bytes per second, depending on the cost-performance options selected. Though those are only a fraction



1. Digital domestic. While the I^2C bus interconnects integrated-circuit modules in small systems, the D^2B bus operates as a home network. The D^2B bus can also serve as a distributed data-processing and control network in offices, automobiles, and industrial apparatus.

of the rates of the larger local networks, the result is that control units can be fabricated on a corner of a microcomputer chip. The highest-performance I²C control unit takes less than 1,000 transistors and a D²B unit less than 3,000. In contrast, conventional local-net controllers range from complete microcomputers in typical low-cost networks to dedicated VLSI subsystems containing more than 100,000 transistors in Ethernet-class networks. I²C and D²B cabling costs have also been scaled down to the economics of the new applications. The control units are being built into general-purpose microcomputer components, so that the same chip can control a bus and attached equipment.

Philips is already producing the 8400 series of I²C-compatible, one-chip microcomputers. These have Intel's 8021 architecture with larger on-chip memories—up to 128 bytes of random-access memory and up to 4-K bytes of read-only memory. I²C-compatible peripherals in production or design include memories, display drivers, timers, tuners, analog-to-digital and digital-to-analog converters, and complementary-MOS gate arrays.

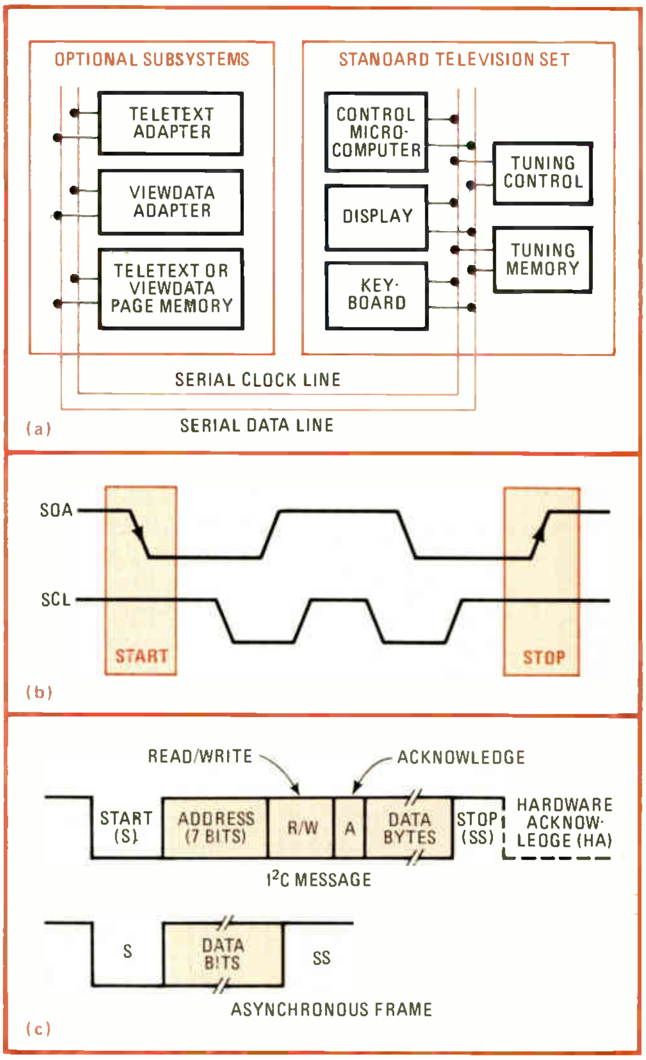
Moreover, Intel Corp., NV Philips, and Signetics Corp. (a subsidiary of U. S. Philips Corp.) have just announced a licensing agreement for alternate sourcing of yet other components. These three will produce a C-MOS version of Intel one-chip microcomputers in the 8048 and 8051 series that include I²C and D²B interfaces. Already program assemblers, emulators, and other system development tools are being readied, and peripheral devices are now being defined for future production.

Two designs, one basic idea

Although their different applications call for differences in protocols and construction, the I²C and D²B buses employ the same basic techniques. For instance, both use essentially the same unique method of arbitrating which control unit has priority when two units attempt to transmit a message simultaneously. The method, which exploits the relatively short propagation delays of small networks, is just one example of how they merge the properties of classical asynchronous-communications and random-access local-networks.

Any control unit (such as a bus interface on a microcomputer chip) can transmit a message when the bus is idle. It claims the bus by issuing a start bit—a bit uniquely identifiable as the beginning of a transmission. But if it first receives a start bit from another unit, it synchronizes its internal clock to the incoming-bit edge. Arbitration then begins with a sequence of bits issued by each control unit, the most significant one first. Both buses are wire-AND designs, so that units can AND their outgoing bits with incoming bits, one by one. Priorities can be established immediately, without overhead, because the bits are part of the initial message field—typically, an address.

For example, unit A might transmit 1101 after the start bit and B might send 1110. Each issues a 1 and sees an AND output of 1 in the first bit period and also in the second (1 AND 1 = 1). But in the third period, A issues and sees a 0 bit while B issues a 1 and sees a 0 (0 AND 0 = 0, and 1 AND 0 = 0). Unit B is the odd man out—it has lost the arbitration and must retire its bid for trans-



2. Inside job. Designed for modular, single-cabinet systems (a), the I²C employs separate data and clock lines for synchronization and to define start and stop bits (b). Its message format resembles an asynchronous data-link frame (c).

mission immediately. Otherwise, the next bit would reverse the situation: A would issue a 1 and see a 0 while B would send and see a 0 bit.

This technique works because the propagation delays are not excessive—a unit can detect another's start bit prior to message transmission. In contrast, in large multiple-access local networks, two widely separated units may not sense each other's transmissions in time to prevent collisions and error-recovery overhead.

Another resemblance to classical asynchronous systems is that both buses have master and slave units. Control is still distributed, though—control-unit logic distinguishes between master and slave and between transmitter and receiver. A master is a unit that initiates a conversation with another unit, which becomes a slave. If the master asks a slave to transmit data, it then switches from transmit to receive modes and the slave becomes a transmitter. With this technique, displays and other devices that normally operate as slaves can be slave-only units to reduce control-unit costs.

Receivers acknowledge information, whether it be address or data, without the usual message transmissions. Because the bus is driven by open-collector devices, a master can complete transmission of data, send some more timing signals, and hold the data line high. The receiver acknowledges whatever comes by pulling the data line low within a prescribed period, and the transmitter can then assume the information was received correctly. Otherwise, the transmitter interprets the high state as a negative acknowledge (NACK) and can resend or take other appropriate action. Since ACK/NACKs also indicate whether units exist at addressed locations, a master can determine system configuration by sending a series of test messages.

Inter-IC networks

Like a local network, the I^2C bus allows designers to organize and reorganize modules with only cursory attention to interconnection design, but within a single cabinet. For example, many television sets are controlled by low-cost microcomputers today. The next step is a microcomputer master with tuning, tuning memory, keyboard, and display modules acting as slaves (Fig. 2a). Modular options like teletext and viewdata, the TV-based information services, could also be masters, accessing page memory directly instead of depending on a central controller for access. This setup not only simplifies the system but also lets functions be located wherever needed to satisfy environmental, constraints. For example, the tuning control belongs in the coolest location to minimize drift, the keyboard in the place most convenient to humans, and the options where field installation is easiest. Moreover, the communications network also means that each module can be upgraded independently to take advantage of lower-cost components and new technology.

The I^2C bus can indeed interconnect ICs on a board, since printed wiring will work as well as other wires at short distances. Length and number of units are not predetermined: they can be traded off within a connection-capacitance limit of 400 picofarads per wire, which ensures correct timing. There are only two single-wire lines driven by ordinary open-collector devices: a serial data line (SDA) and a serial clock line (SCL).

Unlike in other bus designs, there is no single clock source. All units can drive the open-collector clock line and mutually synchronize their clocks. In general, the data line changes state only when the clock line is low; a receiver samples data on the clock pulse's rising edge. However, a start bit goes from high to low on the SDA line while the SCL is high, and a stop bit goes from low to high while the SCL is high. Since the clock pulse is normally low, these unique bits signal all units that a message is coming or ending (Fig. 2b).

A message resembles an asynchronous frame but contains six fields (Fig. 2c). These are: the start bit; the 7-bit slave address; a read-write bit to indicate whether the slave is to transmit or receive; the acknowledge bit; the message in 8-bit characters; and a stop bit. The hardware ACK/NACK signal completes the transfer operation. If arbitration is required, the address field is

Something old, something new in local networks

Data-communications links are either point-to-point or multipoint systems. Like conventional multidrop and loop networks, most new local networks fall into the multipoint category. Small-area networks could be based on either of these approaches, but in fact offset the drawbacks of each with advantages taken from the other.

Traditional asynchronous data links operate with simple, inexpensive logic, so they are a good choice for the really small network. Because data is sent a frame at a time, they are also better for sporadic transmissions than synchronous links. But data-link–control protocols stem from electromechanical switching concepts. They rely on centralized control of network activity. The master polls other units and determines which units should transmit and receive data. In loop and multidrop networks, primary stations must also store and forward data being transmitted among secondary stations.

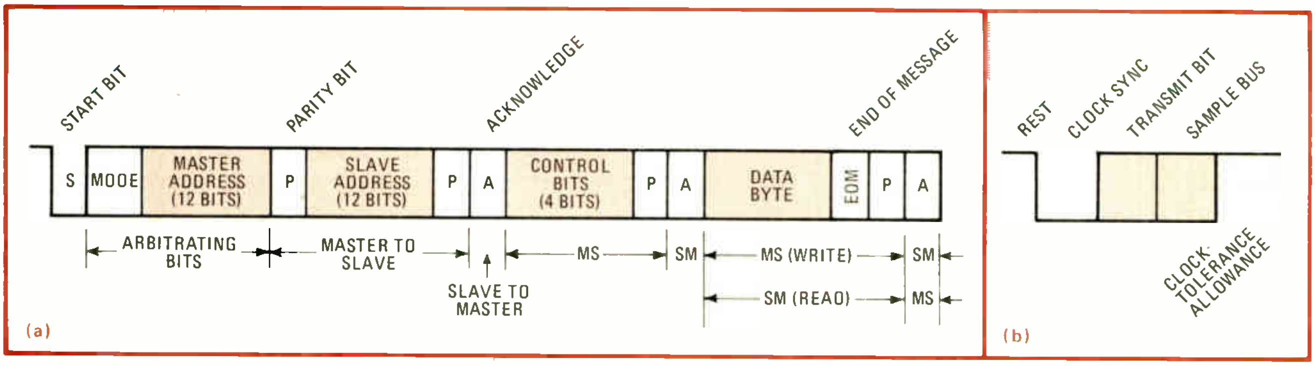
Such systems require complex software, are difficult to reconfigure, fail when the master unit fails, and use up much of their bandwidth in polling overhead. Very often, the control system polls no change in status, so no real data is transmitted between data-gathering and decision-making stations. All of these characteristics are becoming taboo in local networking.

In new local networks, any node-control unit can take charge of the serial-data channel and transmit data to any other unit. Token-passing systems retain an element of master control: a unit waits for a circulating bus grant—the logical token. Random-access systems like Ethernet allow any unit to transmit whenever the bus is idle. Otherwise, they must back off and try again later, an arbitration technique built into the CSMA/CD (carrier-sense, multiple-access with collision detection) protocol.

Thus, instead of being an autocracy, local networks reap the benefits of a democracy. With controllers at each node, they can expand modularly, adapt to changing traffic patterns, and usually continue operating when a control unit fails, among other advantages. Then, too, most are many times faster than conventional links. Typical local networks contain scores to hundreds of work stations and computers and transmit data at rates somewhere between 1 and 10 megabits per second over distances ranging from 400 meters to over a kilometer.

Nonetheless, such networks are obviously overspecified for small-network applications. Performance has a high price, in the form of complex protocols, controllers, and system software; more expensive construction; and for large systems, professional network managers. All that is needed in small-area nets is enough performance to handle the throughput requirements of a modest number of inexpensive microcomputers and peripherals, television tuners, man-machine interfaces, sensors, and the like.

Instead of returning to square one, Philips I^2C and D^2B buses are an amalgam of the old and new data links. They do have masters and slaves that transmit asynchronously. But with the new protocols, any or all control units can be masters. The result is a democratic, modular network. More to the point, the control units require only 1% or 2% as much circuitry as a typical local-network controller, and the wiring is inexpensive.



3. Big bus, big format. Since it will operate in bigger systems with more masters and slaves than the I^2C bus, the D^2B bus uses a higher-level protocol, reflected in the message format (a). The bit format (b) enables units to overcome worst-case timing differences.

employed for wire-AND arbitration.

The system algorithm can be executed with software to reduce hardware costs. A start byte (0000 0001) then follows the start bit to give slaves more time to poll the data line. Typical data rates are 7,500 characters per second at 2.5 bytes per message and 10,900 c/s at 64 bytes per message with hardware and 110 and 153 c/s, respectively, with software execution. These are usable rates that include all overhead, assuming correct reception (no NACKs).

D^2B: more stations, more modes

Since it may connect as many as 50 systems or system components, the D^2B bus has three operating modes, extra methods of identifying and controlling functions attached to the bus, and built-in compensation for timing variations. It also provides high noise immunity and low-noise radiation with unshielded wiring—a single, differentially driven, twisted-pair line. Radiation meets Federal Communications Commission Class B interference requirements.

Mode 0, the slowest operating mode, can be implemented by programming a microcomputer and adding a differential line driver and receiver. Mode 1 requires dedicated hardware but allows clocking with a resistor-capacitor circuit with an accuracy of 25%. Mode 2 takes dedicated hardware and a clock accurate to within 0.1%. All messages are limited to about 9 milliseconds to prevent units from monopolizing the bus. During this time, 1 byte can be transferred in mode 0, 22 bytes in mode 1, and 75 bytes in mode 2. The corresponding data rates are 110, 2,423, and 8,282 bytes/s, respectively, even when control switches between masters.

These modes can be mixed on the same bus so that designers can choose the best cost-performance ratios for individual units and attached equipment. For example, a printer may operate in mode 1 and a disk drive in mode 2, while a processor may switch from one mode to the other to communicate with the peripherals. Slaves generally operate in a single mode since their throughput requirements are generally fixed by their function. On the other hand, a multimode slave can be shared by a variety of low-cost single-mode masters.

Masters arbitrate at two levels. They first transmit a mode-bit pattern that gives priority to the slower unit (since it may require more frequent access). If mode numbers are equal, priority is then determined by the master's address (Fig. 3a). After unit addresses are transferred, 4 control bits specify a data, address or status transfer, read or write operation, and whether or not the slave is to be locked to a particular master. The message format includes the end-of-message bit required for ending or continuing an asynchronous transmission, as well as start, field parity, and acknowledge bits.

Two extra addressing capabilities anticipate the need to keep track of system configurations and to simplify network management and maintenance. The 12-bit unit addresses (4,096 individual addresses) allow unique identification of attached systems and components, such as equipment model numbers, types of tuners, and types of analog-to-digital converters. An address within the data field lets units access memory in other units to determine what functions are performed at those locations and how to control them. These electronic instruction manuals can be employed by diagnostic computers in high-volume applications, for example, or else may be displayed to help system users.

Clock and data signals are time-multiplexed onto the one bus line. Again, since the bus is not a conventional data link, there may be multiple signal sources. During arbitration, for example, one master may drive the clock signals, a second transmit data, and a third sample the data. After arbitration, the remaining master drives the clock, and the addressed slave aligns with the master. Yet the timing of master-to-slave and slave-to-master transmission would probably be different because of component variations. Given the size of the D^2B network, such deviations could lead to endless timing calculations.

To avoid all that, each bit-transmission period is divided into five phases: rest, clock-synchronization, data transmission, data sampling by the receiver, and a clock-tolerance allowance (Fig. 3b). Phase durations vary from mode to mode and from message field to field. These functional variations in bit (and bus) definition take into account worst-case differences in driver and bus delays, rise and fall times, unit timings, and clock signals.

Although primarily an interconnection for packaged systems, the D^2B bus can replace the I^2C bus as a network within a cabinet when better noise immunity or longer wiring is required. Noise immunity is as critical in home applications as in business, automotive, and industrial applications, since TV sets and other sensitive systems cannot tolerate wiring that acts as a receiving and transmitting antenna. □

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Model #625

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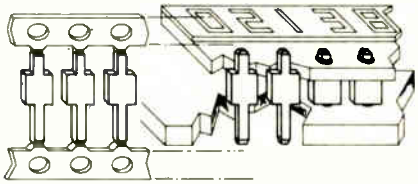

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Which do you choose Serial type *or* Parallel type?

F1632

M3221

Daini Seikosha, in continuing its efforts to develop fully the potentials of LCD's, since its success in mass-producing LCD's for watches, has achieved producing a range dot matrix modules. As there are two types of interface format (serial type and parallel type), you can choose according to your requirement.

[Features]

- Since a character generator and data RAM are built-in, a simple system configuration is sufficient.
- High contrast and wide viewing angle are guaranteed.
- Brightness adjustment of the liquid crystal is possible.
- Since a CMOS IC is used at the drive circuit, power consumption is low and logic voltage range is wide.
- Alphanumeric and symbols are possible.
- Full dot display is also possible with F1632.

[Basic Specifications]

Item / Model	F1632	M3221	M3212
Dimensions (W × L × Hmm)	210 × 80 × 13	190 × 33 × 10	190 × 33 × 10
Number of display characters	Full dot	32 character × 1	32 character × 2
Character composition number of dots	160 × 32	5 × 7 with cursor	5 × 7 with cursor
Drive waveform	1/5 bias 1/16 duty	1/4 bias 1/8 duty	1/5 bias 1/16 duty
Power consumption	33mW	15mW	15mW
Recommended power voltage (Vdd − Vss)	6.5V	5.0V	5.0V
Operating temperature range	0 ~ +50°C	0 ~ +50°C	0 ~ +50°C
Storage temperature range	−30 ~ +70°C	−30 ~ +70°C	−30 ~ +70°C
Interface	Serial	Serial	Paralle

*Other types of dot matrix modules are available in addition to those shown above.

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Circle 123 on reader service card

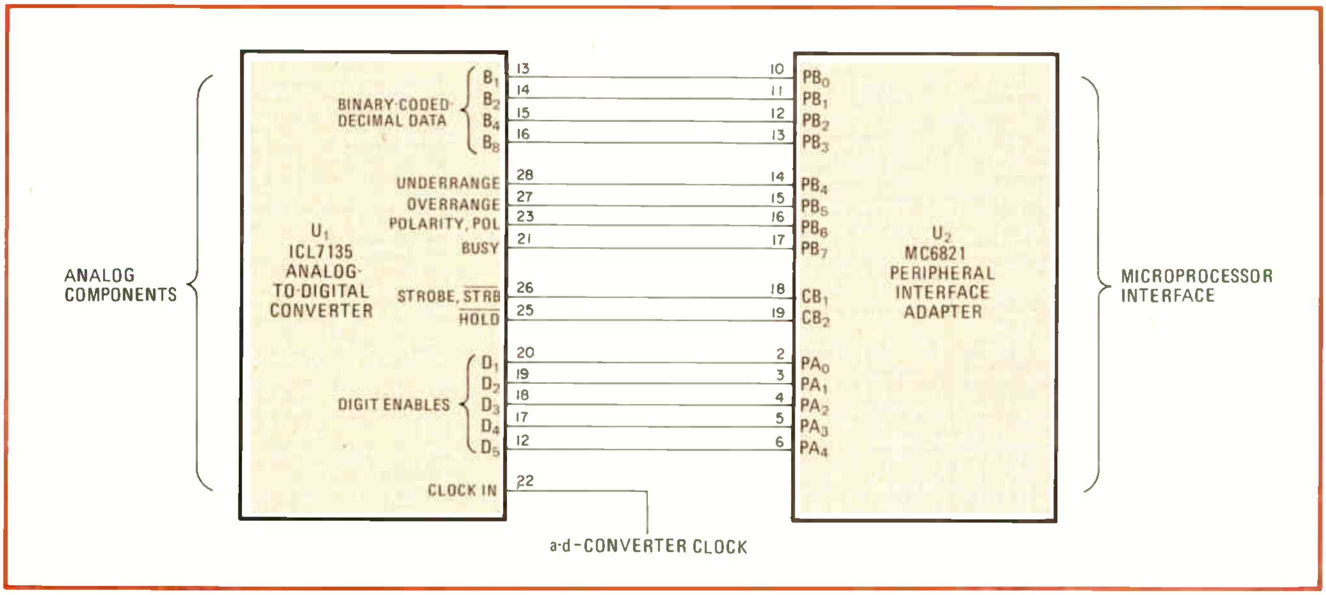
Interface program links a-d chip with microprocessor

by M. F. Smith
Reading University, Reading, England

When combined with a peripheral interface adapter, this microprocessor program eases interfacing an ICL7135 analog-to-digital converter with the MC6800 family of microprocessors. Through placing the 16-bit MC6821 interface chip between the a-d converter and processor interface, all digital data and control signals may be funneled through the parallel interface.

The abbreviated program does not check for polarity or input range. In this routine, the digit strobe of U_1 is used to interrupt the microprocessor through the CB_1 input to U_2. Binary-coded–decimal data from the a-d converter is stored in a temporary buffer, labeled BUFFER TEMP, and the digit status in the buffer is determined by digit output D_1 through D_5 of U_1 (see figure). When the last digit D_1 is sent out, the temporary buffer is moved to a final buffer labeled BUFFER-ADC. Subroutine ADC-INIT initializes MC6821 and allows interrupts before data can be sent from the a-d converter.

This software allows the ICL7135 chip to operate at full speed and without any possibility of misreading the multiplexed digits. The software may be synchronized with the converter, and the final buffer may be provided by a software flag, instead of a hardware strobe. □



Microprocessor interface. Intersil's analog-to-digital converter ICL7135 is linked to Motorola's 6800 microprocessor family with peripheral interface adapter MC6821 and the associated software. This method funnels digital data and control signals through the interface and eliminates the need for additional circuitry. The digit strobe of U_1 interrupts the processor through CB_1.

INTERFACE PROGRAM LINKING 6800 MICROPROCESSOR WITH ICL7135 ANALOG-TO-DIGITAL CONVERTER

Location	Object code	Line	Source statement	Comments
		1	"6800"	
		2		
		3		;ICL7135 4-1/2 DIGIT a-d CONVERTER
		4		
		5		
	(8100)	6	PIA_DIGIT EQU 8100H	;SIDE FOR DIGIT NUMBER
	(8102)	7	PIA_BCD EQU 8102H	;SIDE FOR BINARY-CODED-DECIMAL DATA ERRORS
	(8103)	8	ADC_STROBE EQU 8103H	;STROBE FOR a-d CONVERTER
		9		
		10		

		ORG 0	
			; BUFFERS MUST REMAIN IN ORDER
0000		BUFFER_TEMP RMB 5	; ACTIVE INTERRUPT REQUEST BUFFER
0005		BUFFER_ADC RMB 5	; STATIC BCD BUFFER
		ORG 1000H	
1000		ADC_SERVICE:	
1000	B68103	LDAA ADC_STROBE	; CHECK IF INTERRUPT REQUEST FROM a-d CONVERTER
1003	2A25	BPL IRQ_RETURN	; FALSE ALARM IF NONE
1005	CE0004	LDX #BUFFER_TEMP + 4	; POINT TO BUFFER
1008	B68100	LDAA PIA_DIGIT	; GET DIGITAL BIT PATTERN
			; DETERMINE THE BUFFER POSITION
			; OF THE INTERRUPTING CHARACTER
100B	44	DIGIT_LOOP LSRA	; SHIFT RIGHT INTO CARRY
100C	2503	BCS ADC_DATA	; AND GO ON IF DIGIT IS FOUND
100E	09	DEX	; DECREMENT BUFFER POINTER
100F	20FA	BRA DIGIT_LOOP	; AND CARRY ON
1011		ADC_DATA:	
1011	B68102	LDAA PIA_BCD	; PICK UP BCD DATA
1014	840F	ANDA #00001111B	; MASK OFF POLARITY
1016	A700	STAA 0, X	; SAVE DATA IN TEMPORARY BUFFER
1018	8C0000	CPX #BUFFER_TEMP	; AND TRANSFER INTO a-d-CONVERTER BUFFER
101B	260D	BNE IRQ_RETURN	; WHEN LAST BCD DIGIT IS SENT
101D	C605	LDAB #5	; MOVE TEMPORARY DATA INTO
101F	CE0000	LDX #BUFFER_TEMP	; STATIC BCD BUFFER
1022	A600	MOVE_LOOP LDAA 0, X	
1024	A705	STAA 5, X	
1026	08	INX	
1027	5A	DECB	
1028	26F8	BNE MOVE_LOOP	
102A	0E	IRQ_RETURN CLI	; RETURN FROM INTERRUPT REQUEST
102B	3B	RTI	

INITIALIZATION SUBROUTINE FOR MC6821

Location	Object code	Source statement	Comments
			; INITIALIZE PERIPHERAL INTERFACE ADAPTER FOR
			; a-d CONVERTER ENABLE INTERRUPTS
102C		ADC_INIT:	
102C	8604	LDAA #00000100B	; NO INTERRUPT REQUEST
102E	CE8100	LDX #PIA_DIGIT	; SET DIGITAL SIDE FOR INPUT
1031	8D09	BSR INPUT_SET	; THROUGH SUBROUTINE
1033	863D	LDAA #00111101B	; CA_1 = INTERRUPT-REQUEST-OUTPUT CB_2 = 1
1035	CE8102	LDX #PIA_BCD	; SET DATA SIDE FOR INPUT
1038	8D02	BSR INPUT_SET	; THROUGH SUBROUTINE
103A	0E	CLI	; ALLOW INTERRUPTS
103B	39	RTS	
103C	6F00	INPUT_SET CLR 0,X	
103E	6F01	CLR 1, X	
1040	A701	STAA 1, X	; SET CONTROL WORD
1042	39	RTS	
ERRORS = 0			

Nystrom integration gives dynamic system's response

by David Eagle
Lear-Siegler Inc., Grand Rapids, Mich.

The response of many dynamic systems, described by second-order vector differential equations that are written in the form $\ddot{\bar{X}} = \bar{f}(\bar{X}, \dot{\bar{X}}, t)$, are determined by numerical methods—a popular approach is the fourth-order Runge-Kutta technique. However, this program uses the fourth-order Nystrom-integration method to solve systems of second-order differential equations and can be a faster solution for some dynamic systems.

An integration subroutine beginning at line 1,000 and a driver routine that shows how the program works are the software's main components. In addition, the derivatives are evaluated in the subroutine on line 3,000. The program example demonstrates the usefulness of Nystrom integration and integrates the single second-order differential equation defined by: $\ddot{X}(X,t) = 0.5X^2(1+(1+t)^2 X)$ where $X(0) = 1$ and $X(0) = 0.5$ are the initial conditions.

The above differential equation has the exact solution $X(X,t) = 4/(4-2t-t^2)$ and $\dot{X}(X,t) = 0.5(1+t)X^2$. The example prints the time and values for X and $\dot{X}$, and exact solutions for X and $\dot{X}$ are also included for comparison with the Nystrom-integration method. □

Software notebook is a regular feature in Electronics. We invite readers to submit short original and unpublished programs and software solutions to engineering problems. We'll pay $75 for each item published.

BASIC SUBROUTINE FOR INTEGRATING SECOND-ORDER VECTOR DIFFERENTIAL EQUATIONS

```
1000  * FOURTH-ORDER NYSTROM-INTEGRATION SUBROUTINE
1010  LET T2 = T1
1020  FOR I = 1 TO N1
1030  LET X2(I) = X1(I)
1040  LET V2(I) = V1(I)
1050  NEXT I
1060  GOSUB 3010
1070  *
1080  LET T2 = T1 + A2 * S1
1090  FOR I = 1 TO N1
1100  LET D1(I) = S1*E1(I)
1110  LET X2(I) = X1(I) + S1 * (A2 * V1(I) + A1 * D1(I))
1120  LET V2(I) = V1(I) + A2 * D1(I)
1130  NEXT I
1140  GOSUB 3010
1150  *
1160  LET T2 = T1 + B2 * S1
1170  FOR I = 1 TO N1
1180  LET D2(I) = S1 * E1(I)
1190  LET X2(I) = X1(I) + S1 * (B2 * V1(I) + A6 * D1(I) + A7 * D2(I))
1200  LET V2(I) = V1(I) - A8 * D1(I) + A9 * D2(I)
1210  NEXT I
1220  GOSUB 3010
1230  *
1240  LET T2 = T1 + S1
1250  FOR I = 1 TO N1
1260  LET D3(I) = S1 * E1(I)
1270  LET X2(I) = X1(I) + S1 * (V1(I) + B3 * D1(I) + B4 * D2(I) + B5 * D3(I))
1280  LET V2(I) = V1(I) + B6 * D1(I) - B7 * D2(I) + B8 * D3(I)
1290  NEXT I
1300  GOSUB 3010
1310  *
1320  LET T1 = T1 + S1
1330  FOR I = 1 TO N1
1340  LET D4(I) = S1 * E1(I)
1350  LET X1(I) = X1(I) + S1 * (V1(I) + A3 * D1(I) + A4 * D2(I) + A5 * D3(I))
1360  LET V1(I) = V1(I) + A3 * (D1(I) + D4(I)) + B1 * (D2(I) + D3(I))
1370  NEXT I
1380  RETURN
1390  *
2000  * INTEGRATOR-COEFFICIENTS SUBROUTINE
2010  LET A1 = .045: A2 = .3: A3 = 13/126: A4 = 5/18: A5 = 5/42: A6 = 7/600
2020  LET A7 = 7/30: A8 = 7/15: A9 = 7/6: B1 = 25/63: B2 = .7: B3 = 19/78
2030  LET B4 = 35/312: B5 = 15/104: B6 = 64/39: B7 = 70/39: B8 = 15/13
2040  RETURN
2050  *
3000  * DIFFERENTIAL-EQUATION SUBROUTINE
3010  LET A = (1 + T2) * (1 + T2)
3020  LET B = X2(1) * X2(1)
3030  LET E1(1) = .5 * B * (1 + A* X2(1))
3040  RETURN
```

PROGRAM COMPARING NYSTROM-INTEGRATION METHOD WITH EXACT SOLUTION

```
0010    * PROGRAM "NYM4"
0020    *
0030    * A DEMONSTRATION OF THE FOURTH-ORDER NYSTROM METHOD
0040    * FOR INTEGRATING SYSTEMS OF SECOND-ORDER
0050    * VECTOR DIFFERENTIAL EQUATIONS
0060    *
0070    * SET PRINTER LINE LENGTH
0080    LINE = 110
0090    * DEFINE SIZE OF SYSTEM AND DIMENSION ARRAYS
0100    LET N1 = 1
0110    DIM X1(N1), X2(N1), V1(N1), V2(N1), E1(N1), D1(N1)
0120    *
0130    * COMPUTE INTEGRATOR COEFFICIENTS
0140    GOSUB 2010
0150    *
0160    * INTEGRATION STEP SIZE
0170    LET S1 = 0.05
0180    * INITIAL TIME
0190    LET T1 = 0.0
0200    * INITIAL X
0210    LET X1(1) = 1.0
0220    * INITIAL X DOT
0230    LET V1(1) = 0.5
0240    * FINAL TIME
0250    LET T2 = 0.5
0260    *
0270    * CLEAR SCREEN AND PRINT HEADER
0280    HOME :PRINT TAB(5); "PROGRAM NYM4" :PRINT
0290    PRINT TAB(5); "TIME", "COMPUTED", "COMPUTED", "EXACT", "EXACT"
0300    PRINT TAB(3); "(SECONDS)"; TAB(20); "X"; TAB(35); "X DOT";
0310    PRINT TA8(51); "X"; TAB(65); "X DOT"
0320    *
0330    * INTEGRATE SYSTEM OF EQUATIONS
0340    FOR I1 = 1 TO T2/S1
0350    GOSUB 1010
0360    *
0370    * COMPUTE EXACT SOLUTION
0380    LET X3 = 4/(4-2*T1-T1*T1)
0390    LET V3 = .5*(1+T1)*X1(1)*X1(1)
0400    *
0410    * PRINT RESULTS
0420    PRINT :PRINT TAB(5); T1, X1(1), V1(1), X3, V3
0430    *
0440    NEXT I1
0450    END
0460    *
```

Time (s)	Computed X	Computed $\dot{X}$	Exact X	Exact $\dot{X}$
0.05	1.0262989	0.552976961	1.0262989	0.552976949
0.1	1.05540895	0.612638448	1.05540897	0.612638426
0.15	1.08769542	0.680271785	1.08769544	0.68027176
0.2	1.12359547	0.757480102	1.1235955	0.757480066
0.25	1.16363632	0.846280972	1.16363636	0.846280925
0.3	1.20845916	0.94924286	1.20845921	0.949242799
0.35	1.25885122	1.06967691	1.25885129	1.06967681
0.4	1.31578937	1.2119113	1.31578947	1.21191116

Engineer's newsletter

Transformless rectifier gives bipolar voltage

There has been no way around it: when you need bipolar full-wave rectification you also need a transformer. No longer, though, as Louis N. Ezialowski from Leasametric Inc. in St. Laurent, Quebec, Canada, has taken the transformer out and **uses just four resistors, two diodes, and an operational amplifier to get bipolar voltages.** In the circuit, resistors R_1 through R_4 are connected in a bridge configuration. The input voltage is fed to the node connecting R_1 and R_3, and the positive and negative dc outputs are tapped from the junctions of R_1 and R_2 and R_3 and R_4, respectively. The anode of one diode is attached to the positive output and the cathode of the other latches to the negative output. The free cathode and anode ends of these diodes meet each other at the feedback port of the operational amplifier, whose inverting input is attached to the junction of R_2 and R_4. The noninverting input of the op amp is grounded.

Testing service offered to meet MIL-STD-883B

Intel Corp says its microcomputers, random-access memories, erasable programmable read-only memories, and peripheral component families can now meet MIL-STD-883B method 1015 with the Santa Clara, Calif., firm's Express service. The service is designed for parts that must function beyond commercial temperature ranges. **Customers can specify one of the two test flows: one with burn-in for approximately 168 hours at 125°C, the other without burn-in over two operating temperature ranges,** commercial (0° to 70°C) and extended (−40° to +85°C). The Santa Clara, Calif., firm says that the procedures apply to MOS, bipolar, and large- and very large-scale integrated circuits, and that new products will enter the program as they become commercially available.

Automated pc assembly topic of study

Automated, electronic, and robotic assembly of print-circuit boards will grow tremendously throughout the 1980s. For this reason, an international study entitled "Flexible Automated Assembly Systems for Components of PC Boards" is being researched by CEERIS International Inc. **The study gives both users and manufacturers necessary systems data**—for example, a 1990 market forecast for automated systems and an economic analysis including return on investment. Further information, including a preliminary analysis, a table of contents, a skeleton system configuration, and technology requirements may be obtained from Salvatore A. G. D'Agostino, vice president, CEERIS International Inc., P. O. Box 939, Old Lyme, Conn. 06371.

Sapphire thermometer takes the heat

High-temperature measurements may soon be extended to 2,000°C—500°C above the current high—with an optical-fiber thermometer that is made from a single-crystal sapphire. Developed by Ray Dils of the U. S. Commerce Department's National Bureau of Standards in Washington, D. C., the thermometer is being tested in a black-body furnace and high-temperature flow facility so that its actual stability, precision, and accuracy may be determined. **The device has the potential to be 10 times more accurate than those holding to the current thermocouple standard** and may be useful for measuring and controlling high-temperatures in gas turbines, internal combustion engines, and other such devices. The NBS is seeking a patent for the thermometer.

-Steve Zollo

Now there's a better 1GHz cavity-tuned signal generator.

Marconi 2017 AM/FM Signal Generator

Marconi 2017 AM/FM Signal Generator combines the purity and low noise performance of a cavity-tuned oscillator with keyboard convenience and GPIB.

Marconi's AM/FM Signal Generator 2017 looks special – and it is. It is a stable, low noise generator offering high outputs, up to 4V e.m.f., over the frequency range 10Hz to 1024MHz. It has two manual control systems, digital via the keyboard or analog via rotary controls. It can be programmed via the GPIB to extend the 2017's range of applications to include automatic testing, either as part of a bench-top system or in a full ATE assembly.

Being microprocessor controlled, the 2017 is simple to operate and has a memory facility allowing up to 10 complete settings to be stored for later use. Digital displays and annunciators clearly indicate the instrument's settings at all times.

The microprocessor also performs conversion of RF calibration units and provides an incrementing facility, allowing the carrier frequency to be stepped up or down in steps of any size. A key can be pressed to indicate total shift.

At the heart of the 2017 is a low noise, cavity-tuned oscillator that produces a sideband noise figure of better than −135dBc/Hz at 20kHz offset at 470MHz, with complete freedom from spurious non-harmonic signals. A series of digital dividers and filters ensures that the noise level is even lower at frequencies below 256MHz. Additionally, a slow sweep mode, operating between any two frequencies on a carrier frequency range, facilitates measurements of spurious receiver responses, full spectral purity being retained throughout.

To appreciate all the benefits of this unique signal generator on the bench or in your ATE System call us for a demonstration.

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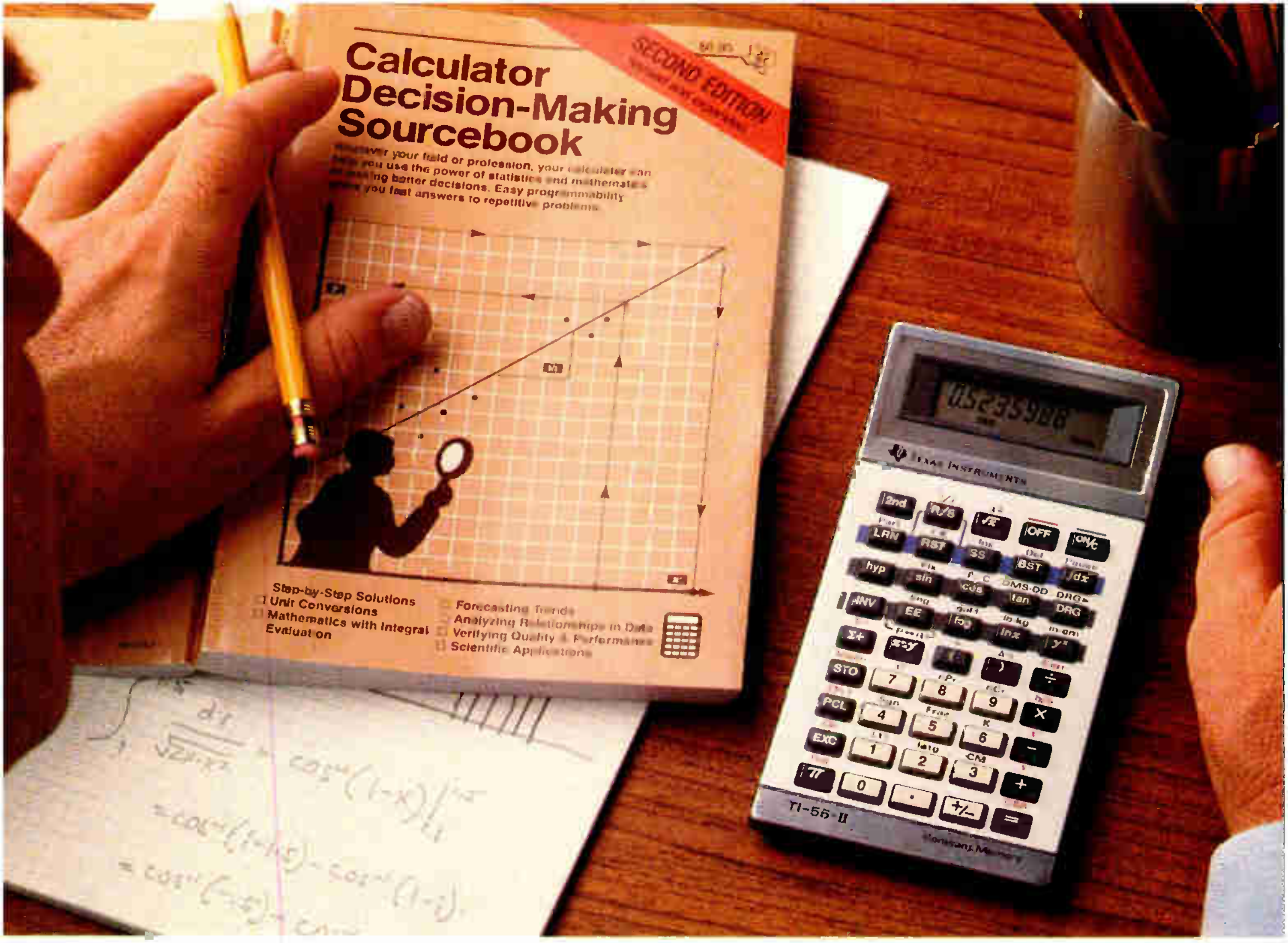
Circle 129 on reader service card



How the TI-55-II makes short work of long problems.

Whenever you can solve complex problems quickly and accurately, you're ahead of the game. And that's exactly what the TI-55-II does for you. By giving you 112 pre-programmed functions (like definite integrals), it allows you to take short cuts without losing accuracy. You'll accomplish a lot more in less time which means increased efficiency.

With our TI-55-II you can tackle problems you thought could only be solved with higher-priced programmables. You're not only getting the standard slide rule functions but also statistical capabilities. This way you can work out linear regressions, permutations and combinations, just to name a few.

The TI-55-II also gives you enough programmability to eliminate a lot of repetitive key punching. Our Constant Memory™ keeps programs and data on tap, even when the calculator is turned off. So once you've entered a formula, you can simply put in the variables to get your solution. The Liquid Crystal Display shows your answers in standard, scientific or engineering notations – clearly and precisely.

We also help you get the most out of your calculator with the Calculator Decision-Making Sourcebook. It gives you step-by-step examples of the best techniques used for solving mathematical, scientific and statistical problems. And we've included a special section on how to program your TI-55-II.

So next time you're facing another time-consuming problem, cut it down to size with the TI-55-II.

TEXAS INSTRUMENTS

Circle 130 on reader service card

Half-height floppy-disk race heats up

Japanese companies enter the fray with disk drives even less than half height; capacities are up to 1 megabyte

by Steve Zollo, Assistant New Products Editor

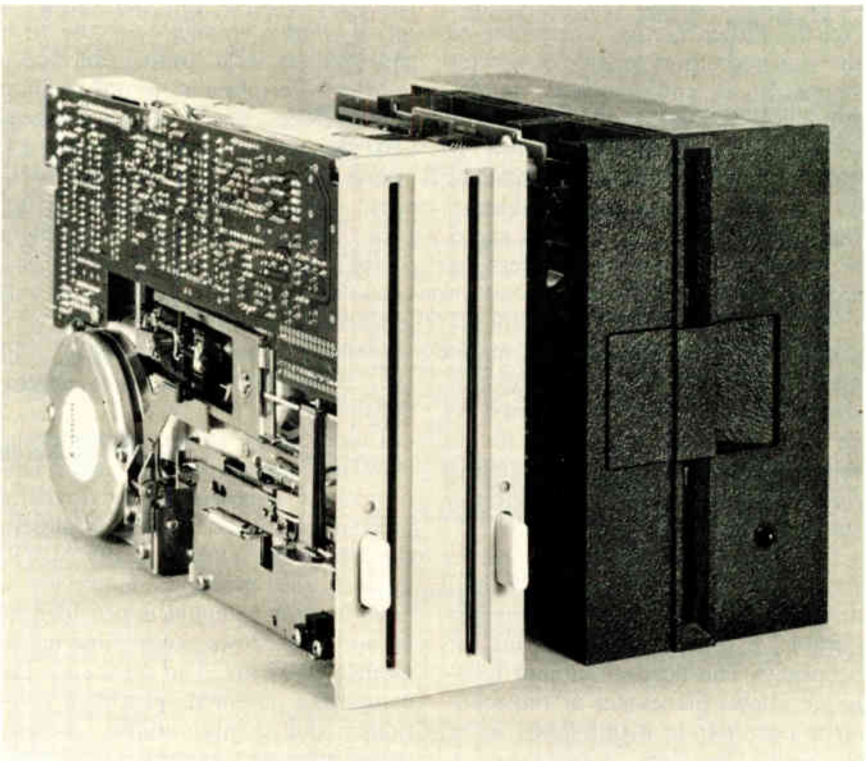
Though half-height disk drives are still hot off the press, already one maker has added a new twist: less-than-half height. All around, vendors like Canon, Remex, Micro Peripherals, Shugart, C. Itoh, and Tandon have chosen diverse routes to achieve similar results on drives they are hurrying to market—up to 1 megabyte of unformatted storage capacity (double-density) on a 5¼-in. floppy-disk drive that takes up just half the room of conventional 5¼-in. drives.

An experienced maker of magnetic heads and other disk-drive parts, Canon USA has joined the disk-drive market with a 5¼-in. floppy disk that measures a low 33 mm high, compared with the *de facto* standard 41-mm height of other half-height floppies. The reduced height can save system designers another 206 cm^3, claims Lee Heller, sales manager of the peripherals division created to market the disk drives.

Heller feels that engineers working on new designs will relish the space saving, but in order not to be shut out of the replacement market, Canon offers a standard 41-mm high bezel as an option. The front panel can easily be changed: it is attached to the lightweight cast-aluminum casing by four screws. The double-sided MDD221 offers a 1-megabyte capacity by using modified-frequency-modulation encoding and a density of 96 tracks/in. Access times are specified at 3 ms track to track and 95 ms average. Head settling takes 15 ms, and head loading 25 ms. The data-transfer rate is 250 kb/s. Canon offers a 500-K-byte drive that retains the 96-track/in. spacing but uses fm encoding. In lots of 1,000, the MDD221 will sell for about $300 each and is available in sample quantities now.

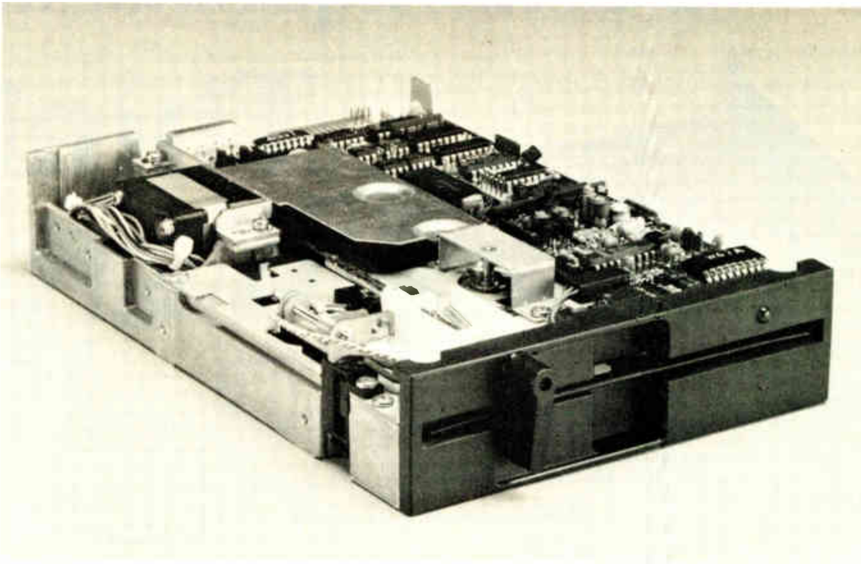
In the drive to make half-height units even smaller, Canon is offering in two versions a double disk drive that stands only 57.5 mm high, or about ⅔ the height of conventional 5¼-in. drives. Storage capacity is doubled to 2 megabytes, but access times remain the same, as does recording method and density. The MDD422 employs two motors, one to turn both disks and the other to position heads for both disks; it sells for $400. The MDD423 uses three motors, allowing the heads for the two drives to seek independently. The third motor adds $50. Samples are available now.

Hybrids. Among other techniques, Canon engineers were able to save space by reducing to two hybrid circuits a number of components, including transistors, resistors, capacitors, and TTL and analog integrated circuits. Also, the brushless direct-drive motors and very thin read-write heads are of Canon's own design. To eliminate the noise that would result from the head and motor resting closer together in the



Siamese twins. Housed in one package two thirds the height of full-sized 5¼-in. drives, Canon's double-sided, dual-drive MDD422 holds 4 megabytes all told. A third motor (model 423) lets the heads on each disk seek independently; with two they move in tandem.

New product roundup



Protector. Longer media and head life are achieved through a disk interlock mechanism and dynamic media clamping. Shugart's mechanism holds the head aside until a disk is inserted in the drive, preventing damage resulting from accidental contact.

smaller than previous models, the new motor contributes to greater drive reliability through fewer parts—the belt, pulley, and bearings needed with previous designs have been eliminated. Also, a microprocessor and custom chips further enhance reliability by reducing the number of components needed to operate the drive electronics.

In lots of 5,000, the SA455 sells for $160 each and the SA465 goes for $195. Samples are available now, and production quantities will be available in the first quarter of next year.

Megabyte. Recently introduced is a Japanese-made 5¼-in. half-height floppy that is sold in the U. S. and Europe exclusively by C. Itoh Electronics and boasts a capacity of over 1 megabyte: up to 1.262 megabytes in a 15-sector-per-track format. Tracks are spaced 96 to the inch. Average seek time is 91 ms, including head-settling time; track-to-track access time is specified at 3 ms. In lots of 1,000, the YD-380T drive sells for $350 and can be delivered in 60 to 90 days.

Bowing at the National Computer Conference in Houston, Texas, this past June was Tandon Corp.'s first half-height model with double-density, single-side capacity of 250-K bytes. The TM50, selling for $50 in large quantities, is a mechanics-only version—designed for engineers who wish to add their own electronics. The 48-track/in. drive has an average access time of 287 ms, including head settling time, and a track-to-track time of 20 ms. This drive also has no head-loading solenoid.

And look for Tandon to expand its line of half-height 5¼-in. drives with new members, one of which will have a 500-K-byte capacity.

Spring of this year saw Shugart introduce a half-height 5¼-in. floppy that was capable of either single- or double-density recording for a capacity of 125- or 250-K bytes. The SA200 sells for $118 in quantities of 5,000 or more.

Canon USA Inc., Peripherals Division, One Canon Plaza, Lake Success, N. Y. 11042. Phone (516) 488-6700 [341]

Remex, 1733 Alton St., Irvine, Calif. 92714. Phone (714) 557-6860 [342]

Micro Peripherals Inc., 9754 Deering Ave., Chatsworth, Calif. 91311. Phone (213) 709-4202 [343]

Shugart Associates, 475 Oakmead Pkwy., Sunnyvale, Calif. 94086. Phone (408) 733-0100 [344]

C. Itoh Electronics Inc., 5301 Beethoven St., Los Angeles, Calif. 90066. Phone (213) 306-6700 [345]

Tandon Corp., 20320 Prairie St., Chatsworth, Calif. 91311. Phone (213) 993-6644 [346]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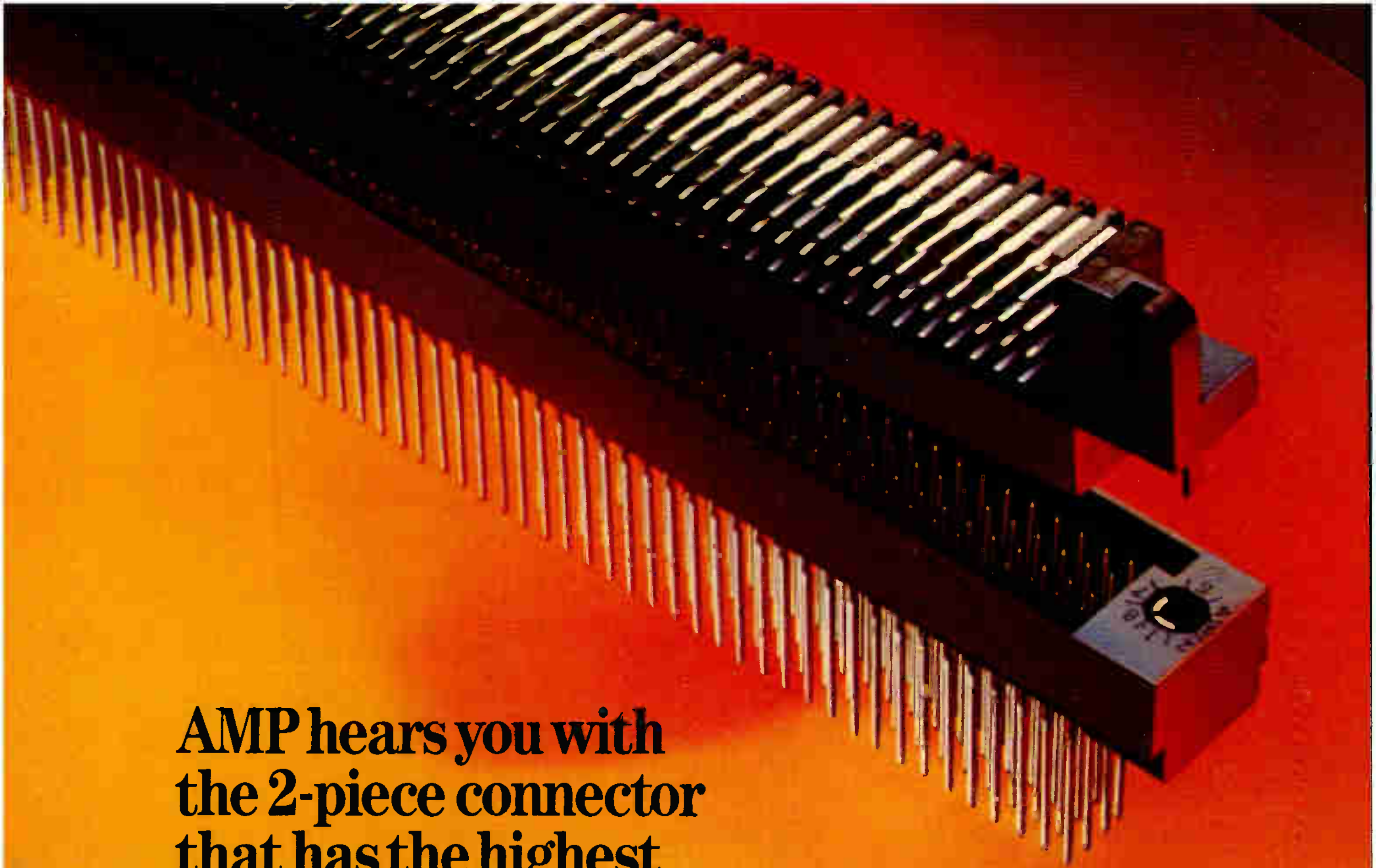

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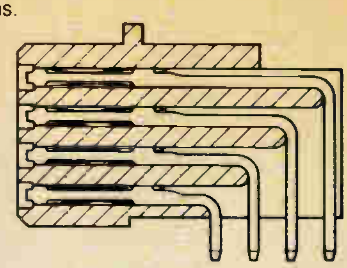

For more information, call the AMP HDI Desk at (717) 780-4400.
AMP Incorporated, Harrisburg, PA 17105.

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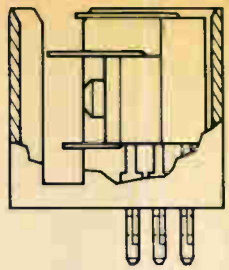

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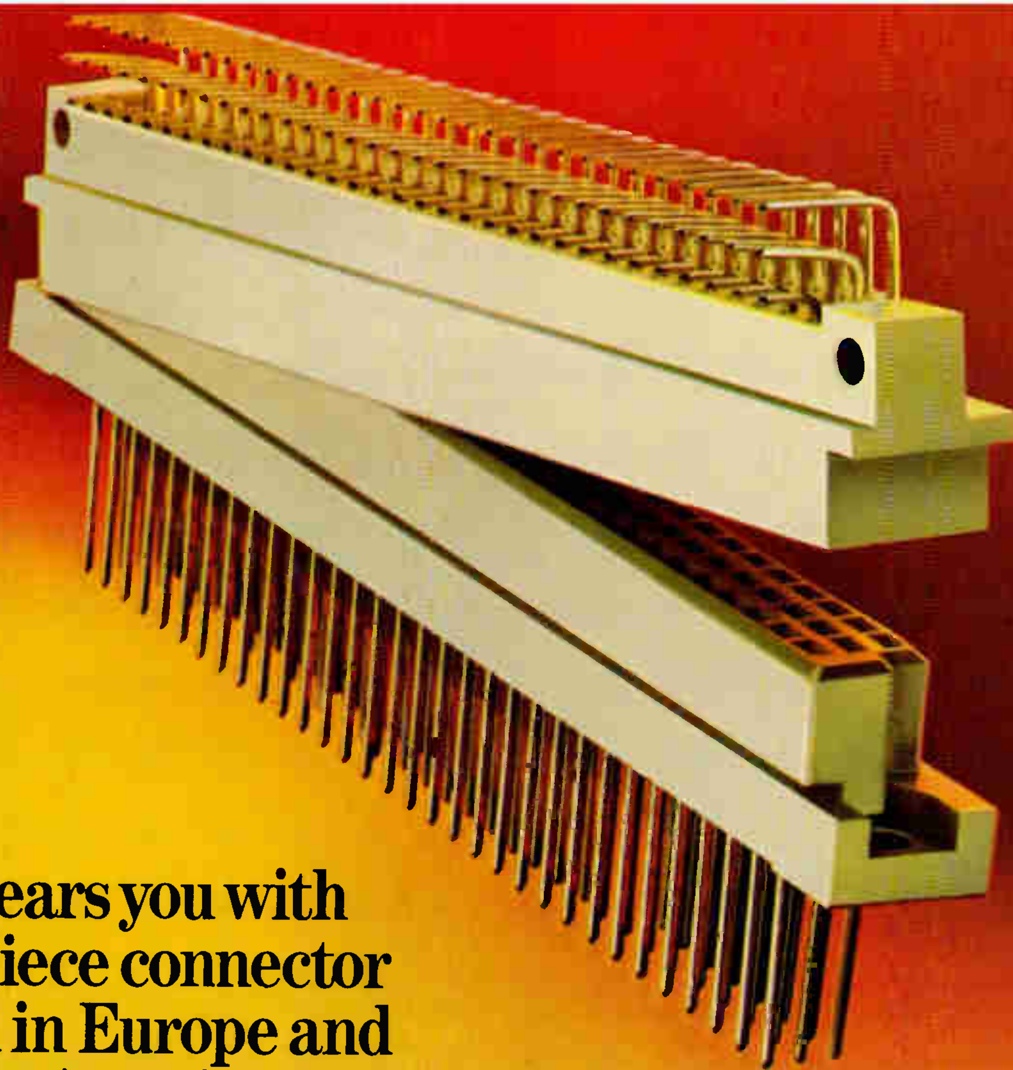

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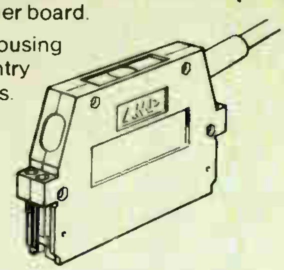

For more information, call the AMP Eurocard Connector Desk at (717) 780-4400.
AMP Incorporated, Harrisburg, PA 17105.

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AMP means productivity.

Industrial controller performs 3 MIPS

Schottky TTL processor has two-level pipeline architecture and high input/output bandwidth, sells for $23,900

by Stephen W. Fields, San Francisco regional bureau manager

Achieving what is probably the highest cost/performance ratio to date in a real-time computer, Hewlett-Packard has unveiled a new top-of-the-line machine in its HP 1000 series. Called the A900, the new computer can process 3 million instructions per second and will sell for $23,900; in original-equipment-manufacturer quantities, the price is $15,550.

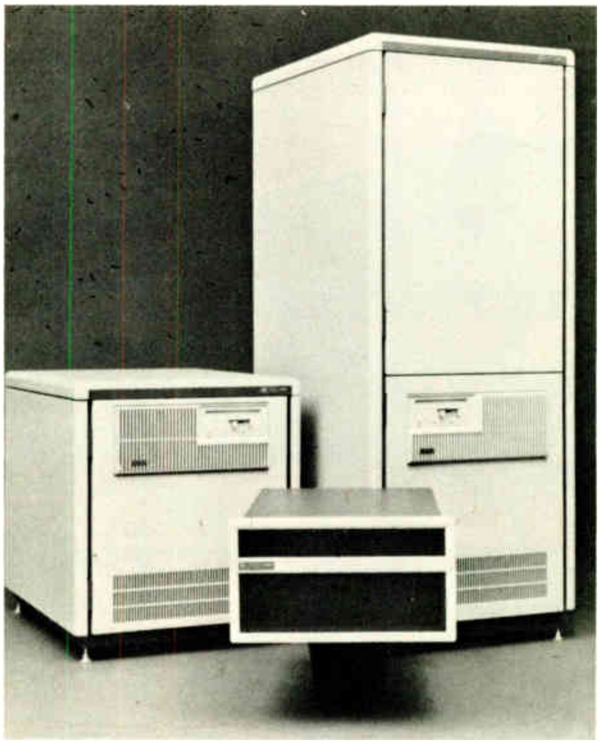
HP's A900 is targeted primarily at the OEM market as a very high-performance real-time engine for industrial-automation and process-control applications. According to Joseph P. Schoendorf, marketing manager for HP's data systems division, "it is particularly well-suited to process monitoring and control, high-speed data acquisition, and image- and signal-processing applications where the A900's raw computational speed, floating-point performance, and sophisticated input/output capabilities are typical customer requirements."

With a very fast cache memory, two-level pipelined architecture, 3.7-megabyte/s peak I/O bandwidth, and a floating-point processor capable of performing a typical mix of floating-point instructions at 560,000 instructions per second, the A900 supports up to 6 megabytes of main memory and provides three times the performance of the previous top-of-the-line HP 1000 machine, the F series.

"We believe the A900 has just redefined the price-performance standard for the minicomputer industry," says Schoendorf. "It's not only the fastest real-time minicomputer we're aware of, but we expect it to be the most reliable minicomputer ever built by HP. It has 25% fewer parts than the HP 1000 F and we expect a mean time before failure of 8,000 hours and a mean time to repair of only 90 minutes—this is especially important to the process-control world," he adds, "where down time can not be tolerated."

Make it fast. In setting the design goals for the A900, Schoendorf says he had essentially one main criterion—to build the fastest machine possible while maintaining complete software compatibility with the other A-series machines, the A600 and A700. The performance was achieved by employing a unique concept in the CPU, which is built with standard Schottky TTL.

According to Schoendorf, most high-speed processors have a pipelined architecture and employ a fast cache memory. "But if the next piece of data the machine needs is not in cache, the processor has to start from ground zero to find it. What we did was design a parallel processor that runs along with the main CPU but always makes the assumption that the data it needs is not in cache. This way it's several steps ahead of where it would be if it assumed that the data was in cache but couldn't find it. We gain almost 1 MIPS this way."



The floating-point processor in the A900 is implemented with three 64-bit large-scale-integrated complementary-MOS-on-sapphire devices developed by HP. It can do a single-precision floating-point addition in 1.6 μs, a division in 5 μs, and a multiplication in 2.8 μs. "To get this performance before, you'd have to spend $100,000 for a computer and put it in a special room. We do it on five cards that can go right on the factory floor—the A900 will operate at 55°C," asserts Schoendorf.

Different word lengths are employed in different sections of the A900. The floating-point section is 64 bits wide, but 16-bit words are used for loading data and 32-bit words are used in the cache-to-main-memory pipeline. The machine-cycle time is 133 ns and most instructions execute in two cycles. When executing the single-precision floating-point whetstone benchmark (B1), the A900 does nearly 1.2 MIPS.

As with all other HP A-series computers, the A900 supports HP's major software packages. These include Graphics/1000-II two- and three-dimensional graphics software and Image/1000 data-base-management software. A-series computers can also use DS/1000-IV networking software to connect to other HP 1000 or HP 3000 systems, as well as X.25 packet-switching communications software. And all A-series computers run under the RTE-A.1 real-time operating system, which supports programming in Fortran 77, Pascal, Basic, and Macro/1000 assembly languages.

Storage. The A900 supports up to 6 megabytes of error-correcting main memory (using 64-K dynamic random-access memory chips) on up to nine boards holding 768-K bytes each. In addition, all A-series machines support up to 250 megabytes of disk storage. There is also a choice of nine models of graphic I/O devices including two new color graphics terminals.

The A900 is available in several packages and configurations. The basic A900 CPU set with 768-K bytes of error-checking and -correcting memory in a rack-mountable chassis with power supply and 15 available I/O slots sells for $23,900; in OEM quantities of 100, it costs $15,550. Add-on memory packages of 768-K bytes, 1.5 megabytes, and 3 megabytes are available for $6,000, $10,000 and $16,000, respectively. A typical system including the A900 CPU set, 768-K bytes of ECC memory, serial and IEEE-488 interfaces, RTE-A.1 operating system, HP 2621B CRT terminal, 16.5-megabyte Winchester disk, desk-style cabinet, freight, and installation comes to $42,675. Deliveries will begin in January 1983, and current delivery estimates are eight weeks after receipt of order.

Inquiries manager, Hewlett-Packard Co., 1820 Embarcadero Road, Palo Alto, Calif. 94303 [338]

The Leading Etch

Business Week said it first by stating that the race to develop a VLSI etcher *"seems to have been won"** by Applied Materials when we introduced our AME 8100 Series Plasma Etch Systems. Less than a year and a half later, VLSI Research confirms it. *"Applied Materials has now emerged as the number one supplier in plasma etching."***

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**Business Week, May 18, 1981, "A Big Stride in Making the Latest Chips"*

***Dan Hutcheson, VLSI Research, Inc., San Jose, CA*

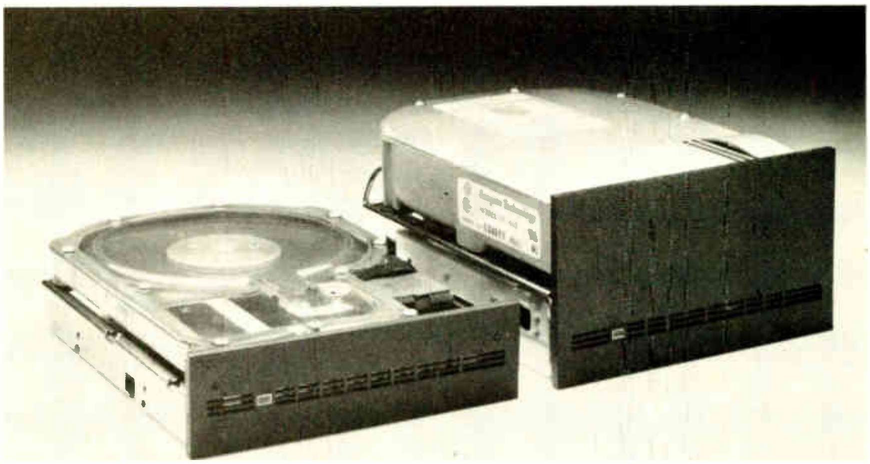
Circle 141 on reader service card

New products

Computers & peripherals

Height of drive is cut in half

5¼-in. Winchester drive fits in half the space required by its predecessors



Seagate Technology packages its entire ST400 line of 5¼-in. Winchester hard-disk drives in the identical 5.75-by-3.25-by-8-in. castings, so the single-disk model ST406 takes up as much space as the three-disk ST419. But with a little tweaking of the air-flow characteristics, a new thin motor, and above all a new casing, Seagate has also come out with a single-disk Winchester drive, the ST206, with 5 megabytes of formatted capacity in a package just 1.625 in. high, or half the height of units in the ST400 line.

The new drive has the same specifications as full-sized models, plus the same power requirements, system interface, and controller. A split-band stepper motor acts as the head actuator, achieving an 85-ms average access time. The unit uses Seagate's industry-standard 5-megabyte/s data-transfer rate. But the ST206 drive may be packaged with a half-height floppy-disk in the same space taken up by a single standard 5¼-in. floppy-disk drive, enabling an original-equipment manufacturer to enclose a cathode-ray tube, the Winchester, and the floppy-disk in a single box.

Tough. Because the new drive is intended mainly for personal and even portable computers, Seagate has used a thin-film–plated medium in the new drive. The plated disks, obtained from the Ampex Corp. and Polydisc, withstand shock and vibration better than conventional oxide media, according to Seagate.

Cost to the OEM will be about the same as that of the full-scale 5¼-in. Winchester, according to Seagate vice president Finis Connor, or approximately $600 in lots of 1,000. "The real advantage is in the low profile," Connor says.

The ST206 will be shown first at Comdex; Seagate will have evaluation models for customers by January and will be in full production by the second quarter.

Seagate Technology, 360 East El Pueblo Rd., Scotts Valley, Calif. 95066. Phone (408) 438-6550 [361]

5¼-in. drive holds 105 megabytes

Six-platter Winchester uses new head technology, has 35-ms average access time

Capitalizing on the fact that as much as 80% of the cost of a disk drive may be considered overhead, start-up firm Maxtor Corp. has come up with a new multiplatter Winchester drive. Because the cost of the casting, printed-circuit board, motor assembly, and actuator remain the same no matter how many platters are on the spindle, multiple platters have a definite advantage in terms of cost per megabyte.

In order to maximize storage capacity on a 5¼-in. Winchester drive, Maxtor has designed a brushless dc motor that fits inside the spindle, adopted a thinner head fixture based on IBM 3370 technology, and utilized an ultrathin surface-mounted pc board, thus opening enough space inside the casting for six platters. The resulting drive, even using conventional oxide-coated disks, stores more than 105 megabytes of unformatted data (82.5 megabytes formatted). Use of a rotary voice-coil actuator gives the unit an average access time of 35 ms.

The XT-1105 may be the largest of the new crop of high-capacity 5¼-in. Winchesters to be shown at Comdex. The Maxtor family also has three-, four-, and five-platter versions storing 48, 67, and 86 megabytes each, respectively (32.5, 52.5, and 67.5 megabytes formatted).

The dc motor consists of a wire-wrapped stator at the center of the spindle, plus magnets set into the inner wall of the cylinder that spins the platters. This design eliminates the space normally taken up by a motor sitting at the base of a spindle.

The XT series can use either thin-film or coated media at its specified density of 980 tracks/in. and 10,200 bits/in. The new IBM technology is a design for the suspension system for thin-film heads, meaning that Maxtor can exchange the heads without a redesign. The composite heads now used are still lighter and smaller than the 3350-style heads and will fly closer to the disks, saving yet more space.

The miniature integrated circuits of the controller, surface-mounted on a thin pc board with no plated holes, take up less than half the space of a conventional pc board. "Surface mounting alone saved us the space of at least one disk," says Maxtor marketing vice president Robert G. Teal. The miniature chips are a little more expensive, he says, but the boards are very much cheaper. Total cost is still slightly larger for surface mounting, but Teal expects that it will be equivalent within a year.

The drive utilizes the standard Seagate data rate of 5 Mb/s. For upgrading, Maxtor plans to utilize other interfaces, such as the intelligent Shugart Associates System Interface (SASI). With thin-film media and advanced run-length-limited codes, Maxtor expects to push 5¼-in. capacity past 200 megabytes.

Maxtor Corp., 5201 Lafayette St., Santa Clara, Calif. Phone (408) 748-7740 [369]

Fast drive stores 57 megabytes

5¼-in. Winchester drive uses thin-film-plated media, accesses in 30 ms, average

The appearance of low-cost 5¼-in. Winchester disk drives during the past year has been a boon to personal-computer owners who had found out the hard way that the floppy diskette was never intended to function as a system disk. But at 5 to 10 or even 20 megabytes of storage, Winchester disks lack enough capacity for multiuser, multitasking systems intended for small businesses. Vertex Peripherals Corp., a new company formed by a phalanx of executives from small-disk-drive pioneer Shugart Associates, has addressed that market with a line of 5¼-in. Winchesters storing 24.4, 40.6, and 56.8 megabytes of formatted data. Called the V100 family, they will be introduced at Comdex.

The market for high-capacity systems (25 to over 100 megabytes) will be about 10 million units next year—some 12% of the market, according to Vertex executive vice president James Adkisson. By 1986, Adkisson says, high-capacity drives will be selling at the rate of 220 million units a year and account for a 30% share of the 5¼-in. Winchester market.

Experience. To establish itself in this market, Vertex is betting on a combination of experienced management and advanced technology. Its top echelon includes three former vice presidents and four former directors of Shugart. President Joe Hooker was a Shugart founder.

The Vertex drives employ thin-film-plated media for high reliability and greater packing density, plus a closed-loop servo that is insensitive to media defects and servo-head azimuth misalignments. The drives are compatible with the Seagate industry-standard 5-megabyte/s data-transfer rate, which means that they can use the same controllers and data separators.

The servo technique used in the V100 family is actually an old one: a position-error signal is derived from the amplitude difference between two reference frequencies on alternate tracks of the disk surface dedicated to servo data. Because the method uses continuous sampling, Adkisson says, it is more accurate than the process in which the phase relation of two adjacent pulses is compared once each revolution. Yet the method is so insensitive to media problems that a surface rejected for data can be used for the servo information. The reference frequencies are chosen so as to be much lower than data frequencies, eliminating the problem of crosstalk between the servo-data signal and other data signals.

The plated medium allows a recording density of 9,920 b/in. and 960 tracks/in. Vertex uses IBM 3350 head technology (though the heads themselves are made with a composite of manganese-zinc and ferrite). A rotary voice coil serves as the actuator. The average access time is 30 ms.

The V100 series will be available in production quantities in the first quarter of 1983. Prices will range from $1,100 to $1,500 in moderate original-equipment-manufacturer quantities. Vertex will introduce further high-capacity 5¼-in. Winchester disk drives, storing up to 100 and 160 megabytes, later in the year.

Vertex Peripherals Corp., 2150 Bering Dr., San Jose, Calif. 95131. Phone (408) 942-0606 [362]

3-d graphics system stands alone or links to host

With the CS-3, an integrated graphics work station, designers can model and manipulate three-dimensional solid objects with display attributes such as smooth shading of surfaces and anti-aliasing on a 512-by-512-picture-element color display (12 b/pixel). The user can display up to 4,096 different colors in a single image, selected from a palette of 16 million.

In its standard configuration, the CS-3 acts as an intelligent graphics terminal, interfacing with a host computer through a RS-232-C port. With the addition of an optional

Winchester–floppy-disk-drive subsystem, the CS-3 becomes a 16-bit microcomputer with 3-d graphics capabilities. The unit's proprietary imaging routines allow the user to model solid objects quickly and easily, as well as to perform conventional functions such as wire-frame construction and 2-d graphics.

The central processing unit is composed of Intel's 8086 microprocessor, enhanced by an 8087 numeric processor, along with 128-K bytes of random-access memory, expandable to 512-K bytes. Options include a joystick, digitizing tablet, Ethernet interfaces, and preprocessing software to emulate various graphics terminals and languages.

The basic system price, including the graphics firmware, keyboard, and 19-in. color monitor, is $9,870 for evaluation units. The standalone system with the Winchester–floppy-disk drives is $17,870. Delivery takes about 60 days.

Cubic Systems, 2372 Ellsworth St., Berkeley, Calif. 94704. Phone (415) 540-5733 [363]

Subsystem makes computers out of work stations

With the flip of a switch, series IV and series 5000 multifunction work stations are transformed into personal computers after attaching either the PC I to any series IV cathode-ray tube or the PC III to a Fastrak work station on the Series 5000 terminals. Each is a free-standing desktop microcomputer whose central processing unit, memory, and input/output controllers are contained on one board in the same cabinet as two 5¼-in. floppy-disk drives. Both can support two additional drives.

The PC I and III are highly optimized Z80A-based systems that operate under CP/M and include 128-K bytes of random-access memory, 1.6 megabytes on the two disk drives, a hard-disk interface, built-in printer and communications ports, and an 8-in. floppy-disk controller.

Selected software packages, collectively called the PC Portfolio, include Digital Research's CBasic,

Evolution of the species

Circle 145 on reader service card

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	ORGANIZATION	ACCESS TIME	CONSUMPTION
ET 2716 Q ET 2716 Q-1	2 K×8 2 K×8	450 ns 350 ns	525/132 mW 525/132 mW
ET 2732 Q ET 2732 Q-3	4 K×8 4 K×8	450 ns 350 ns	790/185 mW 790/185 mW
ETC 2716 Q ETC 2716 Q-1	2 K×8 2 K×8	450 ns 350 ns	25/0,5 mW 25/0,5 mW

As the leading European manufacturer of EPROM memories in both NMOS and CMOS technologies, Eurotechnique now offers you its CMOS EPROM memory, the ETC 2716. Thanks to its single + 5V power supply and to its active working performance (5 mA), and standby (0,1 mA), Eurotechnique's ETC 2716 memory is ideal for all systems with a high density programmable memory designed around a CMOS microprocessor. Because of its low power consumption, it allows you to not only reduce the cost of your system, but also to increase its reliability. The CMOS ETC 2716 EPROM memory extends a range of EPROM memories already including the ET 2716 and 2732. These products are available ex-stock.

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New products

Pascal/MT+, and Sorcim's SuperCalc. The basic PC I and III configurations sell for $3,610 each; the PC Portfolio adds $450. The units will be available in the second quarter of next year.

Four-Phase Systems, 10700 North DeAnza Blvd., Cupertino, Calif. 95014. Phone (408) 255-0900 [366]

AWS work station is enhanced with no price increase

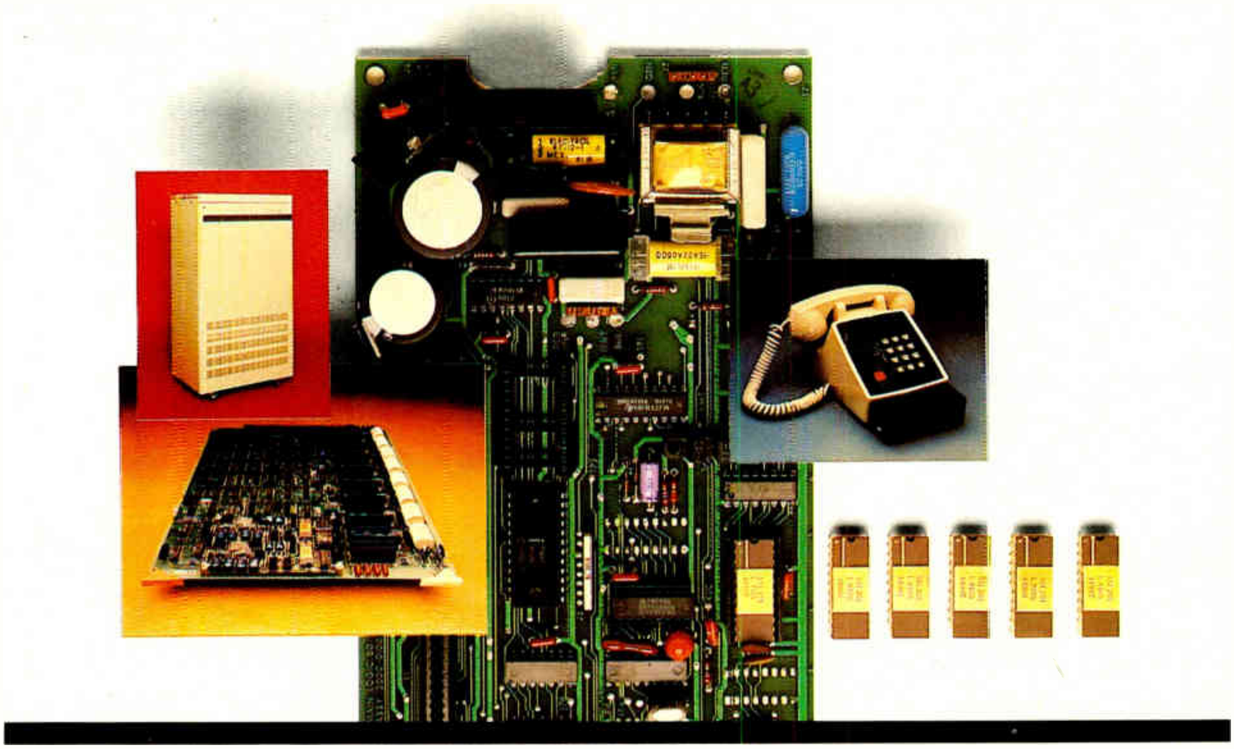
Called the AWS Turbo Workstation, Convergent Technologies' year-old unit now boasts four times the performance of the earlier units with no increase in cost. The Turbo multiplies processing performance through the use of an 8-MHz 16-bit 8086 processor and through a proprietary memory management scheme that increases the speed of memory-access cycles. All central processing units and up to 512-K bytes of random-access memory are on a single circuit board.

In addition, the Turbo line offers double the disk-storage capacity in equivalent work-station units with double-sided, double-density floppy-disk drives. Up to 5 megabytes of storage are available in a combination of minifloppy- and Winchester-disk drives mounted on a single pedestal with the processor and display. The new units are compatible with all members of the firm's work-station family.

The work stations use the firm's CTOS operating system and support Cobol, Fortran, Basic, and Pascal. Two RS-232-C ports may be programmed for a variety of tasks with software-selectable bit rates up to 19.2 kb/s.

The four Turbo models range in price from $4,790 for the model 215 cluster station with 256-K bytes of RAM and no mass storage to $9,990 for the model 245 with 256-K bytes of RAM, one floppy-disk drive and one Winchester disk drive, offering a total of 5 megabytes of storage.

Convergent Technologies, 2500 Augustine Dr., Santa Clara, Calif. 95051. Phone (408) 727-8830 or (800) 538-7560 [365]



PCB's and photos of PBX and transaction terminal courtesy of American Telecom, Inc. and DMC Systems, Inc.

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Microcomputers & systems

Portable unit runs MS-DOS, CP/M-80

8088-based microcomputer has built-in printer option and 3½-in. floppy-disk drives

A medium-priced portable personal computer, the 8088-based Dot runs MS-DOS to take advantage of software written for the IBM Personal Computer, but has an optional Z80 processor for running CP/M programs. It costs $2,995 in its sparest configuration—32-K bytes of main memory, one Sony 3½-in. floppy-disk drive, a detachable keyboard, a 5-by-9-in. cathode-ray tube with bit-mapped graphics capability, two expansion-board slots, and a 90-day warranty. The Z80 option, which includes CP/M 2.2, adds only $155.

The Dot computer [*Electronics*, Oct. 20, p. 15] is available in configurations that include an 8087 arithmetic coprocessor, a high-resolution dot-matrix printer, and a modem. Main memory can be expanded on the main board to 256-K bytes and to 704-K bytes with an expansion card; in addition, 32-K bytes of memory dedicated to the graphics display is standard.

"What we have is a totally integrated 16-bit high-performance machine. And we've put everything in a small box," notes Computer Devices Inc. president Si Lyle. "We like to think of it as a corner-top computer," he adds, referring to the fact that the 26-lb, 17.75-by-14.5-by-7.5-in. unit fits on the corner of a desk. The 287-K-byte Sony disk drive is instrumental in helping the firm keep the unit small. The 135-track/in. disk now has only one usable side but "will be improved," according to Lyle.

Large display. The CRT can display up to 132 characters per line and either 16 or 25 lines of text. Using software written for the IBM Personal Computer, graphics resolution is 640 by 200 picture elements. But separate control circuits in the Dot allow a 1,024-by-248-pixel resolution to be seen. "We are currently working with a number of software houses that are designing applications for our bit-map graphics mode," notes Lyle. The display supports multiple-window operation.

The firm has drawn on its expertise as a portable-printer and modem vendor in incorporating these add-ons within its compact box. With bidirectional speeds of up to 160 characters/s, the thin-film thermal printer produces fully formed 5-by-10-dot-matrix characters in upper and lower case and can print incoming data directly from a 1,200-b/s phone connection. It prints up to 132 characters/line and has a graphics mode with a density of up to 128 dots/in. horizontally and 64 dots/in. vertically. The printer has a 2-K-byte buffer and an 8031-based controller with control code in 16-K bytes of programmable read-only memory.

With the printer, 64-K bytes of main memory, an RS-232-C port, and MS-DOS, the Dot is priced at $3,995. A built-in 300-b/s modem is available for an additional $225 and a built-in 1,200-b/s modem adds $895 to the price. A second disk drive costs an additional $649. Delivery is in 90 days.

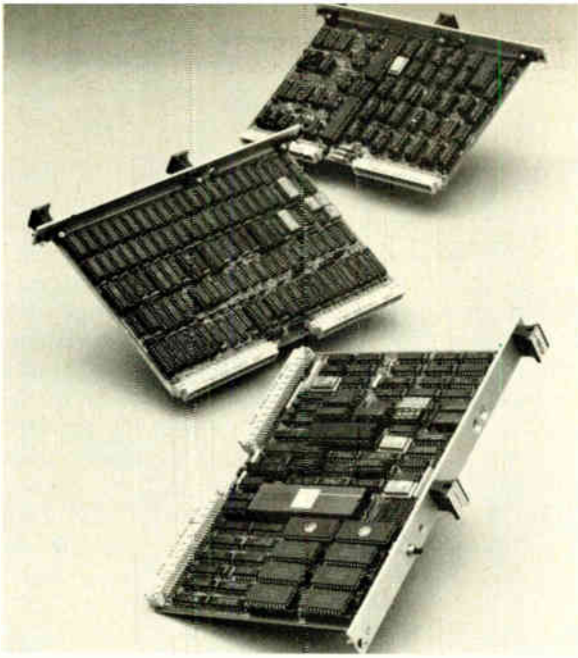
Computer Devices Inc., 25 North Ave., Burlington, Mass. 01803 [380]

VME-bus family is launched

68000-based computer, I/O, and memory modules mark Mostek's move to systems

Intending to turn its VME-bus board line into a system-oriented business, Mostek Corp. is making available its initial three modules in the 68000-based family. These cards—a single-board computer, a dynamic random-access memory module, and a serial input/output board—are intended as basic building blocks to let customers try out the VME concept, which was first announced a year ago by Mostek, Motorola Inc., and Signetics Corp.

Next month, the subsidiary of United Technologies Corp. plans to



offer a VME-bus enclosure that will hold up to 10 VME cards and three 5¼-in. disk drives. The box, 12¼ in. wide and 23 in. deep, will be followed in January by three additional building blocks—a floppy-disk–drive controller, a hard-disk controller, and a memory management module.

Mostek, which is initially targeting most of its VME activites at high-end 16-bit users, is expected soon to back an operating system for software development, and it is reported to be leaning toward Unix. By the third quarter of next year, it plans to announce a VME system product.

VME, which will support 32-bit data transfers and the future 32-bit version of the 68000 (the 68020), uses printed-circuit boards and backplanes meeting the DIN 41612 and 41494 mechanical standards—commonly known as the Eurocard form factor. Generally, one of the two 96-pin connectors on the double-width Eurocard carries primary signals for 16-bit systems, and the other is reserved for multiprocessing and future 32-bit system requirements.

Motorola in July began phasing in some 17 VME modules and will continue into the first quarter of 1983. Signetics, meanwhile, will make its first four VME boards available by December. A fifth board—a cathode-ray-tube controller—is slated to be introduced next year.

Mostek's 16-bit single-board computer, the MK7564, uses an 8-MHz 68000. The standard card comes with 12-K bytes of static RAM and two programmable read-only memories containing a monitor and debugger. A module with 4-K bytes of static RAM and six empty memory sockets for 2764 8-K-by-8-bit erasable PROMs is also in the lineup.

Semicustom logic arrays are used to alter the cards to suit various addressing schemes and memory-chip speeds. The 7564 features an RS-232-C serial I/O channel using Mostek's serial-timer-interrupt chip, the MK3801. The module also has an 8-bit switch-input register and a common status register, which makes possible software control of the 3801, bus time-out status, self-testing light-emitting-diode indicators, and individual enable bits. The standard board runs $1,695, and the optional version is $1,555.

The 64-K-by-32-bit dynamic-RAM module, designated MK75701, offers self-contained parity generation and checking. It can perform 32-bit data transfers using the second VME-bus connector. Logic arrays change addressing schemes. Refresh signals are generated on the card, which has a typical read-access time, including parity checking, of 434 ns and a write-access time of 200 ns. The standard card is $2,395, and a version without parity bits is $2,260.

The MK75801 I/O card uses two MK3887 serial I/O chips to handle a number of byte- and bit-oriented protocols, such as IBM's bisynchronous High-level Data-Link Control and Synchronous Data-Link Control. Address strapping makes it easy to customize the cards through the VME backplane.

The I/O card can produce and check cyclic-redundancy-checking codes in any synchronous mode. For asynchronous communication, the board can run at 19.2 kb/s; in synchronous operation, it can handle 307.2 kb/s. One version of this card, at $925, has two fixed RS-232-C channels; the other, at $980, offers two channels that can be set up as RS-232-C or RS-422 interfaces.

Mostek Corp., 1215 West Crosby Rd., Carrolton, Texas 75006. Phone (214) 466-6000 [360]

$3,650 computer has 68000 CPU

Personal computer is targeted for technically oriented users, comes with graphics package

A compact, low-priced personal technical computer—the HP series 200 model 16—is Hewlett-Packard's first 16-bit machine to be packaged like a personal computer. Its small size—it takes up only 1.7 ft^2 of desk space—comes from a new cathode-ray-tube and central-processing-unit package and the use of Sony's 3½-in. micro floppy-disk drives. And it is the first 16-bit computer that HP will offer through both direct sales and retail outlets.

Based on Motorola's 68000 microprocessor, the model 16 is actually a low-end addition to HP's 9826 and 9836 series of desktop computers, which the firm has renamed the models 26 and 36. "We call the 16 a personal technical computer because, while it was designed for scientists and engineers, it can be used by anyone who needs a personal computer

with maximum [16-bit] computing power," says Patrick R. Welch, marketing manager for HP's desktop computer division.

"Its 16/32-bit processor, 8-MHz system clock, and software execution power provide the speed required for scientific and engineering applications," says Welch. "And because power is not something that just technical users should have, we expect the model 16 to be attractive to many people who want a personal computer packing the highest performance they can get."

The model 16 consists of a 9-in. CRT, a detached ASCII keyboard, and a choice of several disk-drive configurations based on the 3½-in. floppy-disk drives, including single or dual 3½-in. units, providing 270-K bytes of storage per drive, and a single microfloppy packaged with a 4.6-megabyte Winchester hard disk. The standard 128-K bytes of main memory can be increased to 768-K bytes, and with an external expander, main memory can be as large as 4.6 megabytes.

Graphics. The CRT has an 80-character-by-25-line display. When used with its built-in graphics capability, the display has a resolution of 300 by 400 picture elements. Besides the standard ASCII keys, the keyboard has five user-definable keys (10 with the shift key) and a special rotary control knob used for fast editing of programs, cursor positioning, analog control of instruments tied to the computer, and other applications requiring linear input.

Three languages are available for the 16—Basic, HPL, and Pascal. HP Basic includes enhancements typically found in more powerful languages such as Fortran or Algol, including subroutines, multidimensional arrays, unified input/output and mass storage, labeled common blocks, and external program control. "It actually may be a disservice to call it Basic," says Welch, "because it is so powerful."

Several application packages are also available. These include computer-aided engineering tools such as ac-circuit analysis and digital-filter design; mathematics modules such as numerical analysis and statistics; and business aids such as VisiCalc, project management and graphics presentation programs. Considering that an engineer may spend 80% of his time generating reports and documents, these packages should prove very useful. HP is also considering offering CP/M and Unix for the series 200, opening up the huge base of software designed to run on these operating systems.

Communications interfaces in the 16 include the HP-IB (IEEE-488) bus and an RS-232-C port. Other interfaces are available as plug-in cards. And the 16 can be linked with other 16s in a network with shared disks and printers. "We call this shared-resource management [SRM]," says Welch, "because it lets several users share files and use the same central printer and disk drives, which can mean tremendous cost savings." The SRM network can also incorporate other HP desktop computers, including the HP 9845, a full engineering work station with color graphics.

The base price of the model 16 is $3,650, including processor, display, keyboard and 128-K bytes of memory. A single 3½-in. microfloppy drive costs $1,200, a dual microfloppy unit is $1,775, and a unit with one microfloppy and the 4.6-megabyte Winchester is priced at $4,975. Deliveries are in 4 to 10 weeks.

Hewlett-Packard Co., 1820 Embarcadero Rd., Palo Alto, Calif. 94303 [371]

Small systems support networks

8086-based units stand alone or act as gateways between Ethernet and twisted-pair net

Most low-cost local networks use personal computers, simplified versions of Ethernet controllers, and twisted-pair cable. But it would cost less to start with a built-in interface on a multiuser computer, upgrade to a small local network, and, in large companies, then supplement an Ethernet "backbone" with several low-cost networks, argues Altos Computer Systems.

To make its point, the firm is launching a series of 16-bit microcomputers designed to provide such a progression while holding per-user cost to around $1,000. Members of the Altos 586 series can be used as stand-alone multiuser systems, as multiuser stations on the recently announced Altos Net or on a standard Ethernet, or as gateways linking the two types of networks. Moreover, if internetwork traffic is light, a gateway can also serve as a multiuser station.

Each 586 system supports six users (expandable to nine) at terminals on RS-232-C links. Its main processor is a 10-MHz 8086 unburdened by a Z80-based intelligent input/output subsystem that controls the Altos-Net, the RS-232-C ports, a real-time clock, and a floppy-disk controller. A hard-disk model (586-10) also contains an intelligent disk-drive controller and a 16-K-byte buffer memory on a second board, which plugs into the system's Multibus backplane.

The floppy-disk system costs $4,990 with 256-K bytes of memory

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Circle 151 on reader service card

and two 1-megabyte 5.25-in. floppy-disk drives. The other system provides 512-K bytes of memory, a 10-megabyte hard-disk drive, and a floppy-disk drive for $7,990. Both expand to 1 megabyte of main memory and, early next year, to 80 megabytes of disk storage. Another upcoming enhancement is a communications board for operation with IBM and X.25 protocols on conventional networks.

Optional software. An optional Altos-Net software package, priced at $295 per system, enables up to 32 systems to be linked with a twisted-pair cable. The same software and an optional Ethernet controller converts a 586 system into a multiuser Ethernet station or into a gateway at a total cost of $2,500, plus cabling (a price that will soon be cut by new Ethernet chips). Altos ACS8600 computers can also operate on an Ethernet with the second option.

A separate Altos-Net controller is not needed because the smaller network operates without the conventional carrier-sense multiple-access protocol, explains Peter Kaveler, Altos software engineer. The data packets are transmitted at rates of up to 800 kb/s by a standard RS-422 driver chip while a Zilog communications chip runs a protocol similar to the Synchronous Data-Link Control protocol. Each packet contains opening and closing flags, station address, the data, and a 2-byte cyclic-redundancy check word. The optional controller transmits Ethernet packets over coaxial cable at the standard 10-Mb/s rate.

The remaining five layers of the International Standards Organization seven-layer network model are implemented in the software package, which runs the network transmission-control and internetwork protocols and also provides for file transfers, virtual-terminal operation and electronic mail. This software is based on 3COM Corp.'s Unet system, which runs under Bell Laboratories' Unix operating system. Altos 586 systems support the package with the Xenix operating system and a proprietary memory management system designed to enhance Xenix operations. Other software options include the MP/M-86, Oasis-16, Pick, and MS-DOS operating systems, and the Basic, Cobol, Fortran, C, and Pascal languages.

Altos Computer Systems, 2360 Bering Dr., San Jose, Calif. 95131. Phone (408) 946-6700 [372]

S-100 system serves four users

Microcomputer is optimized to run under MP/M, is faster and cheaper than predecessor

The latest in a line of CP/M-compatible microcomputers for S-100–bus environments, the QDP-300 is representative of the maturity of the market for machines aimed at the multiuser business environment. Its single-board design enables the manufacturer, QDP Computer Systems Inc., to cut the price of improved performance, especially in multiple-user environments.

The new system offers about twice the throughput of the QDP-100 when running the multiuser MP/M operating system, according to Kenneth P. Perich, sales and marketing director for the three-year-old firm. At a suggested retail price of $3,695 and discounts of up to 30% for original-equipment manufacturers, this undercuts the older system's price by more than 20%.

The improvement in performance is due to a number of factors, including a 6-MHz Z80B central processing unit, a 64-K-byte cache memory for disk-track buffering, and a Z80A direct-memory-access processor that handles disk transfers and memory-bank data switching. QDP engineers were able to pack all the electronics onto a single double-height (10-by-9-in.) S-100 card, including up to 256-K bytes of memory using 64-K random-access memory chips. The board replaces up to six cards in previous systems, so the QDP-300 is able to take full advantage of the CPU's speed by avoiding interboard communication via the S-100 bus.

Ten ports. Two double-sided, double-density, half-height 8-in. floppy-disk drives are standard, for a total of 2.4 megabytes of formatted storage. A 5.25-in. internal hard-disk option is available, adding 10 or 15 megabytes. Two RS-232-C serial ports and two parallel ports come with the system; options expand this to up to six serial and four parallel ports. In its maximum configuration, the QDP-300 can support up to four terminals and six peripherals.

For a high level of reliability, the 300 employs a large transformer and filtered power supply that tolerate fluctuations in line current better than the switching supplies employed in many systems, says the firm. A built-in temperature sensor sounds an audible alarm if overheating occurs. The 18-by-19.5-by-7.75-in. cabinet is made of rugged 0.1-in.-thick aluminum and has room inside for two S-100 cards of the user's choice, such as special-purpose graphics processors or the 512-K-byte memory card that will be available from QDP in December.

By early next year, the company plans to offer a card that will house either an Intel 8086 or an iAPX 186 processor, plus software that will upgrade the 300 to a 16-bit system.


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Circle 153 on reader service card

The QDP-300 will be available for delivery late next month. It accommodates worldwide markets with conversion to 115- or 220-V operation at the flick of a switch. The one-year warranty is backed by service performed domestically by the Installation and Service Engineering division of General Electric Co. Overseas QDP dealers have parts in stock, says Perich, and the company supports a component-exchange program that includes airmail shipment of replacement parts.

QDP Computer Systems Inc., 10330 Brecksville Rd., Cleveland, Ohio 44141. Phone (216) 526-0838 [379]

Logic interface circuit serves 5¼- and 8-in. disk drives

Incorporating a digital data separator, write precompensation logic, a head-load timer, and a crystal oscillator in a 20-pin dual in-line package, the FDC 9229 floppy-disk logic interface circuit aids such popular disk–controller-formatter large-scale integrated circuits as the FDC 179X and 176X family of controllers.

The digital data separator converts a jittery serial bit stream from a floppy-disk drive into separate clock and data signals for a floppy-disk controller. The write precompensation circuit allows a number of different precompensation values (ranging from 0 to 625 ns) to be dynamically selected in the course of writing to the inner and outer track of the floppy-disk drives. Employing a single pin, the 9929 can work with either the 179X or μPD765 family of controllers to reduce the amount of external components required to construct a floppy-disk controller or interface module.

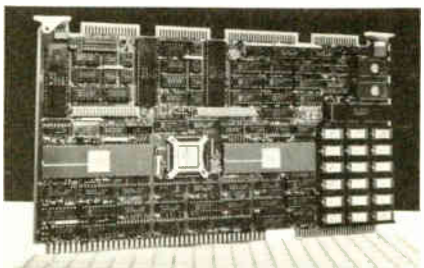
The 9229 operates from a 5-V supply and requires a 16- or 8-MHz crystal or TTL-level clock. It is available from stock in plastic and ceramic packages in two versions: the 8-MHz FDC 9229, intended for 5¼-in. drives, and the 16-MHz model 9229B for 5¼- and 8-in. drives. The price for the 9229 in a plastic package in 100-piece amounts is $11.30 each, the 9229B version costs $12.50 each, also in a plastic package in quantities of 100.

Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, N. Y. 11788. Phone (516) 273-3100 [373]

68000-based SBC geared for multiuser Unix systems

Compatible with the 24-bit Intel Multibus, the HK68 single-board microcomputer is designed around the Motorola MC68000 8-MHz microprocessor and sports a powerful array of on-card features such as the MC68450 four-channel 16-bit direct-memory-access controller and the MC68451 segmented memory-management unit to facilitate the operation of a four-to-eight-user Unix system.

The HK68 has 256- or 128-K bytes of dual-port random-access memory with two parity bits a word. Using the National 8409 dynamic-RAM controller, the RAM can be expanded to 1 megabyte when 256-K-byte memory chips are available. The single-board microcomputer is equipped with two sockets allowing for the use of 2716, 2732, 2764, or 27128 erasable programmable read-only memories for a 64-K-byte capacity; two Z8530 serial communications controllers capable of im-



plementing asynchronous and synchronous protocols; and interfaces for Winchester disk and streaming tape-drive controllers.

The single board price for the HK68, fully loaded, is $3,895. Partially populated versions are also available from stock.

Heurikon Corp., 3001 Latham Dr., Madison, Wis. 53713. Phone (608) 271-8700 [376]

Plug-in board brings CP/M software to TRS-80 users

Thanks to the Shuffleboard III plug-in board, users of the TRS-80 can tap into a wealth of CP/M-based software such as WordStar, SuperCalc, DBase II, and MailMerge.

The Shuffleboard III has 16-K bytes of random-access memory that gives the TRS-80 model III the power of CP/M 2.2 without interfering with the read-only or video memory. In addition, it will not interfere with any TRS-80–compatible DOS such as TRSDOS, NEWDOS, and LDOS.

Available completely assembled, burned in, and tested, the board can be installed by plugging it into two existing sockets inside the model III microcomputers. Shuffleboard is currently available with CP/M 2.2 and Basic 5.0 software plus an installation and users' manual at a price of $299. It comes with a full one-year warranty.

Memory Merchant, 14666 Doolittle Dr., San Leandro, Calif. 94577. Phone (415) 483-1008 [377]

Memory module expands abilities of the Atari 400

The Ramcram Plus memory-expansion module provides users of the Atari 400 computer with 48-K bytes of random-access memory in a single module. According to the company, the memory-expansion module allows the Atari 400 owner to upgrade his or her system to equal the computer power of the larger, more expensive Atari 800.

The Ramcram Plus is plug-compatible with existing read-only memory cartridges and does not need to be soldered to the Atari computer. It can be easily installed in less than 10 minutes using a screwdriver.

The Ramcram Plus memory-expansion module is offered with gold-plated contacts and comes fully socketed. It retails for $229.95.

Axlon Inc., 170 North Wolfe Rd., Sunnyvale, Calif. 94086. Phone (408) 730-0216 [378]

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We deliver better electronics plants

Circle 156 on reader service card

Instruments

Software speeds signature tests

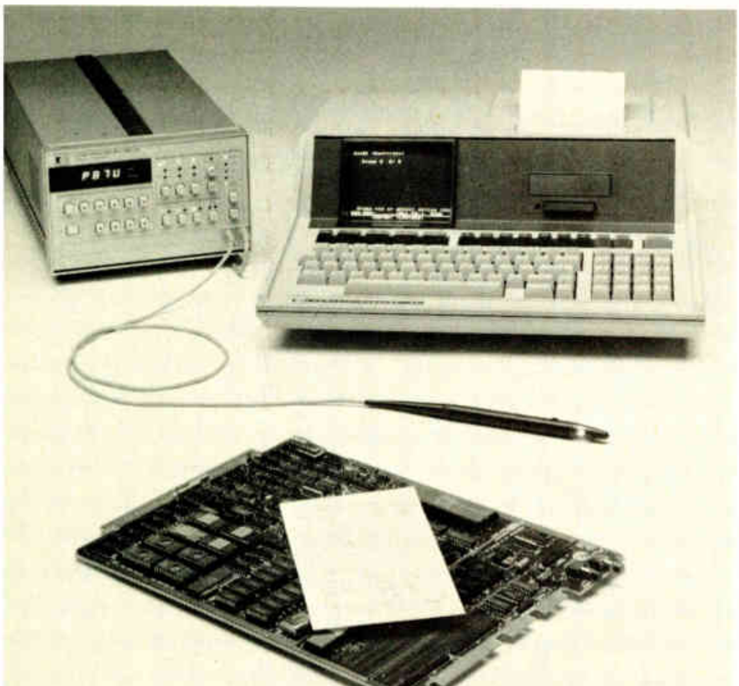
Package makes test system of signature-analysis meter and desktop computer

The soft instrument—a measurement device whose capabilities are determined by the software, rather than the hardware, it can accommodate—has long been a dream of instrument designers and users alike. In its latest product for the production-and-service arena, Hewlett-Packard Co. has come quite close to this ideal.

Called the logic troubleshooting system model 55005A, the system takes advantage of hardware that has been around for some time. It uses an HP-85 desktop computer, which controls an HP 5005B meter [*Electronics*, July 14, p. 223], the IEEE-488–compatible version of the year-old 5005A signature multimeter. Thus, what makes the system worthy of note is not its hardware, but how the company has created a powerful troubleshooting tool for field depots and production lines by tackling some complex procedural problems in software.

To make use of the system in either a production or a service environment, the user must begin with a board that is known to function in the intended way—a prototype, for instance. The troubleshooting system then prompts an individual, preferably an engineer or someone familiar with the board, through a process of identifying particular devices and their pins. This individual then gathers signatures for the pins, identifying them as inputs, outputs, grounds, or power-supply pins. Further, the person setting up the system notes which pins are tied together as he or she goes along, again responding to prompts from the system, which keeps track of signatures that are identical to others.

Prompts. Once this information has been gathered and stored in a quick, routine fashion, troubleshooting a board is simply a matter of identifying the board and placing a probe on the pin indicated by the computer, just like following the guided-probe routine of a board-test system. An operator can find a problem without any special knowledge of the board being tested. Prompted by the system, he or she backtraces until the inputs to a device match those correct signatures previously stored. The device with the correct inputs but bad outputs is the obvious culprit.



Further, the system permits more experienced operators to "jump around" when looking for a fault. If the operator suspects that a problem lies in a certain functional area of a board, the search can be limited to that area ahead of time, and only signatures that should occur in that area will be checked by the system in comparing actual to stored information.

In writing this software for the 55005A, HP engineers were faced with a particular challenge—putting an entire processing scheme and electronic data base into the HP-85's 32-K bytes of internally available space. In the past, functionally similar programs had never fit into such a compact amount of memory. Project manager Ken Rothmuller observes, "Previous backtracing schemes have been written for larger machines, the smallest of which takes up about 128-K bytes on a minicomputer."

To fit the HP 55005A program into the HP-85, the data structure had to eschew duplication yet be accessed in a number of different ways. "You have to be able to ask a good many questions of the data base, and it must answer each of them in an efficient way," notes Rothmuller. For example, at some point in a troubleshooting routine the system, on behalf of but unknown to the user, may ask the data base whether an integrated circuit and pin number exists, what is connected to the node, what are the driving pins to the node, and what pins affect those driving pins.

One way in which the program saves on user memory is by using a ring structure for pointers. "In a ring system, the bottom element will contain a pointer that points back to the element at the top of the list," notes Rothmuller. "This gives us a way of getting back to the original piece of information in a search without having to create duplicate pointers to reverse the process."

In constructing the data-base software, separate node-list editors, logic-dependency tables, and troubleshooting trees were discarded in favor of a single incremental data-base structure pointer. A change in the data base is immediately represented, and all related items made consistent. The report and probing subsystems can access the changed knowledge base as soon as the change is made.

The system is priced so that it can

be purchased by production and service managers without having to spend months justifying its purchase: a basic, bundled system costs $9,675. The 55005A can be enhanced with disk drives to enlarge the data base and a printer for hard-copy logs of repair activity. System deliveries begin starting in November.

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Rd., Palo Alto, Calif. 94303 [352]

Dedicated memory testers check RAMs 16 Mb in size

Dedicated memory-test systems have become popular thanks to their speed and often initially low cost. But they can seldom be upgraded in the field to accommodate the increasingly complex memories that appear each year. The Test Systems division of Eaton's Semiconductor Equipment operation has developed a series of memory-test systems to answer this need.

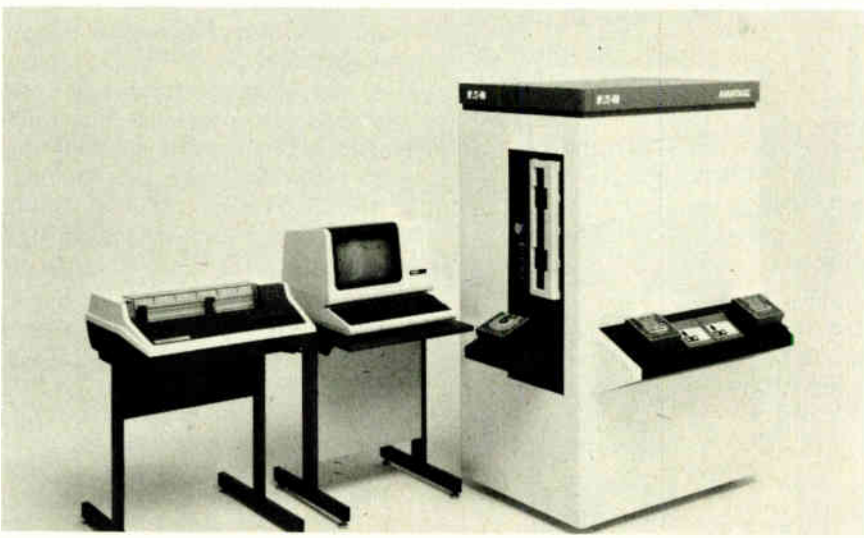
The Avantage family covers the complete range of test requirements from engineering and device characterization to production (wafer probing and final testing) to incoming inspection. Each is field-programmable and expandable from the simplest to the most complex.

The key to the Avantage's flexibility is what Ron Thomas, project engineer at Eaton, calls flex registers. According to Thomas, "Most memory testers have fixed data and address registers so the test programmer is limited in what he can use. But with the Avantage series we employ a 25-MHz pattern processor with eight 24-bit registers that can be used for either data or address information." Signal skew is held to ±500 ps at the test head by automatic calibration facilities.

Each of the three testers in the series is controlled by a Digital Equipment Corp. LSI-11/23 microcomputer with 256-K bytes of memory. They are programmed with the procedural high-level Eaton test language, called ETL, which runs under the DEC RT-11 real-time disk operating system.

The model 200 tests random-access memories up to 16 Mb in size (as they become available), read-only memories up to 256-K, and a variety of small- and medium-scale-integrated logic parts. It can also test programmable ROMs and erasable PROMs. Intended for incoming test applications, the 200 comes with a Winchester disk drive and a line printer and can test four components at a time with two dual test heads. It may also be fitted with a third test head so that the user can do engineering, quality assurance, or other short tests without having to remove the part handlers from the parallel test heads.

At the low end of the series is the model 100. Designed for wafer probing and final-test applications, it interfaces with laser systems for switching in redundant rows or columns of cells in RAMs.



The model 300 is the engineering version of the series. It includes a color cathode-ray-tube terminal and a software package for generating multicolor shmoo plots, timing-analysis displays, histograms, and graphics for other engineering utilities.

Deliveries of all three testers will begin in March 1983. The 100 is priced at $140,000, the 200 at $200,000, and the 300 at $275,000.

Eaton Semiconductor Equipment Operation, Test Systems Division, 655 River Oaks Parkway, San Jose, Calif. 95134. Phone (408) 942-1555 [351]

6800, 68000 families get low-cost development tools

The HDS-200 microcomputer emulator-analyzer, when linked with an EXORset, EXORmacs, or EXORcisor software-development system, provides a complete hardware-software development system for the Motorola 6804, 6805, and 146805 families of microcomputers. It has a control station containing the functional circuitry for complete emulation and a separate emulator module that matches the internal microcomputer and memory capacity of the particular chip it will emulate.

Some of its features include real-time emulation, 16 programmed breakpoints, prioritized breakpoints, and a line-by-line assembly and disassembly capability. The control station sells for $1,950 each in lots of one to five, and the emulators go for $2,000 each in like quantities. They are available immediately.

Working with its host EXORmacs development system, the HDS-400, a microprocessor hardware development system, provides real-time 10-MHz no-wait-state emulation for the 16-bit 68000 microprocessor. The user can edit and assemble his program using the software-development capabilities of EXORmacs and then download the resulting object file into the 400 for integrating his hardware and software components.

The 400 consists of a four-slot chassis with a 30-A power supply, a work-station control module, and a 68000 emulator as well as symbolic debugging software and a link to the EXORmacs. Available in 60 days, the 400 sells for $6,000 and the 68000 emulator module, another $4,000.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 244-5768 [353]

20-MHz logic analyzer handles 32 channels

A 20-MHz logic-analyzer development system comes complete with 36 channels, two data qualifiers, four clock qualifiers, and two external inputs. The instrument has a logic-

state analyzing function for self-contained microprocessor analysis and a logic-timing analysis function for evaluation of microprocessor peripheral operation.

A map-display format is also available, as are personality modules for the more popular microprocessors. These modules adapt the 3620 to the characteristics of a specific microprocessor as a dedicated logic analyzer. With the personality probe, it is also possible to display the data in assembler mnemonics.

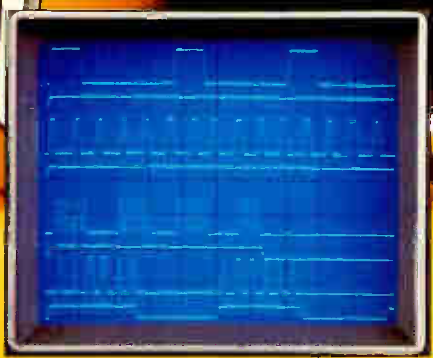
The 3620 also features a glitch-capture mode, video output, 1-K byte of memory, a sequential trigger, a memory comparison feature, clock delay, and selectable threshold levels. With the probes, the instrument sells for $7,995 and is available 45

Catch & Compare

Digital storage on the PM 3310 combines easy signal capture with sophisticated signal comparison and analysis. Here's how:

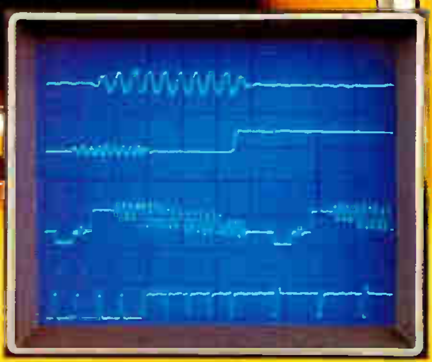
- 50 MHz clock rate (fastest yet in a portable scope) retains signal detail for fast, single-shot phenomena.
- 4 memories and 2 channels give multiple display modes over a 60 MHz bandwidth.
- A trigger delay of −9 to + 9999 divisions that effectively stretches memory capacity and provides pre-/post-triggering.
- IEEE/IEC-Bus for systems operation and further signal analysis.
- Multiple single-shot mode for capture of successive transients.
- Plus TV triggering, X-t recorder type roll mode and X-Y recorder output.

PM 3310 sets a new standard in digital storage



Two input channels and four memories allow eight traces to be displayed for detailed analysis and comparison. The in-house developed Profiled Peristaltic Charge Coupled Device (P^2 CCD) allows 50 MHz data to be sampled in a cost-effective manner.

Easy operation is another big PM 3310 plus. Parameter settings, for example, are stored with the relevant signals and can be recalled for display.



An accurate −9 to + 9999 division trigger delay extends the basic benefits of A/D conversion. This facility is used here to pick out a particular TV colour burst.

Philips Industries, TQ III-4-62.
Eindhoven, The Netherlands.

From Philips, of course

PHILIPS Test & Measuring Instruments

PHILIPS

Circle 159 on reader service card

New products

days after receipt of order.

Soltec Corp., 11684 Pendleton St., Sun Valley, Calif. 91352. Phone (800) 423-2344 [354]

Digitizer makes 7000-series scopes fully programmable

The 7D20 programmable digitizer plug-in upgrade gives the Tektronix 7000 series oscilloscopes digital capabilities as well as full IEEE-488–bus compatibility. The unit is fully programmable and fits into any of the Tektronix 7000 mainframes,

except the 7104 1-GHz scope.

A 40-Mb/s sampling rate enables the 7D20 to capture and store single-shot and transient events up to 10 MHz, and its equivalent-time digitizing (the firm's process by which repetitive waveforms are quickly reconstructed) enables it to capture and store repetitive events up to 70 MHz. Beyond basic waveform acquisition, the unit offers signal averaging for reducing uncorrelated noise, envelope displays for comparing dynamic characteristics of changing signals, and pre- and post-triggering during equivalent-time digitizing. It also has 1,024 points of storage for each of six waveforms plus a reference waveform and cursors for accurate and repeatable time and amplitude measurements.

Up to six front-panel setups can be saved and recalled from a front-panel switch. Each setting is stored in a nonvolatile, electrically alterable read-only memory. The 7D20 is priced at $7,750 and can be delivered in eight weeks.

Tektronix Inc., P. O. Box 500, Beaverton, Ore. 97077. Phone (800) 547-1845 [355]

Our new CMOS 32K Static ROM may soon make NMOS a memory.

RCA announces a new family of high-speed, high density CMOS ROMs that are pin-for-pin compatible with NMOS EPROMs and ROMs.

Now you can get the best of both worlds in your static ROMs: Fast access times plus CMOS power saving and noise immunity benefits.

Our new CDM5332 and CDM5333 are 32,768-bit mask-programmable CMOS ROMs, organized as 4096-words x 8-bits.

The features include:

- -40° C to +85° C temperature operating range.
- Fast access time: 300 ns max at 5V ± 10% from address.
- Quiescent device current of 100 μA.
- Two programmable chip-select inputs for memory expansion.
- Choice of two industry-standard pinouts for compatibility with a very wide range of devices.

And our prices are as impressive as our performance: only $8.86.* Extra Value version is offered ($10.63)* with 160 hour burn-in and can be ordered by adding an "X" after the suffix.

You can use these devices in any general-purpose 8-bit microprocessor system including, of course, the RCA 1800-series and the new RCA 6805-series: The broadest, most powerful line of CMOS micros, memories, I/Os, peripherals and support devices in the industry.

Now, there's only one name to remember in ROMs: RCA, the people who invented CMOS.

For more information, contact any RCA Solid State sales office or appointed distributor.

Or call (800) 526-2177.

*U.S. optional distributor resale, 1000+ price.

RCA Solid State headquarters Somerville, NJ. Brussels. Paris London Hamburg Sao Paulo Hong Kong

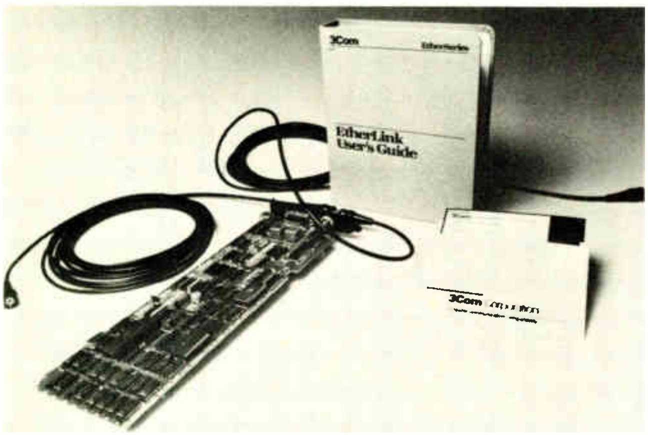
Circle 161 on reader service card

Communications

Ethernet comes to desktop stations

Net links IBM microcomputers, offers shared hard-disk drive and printers, electronic mail

A series of hardware and software products has been introduced to link IBM Personal Computers to an Ethernet local network and to permit users of the network to share printers and hard-disk drives, as well as add electronic-mail facilities. 3COM Corp., manufacturer of the series [*Electronics*, Oct. 6, p. 190], plans to offer hardware and software tailored to other personal computers from such vendors as Apple Inc. and Digital Equipment Corp. soon.



Each microcomputer is attached to the network using a $950 package called EtherLink, which includes a card that plugs into an expansion slot in the IBM unit and a floppy disk with communications software. An IBM microcomputer running the program (it cannot run other programs at the same time) can share its disk files and attached printer with other network stations, or an EtherShare Network Server can be attached to the net to provide all network stations with access to one or two Winchester drives and spooled printer services. The 3COM EtherShare unit, which has a 10-MHz 8086 central processing unit, 512-K bytes of parity-checked random-access memory, and 10 megabytes (expandable to 40 megabytes) of hard-disk storage, costs $11,500 and can run the EtherMail electronic-mail software in addition to the EtherPrint spooling printer package.

Thin cable. Without repeaters, the network can support up to 100 computers and can be up to 300 m long using thin coaxial cable (RG58A/U 50-Ω PVC type), up to 500 m long using RG213/U-type cable, or 1,000 m long if 3COM transceivers are used at each station in addition to 213/U cable. Repeaters can connect cable segments up to 2.5 km apart and allow up to 1,000 computers to be linked to one network. Communication is at 10 Mb/s.

When a network is equipped with the EtherShare hardware, users can share not only the disk storage (the drive has an 85-ms average access time), but the data stored there. Disk files are transferred in a transparent fashion using the copy command of the MS-DOS operating system employed by the communications system. Users who wish to restrict access to files can declare them private, in which case they are protected by passwords. Public data files are open to all users and can be accessed concurrently.

Files on the EtherShare disks can be backed up by EtherShare's floppy-disk drive; a cartridge tape drive is also available for this purpose. It copies up to 17 megabytes on each cartridge.

When it runs the EtherMail package, EtherShare acts as a central post office and controls the reception and distribution of messages. The software is composed of two modules, one of which runs on EtherShare; the other runs on the IBM Personal Computers on the net. Its facilities permit users to send, receive, display, compose, reply to, or forward messages, which can even have attachments such as a specified MS-DOS file. Distribution lists may be used if desired.

The EtherMail software, supplied on floppy disk, and a user manual, is priced at $1,500. The EtherPrint package is $750. Volume shipments of the series of products are scheduled for December and will be within six weeks of receipt of order.

3COM Corp., 1390 Shorebird Way, Mountain View, Calif. 94043. Phone (415) 961-9602 [401]

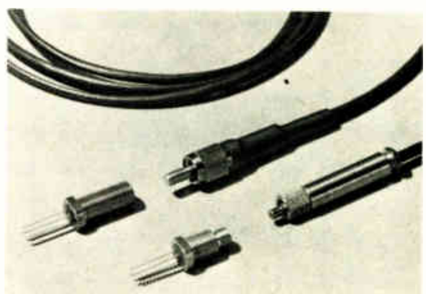
40-Mb/s fiber-optic equipment bows

Finding local-network and telecommunications applications spurring growth in its component product lines, Hewlett-Packard is expanding its offerings of fiber-optic receivers, transmitters, and cables on several fronts: for tougher environments, longer links, faster data transfers, and less-expensive systems.

A new receiver, HFBR-2203, along with transmitter -1201, extends digital transmission to 40-Mb/s rates over 800-m links using the firm's HFBR-3000 cables. Typical links can extend to 2 km, and the analog bandwidth of 25 MHz suits the pair for video transmissions.

Those components, built to HP's own connector standards, are complemented with an equivalent pair of devices meeting the subminiature type A connector dimensions: the HFBR-2204 receiver and -1202 transmitter.

For either packaging style, the



Switch to the future with Cutler-Hammer miniatures.

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Eaton Corporation, Aerospace/Commercial Controls Division, 4201 N. 27th St., Milwaukee, WI 53216.

EATON Electrical/Electronic Control

Circle 163 on reader service card

receiver costs $39 in lots of 1,000, and the transmitter goes for $29 in those quantities. HFBR-3000 simplex glass cable costs $2 a meter for lengths up to 10 km; $4.50 buys a meter of duplex -3100 cable.

In addition, HP is adding SMA connector versions to an existing product line. The HFBR-2202 receiver works with the -1202 transmitter in 5-Mb/s links up to 1,000 m long. The -2202 receiver costs $36 in 1,000s. Mounting hardware for the pair costs $1.55 in like quantities.

For lower-cost plastic cable systems, the company is offering the HFBR-2501 receiver and -1501 transmitter, which can support links at 5 Mb/s up to 10 m, and the 2502/1502 pair, which handles 1-Mb/s data transfers over a 22-m link. In 10,000-piece lots, the 1501 and 1502 cost $5.90 and $6.30, respectively; the 2501 and 2502 are priced at $7.10 and $6.45.

Also, evaluation kits (HFBR-0500) containing the 1501/2501 pair and 5 ms of simplex plastic cable are available for $27.50 each. All the offerings are available from stock.

Hewlett-Packard Co., 1802 Embarcadero Rd., Palo Alto, Calif., 94304 [402]

Modem on a board eats up just 26 in.^{2}

Housed on one 100-by-160-mm printed-circuit board (less than 26 in.^{2}), the R24LL is a low-cost, downsized 2,400-b/s modem that operates on leased lines or the dial-up, switched network. The R24LL is a serial synchronous differential phase-shift–keying modem intended to be designed as an integral part of data systems, box or rack-mountable modems, statistical multiplexers, error correctors, and terminals.

It can operate in either full- or half-duplex modes. The R24LL is compatible with Bell 201 and International Consultative Committee for Telegraphy and Telephony recommendations V.26 A/B and V.26 bis for four-wire leased and switched telephone networks, respectively. The modem also contains a CCITT-compatible V.27 scrambler function and a data-terminal equipment interface. Typically it consumes less than 3 W at +5 and ±12 V.

The unit includes answer-back tone generation, clear-to-send delay options, and an option for rapid resynchronization in multipoint applications. The R24LL offers transmitter differential phase modulation and receiver coherent phase detection. It also has diagnostic outputs for eye-pattern generation and data-quality monitoring.

The R24LL is priced at under $250 in large quantities; interface circuitry generally costs under $50. Samples are available now, with production quantities scheduled for January deliveries.

Rockwell International, Electronic Devices Division, 4311 Jamboree Rd., P. O. Box C, Newport Beach, Calif. 92660. Phone (714) 833-4460 [403]

Miniature filter banks meet defense needs

Designed for channelized receivers and fast-hop synthesizers, a line of surface-acoustic-wave filter banks are suitable for defense-system applications. A typical filter bank exhibits 1.3-MHz 3-dB bandwidths on 5-MHz centers with 20-dB unmatched insertion loss.

These filters feature the high temperature stability of their quartz substrates, greater than 60-dB out-of-band rejection, and better than 50-dB time-domain spurious suppression. The firm claims that packaging an entire filter bank with each filter in a TO-8 can result in a reliable miniaturized multichannel module.

SAW filter and module designs in the very high- and ultrahigh-frequency ranges feature a variety of bandwidths, shape factors, and channels. Pricing varies according to the frequency, the number of filters in a bank, and their characteristics, but averages about $200 a filter.

Sawtek Inc., 2541 Shader Rd., P. 0. Box 7756, Orlando, Fla. Phone (305) 299-4441 [404]

Semiconductors

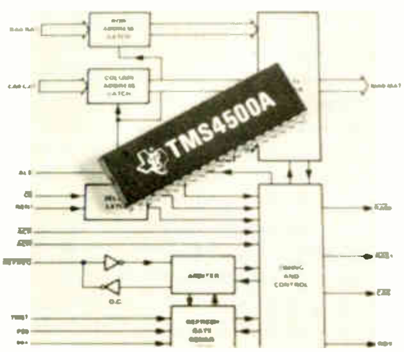
Chip controls 32 dynamic RAMs

MOS controller for dynamic random-access memory cuts number of ICs needed for job

Though a number of bipolar devices have appeared in the last few years to integrate the refresh and control logic that interfaces microprocessors with dynamic random-access memories, generally a few small-scale integrated circuits are still needed to complete any given design.

With an eye on low-cost, medium-performance applications, Texas Instruments Inc. has come up with a single-chip dynamic-RAM controller that operates using signals already present in a microprocessor-based system. The controller runs synchronously with the system to avoid refresh arbitration delays. TI's MOS operation in Houston is using its scaled n-channel MOS to fabricate the TMS4500A controller. The chip, without outside help, makes dynamic RAMs appear as static parts to the microprocessor.

The 40-pin controller is made up of six basic building blocks: address and select input latches, an 8-bit refresh counter, a memory-address output multiplexer, a refresh rate generator, a bus-contention arbiter, and a timing and control segment. The scaled MOS process and 2.5-μm design rules permit TI to pack these interface blocks onto a 14,000-mil^2 chip. The manufacturer estimates that the controller replaces from 10 to 15 small- and medium-scale integrated circuits.



Available for delivery now, the 4500A is priced at $18.45 each in 100-piece quantities. The chip operates from a 5-V supply and has a continuous power dissipation of 770 mW. In a standard dual in-line plastic package, it operates at temperatures from 0° to 70°C.

Different RAMs. The device can be used with several types of dynamic RAMs, including those with 16-K-by-1-, 64-K-by-1-, and 16-K-by-4-bit organizations. Future 64-K-by-4-bit devices can be handled, but the 40-pin limitation prevents the 4500A's use with 256-K-by-1-bit RAMs. The interface is designed to accommodate the 68000, 8085, 8086, Z80, Z8000, and TI's own 9900 and 99000 microprocessors.

To match RAM speeds to a given processor, the device provides strap-selectable wait-state generation. It can also by synchronized or interleaved with a number of other memory controllers. Three-state outputs make multiple-port configurations possible.

The 4500A can directly address and drive up to 256-K bytes of memory, and through an on-chip 16-bit multiplexer that provides row, column, and refresh addresses, a single chip can handle up to 32 dynamic RAMs. The controller contains refresh and access arbitration circuitry that resolves conflicts between memory-access requests and refresh cycles. The chip can also provide fail-safe refreshing during direct-memory accesses and times when a processor is in a hold state or being reset.

Texas Instruments Inc., Literature Response Center (SC-365), P. O. Box 202129, Dallas, Texas 75220 [411]

Gate arrays put linear and digital activity on one chip

Performing high-complexity digital and high-performance linear functions on the same chip, nine Digilin universal logic arrays range in complexity from 100 gates (with 356 active and 531 passive components) to 730 gates (with 1,644 active and 2,660 passive components) and are available in packages with 14 to 40 pins. In addition to providing the interface capabilities available from traditional ULAs, the Digilin arrays can also be configured as voltage regulators, references, comparators, amplifiers, sample-and-hold circuits, and other such devices.

The arrays contain standard and predefined support functions commonly used in applications requiring digital signal conditioning of analog circuits. Included are high-gain, low-current transistors, 100-mA drive transistors, 100-Ω-to-1-MΩ resistors, on-chip bandgap references, series and shunt regulators, and shaping capacitors.

Development charges for Digilin arrays range from $8,000 to $40,000, depending on size and production. Production unit prices range from $5 to $14 each in lots of 10,000. Delivery of engineering samples takes 18 to 20 weeks; production quantities can be delivered 8 to 10 weeks after prototypes are approved.

Ferranti Semiconductors, 87 Modular Ave., Commack, N. Y. 11725. Phone (516) 543-0200 [413]

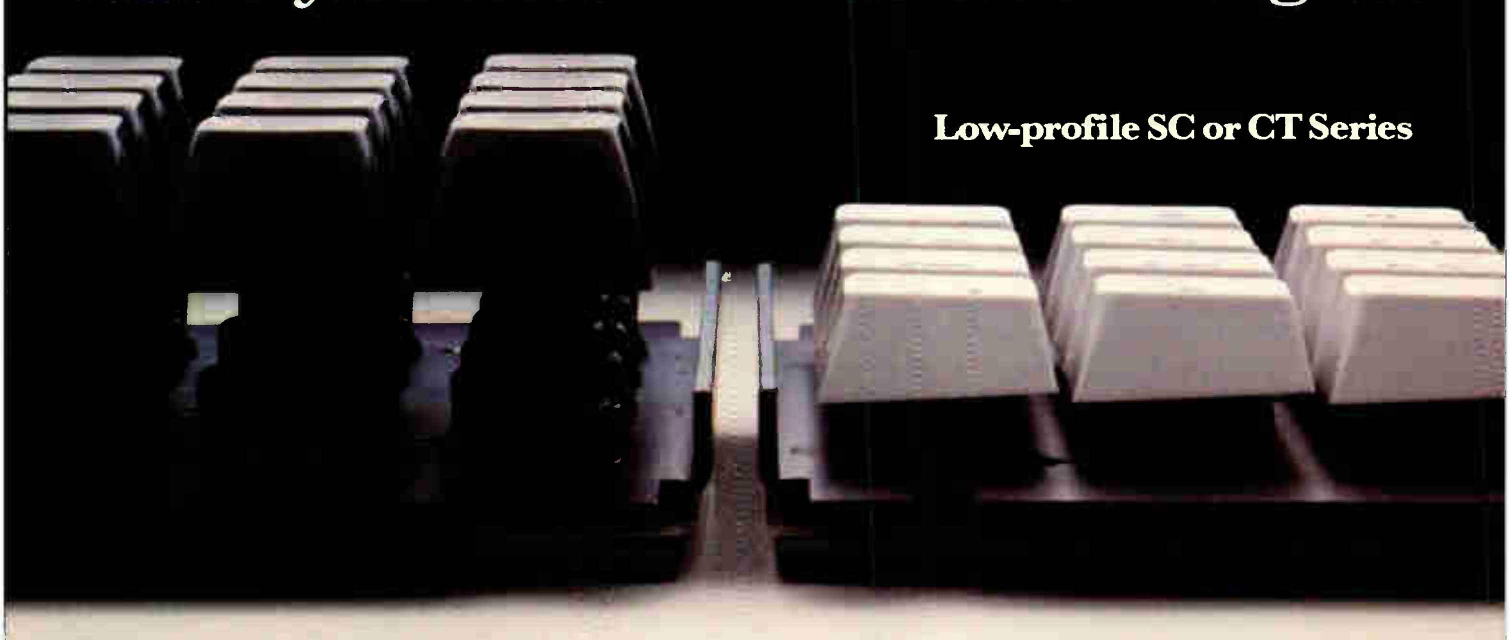
PAL is designed to make copying more difficult

Complementing its series 20 of programmable array logic, the series 24 provides two additional inputs and two extra outputs, allowing more complex functions in a single package. The family's members are housed in a 24-pin dual in-line package that is 300 mils wide.

In addition to providing more logic functions per chip, the 24 pins make possible logic functions previously unavailable in 20-pin packages. Such additions include 8-bit parallel-in, parallel-out counters and shift registers, 16-line-to-1-line multiplexers, dual 8-line-to-1-line multiplexers, and quad 4-line-to-1-line multiplexers.

The family lets a system engineer

Our keyboards have reached new heights.



Introducing full-travel low-profile keyboards from MICRO SWITCH. Low-profile keyboards that don't compromise on human factors, selection, or performance. They allow you to meet European ergonomic standards, even when they're mounted up to a nine degree angle. And they're available in capacitance and contact membrane versions. Now those are new heights.

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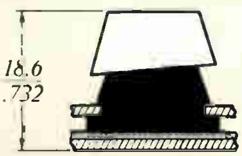

Actual size cutaway of low-profile actuator module

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Circle 167 on reader service card

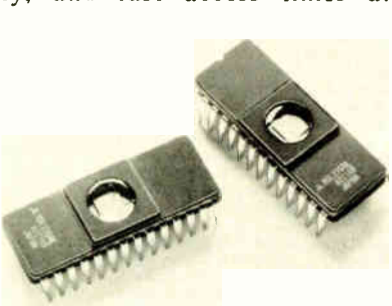
design a chip by blowing fusible links to configure AND and OR gates that will perform the desired logic function. The entire PAL family is programmed on conventional programmable read-only memory programmers using the appropriate personality cards and socket adapters. Once the PAL is programmed and verified, two extra fuses may be blown. This feature gives the user a proprietary circuit that is difficult for others to copy.

Series 24 is composed of the PAL20L10 combinatorial logic device and the DMPAL20X10, DMPAL20X8, and DMPAL20X4 sequential logic devices. Any one of these medium-sized PAL devices can replace from five to 15 small- and medium-scale integrated logic devices. The units are available now in plastic and ceramic packages ranging in price from $13 to $29 each in lots of 100.

National Semiconductor, 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 737-5000 [414]

64-K E-PROM drains only 150 mA from 5-V supply

Organized as 8-K by 8 bits and constructed in n-channel double–poly-silicon-gate technology, the M5L2764K erasable programmable read-only memory is suited to microprocessor programming applications where rapid turnaround, high capacity, and fast access times are



required. The 64-K device is packaged in the industry-standard 28-pin dual in-line package and is interchangeable with the 2764 E-PROM from Intel.

In the active mode, the part requires a maximum of 150 mA from its single 5-V power supply and in standby mode, the chip saves power, drawing a current of only 35 mA, typically. Its inputs and outputs are TTL-compatible in both read and program modes, and a three-state output buffer simplifies interfacing. The device also furnishes output- and chip-enable control lines.

The M5L2764K comes in versions with 200-, 250-, and 300-ns access times and are priced at $24, $18, and $16.50 each, respectively, in 100-piece quantities. The devices, which operate over a 0° to 70°C range, are available now from stock.

Mitsubishi Electronics America Inc., 1230 Oakmead Prkwy., Suite 206, Sunnyvale, Calif. 94086. Phone (408) 730-5900 [415]

CRT controller gives choice of two screen formats

Providing the flexibility of two selectable screen formats with the economy of mask-programmed read-only-memory–based registers, the MC6835 cathode-ray-tube controller has alphanumeric, semigraphic, and graphic capabilities. There is also a programmable cursor register for control of cursor position. A screen-refresh memory may be multiplexed between the controller and the microprocessor, thereby limiting the need for line buffers or external direct-memory-access devices.

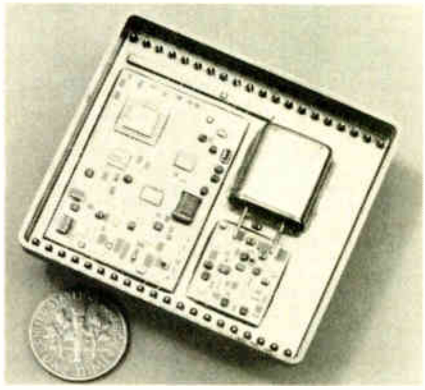
Additional features include mask programmable interlace or noninterlace modes, 14-bit addressing that allows up to 16-K bytes of refresh memory for use in character or semigraphic displays, and a 5-bit row addressing that allows up to 32 scan-line character blocks. The MC6835 has refresh addresses, provided during retrace, that allow row addresses to refresh dynamic random-access memories.

The controller is also pin-compatible with the MC6845, which may be used as a prototype part to emulate the MC6835. The MC6835 is available now and priced at $5.95 in orders of 1,000 pieces or more.

Motorola Inc., MOS Microprocessor Division, 3501 Ed Bluestein Blvd., Austin, Texas 78721. Phone (512) 928-6863 [416]

Quartz-crystal oscillator is digitally compensated

Using digital techniques to compensate for temperature-based frequency drift, the DCXO quartz-crystal oscillator is designed for portable or remotely located equipment requiring low power and high stability.



The DCXOs are a practical alternative to oscillators in ovens. Their advantages include a power consumption less than 250 mW, a warm-up time under 250 ms, and a small volume of only 1 in.^{3}

Available design options include a choice of output logic (TTL, complementary-MOS, or emitter-coupled logic); choice of supply voltage; package options; stability optimized for specified temperature ranges; and digital frequency adjustment for aging correction or for synchronization with the system.

The oscillator can generate frequencies between 1 and 30 MHz, with frequency stability of ±1.0 ppm over a temperature range of −45° to +85°C and ±0.3 ppm in the range of 0° to 70°C. Single unit pricing for the DCXO is $900 with delivery eight weeks after receipt of order. Customized units are available to meet the requirements of specific applications.

Hughes Aircraft Co., Solid State Products Division, 500 Superior Ave., Newport Beach, Calif. 92663. Phone (714) 759-2430 [418]

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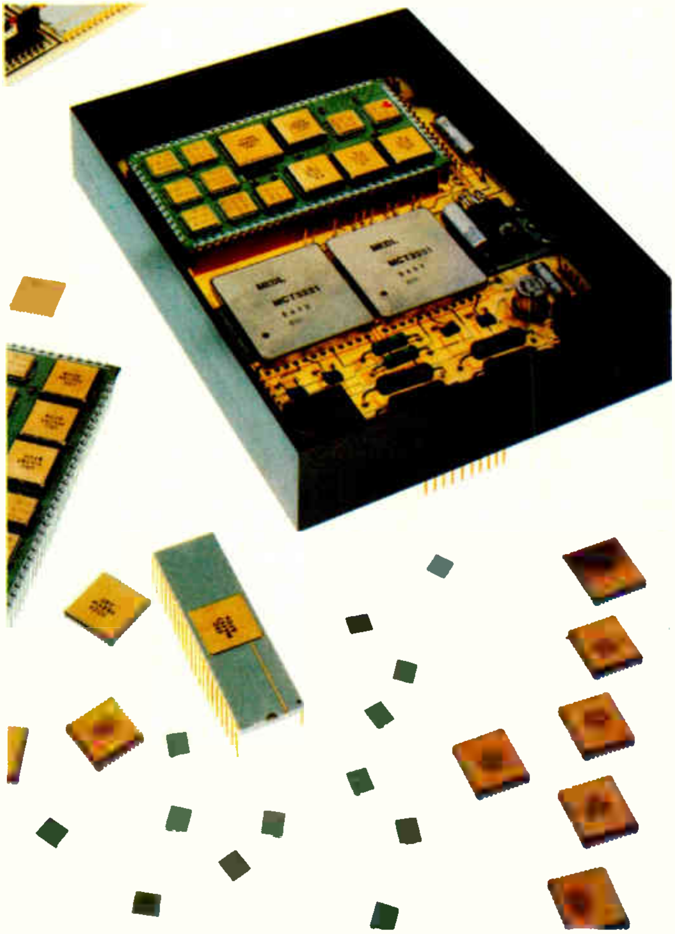

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Marconi
Electronic Devices

Marconi Electronic Devices Limited, Doddington Road, Lincoln LN6 0LF, England. Telephone: 0522 688121. Telex: 56380.

Power supplies

280-W supply is simple, rugged

Unit operating on principle of ferroresonant stabilization gains power in same volume

Joining the PRM line of ferroresonant-stabilized power supplies, a line that ranges in capacity from 60 to 1,000 W, is a series of 280-W units housed in approximately the same size packages as are the popular 180-W models. Thanks to improved magnetic design and high-density filter capacitors, Kepco's engineers were able to up the available power by more than 55% without changing package dimensions appreciably. The open- or closed-frame power supplies measure 10.9 by 5 by 6.9 in.—the AA package size—distinguishing them from the 180-W model's A-size package, which is ⅟₁₆ in. shorter on the 10.9-in. side.

Though the increased power density of the 280-W PRM models still does not compete with high-frequency designs (0.72 W/in.^{3} versus 1.1 W/in.^{3}), the inherent reliability and simplicity of the ferroresonant approach to voltage stabilization produces, the company claims, a combination of low cost, long life, high efficiency, and safety. For example, the 280-W model boasts an efficiency in excess of 75% and a mean time before failure of over 150,000 h.

The 280-W models feature line regulation within 1% and a typical load effect of under 5% (at 50% to 100% of load). The maximum ripple is claimed to be 300 mV root mean square, 400 mV rms maximum on models with 48- and 120-V ratings.

Like their brethren in the PRM family, the 280-W units have no overvoltage risk and thus no overvoltage protection. Automatic current limiting between 125% and 150% of the rated load current is designed in a rectangular rather than a foldback pattern to facilitate driving nonlinear or high-surge-current loads.

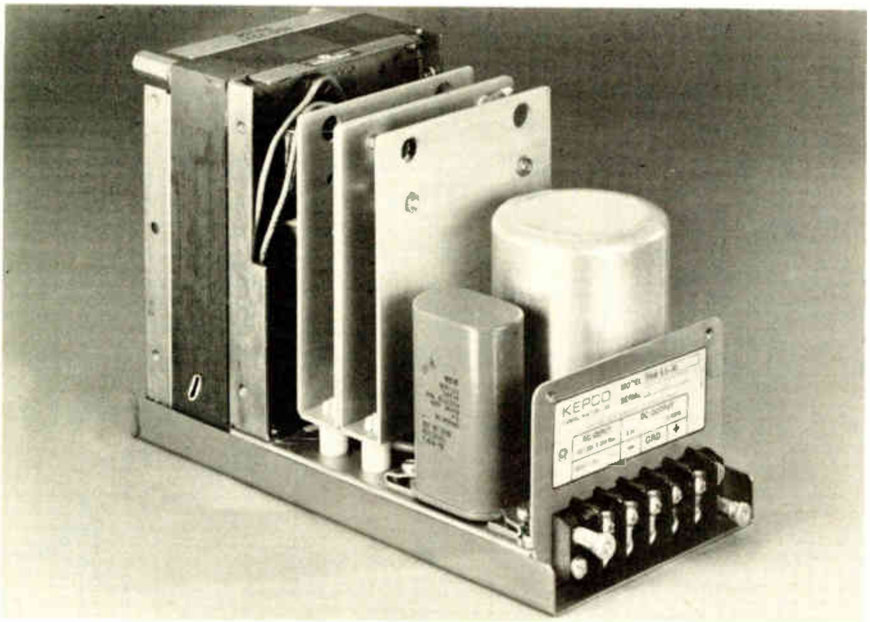
The line is intended for single-phase 60-Hz operation requiring 115 V ac ±15 V at approximately 3.6 A. All models function at 90% of rated load capacity to brownout source levels as low as 75% of nominal. The supplies can operate at temperatures from −20 to +55°C and are capable of full output at +55°C. Because cooling is by convection, no external heat sink is required.

The ferroresonant voltage-stabilizer principle, on which all the PRM supplies operate, depends on the saturation of a portion of the transformer's iron by the use of a resonating capacitor. The square waveform in the tank winding is isolated from the primary winding by a special magnetic shunt. This isolation insulates the unit from line-borne noise and spikes. The energy stored in the tank provides sufficient hold-up to bridge a lost cycle in the power main; in case of an overload, it will collapse.

Saturation. The supply consists of a transformer, rectifier, and filter, plus the resonating capacitor. It is designed without a series regulator or the need for crowbar protection and switches or oscillators, which can produce noise. The output voltage is independent of delicate control settings or diode references and is established by magnetic-flux saturation in an iron lamination, a setup that suits the PRM supplies to rugged applications such as automatically controlled machinery and medical equipment.

The 280-W model is priced at only $259 in orders of 1 to 50 ($279 for 8.5-V, 30-A models). All PRM power supplies comply with Underwriters Laboratories' specifications. The 280-W line comprises seven models ranging from 8.5 V at 30 A to 120 V at 2.4 A.

Kepco Inc., 131-38 Sanford Ave., Flushing, N.Y. 11352. Phone (212) 461-7000 [381]



Uninterruptible power supply responds within 16 ms

Rated at 250 W continuously and 500 W for surges, the 1407 frequency-stable uninterruptible ac power system is designed to protect devices like small computers, point-of-sale terminals, process controllers, private branch exchanges, and security systems from unexpected power interruptions. The 1407 has a waveshape that is stable within 0.15 Hz, a 2:1 output-surge capability, and is 80% efficient.

In addition, the supply can sense and respond to a power lapse within 16 ms. The standard model provides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a single-phase output of 115 V, 60 Hz, and its output waveform is compatible with almost any load. Separate versions of the supply are available for use with either 24- or 12-V batteries.

In small quantities, the model 1407 sells for $610 and is available from stock.

Wilmore Electronics Co., P. O. Box 1329, Hillsborough, N. C. 27278. Phone (919) 732-9351 [382]

High-voltage power supply has adjustable current, voltage

Designed as a general-purpose high-voltage power supply for photomultipliers, proportional tubes and chambers, and other electron multipliers, the model 2415 can supply currents and voltages up to 2.5 mA and ±3.5 kV or 1 mA and ±7 kV. Both current and voltage can be manually or remotely set and read.

Programming and monitoring are accomplished through the front panel or an IEEE-583 standard control. Because of their modular format, several 2415s can be used and controlled side by side in a single housing. The supply can also be used without the housing if powered from +6- or ±24-V supplies.

The supply's output ripple is less than 50 mV root mean square, and its output voltage is regulated to within 0.014% of the range chosen. The 2415 is short-circuit–protected and indicates current overloads through a light-emitting diode.

Available from stock, the 2415 sells for $1,050 each.

LeCroy Research Systems Corp., 700 South Main St., Spring Valley, N. Y. 10977. Phone (914) 425-2000 [384]

Switching power supplies can be customized

The ES series of high-speed switching power supplies offers a wide input range between 90 and 132 V ac or 180 and 260 V ac and has outputs of 25, 50, and 100 W at 5, 12, 15, and 24 V. The supplies can be customized to suit particular requirements, and their ranges can be selected through terminals.

The supplies switch at 100 kHz and are 70% efficient. They also include a built-in over-current and -voltage protection scheme, ac- and field-ground terminals, and high reliability. The ES series is designed to meet Federal Communications Commission and Underwriters Laboratories specifications.

The supplies, manufactured by Volgen Electric Co. of Japan, are priced at $84 each for a 50-W unit and $130 each for a 100-W unit, both in lots of 1,000. Delivery is from stock.

KSC Electronics Inc., 543 West Algonquin Rd., Arlington Heights, Ill. 60005. Phone (312) 981-5655 [383]

600-W switcher has multiple outputs

A 600-W multiple-output switching power supply that meets a host of military requirements operates from a power source of 95 to 130 V root mean square or 180 to 250 V rms at 47 to 440 Hz, single phase. A three-phase input configuration is also available. Specifically, the model M4100 meets MIL-810-C standards for shock, vibration, and humidity as well as MIL-461, MIL-T-28200, MIL-454, and MIL-Q-9858.

The unit's input surge current is limited to 60 A through the use of soft-start circuitry. Its efficiency is 80% maximum when operating above 10% of its 600-W rating. In its standard configuration, the M4100 will supply 5 V dc at 60 A as a primary output and ±15 V dc at 10 A as secondary outputs. All outputs may be adjusted at the factory by 10%. The M4100's operating temperature is specified at 0° to 71°C with no derating at 71°C.

Load and line regulation is ±0.2% for all excursions from nominal, for all combinations of load and line within the specified limits. The maximum output noise, ripple, and spikes is 100 mV peak to peak with a maximum temperature coefficient of ±0.03%/°C. The M4100 is priced at $3,250 each with delivery from stock to eight weeks.

Ceag Electric Corp., Power Supply Division, 1324 Motor Pkwy., Hauppauge, N. Y. 11788. Phone (516) 582-4422 [385]

Line conditioner is 97% efficient

Claiming 97% efficiency, the DLCA-8 and -16 automatic line conditioners block radio-frequency noise and voltage surges while monitoring and maintaining proper line voltage even with brownouts down to 80 V on 115-V lines or down to 160 V on 220-V cables.

The company claims the conditioners are smaller, lighter, more effective, and less expensive replacements for older designs using either ferroresonant transformer voltage regulators or tap-switching regulators with an isolation transformer. Using a tap-switched 20% boost-buck autotransformer, the units can deliver the high surge currents necessary for starting large disk-memory systems and still not overload for the average power requirements.

The DLCA-8 provides an 8-A regulated output at 115 V within 10% and sells for $535 each; the -16 provides 16 A and goes for $795 each. The 8-A, 1-kV unit weighs 15 lb and measures 5 by 8 by 11 in., while the 16-A, 2-kV unit weighs 25 lb and measures 5 by 10 by 14 in.

The 1- and 2-kV units are also available at 220 V. Delivery on 115-V supplies is from stock. The 220-V models can be shipped 8 weeks after receipt of order.

Displex Inc., 79 Hazel St., Glen Cove, N. Y. 11542. Phone (516) 671-4400 [386]

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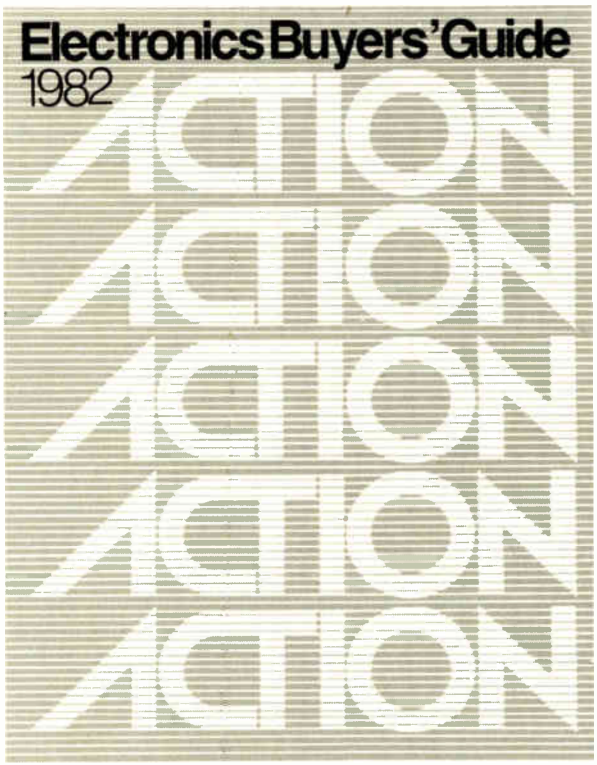

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Products Newsletter

Array processor unburdens host

A 32-bit floating-point array processor that performs 9 million floating operations per second is able to assume many of the decision-making and input/output tasks that traditionally burden a host minicomputer or mainframe computer. Analogic Corp.'s AP500 **can perform a 100-by-100-bit matrix inversion in 649 ms and a 1,024-point complex fast Fourier transform in 4.7 ms.** In a typical system, the host downloads a complete subtask to the AP500, which then operates autonomously, interrupting the host only when summary processing reports have been compiled. The Wakefield, Mass., firm's array processor uses a 12-MHz 68000 processor and comes with 128-K bytes of memory, expandable to 256-K bytes. Pricing with a one-year warranty begins at $25,000.

Unit finds contaminants at 10 parts in 1 billion

Tapping its experience in the water-purification business, O. I. Corp. is targeting a carbon-contaminant measurement system at very large-scale IC manufacturers. The College Station, Texas, company decided to modify one of its laboratory monitors to better suit the semiconductor industry after **discovering that chip makers were using its systems to analyze the carbon content of water for VLSI processing.** O. I.'s VLSI contaminant monitor, priced at $22,500, is capable of measuring carbon concentrations of 10 parts per billion to 50 parts per million, which is considered a critical range for VLSI wafers. The monitor uses a proprietary trace-enrichment trapping technique to detect the low levels of carbon.

C-MOS logic cells boast 4-μm geometries

A library of 4-μm single-level–metal complementary-MOS standard cells has been added to NCR Corp.'s semicustom logic arrays. **Density levels of 1,000, 2,000, and 3,000 equivalent gates are available,** priced at $10, $16, and $18, respectively, each in 10,000-piece lots. Minimum engineering charges of $25,000 are included. NCR's Fort Collins, Colo., Microelectronics division is also planning to introduce next year a scaled-down version of the same 21-cell C-MOS library that will be fabricated with a 3-μm double-level metal process.

Business computer has 8-, 16-bit processors

Japan's largest computer maker, Fujitsu Ltd., will enter the U. S. computer market at Comdex with a personal business computer, the Micro 16S. The machine will have two central processing units—a Z80 and an 8088—allowing it to run both 8- and 16-bit CP/M software. **It will include 128-K bytes of parity-checking random-access memory, expandable to 1 megabyte,** and two floppy-disk drives with 320-K bytes of storage capacity each. The $4,000 computer will be marketed in the U. S. by the Professional Microsystems division, an arm of Fujitsu Microelectronics Inc. in Santa Clara, Calif.

Color graphics added to AWS computers

A work station to be shown at Comdex by Convergent Technologies will add color graphics to the Santa Clara, Calif., firm's low-cost Application Work Station line of computers. Like its black and white cousin, the color-graphics station is built around an 8-MHz 8086 microprocessor. **Its display is generated from three 512-by-512-bit memory planes, with screen resolution of 432 by 319 picture elements.** Prices start at about $5,650 for a system with 256-K bytes of memory and no mass storage.

Career outlook

Steering new course

It has long been a shibboleth of the electrical engineering profession, though perhaps it is becoming outworn in this day of rapid technological growth and cyclical employment patterns, that EEs fresh out of college generally start at higher salaries than their fellow graduates in liberal arts, business, or other disciplines. But the other side of the story is that engineers tend to stay closer to that starting salary longer; the only way up the salary ladder seems to be to leave the engineering life behind and embark on a sales or management track.

For the most part, engineers promoted to a management post are ill-prepared for the move. They generally wind up managing by instinct, a method that is akin to slipping behind the wheel of a car for the first time with preparation limited to watching someone else drive. It can be done, but the trials and the errors could easily prove daunting. True, some large companies offer in-plant training courses in techniques for handling others, but such educational opportunities often are not available for new managers in a small- or medium-sized company. They may enroll in a community college, but that means going to class after work or on weekends.

An option. However, new managers who are not content to rely on their instincts and would like to study the subject beyond taking some books out of the library have another recourse. An organization called the Association for Media-based Continuing Education for Engineers Inc. has made available a videotaped short course for engineers and scientists who have recently entered the managerial ranks or who expect to. The course is an introduction to the five functions of a manager—planning, organizing, staffing, leading, and controlling.

Designed to teach the skills required to manage people and work, the course was produced at the University of Southern California. It consists of six color video cassettes, lecture notes, and a textbook. The author and lecturer is Milton Rosenau, who has done other course work for the AMCEE.

The complete course can be rented for $650 or purchased for $2,600 from the AMCEE, which is at 225 North Ave., N. W., Atlanta, Ga. 30322. Lecture notes may be bought for $14.50 a copy and the texts for $25. In addition, a two-week preview package, comprising one cassette and one copy each of the lecture notes and texts, is available for $95. Only the cassette need be returned.

At first glance, the cost seems high. But many firms have tuition-refund plans. Also, a company might organize a class to take the course and reduce per-capita cost.

Organized in 1976 by 12 engineering colleges and universities with Colorado State University engineering dean Lionel Baldwin as its prime mover, the nonprofit group now numbers 23 in its consortium. Its catalog lists more than 470 offerings in 18 engineering disciplines. Most are on the post-graduate level, but many are so-called short topics, like the course for new managers.

Additionally, there are many full-length one-semester courses. Though AMCEE itself can offer no credits, often an arrangement can be made with the university that prepared the tapes and texts for a particular course. If the 23 colleges have anything in common, it is that they are all active in offering off-campus courses via videotape and television. In fact, the group's Atlanta headquarters—it has five persons on its fulltime staff and five student assistants—is on the campus of the Georgia Institute of Technology.

The cost of the AMCEE's short courses generally are $50 to $75 per cassette per week for rentals, and $250 to $300 for purchase. As Gail L. Reed, assistant director of the association, points out, "The courses aren't designed for home study by one person—they're too expensive for that. But they are extremely cost-effective for in-plant training because we charge a flat rate. In fact, many of our clients are in industry." **-Howard Wolff**

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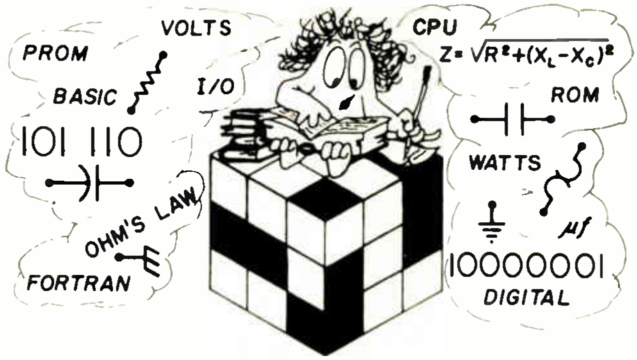

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