TI'S ANSWER TO THE RISING NEED FOR FASTER VLSI: ExCL/73

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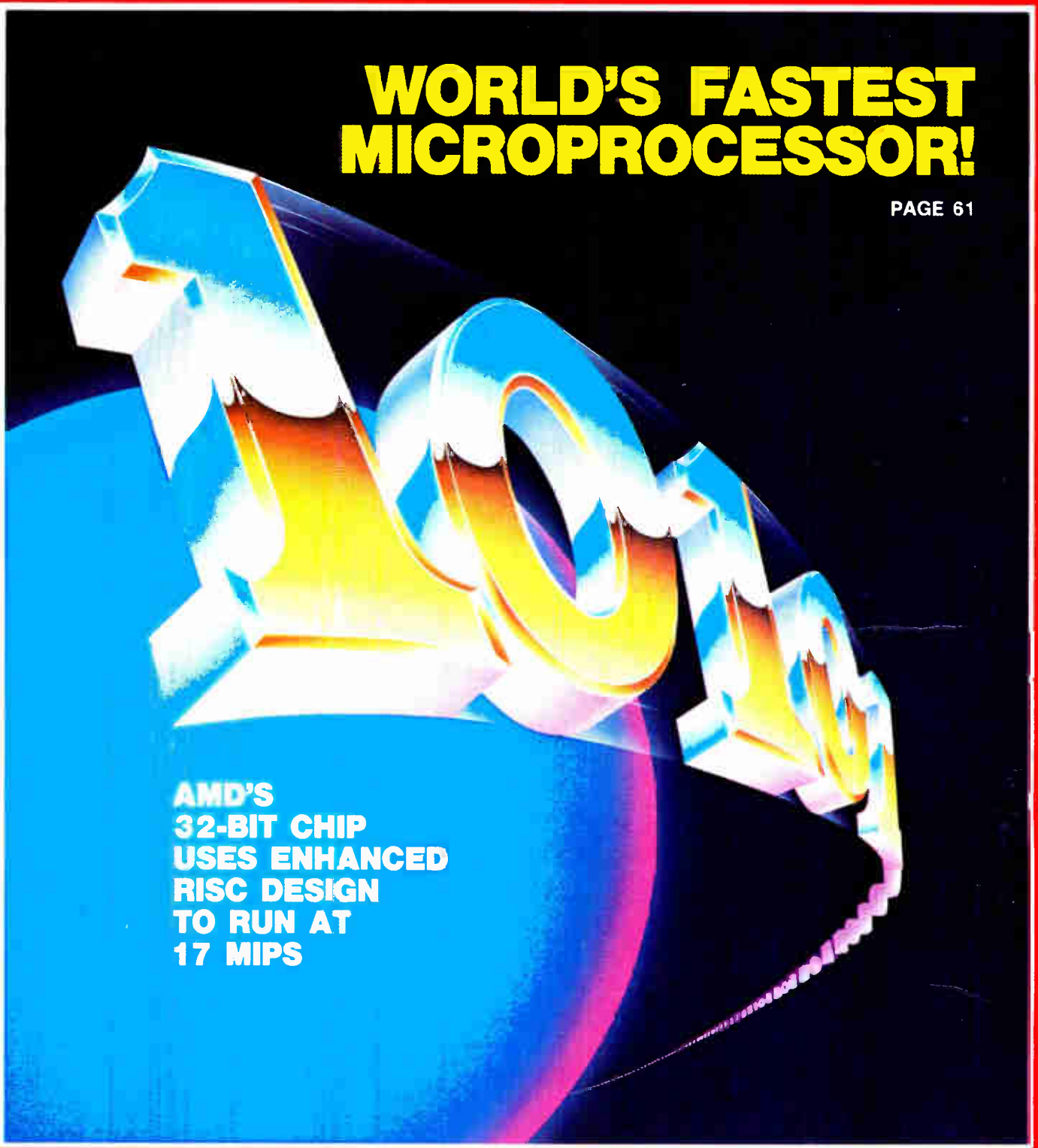
A McGRAW-HILL PUBLICATION SIX DOLLARS MARCH 19, 1987

Electronics

WORLD'S FASTEST MICROPROCESSOR!

PAGE 61



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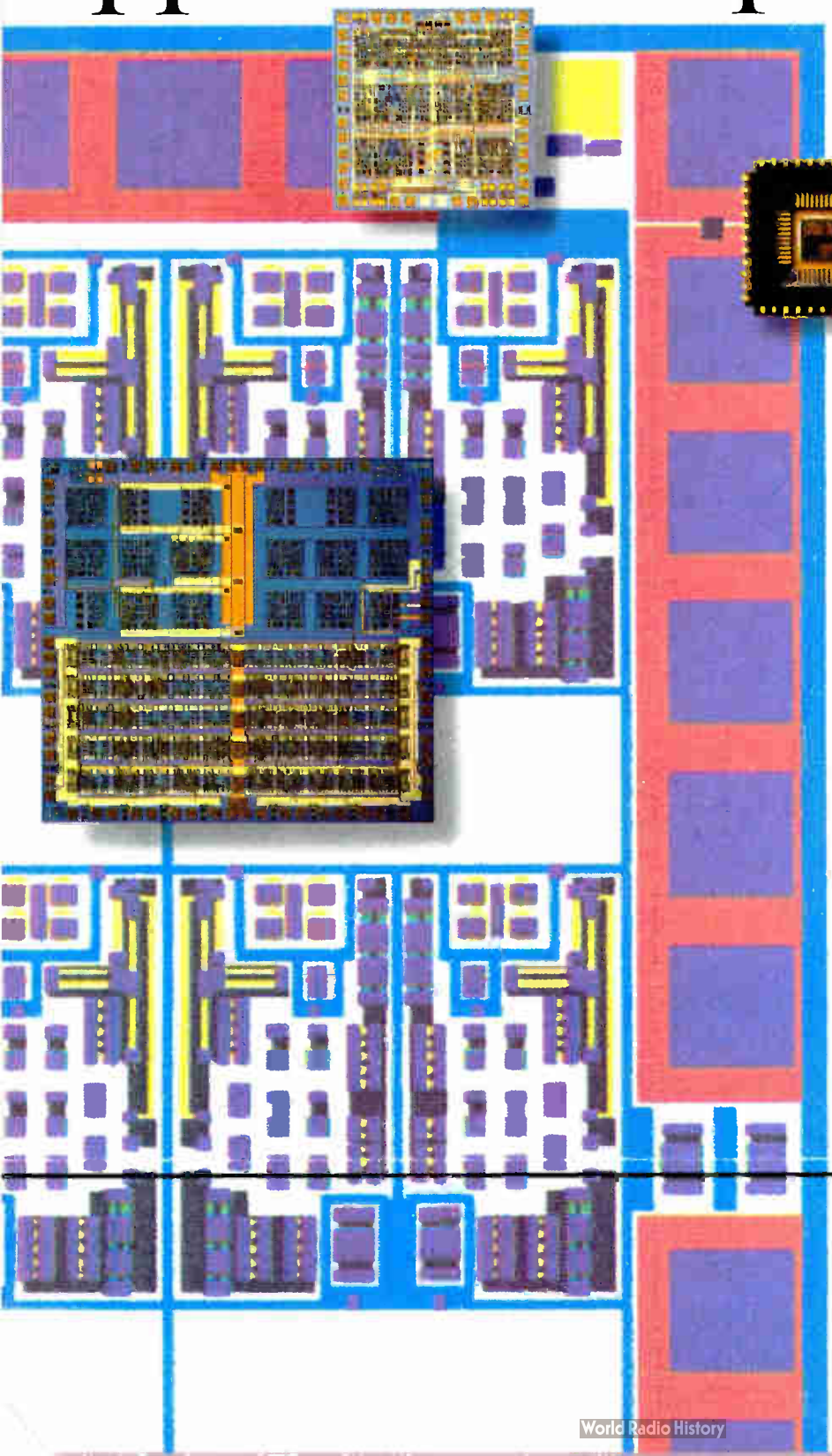

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Electronics

We are always looking for better ways to deliver more comprehensive and useful information to the readers of *Electronics*. Anyone can publish lists of companies, markets, products, or spec sheets. Indeed, the publishing business is shot through with enterprises that do little more than that, dressed up with nifty graphics and printed on heavy paper. We think you deserve more.

WOLFE: Approaching the story from the leading edge.

That's where our new product special reports come in. Started in February, these articles, each one rounding up a particular product category and technology, go far beyond the conventional listings. We do the kind of job that only *Electronics* can when we report and analyze the business side of the technology, exploring not only the state of the art but bringing our experience and expertise to bear on the marketing side. In that way, we can provide you, the reader, with a uniquely broad perspective on a particular product category.

Take the product roundup on single-board computers that begins on p. 87. Software & Microsystems editor Alex Wolfe pulls together the latest happenings in a dynamic 10-year-old technology and tells what they mean to sellers and buyers alike. Alex, who earlier designed software during his engineering career, says the most striking aspect of the single-board-computer market is its rate of change.

"The reason it's so dynamic at this moment is Multibus II, the Intel-supported 32-bit standard, which is about to come on in a big way. The whole idea of putting 32-bit microprocessors on single-board computers is revolutionizing the entire business."

Alex had help from New Products editor Jack Shandle in putting the marketing trends in perspective and keeping an eye on the latest boards as they were introduced. "It was a good partnership," says Alex. "Jack's expertise in tracking the products from week to week and my broad view of the technology picture enabled us to put together a complete report."

Still, there has to be a limit. "There are so many exciting and worthy products that it's impossible to include them all," says Alex. "One of our biggest problems was deciding where to draw the line. So what we had to do was approach the story from the standpoint of informing the reader of the leading-edge products and what they can do."

The team approach that was used by Wolfe and Shandle is a hallmark of *Electronics* journalism. The synergy that results can be traced to the varied experience and backgrounds of our editors and writers. For example, Alex was an engineer for five years before joining the magazine in 1984; some of the software he worked on is now used on the Lockheed P3B Orion, a Navy antisubmarine-warfare aircraft. And Jack, who joined the staff last fall, has degrees in engineering and journalism and was a political writer in Pennsylvania for several years.

That's the kind of mix that is required when you're writing a recipe for reporting with depth and value.

Laurence Altman

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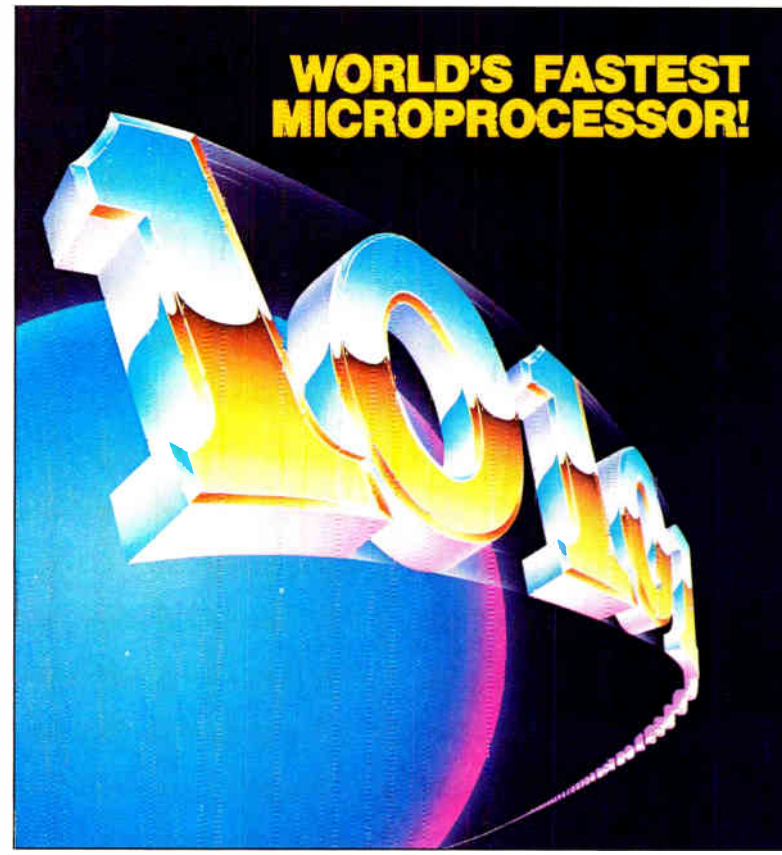
MARCH 19, 1987

Electronics

NEWS

INSIDE TECHNOLOGY

COVER: DAVID MYERS



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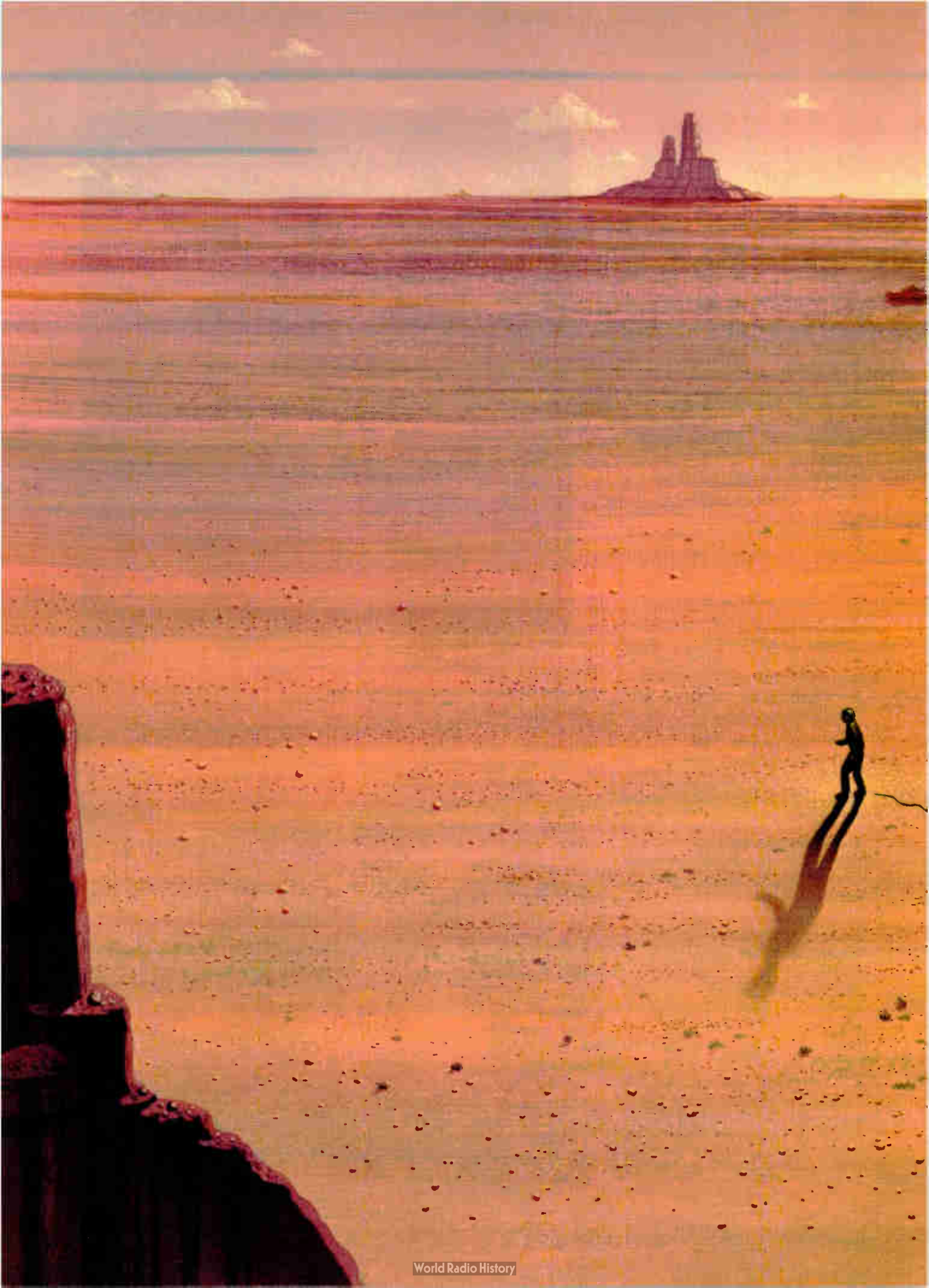
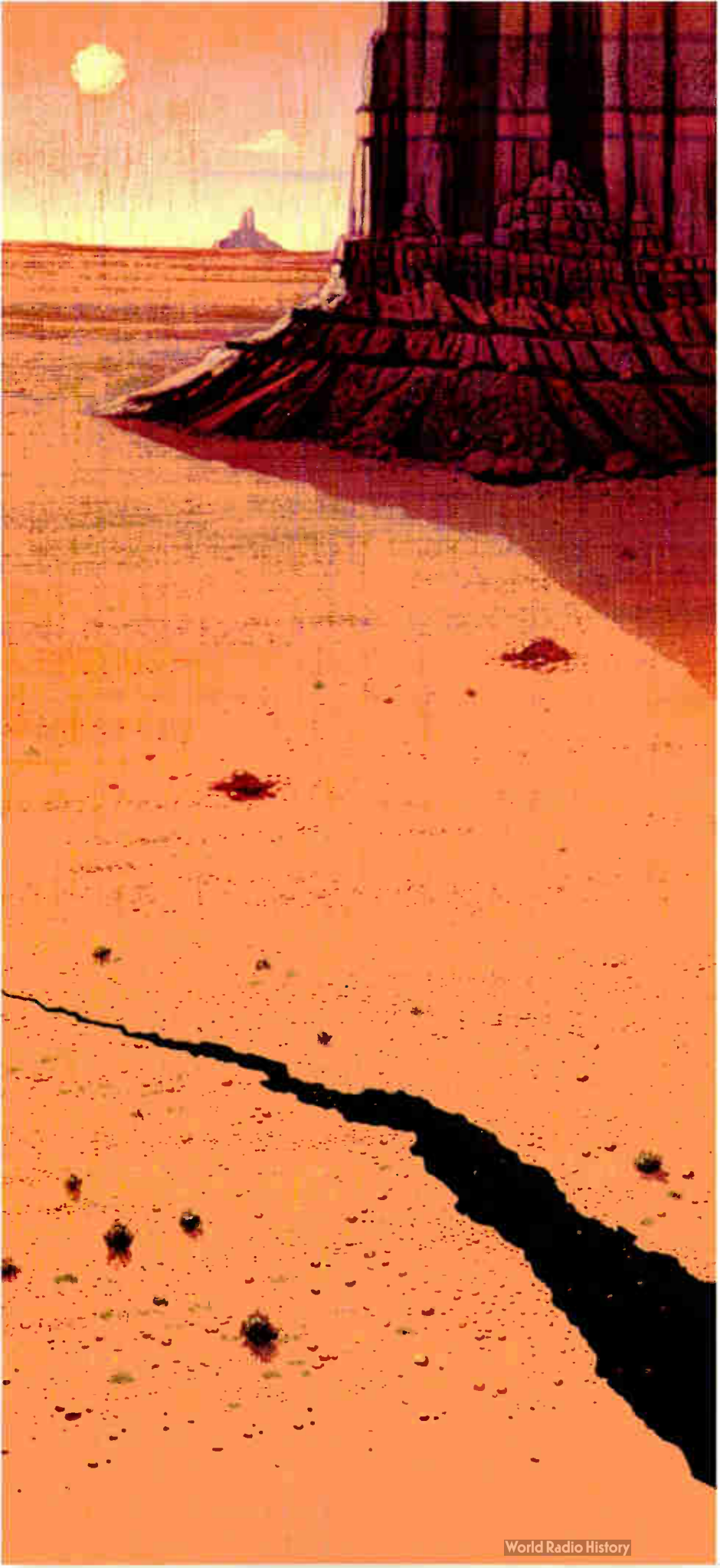
NEW PRODUCTS

DEPARTMENTS





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Altera's Smith: 'A real case could be made for a U.S. consortium fab line, where its capacity would be allocated by a company's investment; that's what should be built'

With all the hullabaloo that's been going on over Sematech, the proposed U.S. government-industry consortium to develop advanced semiconductor manufacturing techniques, and the race now to solve the funding and antitrust problems (see p. 31), there are still those chip makers—particularly the up-and-coming niche companies—that claim manufacturing is no longer where the action is.

Altera Corp., technology leader in user-configurable integrated circuits, is one of them. The Santa Clara, Calif., company has never made wafers—and never intended to. "That [kind of strategy] was inconceivable 10 years ago," Rodney Smith, president, declared recently. What has changed, he told a Kidder-Peabody conference in New York on March 12, is that the manufacture of wafers has ceased to be an art and has become a true manufacturing process.

"Maybe Jerry Sanders [president of AMD] did not realize how prophetic he was," Smith noted, "when he said, 'silicon is the crude oil of the '80s.' Like oil, the price of silicon has fallen dramatically, and a significant capacity surplus exists."

Smith thinks the analogy here is steel. "At the turn of the century, to be a factor in the manufacturing business, you had to make steel. Today, General Motors doesn't make steel—they buy it." In that industry, the evolution took maybe 100 years, he said. But in the integrated-circuit business, the process will take more like 35 years. "There is no doubt," Smith said, "that the next decade will see wide availability of high-technology silicon available for purchase."

So, for a new company such as Altera, investing in manufacturing capacity is not a good use of capital. Rather than investing in silicon, Smith figures that "a company should invest in the value-added areas of architecture, circuit design, and software."

However, he told *Electronics* before the conference that "a real case could be made for a U.S. consortium fab line, where its capacity would be allocated by a company's investment. That's what should be built." But, he noted, some laws will have to be changed in order for that to happen. If it did, Smith allowed that he might be interested in participating. "If the opportunity to participate is offered—say, a half-micron facility—I might make a strategic investment." He said 30% of his business goes to the military, and the Pentagon just might say: "make it here."

ROBERT W. HENKEL

From DC to 400 MHz to your PC

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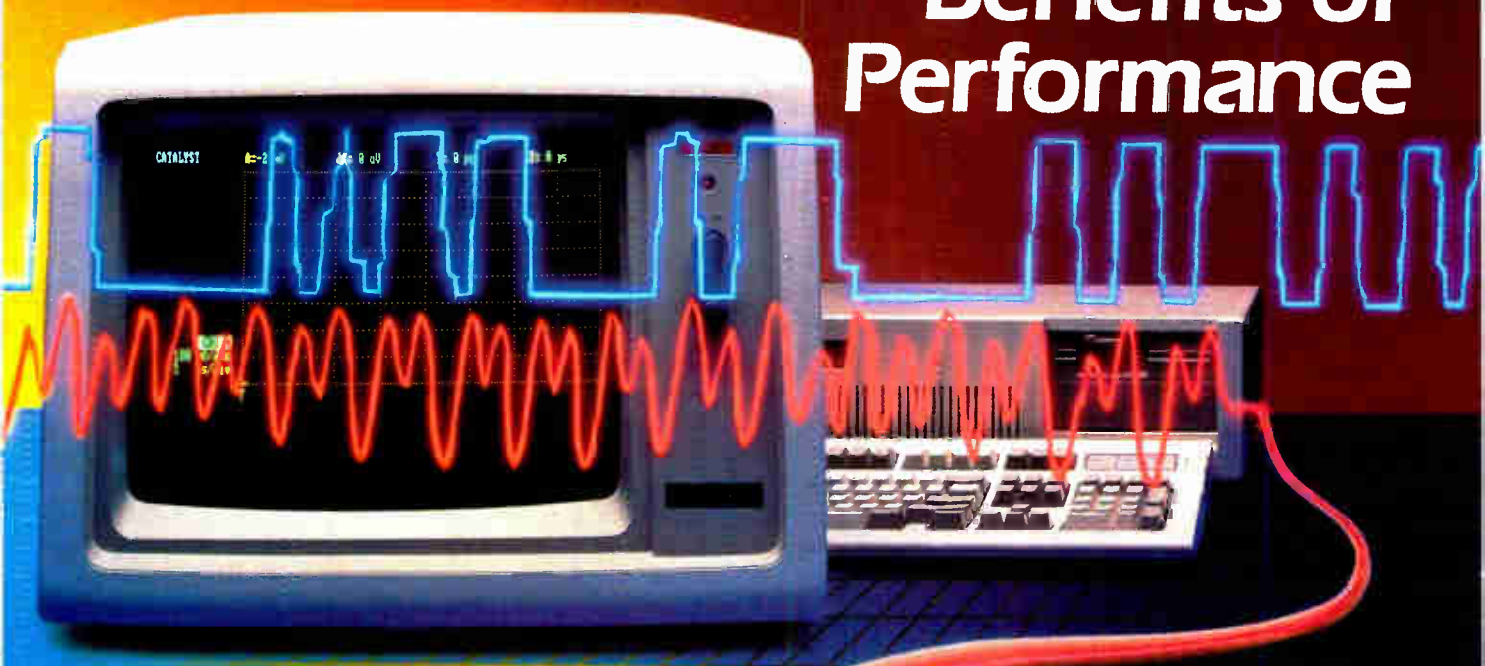

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64K CMOS SRAMs	
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IMS1620M (x4)*	45, 55, 70ns
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LETTERS

Clearing the air

To the editor: I would like to take this opportunity to thank you for including Xydar RC-210 [*Electronics,* Feb. 5, 1987, "Polymers Yield Strong IC Packages," p. 103] and also to call to your attention one small mistake that was made in the article as the result of our release being unclear.

The last paragraph covering cost is technically incorrect. The $7.35 to $9.75 per pound price for orders of 10,000 pounds or more pertains to the entire line of Xydar product grades. The RC-210 grade, to which the article refers, sells for $9.75 per pound for quantities of 10,000 pounds or more. We wanted to bring this to your attention in case a reader may have a question.

Dan Love
Dartco Technology Center
Augusta, Ga.

Technology by design

To the editor: You stated incorrectly that "[Intel acquired] the CHMOS-based [erasable programmable logic device] technology from Altera Corp. . ." [*Electronics,* Feb. 5, 1987, p. 23]. Actually, it is Altera that "acquired" the use of Intel's CHMOS EPROM technology for development of EPLD designs. Intel is an alternate source for EPLDs designed prior to 1986 by Altera on Intel's proprietary CHMOS technology.

Mohammad Aboobaker
General Manager
EPLD Operation
Intel Corp.
Folsom, Calif.

☐ *Reader Aboobaker interprets "technology" to mean process. It was used to mean "technology of design."*

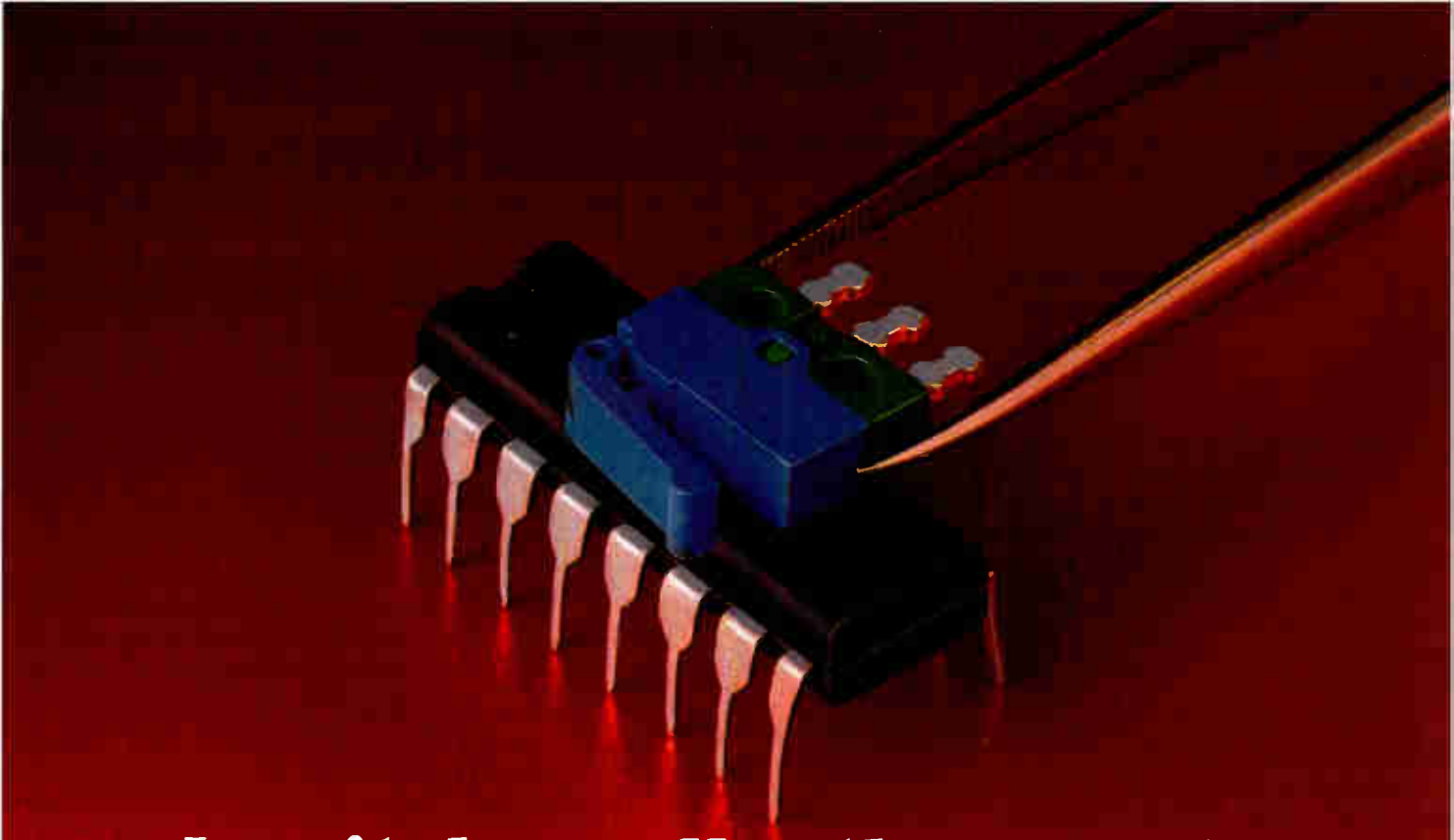
The IEEE needs you!

To the editor: The IEEE is sponsoring the Computer Dictionary project to produce a dictionary of computer-related terminology. Technical reviewers are needed for definitions for the Hardware section. Anyone interested should contact Mary Yee, Membership Coordinator, P610 IEEE Computer Dictionary Working Group, Logicon, 475 School St., S. W., Washington, D. C. 20024; (202) 646-2148.

Mary Yee
IEEE Inc.
Washington, D. C.

What's the number?

Correction: *In the Editorial Index for the Feb. 5 issue of* Electronics, *an entry for Silicon Compilers Inc. carried an incorrect phone number. The correct number for the San Jose, Calif., company is (408) 371-2900.*



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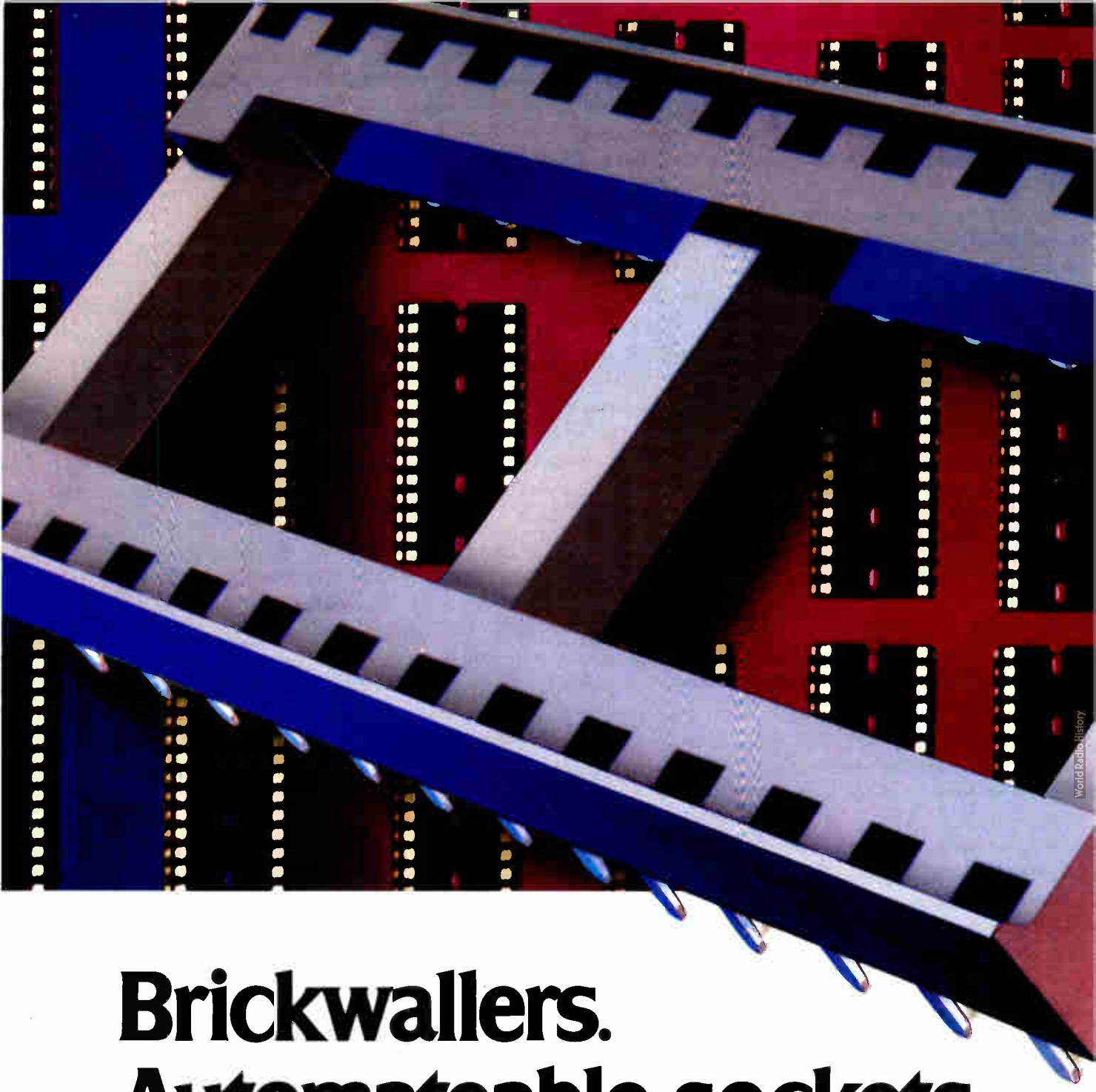

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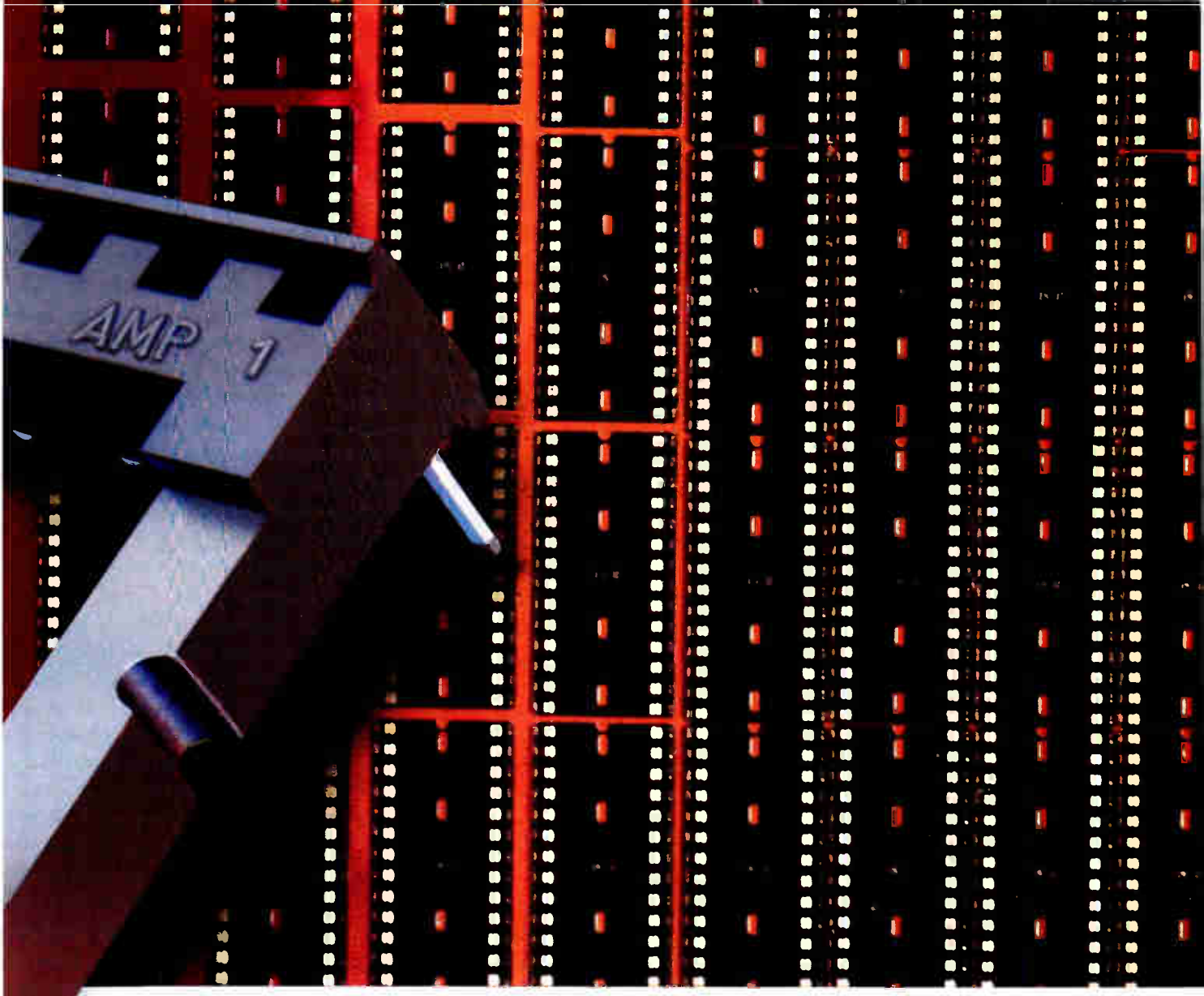

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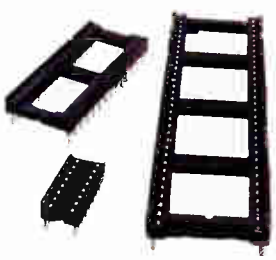

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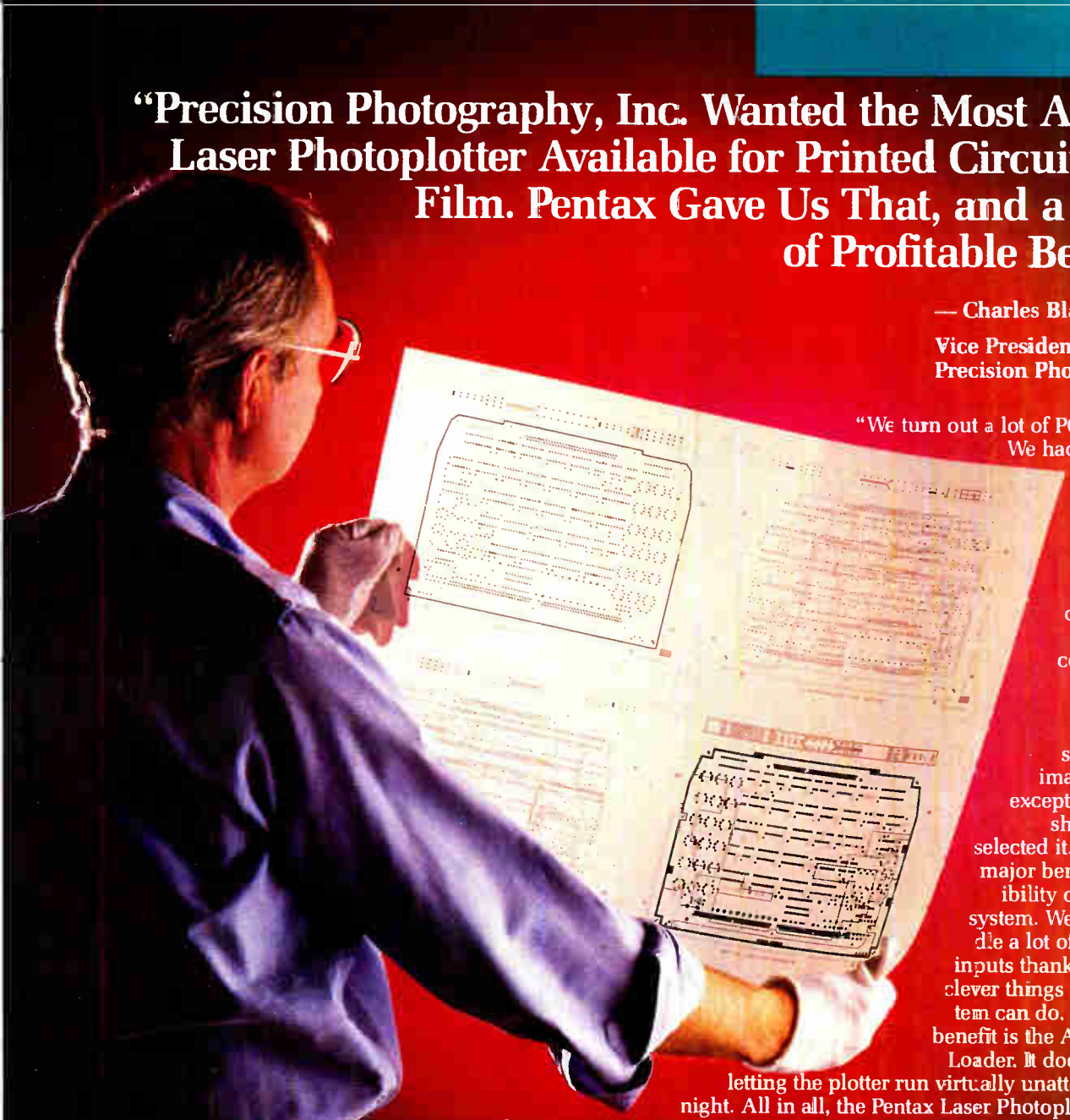

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ELECTRONICS NEWSLETTER

IBM GETS SET TO UNVEIL ITS NEXT GENERATION OF PCs...

Computer-industry insiders say IBM Corp. will completely revamp its personal computer product line in early April. Such a move has been anticipated for nearly two years, but speculation about the new generation has been heating up in recent weeks. The new lineup is likely to include two low-end machines, at least one of them powered by Intel Corp.'s 8086 processor; two midrange computers built around 12-MHz 80286 microprocessors; and a new super PC that will sport Intel's powerful 32-bit 80386. They will supplant IBM's original PC, as well as its more powerful XT and AT models. □

...AND THE QUESTION IS: WHAT WILL THE OPERATING SYSTEM LOOK LIKE?

While IBM prepares to unveil its new personal computer line, computer software companies are anxiously awaiting the design details. Still unclear is how open IBM's new systems will be and what operating software is to be offered. On the low end, PC-DOS will almost certainly be the operating system of choice, but on the upper end, IBM could go several ways. It could offer the first version of New DOS from Microsoft Corp. as an option, for example. New DOS, aimed at the 286 and 386 processors, would use the protected-memory feature of the 286 to allow the running of advanced application programs using large physical and even larger virtual memory. An upgraded version of New DOS, taking full advantage of the 80386's additional features, such as virtual-machine capability, should follow in late 1988 or early 1989. Also, Microsoft reportedly has developed a new version of DOS 3.2 that can use the virtual-machine feature of the 80386 to run multiple programs concurrently. Another scenario has IBM offering a proprietary operating system. A closed super-PC with a System 370-style operating system is also possible. □

TI's THIRD-GENERATION DSP CHIP IS ON THE WAY

Texas Instruments Inc. intends to boost digital signal processor performance substantially with a next-generation DSP chip it is developing under the code name Brahma. The part, which will be designated the TMS320C30, increases the data and instruction-word widths to 32 bits, compared with the 16 bits used in TI's current line of DSPs. The 1-μm CMOS chip, which will have a 60-ns cycle time, is capable of executing 33 million floating-point operations/s, since it performs parallel operations in a single cycle. The chip will contain two blocks of dual-access 1-K-by-32-bit random-access memory and will also have a block of dual-access 4-K-by-32-bit read-only memory. With an address range of 16 million 32-bit words, the chip can access off-chip memory, and it boasts an on-chip direct-memory-access controller. TI managers in Houston will not confirm these reports, but company engineers will discuss the chip at the International Conference on Acoustics, Speech & Signal Processing on April 6-9 in Dallas. □

ANOTHER STARTUP TAKES AIM AT CRAY'S SUPERCOMPUTER BUSINESS

Now there are three U. S. companies vying to design and build the fastest computer in the world. Chopp Computer Corp. joins Cray Research Inc. and ETA Systems Inc., both of Minneapolis, in competition with Fujitsu, Hitachi, and NEC, all of Japan. Chopp, La Jolla, Calif., has developed a new supercomputer architecture for its forthcoming machine with performance 10 times that of Cray's X-MP product line, the company claims. The new architecture relies on a large-word instruction format to pack nine instructions into each 60-ns clock period. The company will show a prototype system at the First World Supercomputer Exhibition in Santa Clara, Calif., in May. □

ELECTRONICS NEWSLETTER

FUJITSU'S BID FOR FAIRCHILD COULD BE ENDANGERED BY TRADE BATTLES

The pending takeover of Fairchild Semiconductor Corp. by Fujitsu Ltd. may fall victim to the mounting trade dispute with Japan. Secretary of Commerce Malcolm Baldrige said last week that he wants "Cabinet-level discussions to look into the ramifications of the proposed acquisition—trade, antitrust, and national security." The Justice Department has been investigating the deal, but Fairchild officials say they are 100% sure the deal will go through, since the two companies' product lines do not overlap. Gene Norrett, of market researcher Dataquest Inc., says the deal is in trouble because the Commerce Department wants to use the sale as a weapon to fight alleged Japanese trade restrictions and to reduce the current trade imbalance between the U. S. and Japan. □

GE READIES ITS 0.8-MICRON CMOS PROCESS

General Electric Co. may still be trying to peddle its merchant chip businesses to the highest bidder, but the company is certainly not moving out of semiconductor technology. "Our relationships with the commercial divisions are as if they're going to be with us forever," says Kenneth Pickar, manager of the Electronics Laboratories at the company's Corporate Research and Development Center in Schenectady, N. Y. That relationship will be tested in the coming months, when the labs transfer GE's most advanced 0.8-μm CMOS process—the result of its Very High-Speed Integrated Circuits effort, which is not under a government contract—and the team that developed it to the company's design center at Research Triangle Park, N. C. Meanwhile, another team in Schenectady is already working on GE's next-generation 0.5-μm process. □

NCR MAY SELL ITS NEW MULTIBUS II CHIP SET COMMERCIALLY

Look for NCR Corp.'s Microelectronics Division in Colorado Springs, Colo., to spin out a family of circuits for use with the Multibus II 32-bit bus standard. The NCR chips, designed for the company's Tower 32/800 computer, are being considered for sale on the open market. Premier among the group is a three-chip protocol handler that takes aim at the single-chip message-passing coprocessor offered by Intel Corp. and VLSI Technology Inc. [*Electronics*, April 21, 1986, p. 17]. The chips can handle all Multibus II communications modes supported by the MPC. But the NCR circuit set contains five built-in direct-memory-access channels that make possible memory-to-memory transfers of data packets up to 1-K bytes long, compared with the MPC's maximum of 32-byte data packets. The chips can also receive direct-memory-access transfers simultaneously from up to 20 processors using an interleaved packet approach, which can increase throughput in multiprocessor systems, NCR says. □

MOTOROLA, NORTHERN TELECOM TO DISCLOSE MORE ISDN CHIPS

Motorola Inc. and Northern Telecom Inc. are adding a new chip to their line of jointly developed products for the integrated services digital network. The two will announce development of a dual data-link controller at the International Switching Symposium '87 in Phoenix, Ariz. The new dual data-link controller, designated MC145488, will perform direct memory addressing to limit interruptions of a terminal's host microprocessor during ISDN transmissions. The chip design has address-recognition capabilities that reduce the overhead on terminals by filtering out data frames not addressed to the host. Samples are expected to be available in the first quarter of next year. □

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Electronics
3/19/87

PRODUCTS NEWSLETTER

HITACHI'S 64-K RAMs BOAST 7-ns ACCESS SPEEDS

High speed and low power dissipation make Hitachi Ltd.'s new 64-K-by-1-bit emitter-coupled-logic random-access-memory chips ideal for supercomputer main memories and as second-level caches in mainframes and superminis. Access speeds of 7 ns typical and 12 ns maximum, at a typical dissipation of 420 mW, are obtained by implementing the chips in a 1.3-μm bipolar-CMOS process that the Japanese company calls Hi-BiCMOS. It provides 1.6 times the speed of the company's 64-K chips in 2.0-μm Hi-BiCMOS. The new devices consume only 60% of the power of conventional 16-K products and have four times the capacity, but are only 1.2 times their size. Versions compatible with the input-output interface of both Motorola Inc.'s ECL10K and Fairchild Semiconductor Corp.'s ECL100K, the two most popular versions of ECL, are available. The ECL100K version has the slightly lower maximum access time of 15 ns but typically dissipates only 320 mW. Both come in ceramic DIPs and leadless chip carriers. The ECL100K-compatible HM100490-15 costs $143 apiece in sample quantities and $91 in lots of 10,000. The ECL10K-compatible HM10490-15 costs $130 each in samples and $78 in lots of 10,000. Delivery in Japan is from stock. □

SUMMATION'S TESTER HANDLES 672 CHANNELS WITH 20-MHz SPEED

Summation Inc.'s personal-computer-based digital tester can handle up to 672 channels—more than six times as many as competitive units. Its 20-MHz rate for test-vector generation can accommodate 90% of all microprocessor boards and high-pin-count custom circuits in use today. The High Speed Digital Test System can be expanded with up to eleven 32-pin modules for testing high-pin-count devices. Other modules can be added on to provide such capabilities as analog testing and the use of other manufacturers' equipment in the system. Available now, the Kirkland, Wash., company's basic 32-pin system costs from $25,175 with a Wyse Corp. personal computer as the platform, to $28,650 with Compaq Computer Corp.'s 32-bit Compaq 386. Each 32-pin DSR10 expansion module costs $4,250. □

DATACUBE SHARPENS IMAGE-RECOGNITION ABILITY WITH NEW BOARD

Datacube Inc. is adding a second-generation edge-sharpening computer board that permits finer manipulations of video or acoustic signals to its MaxVideo product line of 18 real-time digital signal-processing boards. The Peabody, Mass., company's latest board, the VFIR-MKII, enhances edges by expanding the size of the kernels used in image processing from the 3-by-3 pixels of its predecessor to either 8-by-8 or 64-by-1 pixels. Several MaxVideo boards, which run on VMEbus-based work stations, are usually linked together for the image-recognition tasks necessary in robotic control, factory automation, artificial intelligence labs, and the development of autonomous land vehicles. Available now, each VFIR-MKII board costs $7,800. □

ROCKWELL MODEM TRANSMITS FACSIMILE INFORMATION AT 14,400 BITS/S

Asynchronous, half-duplex modem board from Rockwell International Corp. that handles facsimile transmissions at a 14,400-bit/s clip promises to boost throughput by 50% over existing 9,600-baud equipment operating under the CCITT V.29 facsimile standard. The R144HD can run over public telephone lines as well as leased lines, according to the Irvine, Calif., company. The board will appeal to original-equipment manufacturers with applications in still-frame video telephone equipment, electronic publishing, and similar systems. In quantities of 1,000, the R144HD costs $140 each. Shipments begin in April. □

YOU'VE READ A LOT LATELY ABOUT DSP.

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As evidenced by the Zoran Vector Signal Processor (VSP)™ and Digital Filter Processor (DFP).

Two new signal processors that enable you to do something you've never done before. Like design your system from the top down.

With a systems perspective in mind, which enables you to focus on your application, instead of on your implementation.

Using single, highly integrated system-processor devices that use parallel processing to deliver all the speed of building blocks. Without all the hassles of discrete components and extensive programming.

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Best of all, we're shipping products now. Instead of simply announcing them. Which means you don't have to wait to get the jump on your competition.

High performance never looked so easy. We didn't think it was enough for the VSP and the DFP to be the fastest DSP devices. So we also made them the easiest to use.

We developed proprietary architectures and optimized them for faster, more efficient execution of embedded DSP algorithms, such as FFTs and FIRs.

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On top of that, we developed a modular design that lets you configure multiple VSPs and DFPs in parallel to achieve even higher performance.

And we utilized proven double-layer metal CMOS technology for lower power consumption and higher reliability.

VSP: Powerful vector processing capability. Until now, you needed the power of an array processor if you wanted to do vector processing. But that was before Zoran developed the Vector Signal Processor.

```
LD   MMPT:128      MBA:IN_DATA        ; LOAD 128 POINTS
FFT  MMBT:128      FPS:64   LPS:1     ; DO 128-PT FFT
ST   MMPT:128      MBA:OUT_DATA       ; STORE 128 POINTS
```

Three simple VSP instructions execute a 128-point complex FFT in 237 microseconds.

The world's most powerful DSP processor. And the first to process data in blocks, or vectors, instead of processing only one input at a time, as is the case with scalar processors.

Which means you can easily achieve bit-slice performance with a single component. And you can do it in a lot less time.

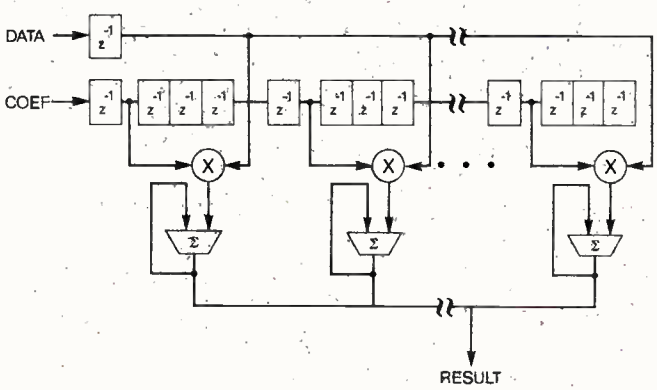
Because our embedded high-level instruction set eliminates the need to write lines and lines of code.

So you can concentrate on your end application, instead of getting bogged down in the details of software implementation.

And with our unique VSP architecture, multiple tasks, such as managing the bus interface and executing algorithms, are handled concurrently for even faster operation.

A 1024-point complex FFT, for example, takes just 2.6 ms with the VSP. Using only a kernel of three simple instructions.

The VSP also provides better dynamic range, thanks to the use of 16-bit block floating point arithmetic. Which retains the precision of the original signal during FFT operations.



DFP architecture utilizes parallel processing to deliver 320 million operations per second.

DFP: Faster FIR filtering with parallel processing. Designed for extremely high-speed FIR filtering and 2D real-time convolutions, the DFP family delivers the high performance of building blocks. But with the high integration of a single device.

Each DFP consists of four or eight filter cells configured as a unique parallel-processing system. Each cell contains an 8x8 or 9x9 bit multiplier, a 26-bit accumulator and three decimation registers.

And with each cell computing 20 million additions and 20 million multiplications per second, the DFP is capable of performing 320 million operations per second. At a blazing 20MHz throughput. So you can easily convolve images in real time.

Moreover, you can cascade multiple DFPs for higher-order filters, or implement them in parallel for even greater precision.

All the tools and support you'll ever need. Most DSP support doesn't give you much to lean on. So we decided to provide you with all the help you need to shorten your development cycle and get to market faster, ahead of the competition.

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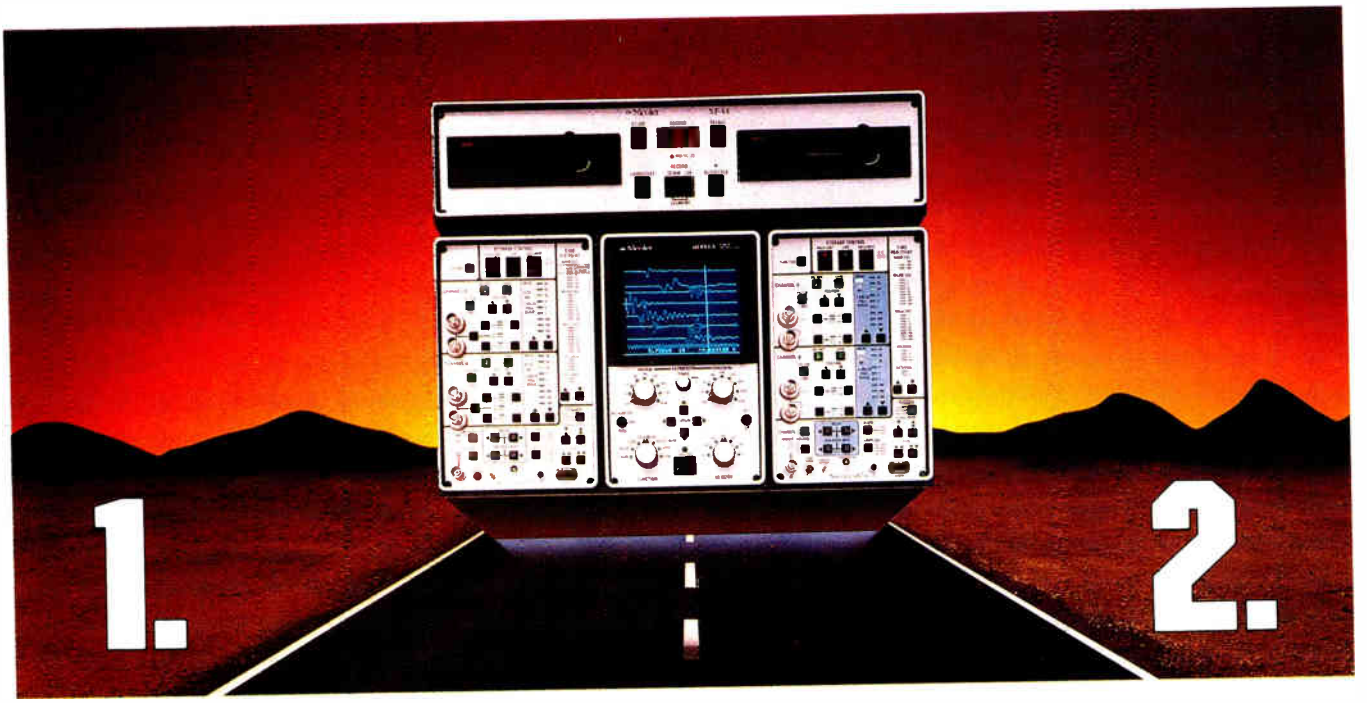
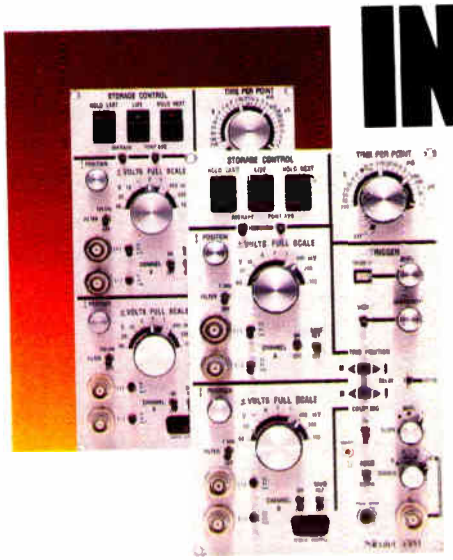


TWO DIGITAL SCOPES IN ONE.



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Electronics

WILL SEMATECH FLY? THE NEXT THREE MONTHS WILL TELL

ITS SUPPORTERS MUST OVERCOME OBSTACLES OF FINANCING AND LEGALITY

NEW YORK

Now comes the hard part. With Sematech finally getting a green light from the Semiconductor Industry Association, the consortium that some consider the last, best hope for the U. S. chip industry must make its way through an obstacle course of organizational, legal, and fiscal hurdles.

The industry leaders and their government allies who are driving Sematech—the name stands for Semiconductor Manufacturing Technology—are deploying along three major fronts to meet a legislative deadline of the Fourth of July. At stake is the future of a cooperative effort to develop advanced manufacturing techniques for semiconductor makers in an attempt to stave off Japanese competitors. The three hurdles:

- Deal with the companies made unhappy by the SIA's decision March 2 that Sematech will produce limited, prototype quantities rather than go into full-scale manufacturing. They must also determine the role that makers of semiconductor-manufacturing equipment will play in the consortium.
- Persuade Congress to grant an antitrust waiver.
- Convince Congress that Sematech is worth $100 million to $200 million a year of the Pentagon's money.

The Sematech promoters must move quickly. The Senate's Subcommittee on Defense Industry and Technology has already begun hearings on Sematech in a tight schedule designed to get legislation on President Reagan's desk by July 4.

YES AND NO. Junkins, left, is positive, but pioneer Petritz says no to the idea of a government-backed semiconductor consortium.

Meanwhile, the industry is abuzz with speculation and opinion. For example, there is some surprise at Texas Instruments Inc.'s support of Sematech. The company stayed in the 256-K dynamic random-access-memory business when just about all other American makers quit, leaving the market to the Japanese. TI has been betting its decision will give it the process lead, so many observers figured the company would oppose any cooperative effort.

But, says executive vice president William N. Sick, "We believe it is important not only to the U. S. but to TI to have the infrastructure in place in this country." So TI, which now produces most of its DRAMs in Japan, is preparing to move more production of 256-K and, eventually, 1-Mb DRAMs back to Texas.

President Jerry R. Junkins adds, "We are a member of SIA, so I don't think we should boycott something that is as important to our industry as the SIA believes Sematech is." Yet Junkins has doubts, based on the competitive nature of the chip business. "You can get a couple of companies together for a specific purpose and move forward, but I frankly am not sure if we can go on for several years in general research," he says.

At least one industry pioneer raises his voice in condemnation of the consortium. "I'm very much opposed to the notion that we have to have the government spending money on R&D," says Richard Petritz, who helped found Mostek Corp. and then, with money from the British government, Inmos Ltd. "The R&D should be handled the way it always has been—by industry. It really pains me to see some of the old entrepreneurs trying to get this kind of money from the government." Petritz believes innovation is the solution to the industry's current problems. "If you are going to ask the government for money, ask it for invest-

A NEW LOBBYING GROUP JOINS THE FIGHT TO SAVE R&D TAX CREDITS

Even as Sematech, the semiconductor industry consortium, inches ahead, sponsors of a new lobbying group that has been dubbed Coretech are working on an agenda to set the federal policy on research, which they hope to present to the second session of the current Congress. Established in January, Coretech is supported by some 30 companies—among them Apple Computer, Hewlett-Packard, IBM, and M/A-Com—and more than 60 universities. It also has on its membership rolls a dozen trade associations and some research institutions.

The immediate concern of Coretech is to make permanent the research and development tax credit and the university basic research credit, both of which are scheduled to expire at the end of 1988, and to kill a proposal to make companies allocate some domestic research costs to income from foreign sources. It has already been instrumental in getting legislation introduced to keep the R&D tax credit and restore its 25% incremental rate, which had been cut by the Congress to 20%.

However, once these fires are out, Coretech intends to sponsor public policy debates that will result in a legislative package on R&D. "R&D policy is part of tax policy," says Robert Rosenzweig, president of the American Association of Universities and a member of Coretech. "The House Ways and Means Committee and the Senate Finance Committee are not trained in R&D." Adds Joseph A. Saloom, vice president of M/A-Com and chairman of Coretech, "The last tax bill reflected a lack of [congressional] understanding of the research process." *–Clifford Barney*

ments in new companies, not in setting up national labs," he adds.

Just the same, the SIA is moving ahead. When its directors met in Washington in early March to approve the consortium, they also decided that although the operation will include a world-class production facility, it will produce only enough chips to prove the processes. That is regarded as a victory for the TI-IBM Corp. view, as opposed to the full-scale volume production proposed by a faction led by Intel Corp. and National Semiconductor Corp. It is still not clear whether this decision is final, or whether it will drive out any potential backers. The final decision has a vital impact on the antitrust question.

Then there is the matter of how to work the equipment makers into the equation. Since Sematech's emphasis will be on manufacturing processes rather than new chips, the role of the equipment houses could be pivotal. But there are still no details. The requirements for joining Sematech will be the same as those for the SIA, except that members must be U.S.-owned. "We don't know our role in Sematech yet," says Larry Kolito, the Semiconductor Equipment and Materials Institute's liaison with the Semiconductor Research Corp., an SIA operation that sponsors university research.

PRECEDENT CITED. Another critical matter is the question of antitrust. The SIA has assigned Jon E. Cornell, senior vice president of Harris Corp.'s Semiconductor Sector and an SIA board member, to investigate that issue. Washington experts believe there is a precedent for writing an antitrust exemption into a bill authorizing funds for Sematech: the arrangement by which the federal government has long supported the U.S. aviation industry, through the National Advisory Committee on Aeronautics and its successor, the National Aeronautics and Space Administration.

Work has already started on the final hurdle—financing. Sen. Jeff Bingaman, a New Mexico Democrat, laid out for SIA directors a tight schedule of hearings designed to meet his Independence Day deadline. Bingaman, chairman of the Armed Services Committee's new Subcommittee on Defense Industry and Technology, started hearings on government funding on March 9. Officials of the federal science establishment were to testify on such issues as competitiveness, security, and technology transfer.

A week later, industry leaders were to testify, and on April 1 sessions will be held to elicit more detail on proposals for Sematech. Then, during the week of April 20, the subcommittee will vote on the Sematech proposal.

Among what the senator calls the big-picture questions facing his subcommittee are: How far should the government go in supporting industry? How should the government deal with the sticky issue of splitting the consortium's cost between stockholders and taxpayers—and how can they split the benefits? When should the government cut off funding and under what conditions?

Underlying all of this is the sense among subcommittee members, and apparently among others in Congress, that they should more seriously consider how to better integrate the country's defense policies and the economy overall. A serious look at this issue is "long overdue," Bingaman says.

And looming over all is a deadline. If the SIA and the industry don't get what they want this time around, they'll have to wait until next year. And that, some executives believe, may be too late.

–Clifford Barney, with J. Robert Lineback and Ron Schneiderman

CONSUMER ICs

IC REDESIGN EXPANDS SMART-POWER MARKET

AUSTIN, TEXAS

An all-out drive by a Japanese camera maker to regain the top spot in 35-mm sales has resulted in a new market for Motorola Inc.'s smart power ICs: battery-powered consumer applications. The windfall is the result of a redesign of the chips to fit inside a camera and use as little power as possible.

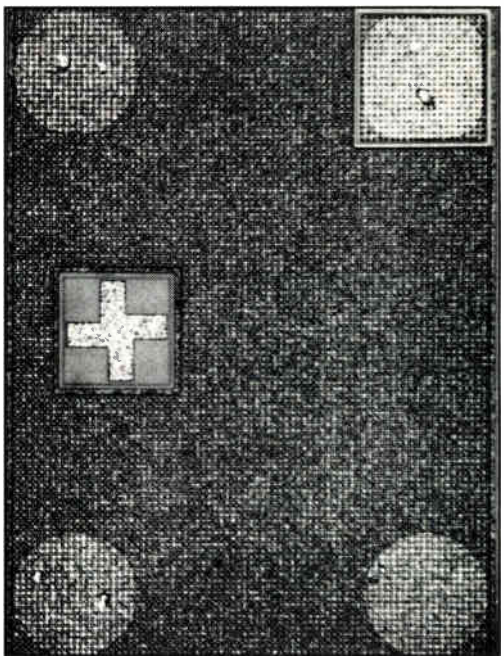
The chips are a motor controller, the MPC1710, and a power FET, the SFX10. Canon Inc. is already using them by the thousands in its two new digitally controlled single-lens reflex 35-mm cameras, the EOS (for Electro-Optical System) 620 and 650. Introduced in March, the EOS line is Canon's bold bid to leapfrog archrival Minolta Camera Co., which jumped to No. 1 in 35-mm cameras in 1985 with Maxxum, the industry's first SLR camera with a built-in autofocusing subsystem.

Motorola had to shrink the motor controller 25% and the power FET 30%, and do it in a hurry. "Canon wanted high-volume deliveries from day one. We had to follow the learning curve much faster than normal," says Daniel Artusi, director of marketing for Motorola power transistors, the proprietary TMOS process, and smart power products in Phoenix, Ariz.

For the 1710, Motorola adapted the design and mixed bipolar-CMOS process of a high-current motor-controller chip, which is already being sold for automobiles and industrial equipment. The result is a bidirectional motor-controller IC that runs at a peak current of just 3 A instead of up to 40 A, as required in many automotive and industrial systems. Besides shipping it to Canon, Motorola is offering the chip in the low-voltage market for use where battery-powered bidirectional motor control is needed, such as toys and small robots. It sells for $2.95 in quantities of 1,000.

The SFX10 custom power FET has more than four times the cell-packing density of Motorola's other current TMOS products. The chip contains a little more than 2 million cells/in.^{2} and has less than 130 mΩ of on resistance. Motorola product managers say the 8-pin power FET is likely to become a volume commodity product soon.

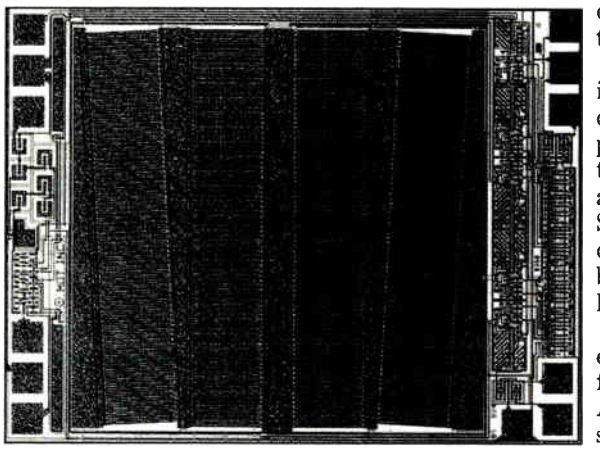
LOADED. Canon's smart new cameras are memory-loaded systems that can actually contain more memory than many of the early home computers—up to 65-K bytes. A collection of slave microcontrollers and processors, under the control of Motorola's 8-bit EEPROM-based 68HC11, performs a variety of tasks in addition to autofocusing: exposure setting, flash control, and high-speed film advance. The 68HC11's EEPROM eliminates the need for potentiometers, instead storing camera-calibrating bits in the microcontroller's nonvolatile memory.



COMING YOUR WAY. The power FET redesigned by Motorola should soon become a volume product.

Work on the smart power products was an engineering challenge that began at Motorola in the fall of 1985. For starters, the motor-controller chip not only had to squeeze into the silicon-packed camera body—Motorola's 5-μm BiCMOS process was shrunk to 3 μm—but it had to match the low-power needs of a lithium-battery-operated camera. There also were process changes, such as the use of shallower junctions, says Gary Fay, device design manager for power MOS/IC products. Since operating conditions would not vary as much as in autos and factories, temperature and current-compensating analog circuits normally included on the company's MPC1700 were dropped. This meant finer-line processes for peripheral control logic surrounding the four power FET transistors. The direction of a motor and braking action can be controlled by selectively turning on the transistors of the H-bridge.

Measuring 100 by 130 mils, the chip contains four 3-A power transistors for the H-bridge, an interface circuit for direct input of data from the microprocessor, and a level shifter that interprets signals from a host to drive the on-board power transistors. It also has a charge-pump that increases voltages over battery levels and a new motor braking device that stops motors suddenly by turning on the two lower transistors of the H-bridge.



MIXED PROCESS. For the motor controller, Motorola redesigned a chip that has a mixed bipolar-CMOS process.

To get a lower on-resistance in its new TMOS power FET, Motorola also modified and shrunk its process, adding bonding pads to the 63-by-83-mil die. Multiple wires and leads also were added to the SFX10 package to further lower on-resistance. It has a minimum breakdown voltage of 15 V and will handle drain current of 2 A.

One 1710 chip is used in the camera's motor drive, exposing three frames a second during shooting. A second chip rewinds the shutter spring. The power FET chip controls the camera's power bus.

–J. Robert Lineback

OPTICAL MEMORIES

GE ROILS THE INTERACTIVE-CD WATERS

SEATTLE

A new method of packing full-motion video onto compact disks could position General Electric Co. to blow open the market for computer-based CD applications. Full-motion video is so data-intensive that until now, the 5¼-in. disks—which can hold more than 80 minutes of audio information—couldn't hold much more than half a minute of video. But now GE says it can record up to 72 minutes of video on a single disk.

The development is a milestone in the evolution of CD read-only memory, which has been struggling largely because the applications for which it has been touted, such as interactive training programs, require more video time than has heretofore been available. Researchers at the David Sarnoff Research Center in Princeton, N. J., believe their solution, involving new data-compression technology, will open up new markets for CDs.

Called DVI (digital video interactive), GE's system is similar to CD-I (compact disk interactive), which was introduced by Sony Corp. and Philips International NV a year ago. But CD-I, which supports single-frame video plus audio and text, can support only 30 s of full-motion digital video per disk.

SQUEEZING DATA. GE's system, on the other hand, uses a special data-compression algorithm to squeeze the original video signal into a form that can be stored in quantity on a CD. In playback, two custom chips expand the data for display on a computer monitor.

GE has yet to develop marketing plans for DVI, according to Arthur Kaiman, director of digital products research at Sarnoff Labs. Indicating that several divisions within GE have shown interest in the technology, he adds that GE will maintain the development effort at Sarnoff, which GE is donating to SRI International, an independent research business based in Menlo Park, Calif. [*Electronics*, Feb. 19, 1987, p. 40].

Most important to GE's effort will be whether or not it can garner support for the technology among other industry players. "The reason we are making this announcement [at the second annual Microsoft CD-ROM conference in Seattle] is that we want to [establish] standards," Kaiman says. "We want to work with interested parties to make this technology happen."

GE: 72 minutes of video on a disk, Sony-Philips: 30 seconds

The DVI project began three years ago as RCA's effort to develop a system combining computer graphics with full-motion video for the business, education, and consumer markets. It was decided then that a system must be digital in order to offer maximum control and interactivity for the user.

The challenge was prodigious, however. Full-motion video requires that the display be refreshed 30 times/s, and a single, uncompressed TV-quality frame requires 600-K bytes of data. Making things more difficult were the limitations of the disk, which holds just 500 megabytes of data, and its drive, which reads data at only 150-K bytes/s—much too slow for full-motion video.

To get around those limitations, GE had to compress the video data by about 120 times, so that each frame could be stored in just 5-K bytes of memory. DVI also supports full-motion graphics, such as rotating three-dimensional figures, and it can combine audio, video, graphics, and text on a single disk. And since the video is digitized, it can be easily manipulated by the user.

The DVI data-compression algorithm can be run on a VAX 11/785 computer and takes about 2 minutes per frame, Kaiman says. But he adds that "we know how to compress at a rate of two to three frames/s." GE is trying to drive down the price of the compression equipment to "something reasonable."

In playback, DVI relies on the powerful new chip set to expand data stored on the disk. The chips were designed in just nine months, thanks to the use of a Genesil system from Silicon Compilers Inc. The pair, a powerful pixel-processing engine that can run 12.5 million instructions/s, and an output display processor that features multiple resolution settings, permit the simultaneous display of graphics and video, as well as other special functions. Resolution for full-motion video is 256 by 200 pixels, and GE plans to improve that to 240 by 256.

–Tobias Naegele and Jonah McLeod

WHY ONE 'CALM' CHIP MARKET EXCITES TI

DALLAS

The eyes of Texas Instruments Inc. are focused on a major new thrust into advanced linear integrated circuits—a relatively calmer market that has been more resistant to the cutthroat competition that has bloodied the players in the digital chip arena. A critical part of TI's effort involves the creation of computer-aided-design tools, the lack of which has so far hampered linear's growth. The right tools could cut in half the time it takes to bring complex analog chips to market, the Dallas chip maker claims.

TI, which has been active in linear chips since the early 1970s, is now focusing on a number of different linear components. Among them are single-chip front-end peripherals to digital signal processors, speedy flash converters, self-calibrating analog ICs with on-board digital control logic, high-performance op amps, video digital-to-analog converters, analog-to-digital circuits, and new high-voltage flat-panel display drivers.

Work on the linear program actually started last year, and the first advanced analog ICs are now waiting for formal introduction. For example, prototypes of a single-chip DSP front-end peripheral have been given to some customers. It is believed to be one of the most complex linear ICs available.

A HAVEN. "The linear market has characteristics not found in others," says Tom Engibous, TI vice president for linear products. "It is probably more defensible against global competition. It's certainly a market where design expertise is a larger portion of the product's value. That expertise will mean fast-turnaround capabilities. For chips that are not too complex, we are looking at doing designs and getting parts to customers in less than 120 days. The days of having 18 months to design a part are over."

TI is not alone in its attempts to grab more of a steadily growing analog-IC market. Recent startups and other U. S. electronics giants are also viewing the analog arena as a sanctuary from the intense competition that has driven profits out of many digital commodity markets. Market researcher Gnostic Concepts Inc. of San Mateo, Calif., predicts that U. S. linear IC production will continue a steady march from $1.8 billion in 1987 to $3.18 billion in 1993

One reason for the new interest in linear ICs, oddly enough, is the relative shortage of design and testing tools. The need for talented engineers and internally developed CAD tools has raised the price for entry into the field, says Eric J. Swanson, vice president at Crystal Semiconductor Corp. Since its first days, the Austin, Texas, startup has had engineers working only on CAD for CMOS designs that place analog circuits under the control of digital logic [*Electronics*, Jan 20, 1986, p. 21].

ENGIBOUS: "The linear market is probably more defensible against global competition."

The trick is dealing with the shortcomings in analog CAD and testing tools. Swanson sees as a key "the ability to get something out of inadequate simulation tools and the too-few testing tools." Robert Dobkin, engineering vice president at Linear Technology Corp. in Milpitas, Calif., agrees: "No matter how good your tools are, they won't replace a good analog designer."

Another problem, Dobkin adds, is that "with analog there are so many modes of operation and so many unknowns. You don't often find out about them until you start evaluating the actual circuit. No matter how good simulation is on complex circuits, a few things will always be missed," he says.

However, some progress is being made. Work on TI's advanced-linear design system started last year, and some pieces are being used. Crystal's Swanson says his analog designers can now work on ICs with three times the complexity of five years ago. But, he says, "the gap is still widening between digital and analog CAD. Analog suffers from a double whammy because it is a smaller market [than digital] without the big dollars focused on it by CAD suppliers. And it is a much more difficult problem to solve compared with digital designs."

Micro Linear Corp. in San Jose, Calif., has been working on design tools for its semicustom chip customers. Today, its library of cells is available on CAD work stations from Daisy Systems Corp. and Analog Design Tools Inc. Still missing, however, are simpler user interfaces, faster work-station processing speeds, and better methods of converging simulations from linear-circuit equations, notes Ken Fields, Micro Linear's marketing manager.

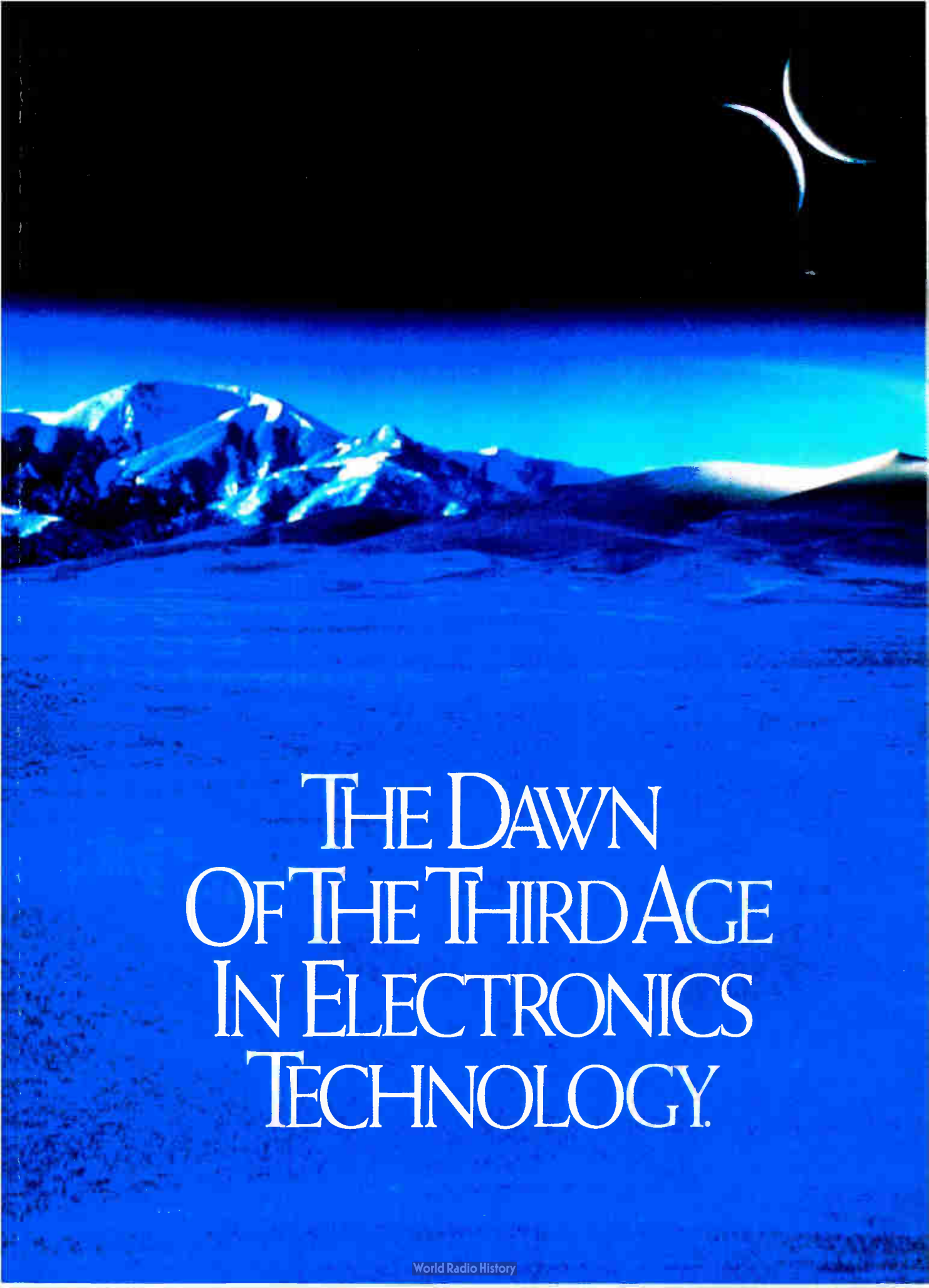
In Colorado Springs, Colo., Honeywell Inc.'s Signal Processing Technologies venture is crafting engineering tools that speed simulation of digital circuits residing on analog ICs. Traditional methods based on Spice models are too slow, says Reddy Penumalli, technology director. Honeywell aims to speed up digital simulation on analog ICs by 40 to 50 times. It is also developing an analog functional simulator that, unlike transistor-level simulators, works on standard cells. In the layout area, it is writing auto-placement and -routing software for interconnection of analog macrocells. *–J. Robert Lineback*

APPLE'S MACINTOSH BEGINS CROWDING IBM'S AGING PC

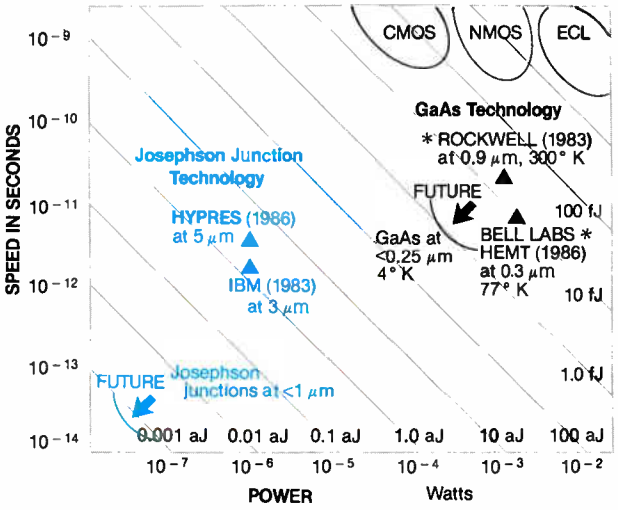
LOS ANGELES

Apple Computer Inc. has taken a major step toward becoming a far bigger threat to IBM Corp. in personal computers. With its new Open Mac architecture, the Cupertino, Calif., company has thrust itself into the mainstream corporate computing picture as IBM moves slowly to upgrade an aging product line.

Apple's new line has two models, the Mac II and the Mac SE, for system expanded [*Electronics*, March 5, 1987, p. 21]. But it is the Mac II, with its six expansion ports, that throws open the Mac environment to third-party hardware and software developers. And Apple has strengthened a strong point: graphics. The Macintoshes always have outdone the IBM PCs in this regard, and the new Mac II can do it even better.



THE DAWN OF THE THIRD AGE IN ELECTRONICS TECHNOLOGY.



aJ = atojoule = 10^{-18} joules ▲ performance actually demonstrated
fJ = femtojoule = 10^{-15} joules * Obtained in ring oscillator circuits

Figure 1: Chart compares Josephson junction with conventional GaAs and silicon technologies. Present day Josephson technology dissipates 1,000 times less power and operates more than 10 times faster. As the graph indicates, "future" marks an even more dramatic increase in speed at yet lower power dissipation.

speed and low power dissipation (see Figure 1), superconductivity allows the designer to take advantage of dense packaging and virtually dispersionless transmission lines. The unique properties of superconductivity will make the highest performance computer and communications systems an inevitable reality.

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HYPRES combined revolutionary chip and cooling concepts to solve conflicting thermal, electrical and mechanical problems of these devices by bathing a corner of the IC, the portion operating in a superconductive mode, in a liquid helium spray. The other corners, less than half a centimeter away, operate at room ambient. These concepts preserved the ultra-high performance expected from Josephson junction technology and resulted in a general purpose signal processor reliably interfaced to room temperature environment through ultra-high performance connectors.

In earlier developments, chips were cooled by immersing the whole circuit in liquid helium or thermally grounding the circuit to a cold finger in a vacuum environment. It took an hour to change a sample. HYPRES invented a rather elegant cooling system to completely eliminate the vacuum and allow the user to change a sample in a minute or less.

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(Subject to change without notice)

INPUTS
Channels: one or two
Coupling: DC; 50 ohms
Voltage range: ± 10 mV, ± 100 mV or ± 1 V
Scales: 50 μV/div to 2 V/div

TRIGGERING
Internal or external level, positive or negative slope

VERTICAL MEASUREMENT
(oscilloscope head)
Risetime: 5 psec internal effective risetime
Dynamic range: 46 dB (1.1 SNR) averaged
Smoothing: fast or slow response
Data points: 1024, 512, 256 or 128/waveform

HORIZONTAL
Effective sweep speed: 5 psec to 1 nsec/div.
Zoom: sweep start and sweep speed reset so time between horizontal markers fills display

DISPLAY
Data formats: 1 to 4 waveforms overlaid in separate colors on 13" screen

CRT
Measurement markers: two vertical and two horizontal markers
Magnify: any portion of the display made to fill the entire display
Units:
Vertical–Volts, Ohms, reflectivity coefficient or operator-selected units
Horizontal–seconds, mm, inches or operator-selected units

AUTO-WAVEFORM MEASUREMENTS
Vertical autoscales and automatic edge finder.
Parameters calculated: period, frequency, pulse duration, risetime/falltime, pulse amplitude, base magnitude, top magnitude, preshoot, overshoot and duty cycle

WAVEFORM COMPUTATION
Averaging: sum or exponential averaging
Add/subtract: any two traces on display
Equation: formula stored in non-volatile memory; operations include integrate/differentiate, multiply/divide and FFT/IFFT

BUILT-IN STORAGE (non-volatile)
Waveforms: 9 waveforms with their setups
Setups: 9 complete plus 4 horizontal and vertical setups.

INPUT/OUTPUT
Direct digital plotting: annotated, color, plotters with plot title
Interface: RS232C and IEEE-488 standard.

COOLING
Cycle time: cools down to operating temperature in approximately 1 minute after head change completed
Type: 15 liter capacity dewar
Refrigerant: liquid helium
Operating time: 8 hours continuous operation plus 16 hours of holding without refill; coolant level automatically checked

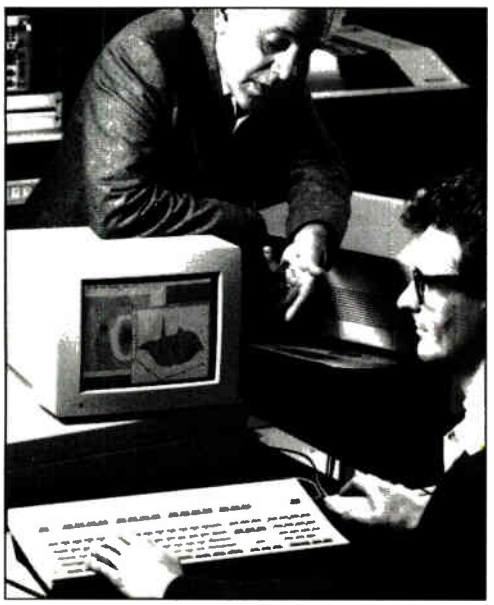
OTHER
Date/time: displayed and saved with data
Text: one line of alphanumeric text entered using front panel keys (shift) or computer
Diagnostics: self test on power up

HYPRES, Inc.
Making Superconducting Electronics a Reality

Finally, the powerful Mac II can tap all the MS-DOS programs built for the IBM machines and their clones and, significantly, should be able to penetrate the engineering work-station market.

Apple's strategy is clearly based on third parties; the new Mac was built to make it easy for others to design add-on products. "We realize the importance of putting development tools in their hands," said Apple Chairman John Sculley at the glitzy Hollywood introduction of the new machines. Already, he says, upwards of 50 suppliers have announced products, with more in the wings.

Both of the machines can handle just about any product those suppliers come up with: the Mac II, besides having six expansion slots, is at least twice as fast as the original Mac. The SE, which has one extra slot, is 20% faster.



UPSCALE. The open-architecture Macintosh II is aimed at advanced business applications.

Apple executives play down the new machines' links to IBM PCs. Sculley says he sees a world in which new software will be done in the Apple environment. Therefore, the Open Mac's ability to tap MS-DOS programs will be relatively unimportant: "IBM compatibility doesn't mean that much," he says. Third-party suppliers may disagree—there already are coprocessor boards from IBM PC supplier AST Research Inc. of Irvine, Calif. But Sculley believes most suppliers eventually will come to see Apple computers as "a better value-added platform to build on."

In the words of one industry watcher, Richard A. Shaffer, publisher of the *Computer Letter*, "Apple now has the clear upward path while MS-DOS has nothing but confusion." Shaffer adds that what MS-DOS needs is the anticipated IBM 32-bit PC based on the Intel 80386, and operating systems to fully exploit it. IBM is expected to announce its new machine as early as next month, but software packages are much further off, notes Shaffer (see p. 21).

Whatever IBM does, Apple clearly has the momentum. The Mac II, which is based on the 15.6-MHz Motorola 68020 chip and will be available later this year, is not only powerful but delivers entertainment-quality graphics at a price of less than $10,000. Some industry watchers say the machine is the future minimum benchmark for work stations.

The impressive performance of the Mac II's video interface card, which drives the high-resolution monitors, is provided largely by a souped-up semicustom chip developed by Brooktree Corp. of San Diego. Brooktree, which specializes in custom-designed digital-signal processors for back-end graphics work, revamped its Bt453 chip to run even faster than its specified 70-MHz maximum clock speed to meet Apple's video-card specifications. The Bt453 has triple 8-bit digital-to-analog converters, and the only other computers to use the Brooktree device are expensive high-end work stations.

With this video card and an expansion kit, both Mac II options, the computer can generate up to 256 colors or shades of gray from a palette of more than 16 million colors. The color monitor has a resolution of 640 by 480 pixels.

The operating system software has passed through seven revisions. But it is about ready to be frozen in the Mac II's read-only memory, notes Charles Farnham, who runs a Cupertino, Calif., on-line information service devoted to the Macintosh and aimed at developers. It needs only some final fine-tuning before the first shipments, which are due to go out in about six weeks, he says.

What the new machines lack is an upgrade path from the Macintosh 512 and Plus computers to Open Mac standards. But Apple points out that when it came out with upward options for previous models, users chose to buy the new equipment anyhow. "They [Apple] are probably right about that," notes *Computer Letter*'s Shaffer. As to the current lack of multitasking software suitable for engineering-work-station chores, Sculley and others say these programs will come along soon.

Sculley predicts the Mac II won't get to full speed until next year, when production reaches volume levels and enhancements come rolling in. But Apple-watcher Farnham says he thinks that the ingredients for success already are in place. The Mac II, he says, is "everything they should have done. They hit 100%." *–Larry Waller*

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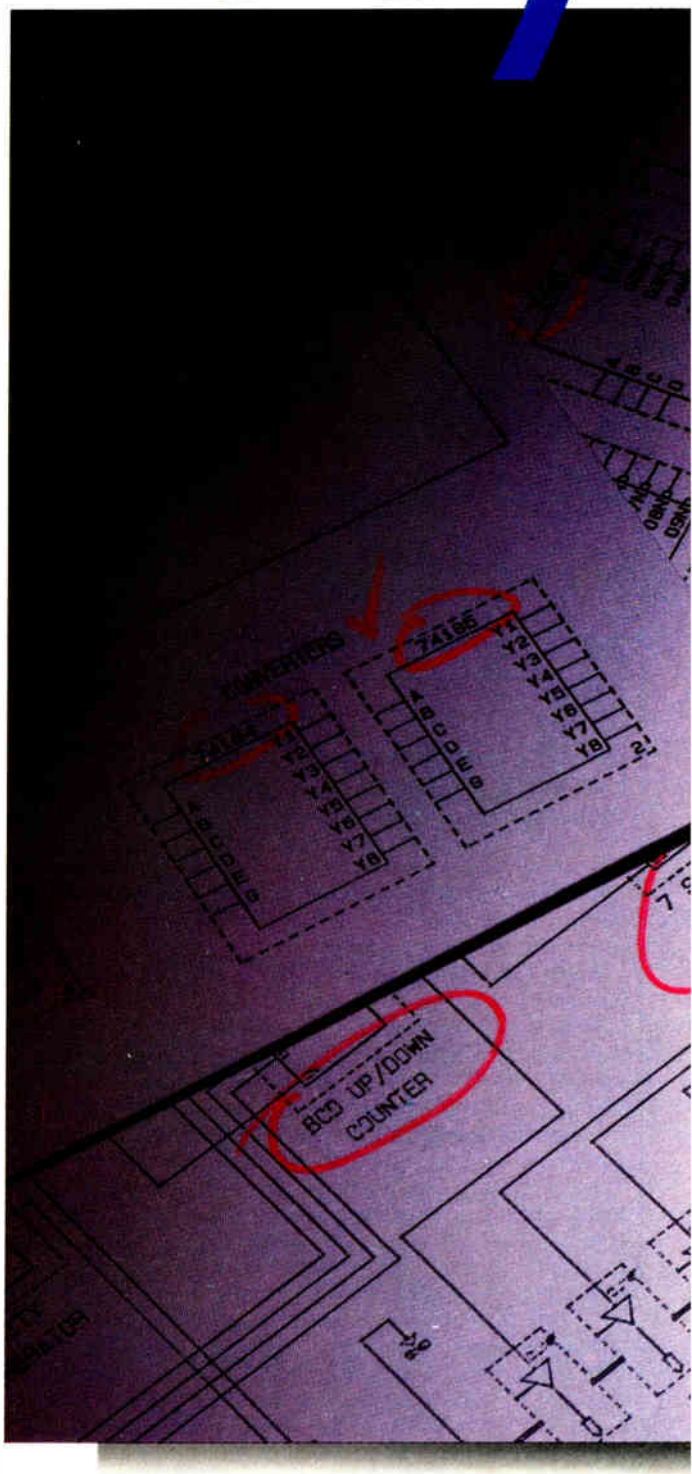

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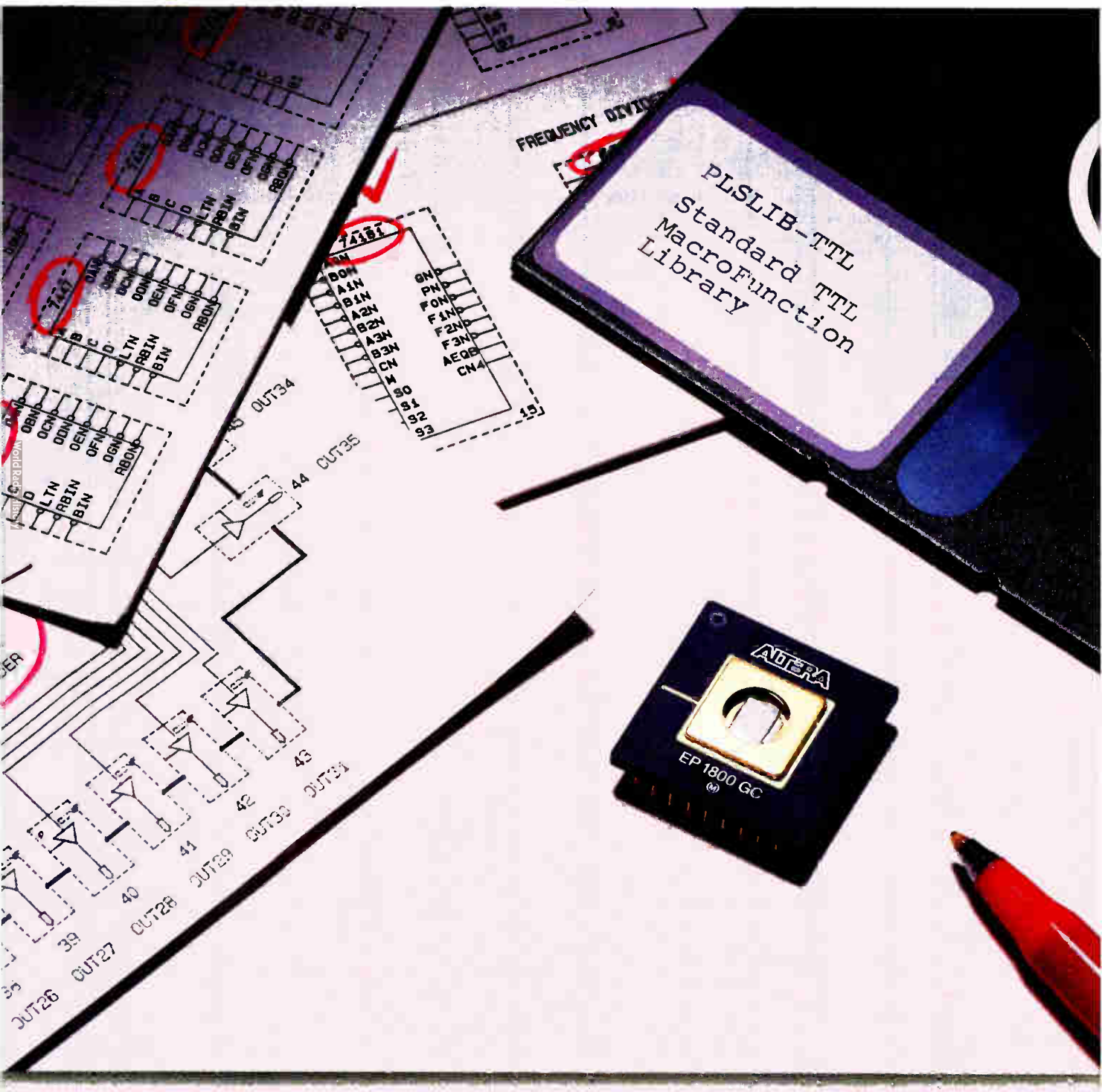


NAVIGATING BY SATELLITE GETS CHEAPER

SUNNYVALE, CALIF.

For years everyone talked about how the Pentagon's Global Positioning System would revolutionize the navigation of ships, planes, and even vehicles—both military and commercial. But even though the GPS system would give them a position fix anywhere to within 100 meters, civilian users have not exactly clamored to buy receivers to pick up the positioning signals from the satellite constellation. The sets simply cost too much. But now that may be changing.

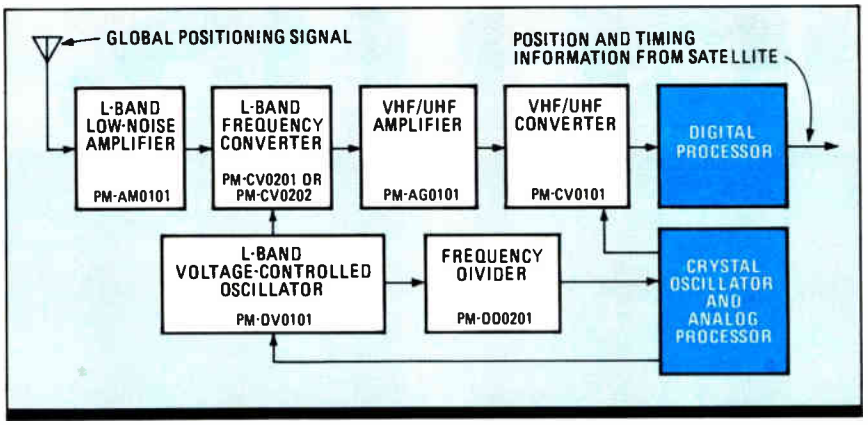
Pacific Monolithics Inc. of Sunnyvale, Calif., is in the sample stage with a set of six gallium arsenide microwave integrated circuits that can be used along with two or three commonly available glue components to design GPS front ends that will be affordable to a far wider spectrum of users.

GPS receivers now cost $15,000 or more. After excluding the cost of the antenna and the control and display elements from that total, as much as half the cost of the set is eaten up by the discrete microwave circuits that are now being used, Pacific Monolithics engineers estimate. At even "a moderate production rate of a few thousand per year," the new chips could drive down front-end prices to a fifth of what they are now, predicts Douglas G. Lockie, senior systems scientist at the company.

In a front end built with the new chips, signals from the GPS satellite—at 1227.6 MHz (restricted mainly to military use) or 1575.4 MHz—first would be amplified and down-converted to an intermediate frequency within the range of 50 MHz to 600 MHz.

Three additional circuits—an automatic gain-controlled amplifier, a vhf/uhf converter, and a frequency divider—convert the GPS signal to a frequency low enough for detection with a frequency discriminator. The frequency out of the front end should be 5 MHz to 30 MHz, says Pang Ho, vice president of engineering. At these relatively low frequencies, detection and digital signal processing take over to decode the satellite messages and glean the navigation and time-reference information from the analog waveform.

SAME PROCESS. For these new ICs, Pacific Monolithics put to work the same 1-μm depletion-mode metal-semiconductor FET process used for the company's C-band low-noise-block down converter [*Electronics Week*, May 27, 1985, p. 48]. The chip set—each about 1 mm on a side—will be marketed as surface-mounted devices for uncomplicated placement on printed-circuit boards. Bare dice will also be available.



UP FRONT. The six front-end MMICs at the left, hooked up with lower-frequency and digital circuits like those at the right, could considerably reduce the cost of GPS receivers.

The first chip that the radio-frequency signal beamed from a GPS satellite sees is a two-stage low-noise amplifier (see figure). This IC achieves 20 dB of gain at a 1.9 dB noise figure while drawing 21 mA from an 8-V power supply.

Next, the signal is filtered and converted to a first i-f with an L-band frequency converter. Pacific Monolithics provides two converters as design options. In addition to frequency conversion the chips perform on-chip rf amplification, local oscillator buffering, and i-f amplification. Local-oscillator buffering reduces the power requirement at the LO port and supplies the mixer with a constant power level. Because it is so close to the mixer diodes, the LO amplifier also reduces phase ripple caused by impedance mismatch. The i-f amplifiers on the converter chip increase the output third-order intercept point, which increases the system's resistance to jamming in addition to upping system gain and output power. *–Terry Feldt*

MOS AND THYRISTORS MAKE A LOVELY COUPLE

MUNICH

Linking the best of two worlds, a new kind of power device in development on both sides of the Atlantic seeks to marry the high-current and high-voltage handling capabilities of a thyristor to the good control characteristics of an MOS transistor, and thus cut the cost of thyristor-based power equipment. The independent projects, using different approaches, are under way in West Germany at Siemens AG and in the U. S. at General Electric Co.

The device, called a MOS gate-turn-off, or GTO, thyristor, should result in lower equipment costs because the control circuitry for turning it off, unlike that used with conventional GTO thyristors, is on-chip. Researchers at Siemens report that with a chip area of 0.1 cm^2, the first functional laboratory units switch currents of 5 A and block voltages of 1,500 V without using a snubber, a sort of RC network. With a snubber, they switch much higher currents.

Similar work was reported late last year at the International Electron Device Meeting by GE researchers from Schenectady, N. Y. However, there are basic differences. Both teams use MOS transistors to short and shut off the thyristor. But GE's approach involves epitaxy, whose fabrication methods can cause problems in attaining high blocking voltages. Siemens, on the other hand, bases its device on a technology using the same large-area silicon pellets as are employed in GTOs and thyristors. That makes possible high blocking voltages.

Continuing work at the Siemen's Corporate Research Laboratories in Munich should lead to MOS-GTO thyristors that can handle up to 4 kV and have a chip area large enough to switch several thousand amperes, says Michael Stoisiek, who is developing the device with Roland Sittig and Dietmar Theis. It could enter production within a few years, Theis says.

Ordinarily, for switching currents of

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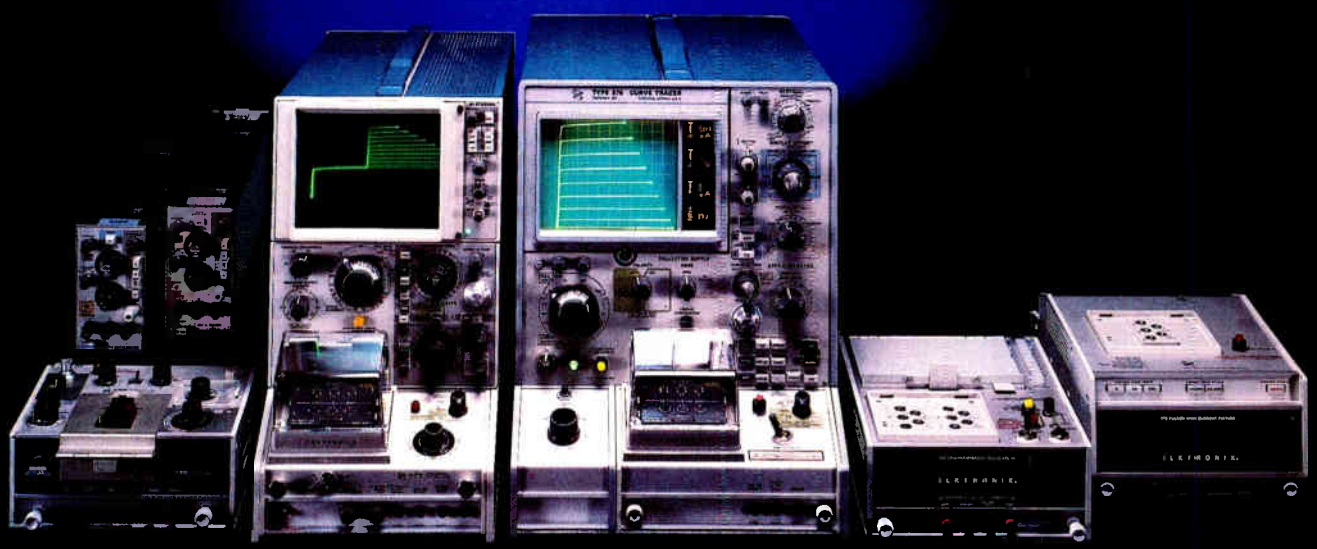

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more than 1,000 A and blocking voltages of several thousand volts, the classic thyristor is unbeatable. But this technologically simple component has one shortcoming: once it conducts, the thyristor shuts off only when the current flowing through it is interrupted for 100 μs or more. The interruption process calls for a second thyristor circuit.

That's where the GTO thyristor, a power component proposed in the U. S. in the early 1960s, comes in. It has a negative gate current, one that flows the other way from the turn-on, or ignition, current, to turn off the device. But this current may amount to several hundred amperes, which means extensive control circuitry that is external to the GTO.

The new part handles all of that. Based on the idea of making the short-circuits inherent in a thyristor switchable, the device uses an integrated MOS transistor to control the shorts. Hence the name MOS-GTO thyristor.

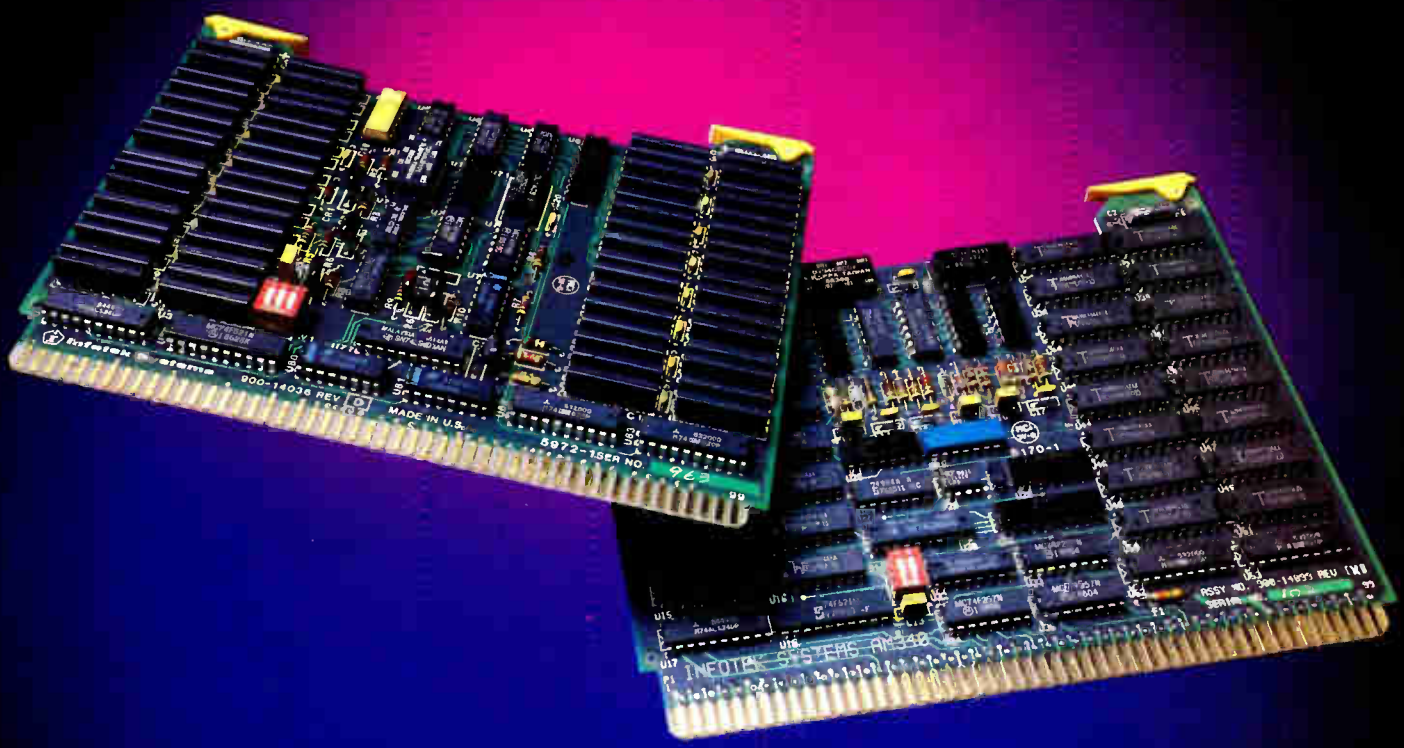
SHORT. When it switches off, the high negative gate, or turn-off, current is short-circuited around the thyristor's base-emitter structure and fed via the emitter contact to the load circuit. Short-circuiting the current is the MOS transistor integrated onto the silicon pellet. It must handle several hundred amperes, but the current lasts only from about 100 ns to 1 μs and has no effect on the thyristor's gate-control circuit, as it flows only in the silicon pellet.

To turn off the MOS-GTO thyristor, Stoisiek explains, all that is needed is the switching current for the MOS transistor, that is, the current for charging its gate capacitance. Because of the fairly large gate area and the fast switching time required, the switching current must be several amperes, but this is still some 100 times less than the turn-off current for a conventional GTO.

In device fabrication, Stoisiek and his associates are using their company's Sipmos (for Siemens power MOS) technology, a 5-μm, self-aligning technology allowing the fabrication of power devices that combine high voltage ratings with a low forward resistance. For the MOS-GTO-thyristor, this technology must be refined so that it can cope with the typically 1.5-mm-thick wafers needed for high-power thyristors. *–John Gosch*

IMPROVE YOUR MEMORY

New Infotek 8 and 4 MByte Memory Cards Give Lowest Cost per Byte for HP 200/300.



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For the many applications requiring 4 MBytes of memory, Infotek again uses 1 MByte DRAMs in single in-line packages to reduce costs. That means you can now have Infotek quality in the lowest-cost 4 MByte board available! Of course, Infotek's popular 1 MByte and 2 MByte memories are also available.

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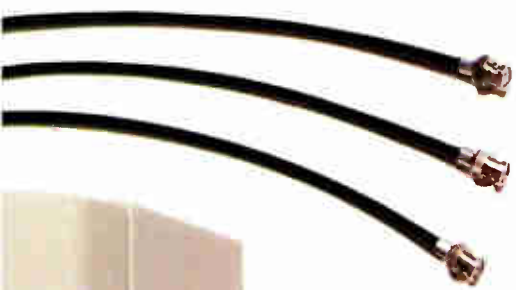
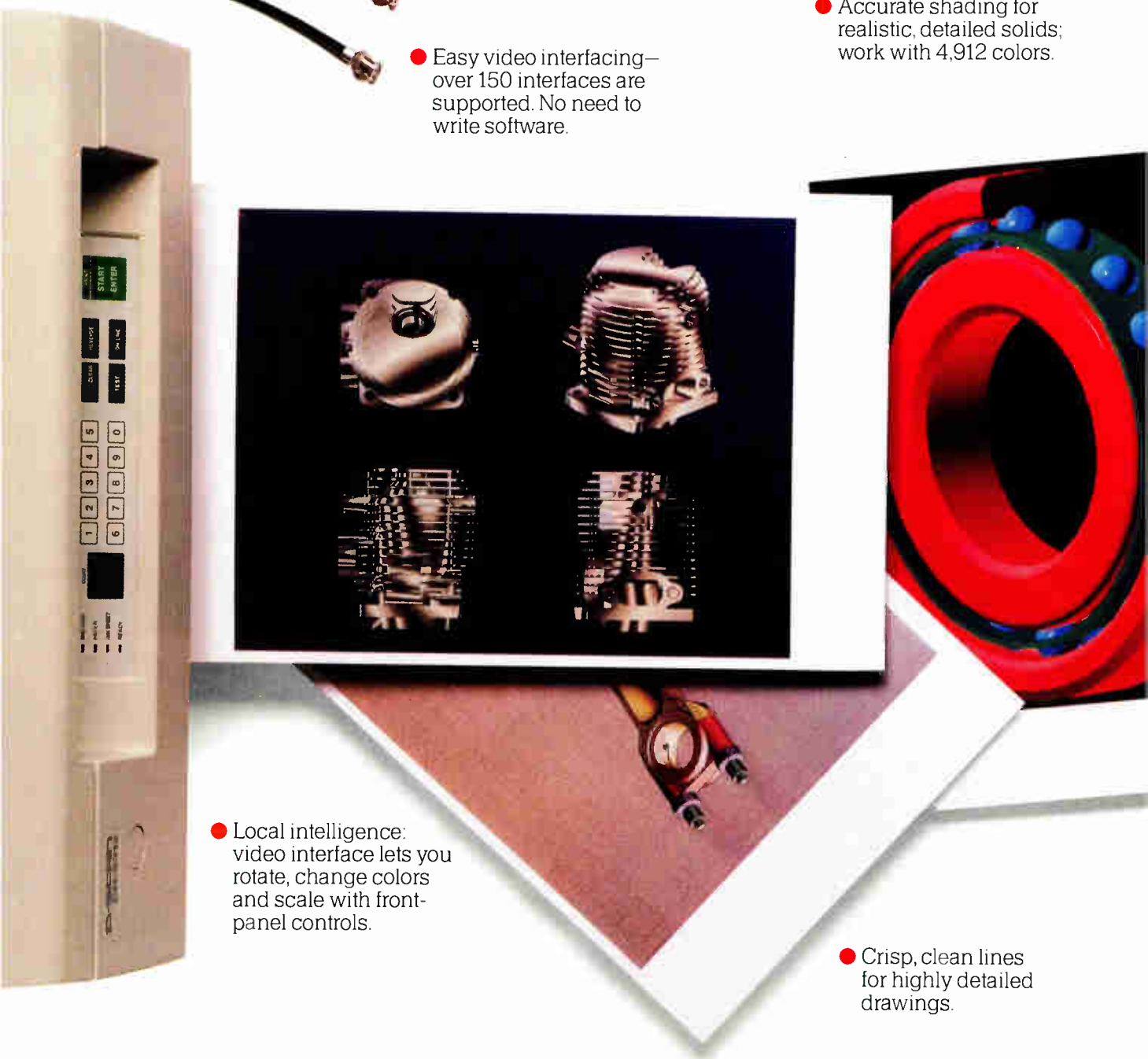


● Easy video interfacing—over 150 interfaces are supported. No need to write software.

● Accurate shading for realistic, detailed solids; work with 4,912 colors.



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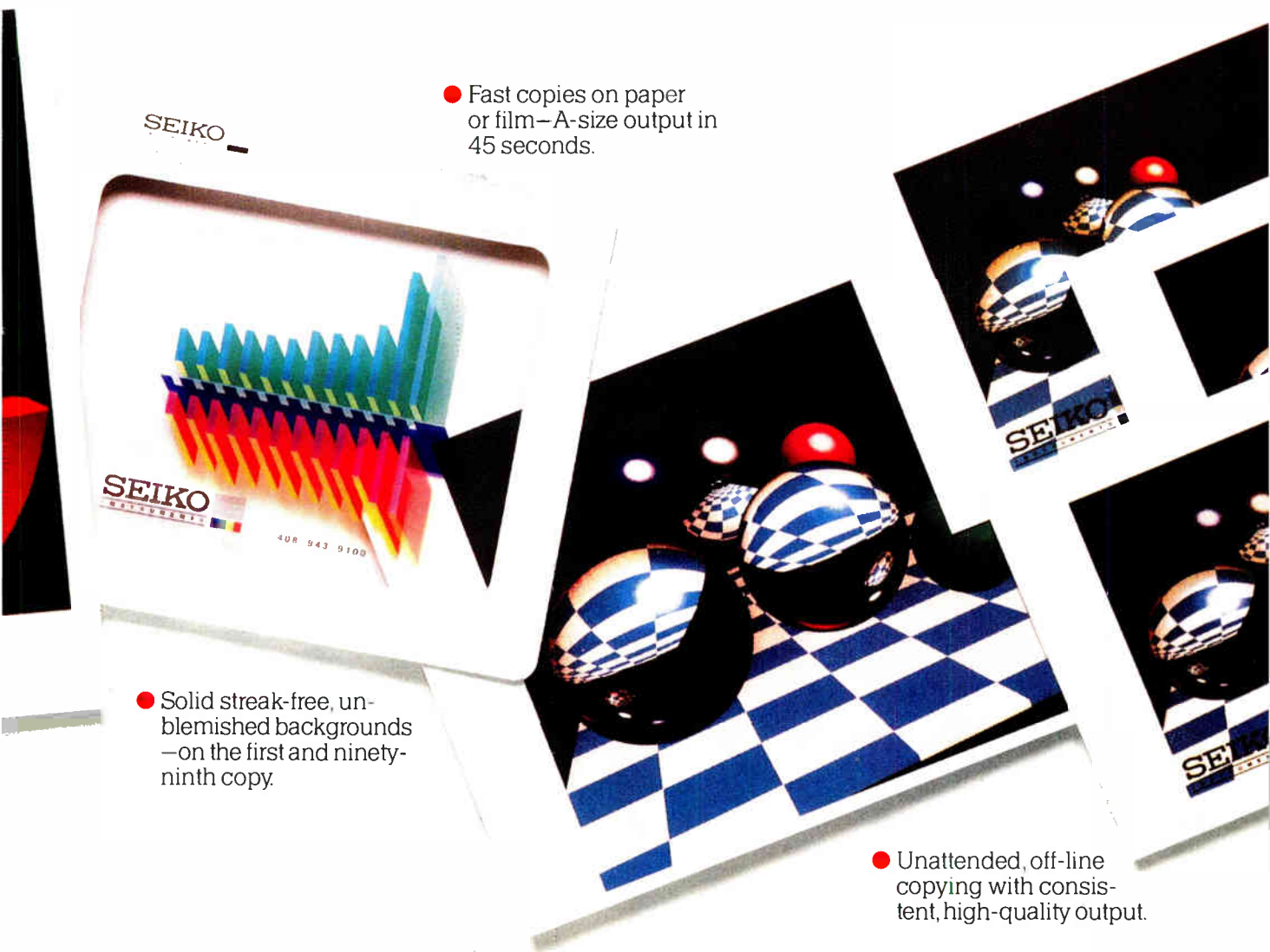

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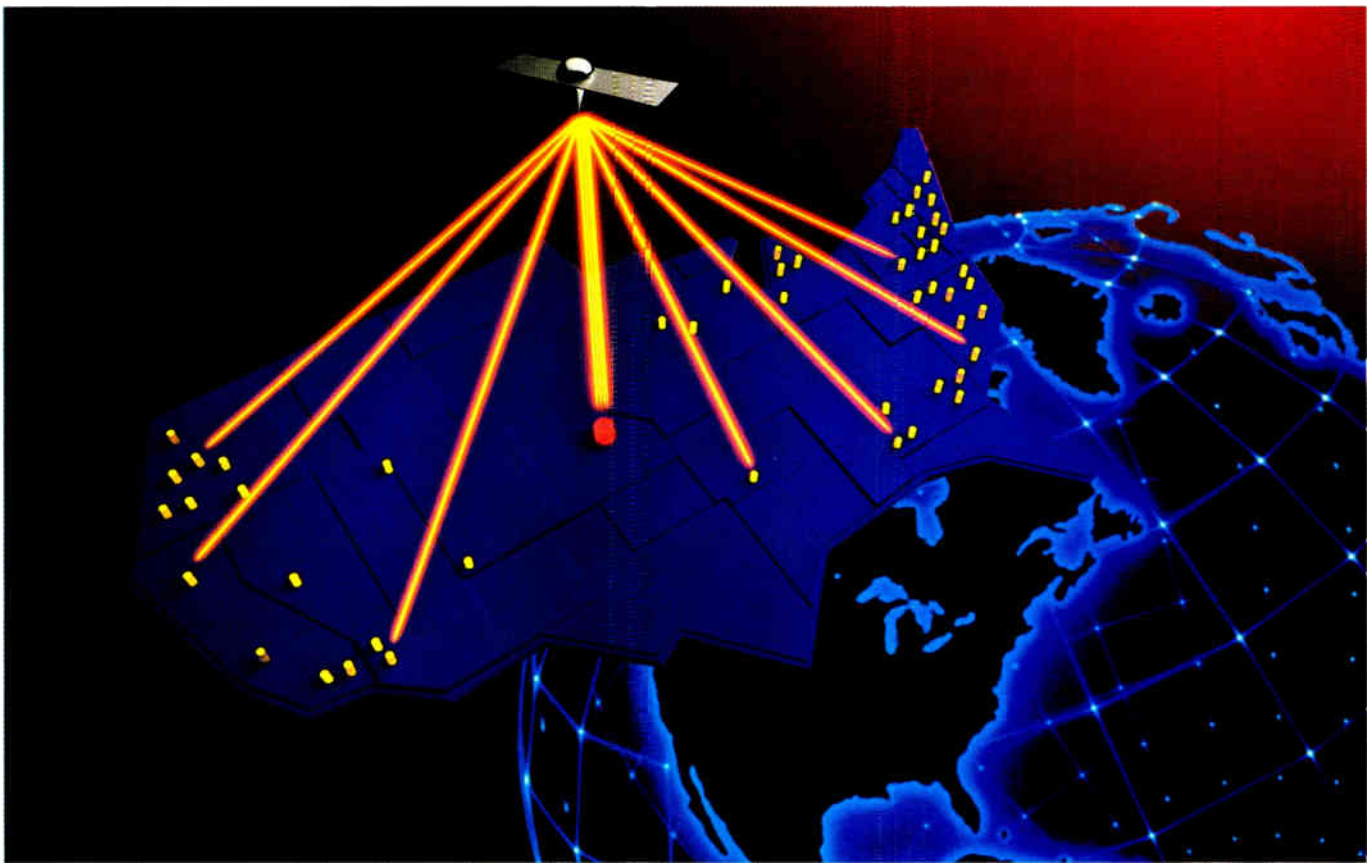

"NEXTAR" MINI EARTH STATION NETWORK.

Private Ku-band satellite communications networks using mini earth stations on customer premises are poised to take off in the US.

Our advanced mini earth station networking system "NEXTAR" offers unprecedented flexibility for transaction-oriented businesses typically using POS, ECR and ATM systems.

The NEXTAR provides interactive data communications between a central hub and many widely-dispersed remote mini earth stations in a "star" network topology. Our exclusive Adaptive Assignment TDMA system automatically assigns the best pathway for each data message to minimize response time for short interactive messages and increase throughput during long batch transmission. NEXTAR transparently interconnects existing remote terminals and the host's front-end processor thanks to its intelligent network features.

The mini earth station, a 1.2 or 1.8m antenna with an integral RF package and compact indoor unit, takes less than a workday to install. Site selection and licensing are also simplified with the Ku-band. The central hub station with comprehensive monitoring, control and diagnostic capabilities can be located adjacent to a data center or at a shared site.

The NEXTAR network can be custom-tailored to a user's exacting needs—data rates from 75bps to 56Kbps plus voice and video capability. It eliminates the wasted transmission capacity and high cost of traditional alternatives.

NUMBER 137

1.3-MICRON OEICs FOR GIGA-BIT LINKS.

Scientists at the NEC Optoelectronics Research Laboratory have successfully tested the world's first optoelectronic ICs to operate in the 1.3μm band at data rates of 1.2Gbps.

The optical transmitter and receiver chip pair set records of a 12-km communication at 1.2Gbps with a 7.7dB margin, and 22-km transmission at 565Mbps with a 9.9dB margin in the experiment using a single-mode fiber.

The new light-emitting chip incorporates a 1.3μm DC-PBH (double-channel planar buried heterostructure) laser diode and three InGaAsP/InP hetero-junction bipolar transistors on the same InP substrate. Modulation up to 2Gbps is possible in NRZ mode. A peak output of 20mW was marked at 1Gbps.

The optical receiver integrates a PIN photo diode and three low-noise InGaAsP junction FETs on a single chip for sensitivity of −14dBm at 1.2Gbps.

NEC's new OEIC pair will be the ideal workhorse in medium- or short-distance ultra-high speed links including LANs, local subscriber loops and interconnections of computers and peripherals because it promises much lower cost and smaller size than prevalent discrete devices.

These OEIC devices will reach the market within a few years.

NEAX61 NOW IN SERVICE AT 1,002 EXCHANGES.

Our NEAX61 digital switching system continues to play a key role in the phenomenal expansion of digital networks around the world.

Since its implementation in 1979 the NEAX61 has captured the attention of telecommunications administrators globewide for its sophisticated modular hardware and software, advanced service features, and full operation and maintenance support.

Today there are NEAX61 switches in service at 1,002 exchanges in 37 nations—more than 5 million equivalent subscriber lines in all. With recent orders from New Zealand (400,000 lines), Hong Kong (600,000 lines) and Venezuela (330,000 lines) the aggregate orders received now exceeds 10 million equivalent subscriber lines.

NEC OPTICAL REPEATERS GO TRANSPACIFIC AND SUBMARINE.

The trend in transoceanic submarine cable systems is undeniably "optical". The use of fiber optic transmission technology increases capacity, extends repeater span and ensures compatibility with land-based digital networks.

Under a contract awarded by KDD, Japan's leading international telecommunications network, NEC is manufacturing optical submersible repeaters and optical terminal equipment for the third Trans-Pacific Cable (TPC-3) which will link Hawaii and Japan with a branch to Guam.

The TPC-3, to be completed in 1988 and owned by 22 telephone operating companies in 10 countries, will have two 280Mbps systems, offering a total capacity equivalent to 7,560 telephone channels—a dramatic increase from 138 channels with TPC-1 and 845 channels with TPC-2.

Incorporating our 1.3μm DC-PBH (double-channel planar buried heterostructure) laser diodes and newly-developed high-speed monolithic ICs, the optical repeaters are designed to maintain high reliability on the ocean floor at a depth up to 8,000 meters.

NEC

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INTERNATIONAL NEWSLETTER

SIEMENS JOINS THE SELECT 4-Mb DRAM CLUB

Add Siemens AG to the short but growing list of companies that have produced working 4-Mb dynamic random-access memory chips. Siemens, the first European company to break the 4-Mb barrier, will join the likes of IBM Corp. and Texas Instruments Inc. in this select club when it announces on April 1 at the Industrial Fair in Hanover, West Germany, that it has built laboratory samples of the 4-Mb devices. The announcement is the latest result of Siemens' "Megaproject," in which the company has been rushing to climb the learning curve in high-density silicon technology. The devices use 0.8-μm CMOS technology and measure only 91 mm^2—less than twice the size of Siemens' 54 mm^2 1-Mb DRAM. The 4-Mb chips employ trench-type cells that extend about 4 μm deep. Siemens says the three-dimensional design helps keep the cell surface small, at just 5 μm^2. Siemens says samples may be available by the end of next year. □

A NEW CD FORMAT STORES BOTH DIGITAL AUDIO AND VIDEO

Digital laser video is heating up. A trio of consumer electronics giants is teaming up to support a new form of compact disk that can hold up to 5 minutes of video and more than 20 minutes of digital audio on a single 12-cm (4¾-in.) disk. Philips, Matsushita, and Nippon Gakki, which markets products in the U. S. under its Yamaha label, will jointly develop this new system, sharing one another's technologies. Their action adds spice to the excitement generated by General Electric Co.'s David Sarnoff Research Center, which says it has developed a way to put more than an hour of full-motion video on a 5¼-in. CD (see story, p. 33). The 12-cm disks have two bands: an outer band that can record up to 5 minutes of combined audio and video, and an inner set of tracks that can store up to 20 minutes of audio. The three firms will market the system, which is compatible with the current audio CD standard, under the name CD-V (for compact disk video) beginning this fall. They say the 12-cm disk will be an ideal medium for popular music videos, and major American and European record companies have already pledged their support to the format. □

TOSHIBA WILL CHASE FAIRCHILD'S FAST FAMILY WITH LOW-POWER BiCMOS

Toshiba Corp. is developing a series of BiCMOS logic devices, making it the first company in the world to apply BiCMOS technology to glue logic circuitry. The new chips will be pin- and performance-compatible with Fairchild's FAST chip family, the company says. Output levels of 24, 48, and 64 mA will be the same as for corresponding FAST parts, and propagation delays will also be identical at 3 ns. The input and logic circuits are implemented in CMOS, and the output circuits are bipolar. Operating power is said to be only one-fifth and standby power one-tenth that of bipolar prototypes. Although only bus drivers will be available initially, Toshiba expects to be supplying 50 different parts worldwide before year's end. □

ALPS TAKES AIM AT IBM's PC AT WITH A 16-MHz 80386-BASED MACHINE

Alps Electric Co. is the latest company to develop a personal computer based on Intel Corp.'s 32-bit 80386 microprocessor. The Alps CP-EX is compatible with IBM Corp.'s PC AT but has three times the processing power, thanks to its 32-bit memory bus and a 16-MHz clock rate. Developed at Alps' Yokohama Division, the machine comes with 2 megabytes of system memory, expandable to 8 megabytes, and features no-wait states. Serial and parallel interfaces are standard, and expansion slots support two 8-bit cards and four 16-bit boards. Alps is planning to sell the machine to other vendors for sale under private labels. □

INTERNATIONAL NEWSLETTER

NEC WON'T BE OFFERING ITS SPICED-UP V30 CPU TO U. S. SYSTEMS HOUSES

Engineers in the U. S. are going to sit up and take notice when word spreads about the latest enhancement to NEC's popular V30 microprocessor—but that's all they'll be able to do. The new CPU, called the μPD9002, provides higher-speed and enhanced graphics; it includes on-chip direct memory access, an interrupt controller, and a timer; and it runs the full Z-80 instruction set. It will not, however, be available in the U. S., at least for now. Despite the V30's popularity among U. S. systems designers, that chip has not found its way into many U. S. products, mainly because U. S. companies have tried to steer clear of NEC's ongoing copyright battle over the chip's microcode with Intel Corp., Santa Clara, Calif. So NEC, of Tokyo, will initially use the chip only in its PC88VA, a 16-bit home computer for the Japanese market. □

JAPANESE CONTINUE THEIR PUSH TO LIMIT COMPETITION FOR KDD

The furor over who will be allowed to compete in Japan's market for international telephone service [*Electronics*, Feb. 19, 1987, p. 46] continues. At issue is who will be allowed to compete with Kokusai Denshin Denwa Co., the Tokyo company that currently has a monopoly over the Japanese international telecom market, and how much foreign companies will be allowed to invest in competitive ventures. Now Japan's largest independent business association, the Japan Federation of Economic Organizations, is joining the fray. It is supporting the government's Ministry of Posts and Communications in its effort to get International Digital Communications Planning Inc. and International Telecom Japan Inc., both of Tokyo, to merge. The ministry wants to limit KDD's competition to a single company. Fumio Watanabe, chairman of the federation's Committee on Information and Telecommunication Policy, has asked International Digital Communications shareholders to persuade Cable & Wireless of the UK to reduce its 20% equity to clear the way for a merger. Watanabe says Cable & Wireless' equity should be less than 3%, thereby eliminating the British company's management role. □

ITT WILL BE FIRST TO MAKE DECODER CHIPS FOR D2-MAC TV STANDARD

The ITT Semiconductors Group will be the first company to turn out chips for decoding satellite TV signals based on France's D2-MAC standard, which provides better pictures and sound than conventional terrestrial standards such as PAL and NTSC. Production of the single-chip decoder will start at the end of this month, and European and Japanese TV makers are lining up for samples, according to sources at ITT subsidiary Intermetall GmbH in Freiburg, West Germany, where the devices will be made. The chip uses 1.5-μm CMOS technology and packs 150,000 transistors into a 7-by-7.5-mm area. Programming supporting the D2-MAC signals will be broadcast by a new German-built satellitte, the TV-SAT, which will be launched in late August or early September on a French Ariane booster rocket. □

PLESSEY WINS A FOREIGN ORDER FOR ITS SYSTEM X TELECOM SWITCH

Plessey Co. has finally won its first major export contract for the British System X digital telephone system, which so far has been a major failure in the international market. By winning a $22.5 million contract from Telecom Colombia, the Colombian national telephone company in Bogota, Plessey beat out Ericsson, NEC, Fujitsu, and Italtel. The company is hoping the sale, which includes 13 telephone exchanges supporting 68,000 lines, will spur further success abroad. Until now, System X had only been installed by British Telecom and the independent Hull telephone authority in England, and on the tiny Caribbean island of St. Vincent. □

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Circle 129 on reader service card

INTERNATIONAL WEEK

JAPAN TELECOM EXPORTS DROP 10%

Japan telecommunications exports declined 10.3% last year, from $3.9 billion to $3.5 billion, because of a slide in shipments to the U.S., according to the Communications Industry Association of Japan. Exports to the U.S. decreased from $1.9 billion in 1985 to $1.4 billion in part because of the stronger yen and import restraints. But exports to Europe increased by 27.4%, from $503.4 million in 1985 to $641.1 million in 1986, and exports to Central and South America rose by 22.1%, from $156.2 million in 1985 to $190.7 million. Meanwhile, total telecommunications imports in 1986 amounted to $230.9 million, which is about the same as the previous year.

SIEMENS SETS UP CAD SYSTEM IN UK

Siemens AG, after installing its Venus VLSI design system at 18 universities in West Germany, has established the first such system abroad—at Uxbridge's Brunel University. The Venus computer-aided design system, considered to be Europe's most advanced, allows chip designers to lay out application-specific integrated circuits with up to 250,000 transistors per chip. The Brunel system supports VLSI designs in emitter-coupled logic and CMOS technology with either 3-, 2-, or 1.5-μm structures.

W. GERMAN BOOM IN COMPUTERS SLOWS

The exceptionally high growth rates of West Germany's information- and communications-technology sectors are beginning to slow down. After a 20% spurt in 1985, sales last year inched up only 4.6% to about $20 billion, of which the data-processing industry accounted for $9.5 billion and telecommunications for $10.6 billion. Industry observers attribute the slowdown in part to users' reluctance to invest in new equipment before integrated services digital networks are introduced over the next few years.

NTT, CORNING SIGN JOINT R&D PACT

Nippon Telegraph and Telephone Corp., Tokyo, and Corning Glass Works, of Corning, N.Y., will conduct joint research at their facilities on fluoride glasses for next-generation optical-fiber communications links. The research will focus on the characteristics of the glasses, including stability against recrystallization and chemical and mechanical durability.

EXPERIMENTS SET FOR SATELLITE

The European Space Agency and Eutelsat, the European telecommunications satellite consortium, will jointly develop telecommunications experiments and demonstrations for the Olympus satellite [*Electronics*, Nov. 27, 1986, p. 48]. They will explore the use of a four-channel repeater at 14-12-GHz and a two-channel repeater at 30-20-GHz in a fixed-satellite service. Olympus, to be launched in 1988, will demonstrate new applications in communications and broadcasting.

OPTICAL LINK IS THE LONGEST OF ITS TYPE

The longest commercial unrepeated underwater optical-fiber link in the world will relay telecommunications data between northern England and the Isle of Man by late this year. The 90-km link is part of a plan to convert the island network to digital operation by 1990. British Telecom and its Isle of Man subsidiary, Manx Telecom, which signed a $4.5 million contract with STC Ltd. to produce the cable, already have started to install optical-fiber land cable to link its exchanges, and they plan to install 11 digital local exchanges.

VOICE-RECOGNITION CHIPS BY TOSHIBA

Toshiba Corp. of Tokyo has developed a high-performance voice-recognition chip set with three CMOS large-scale integration chips that shows better than 95% recognition accuracy—even without training the system to recognize specific voices. The three chips are an analog signal processor for extracting features of the input voice, a digital signal processor for computing similarity between the input voice's features and reference patterns, and a system controller. Toshiba will sell the chip set in Japan by the end of the year for less than $65, but says it does not plan to develop a system for other languages.

MICROSOFT, SEAT, OLIVETTI INK PACT

Italy's Ing. C. Olivetti and Co., SEAT SpA, and Microsoft Corp., of Redmond, Wash., are forming a joint venture in Rome to develop optical-disk software applications for the European market. Eikon, which will start operations in May, will design, develop, produce, and market optical media software applications and related systems solutions. Eikon's initial technology will be licensed from Microsoft.

JOINT VENTURE TO DEVELOP LCDs

France's Thomson-CSF and West Germany's VDO Adolf Schindling GmbH have established Eurodisplay in France to develop full-color liquid-crystal displays. The company, in which Thomson has an 80% and VDO a 20% share, will use the display, for example, in monitoring and display equipment, cockpit information systems and other industrial applications. Contributing its know-how to the venture will be the U.S.'s General Electric Co., the first company to produce LCDs for aircraft.

ERICSSON SELLS TO MEXICO, VENEZUELA

Ericsson Telecom will supply a total of $220 million worth of digital telephone exchanges and other telecommunications equipment to Mexico and Venezuela. Most of the equipment is for Mexico and will be made mainly by Ericsson's Mexican subsidiary, Teleindustria Ericsson SA. The largest single order is for $100 million from Telefonos de Mexico SA for local, transit, and tandem exchanges and extensions to existing exchanges.

PHILIPS' REVENUES DECLINE BY 8%

Philips International NV says sales fell 8% last year, from about 60 billion guilders in 1985 to about 55 billion guilders in 1986. The Dutch company attributes the drop to the devaluation of the dollar compared to major European currencies, which has made Philips products more expensive on U.S. markets. Net profits increased slightly, from 919 million guilders in 1985 to about 1 billion guilders in 1986.

S. KOREA COMPUTER EXPORTS TO RISE 39%

The South Korean computer industry is expected to export about $1 billion worth of computer-related products this year, up 39% from 1986, according to government and business sources. Shipments of peripheral parts are expected to expand, and exports of 8- and 16-bit South Korean personal computers are expected to grow from $390 million in 1986 to $650 million this year.

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INTERNATIONAL PRODUCTS

EMBEDDED SCSI INTERFACE DOUBLES DISK TRANSFER SPEED

Y-E DATA'S 3½-in. DRIVE ATTAINS 1.5 MEGABYTES PER SECOND

A 3½-in. Winchester disk drive with 53.3 megabytes of unformatted capacity and an embedded Small Computer Systems Interface from Y-E Data Inc. offers more than double the data-transfer rates of competing systems.

By using a SCSI interface instead of the ST506 Seagate Technology interface commonly used on 3½-in. drives, the YD-3541 attains a maximum data-transfer rate of 1.5 megabytes/s, compared with 625-K bytes/s with the ST506 interface. Eight-bit data transfer on the command level also helps enhance high-speed data transmission.

UNBURDENS HOST. The embedded SCSI interface also reduces the burden on the host bus, making it easier to develop applications software. System costs are reduced, because the embedded controller replaces discrete devices.

Large-scale-integrated-circuit technology was used to create the high-performance SCSI controller, which is mounted on the drive's printed-circuit board. Basic design and development of the drive was done by Gruczelak & Associates, Newbury Park, Calif.

The controller is compatible with the American National Standards Institute's Advanced Data Communication Control Procedure X3.131 Common Command Set and also includes the CCS standardized by ANSI last July. It supports 13 CCS option commands, and commands can be added or revised to suit user requirements.

The controller can be connected to as many as eight hosts or peripherals, facilitating its use in multitasking applications. Arbitration and disconnection/reconnection are supported.

FOUR DISKS. The system's large data-storage capacity, despite its 3½-in. configuration, is made possible by using four disks. Formatted capacity of the YD-3541 is 45 megabytes. Average seek time, including settling time, is less than 35 ms. A high-performance servo system was designed for the drive to compensate for disk dimensional changes over the temperature range of 5°C to 50°C.

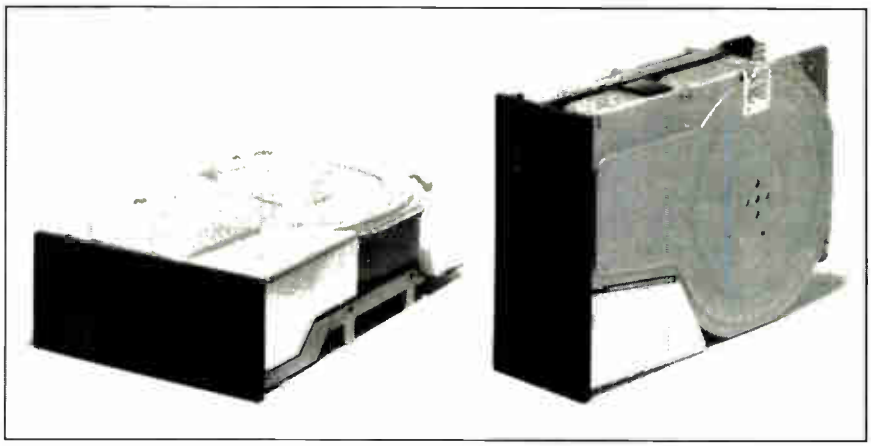
The data heads automatically seek the correct location on the disk and are retracted on power-down to protect the heads and the disks from shock and vibration. The drive safely withstands nonoperating shock in gravitational force up to 40 g, but operating shock must be limited to 10 g. It offers a mean-time-between-failure rating of 20,000 power-on hours. Measuring 101.6-by-41.3-by-41.4-mm, it weighs 0.9 kg.

The YD-3541 will be marketed worldwide by C. Itoh and Co. Ltd. of Japan, through its overseas offices. Delivery of samples is scheduled to begin in April at a price of $2,270. Volume production is scheduled to begin in July at a rate of 10,000 drives per month.

–Charles L. Cohen

C. Itoh Electronics Co. Ltd., Beacon House, 26-28 Worple Rd., Wimbledon SW19 4EE UK.
Phone 44-1-946-4960 [Circle 501]

C. Itoh Electronics GmbH, Rosstrase 96, 4000, Dusseldorf 30, West Germany.
Phone 49-211-454980 [Circle 502]



EXPANSION. The embedded SCSI controller can interface with eight hosts.

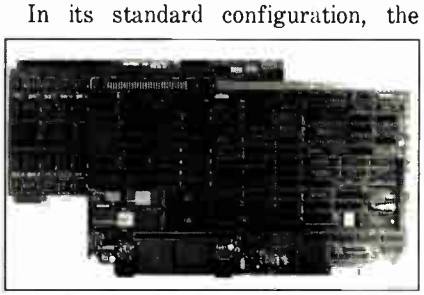
GRAPHICS BOARD RUNS 35,000 VECTORS/S

A color-graphics multiprocessor board for personal computers based on the Multibus I computer board enables users to create images with a resolution of 1,280 pixels by 1,024 lines at up to 35,000 vectors per second. With Matrox Systems Ltd.'s MG-1280, 256 colors can be displayed simultaneously from a palette of over 16 million.

In its standard configuration, the MG-1280 generates a single image with 8 bits per pixel. Two optional configurations are available, one producing two independent images with 4 bits per pixel, the other four independent images with 2 bits per pixel. All contain 2 megabytes of RAM.

In unit purchases the board costs $4,995 (U.S.). Samples will be available in April.

Matrox Electronic Systems Ltd., 1055 St. Regis Blvd., Dorval, Quebec H9P 2T4, Canada.
Phone (514) 685-2630 [Circle 701]



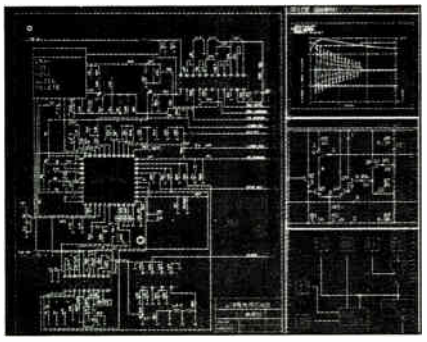
SOFTWARE HANDLES ANALOG DESIGN

The Structured Electronics Engineering Design System software from Sanyo Tool Corp. handles analog circuit design and can be adapted to accommodate large-scale digital integrated circuit en-

gineering. It features a graphics driver that improves interaction between the software and the user and employs artificial intelligence for improved circuit editing.

The SEEDS software package was initially developed by Sanyo Electric Co. in cooperation with IBM Japan Ltd. for use by Sanyo's manufacturing divisions. It is being marketed as part of a package that includes an IBM Corp. 370 and associated software, plus an IBM 5080 graphics system. Sanyo plans to sell about 20 systems a year at an initial price of 35 million yen each. Delivery in Japan takes at least a month.

Sanyo Tool Corp., 1-1-71 Naka Meguro, Meguro-ku, Tokyo, Japan.
Phone 81-3-715-2655 [Circle 702]



POWER SUPPLY HAS TRUE PARALLEL MODE

Outputs on the PL320 Quad-Mode Dual, a 30-V, 2-A power supply, can be configured in any of five modes, including true parallel.

In parallel mode, it becomes a 30-V, 4-A supply. In independent mode, each of the two units outputs up to 31 V and 2.2 A. In isolated mode, the two units operate independently. In series mode, the outputs can be set independently, but they are linked internally.

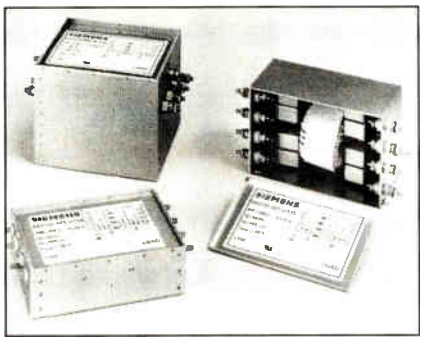
In series-tracking mode, the master voltage control sets equal voltages on both units. Each output's voltage and current levels can be set precisely by means of a dc output switch before connection to the load. Available now, the PL320 costs £339.

Thurlby Electronics Ltd., New Road, St. Ives, Huntingdon, Cambs., EE17 4BG UK.
Phone 0480-63570 [Circle 703]

FILTERS QUIET NOISE ON 3-PHASE AC LINES

Siemens AG's B-84131 filters for three-phase ac power lines suppress interference on mainframe computers and other systems by means of current-compensated toroidal-core chokes with highly permeable Siferrit cores and metalized-plastic interference-suppression capacitors.

Nonsymmetrical attenuation ranges



from 150 KHz to 30 MHz at 60 dB. Test voltage is 1,414 V phase-to-phase or 2,700 V phase-to-ground. The devices come in aluminum packages with plug contacts or screw connections and weigh 1.5 to 4.5 kg.

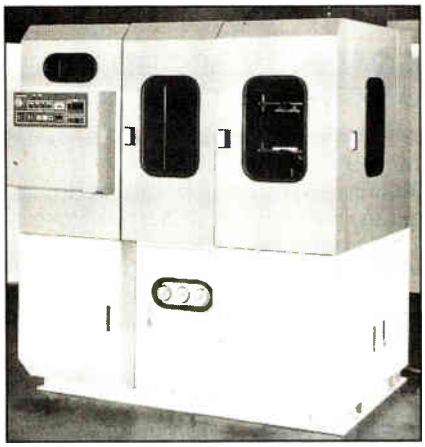
The power line filters cost between 200 and 400 DM depending upon current and attenuation ratings. Delivery takes approximately 12 weeks.

Siemens AG, Postfach 103, D-8000 Munich 1, West Germany.
Phone 49-89-2340 [Circle 704]

AUTO-MOLD SYSTEM BOOSTS THROUGHPUT

A fully automatic semiconductor packaging system from Yamada Seisakusho Co. improves throughput by using a system of multiple plungers for high-speed encapsulation.

The MS-G7 is a general-purpose, auto-mold system designed to accommodate custom, short-run, and multiple-device production schedules. It can handle lead frames up to 230 by 45 mm, and consists of a press, mold die, and control unit. The MS-G7 handles any common mold die and is designed for quick die changes to cope with small-volume runs of different size packages.



The MS-G7 has a clamping force of 20 tons and a cycle time of 20 s. It costs 20 million yen, and delivery takes three to four months.

Yamada Seisakusho Co., Sales Engineering Section, 90 Kamitokuma, Togura-machi, Hanishina-gun, Nagano, 389-08 Japan.
Phone 81-262-75-2111 [Circle 705]

BUBBLE MEMORY USES RAM CARTRIDGES

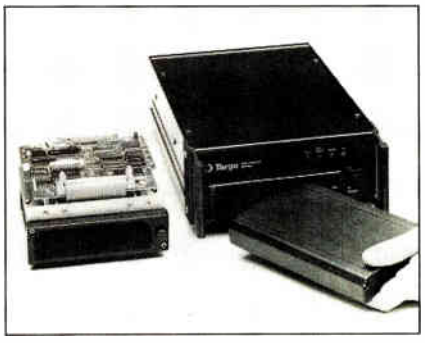
Targa's rugged bubble-memory systems now can be ordered with high-capacity, nonvolatile CMOS RAM cartridges backed by lithium batteries for a minimum data-retention time of five years.

The new cartridges come in two versions: one operates over the temperature range of -40°C to +75°C for harsh environments, the other over the 0°C to 65°C range for industrial use.

The data cartridges come in 128-, 256-, 512-, and 1,024-K-byte capacities. In lots of 10, prices range from $670 to $3,600.

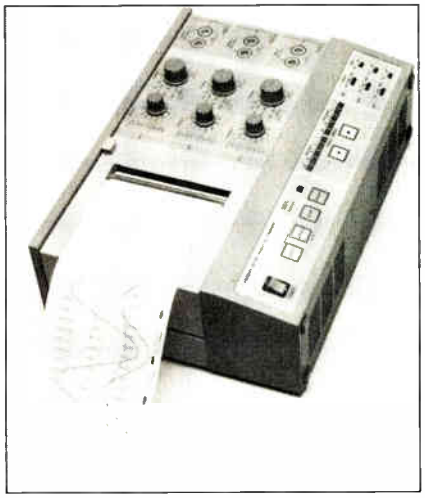
Both versions are completely compatible with Targa's portable data-recorder line, which consists of the DR1102 Industrial, the DR2102 Mobile, and the DR3102 High-Reliability models. Available now, the systems are used in control and data-collection and data-acquisition systems. All have either an IEEE-488 parallel or a selectable RS-232-C and IEEE-422 serial interface.

Targa Electronics Systems Inc., Box 8485, Ottawa, Quebec K1G 3H9, Canada.
Phone (613) 731-9941 [Circle 706]



POWER RECORDER MONITORS 3 CHANNELS

The 8710, an analog-digital recorder of power-supply-line load variations, never misses anomalies, says the manufacturer. It can record data from three channels at the same time. Its true root-



Introducing a new desktop plotter that's small enough to fit in this magazine.

Fujitsu's new FPG-310 plotter is truly compact: it needs only 420 × 260 mm, which leaves you plenty of elbow room. The FPG-310 weighs less than 5 kg and draws less than 35 watts of power.

A wide variety of media

Now you can print figures and text on almost any medium — coated paper, OHP films, tracing paper and, of course, standard paper. And the medium can be any size from postcards to A3 sheets.

Superb graphics

Precise 0.025 mm resolution and 6 bright colors raise your computer's graphics to new heights of effectiveness. The FPG-310 gives you the flexibility of a dot matrix printer but provides far superior quality.

Full compatibility

Three standard interfaces — Centronics, RS-232C and GP-IB — let you connect the plotter to virtually any personal or business computer.

Amazing versatility

Applications include business graphs, education, measurement systems, FA — and even personal CAD. Hobbyists also find the plotter useful for a wide variety of tasks.

Whether you use the FPG-310 in your home office or in a workstation, no job is too big for this little plotter.

Fujitsu Color Plotter FPG-310

FUJITSU MIKROELEKTRONIK GmbH:
Arabella Center 9, OG 7A, Lyoner Straße 44-48, D-6000 Frankfurt am Main 71, F.R. Germany Phone 069-66320 Telex 0411963 Fax 069-6632122
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Telex 2[illegible] Fax 03-216-9771

FUJITSU

mean-square value-indication system also monitors power when measuring distorted ac voltages and currents.

A hybrid recording feature enables the recorder to simultaneously print the recorded values both graphically and numerically, using a built-in thermal graphic printer.

Included with the device is a monitor-print function for adjusting input levels and offsets. A gauge-print function enables it to print a vertical scale for fine divisions and to read input levels accurately.

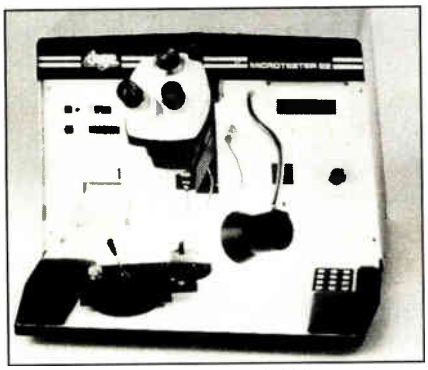
To eliminate the time and cost of reprogramming the recorder, chart speed and other variable settings are stored in the device's battery-powered memory. Retention time is about one week even when the system power is off.

The 8710 sells for 320,000 yen and is available for immediate delivery.

Hioki E.E. Corp., Sales and Marketing International Department, P. O. Box 1, Sasaki, Nagano, 389-06 Japan.
Phone 81-268-82-3030 [Circle 707]

MICROTESTER DOES MIL-SPEC TESTING

Designed to exceed Mil-Spec 883 for bond-testing of semiconductor, resistor, or capacitor chips, the series 22 microtester from Dage (GB) Ltd. offers results analysis, IEEE-422 host-computer hookup, and full self-diagnostics. Test



loads range from 1 to 10,000 grams.

The microtester uses a dc servo drive system for zero overshoot, rapid positioning, and precision when performing production tests for destructive and nondestructive wire-pull and chip-shear.

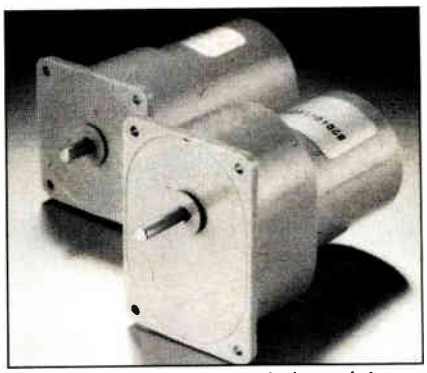
The shear cartridges are designed to keep tool flyback below 1 mm, even at maximum load. Thus chips in closely packed hybrid or tight-cavity dual in-line packages can be shear-tested without damage.

In addition, the series 22 features interchangeable cartridges for accurate preset loads and fast adjustment, an alphanumeric display system for control, and built-in data logging. An optional IEEE-488 port enables data downloading to a host computer. Depending on options, the system costs between £6,000 and £12,000. It is available now.

Dage (GB) Ltd., Intersem Division, Rabans Lane, Aylesbury, Bucks., UK HP19 3RG.
Phone 44-296-33200 [Circle 709]

LIGHTWEIGHT MOTORS COME IN PLASTIC BOX

Philips' line of small, low-cost dc motors now includes a series with a fixed reduction ratio of 81:1 and a torque of 300 milliNewton-meters. All the devices contain an integrated all-plastic gear-



box, which helps keep their weight to 125 grams.

The motors, which put out 5 W and have a typical lifetime of 3,000 hours, are designed for ribbon feeding in printers and for general drive systems. Their nominal speed is 60 rev/min. Models are available with supply-voltage ratings of 6, 12, 13.5, and 24 V. To keep interference low, the motors have a flat commutator, special brushes, and a varistor. Each motor comes in a case that has a flange with four bolt holes for easy mounting.

Pricing depends on importing country and quantity ordered. In the UK, for example, a dc motor would cost £15 for a single-unit order and £6 in quantity.

Philips Elcoma, Electronic Components & Materials Division, P. O. Box 523, 5600 AM Eindhoven, The Netherlands.
Phone 31-40-724324 [Circle 708]

SOCKETS MOUNT AT RIGHT ANGLES

A series of pc-board sockets from Greenpar Connectors Ltd. comes in right-angled versions as well as the conventional straight-socket configuration. All have molded thermoplastic bodies, polypropylene insulators, and silver-plated contacts.

The bodies have a molded thread that is flat on one side. This detail facilitates correct placement in a panel up to 4 mm

thick and helps the device resist axial torque. Sockets are attached to pc boards using self-tapping screws or by soldering.

Additional specifications include a nominal impedance of 50 Ω, a peak working voltage of 500 V dc or ac, and a peak proof voltage of 2 kV dc or ac. Insulation resistance is greater than 500 Ω; operating-temperature range is -40°C to +85°C. Available now, the sockets cost about £1 each.

Greenpar Connectors, Cambridge Rd., Harlow, Essex, UK CM20 2ER.
Phone 44-279-39111 [Circle 711]

RECORDER OFFERS SOLID CONSTRUCTION

The *x-y* recorder LY1600 from Linseis GmbH is an A4-format instrument featuring aluminum construction for durability.

The *x* axis is guided at both ends by steel wires in a butterfly configuration to ensure parallel movement. The pen holder accepts all popular sizes.

Both axes have calibrated input ranges in 12 steps from 0.5 mV/cm to 2 V/cm. A variable sensitivity control allows the expansion of each range by a factor of up to 2.5. The maximum write speeds in the *x* and *y* axes are 70 cm/s and 1 m/s, respectively, giving corresponding response times of 0.35 s and 0.2 s.

Available from stock, the LY1600 costs 2,750 DM.

Linseis GmbH, P. O. Box 1404, D-8672 Selb, West Germany.
Phone 49-9287-79022 [Circle 710]

MICROWAVE HEAD HAS LOW NOISE

The XLN 230 microwave head from Xelex Forsäljnings AB offers a noise preamplifier and an integrated electronic polarization adjustment that keep noise to a minimum.

It comes in three versions. The normal version has a noise factor of 2.3 to 2.5 dB; the premium model, 2.0 to 2.3 dB; and the super, 1.8 to 2.1 dB.

The device handles input frequencies of 10.95 to 11.75 MHz and outputs of 950 to 1,750 MHz. It comes with a feeder horn and a three-point attachment in cast aluminum as standard and can be ordered without a feeder horn or with an upgraded feeder horn that has an integrated electronically controlled polarizer.

In 100-unit quantities, the normal version costs £1,500 (Swedish) each; the premium, £1,875; and the super, £2,345. All are available now.

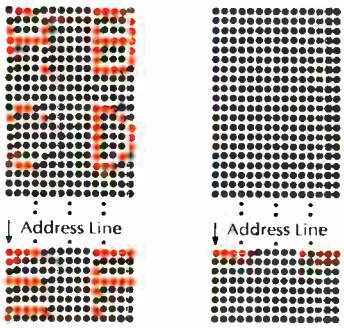
Xelex Forsäljnings AB, P. O. Box 42-137, S-126 12, Stockholm, Sweden.
Phone 46-87 44 2985 [Circle 712]

Slim and trim

The extra-thin plasma displays from Fujitsu

Just 1 inch thick, the new flat-screen plasma displays from Fujitsu are ideal for today's down-sized PCs and OA equipment. Trim down your plasma panels and shape up the quality of your display.

Why Fujitsu's plasma displays are bright and flicker-free?



New Fujitsu memory-type display
All addressed lines light up simultaneously.

Conventional refresh-type display
Only one line lights up at a time.

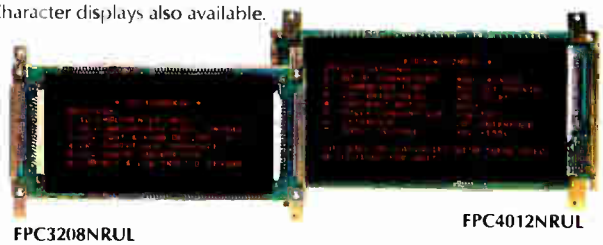
Flicker-free:
Memory-type screen writing eliminates flicker and rolling. This extra sharpness and steadiness reduces eye fatigue even during day-long use.

Extra-bright:
See your data in its best light, thanks to a maximum brightness of 150 cd/m^2.

High resolution:
The FPF8050HFUG's 640 × 400 dot matrix (CRT-compatible) provides crisp displays of graphics and text.

Easy installation:
All the drive circuitry is built in. Low consumption minimizes power supply requirements.

Character displays also available.



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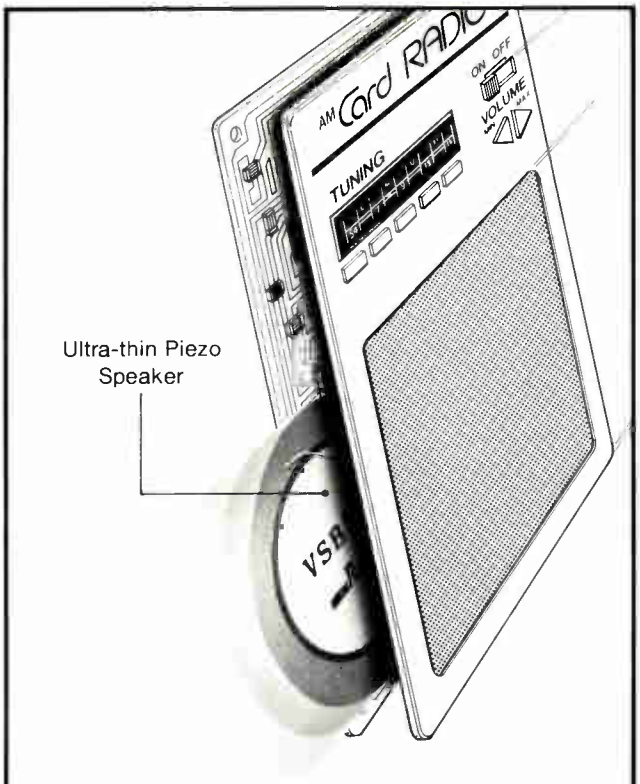
Circle 132 on reader service card



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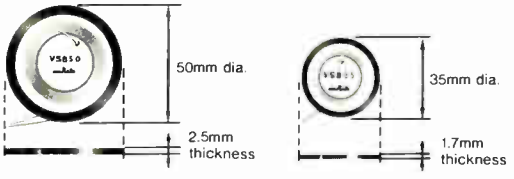

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ABOUT THE MEMORY OF TOSHIBA MEMORIES.

Despite all his good-naturedness, Loxodonta africana, otherwise known as our African elephant, is noted for being a creature that doesn't easily forget. This wins him the admiration of the zoologist who speaks of jumbo's extraordinary memory. And this is a characteristic which our thick-skinned friend shares with the tiny members of the Toshiba memory family. There are other points in common, too: in addition to high information storage capacity (e. g. 1 MDRAM), exceptionally good service life, performance, and unbeatable insensitivity.

Also remarkable is what Toshiba's semiconductor technology achieves in other areas: on GTR modules, optical couplers, CPUs, LED lamps, custom ICs, CMOS logic, transistors, and bipolar ICs. Tell us about your problems and needs. You won't have to wait long for an answer.

☐ Please send me detailed information on Toshiba memories

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☐ I wish to arrange a visit from one of your engineers, without any obligation on my part.

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IEC/IEEE bus, RS-232-C, Centronics, TTL I/O (56), 14 bit D/A, Multibus I (PCA 12/15 only).

IEC 625 Bus

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MS-DOS 3.1, extended Basic incl. interfaces, extended Pascal incl. interfaces, UDI, XRUN, Kermit, dBase II, Wordstar, Knowledgeman, Multiplan, Pictures graphics software (PCA 12/15 only).

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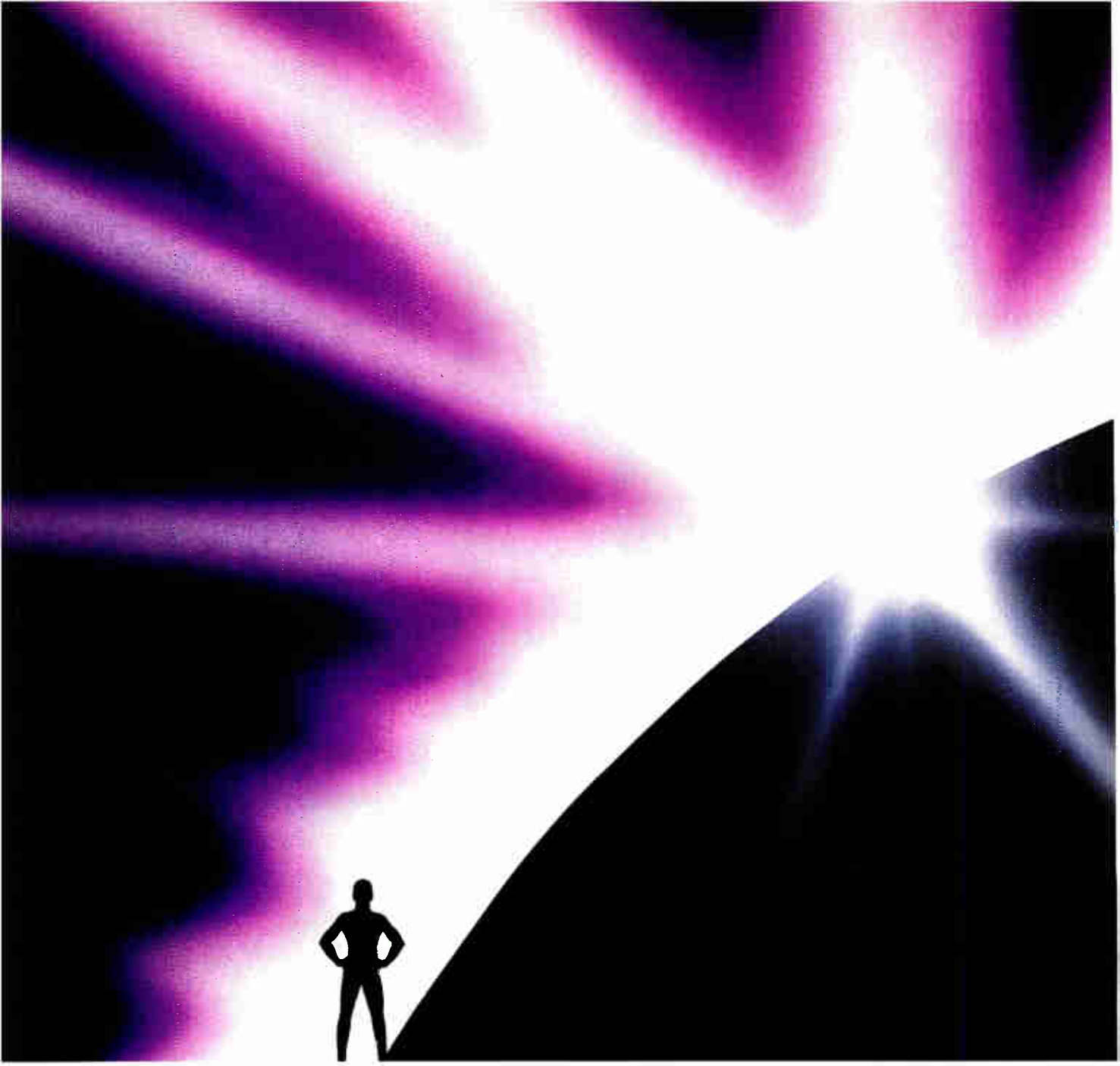

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Not only can any type of data be stored (in effect you can create your own data types), but you can implement your own customized operators to act on your data. It's that flexible.

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8 BIT Microcontroller Core Processor

Key Features

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Speed:	20 MHz Clock
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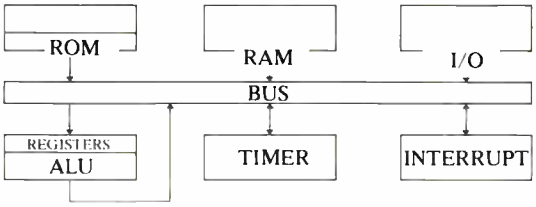

100% compatible with National's COP820C 8-bit microcontroller, this core processor features modifications on its pinout to make it more flexible. Because of its small size and versatile architecture, it can be combined — on a single chip — with digital, analog, EEPROM and peripheral megacells from our library, such as keyboard encoder, UART, RTC, LCD/LED driver, and Watch Dog timer. The net result is a dramatic savings in part cost and board area.

FEBRUARY

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Key Features

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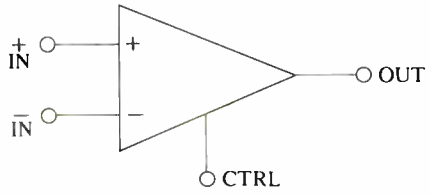
Output Pulse Width	12 ns (min)
Internal Hysteresis	150 mV (typ)
Output Drive Current @ Vol = 0.5V	48 mA (min)
Operating Range	4.5 to 5.5 Volts 0 to 70° C
Technology	2μ CMOS



Designed for high-speed data transmission in a noisy environment, this new cell lets you integrate analog interface circuitry with digital design. It can be simulated, along with digital circuitry. It's fully compatible with our 280 digital cells, 30 analog cells, and 20 EEPROM cells. It also gives you 2 micron technology. In CMOS. So you can look for reduced board space, and low power consumption.

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together, since they've all come from the same source. Of course, we already give you the richest cell library in the industry. But every month this year, we'll use this space to introduce our latest ideas. To give you more possibilities than ever. If you'd like to see our complete library card, just write or call. In the meantime, just look what we've done for you lately.

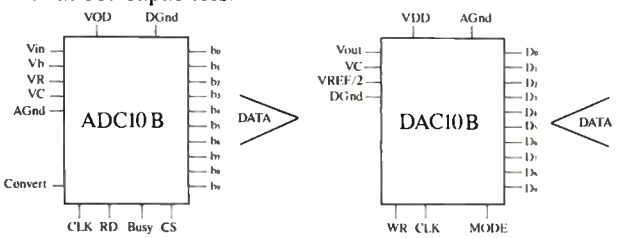
MARCH

ADC10B 10-BIT A/D Converter

Key Features (Both cells)

Accuracy	10-bit
Power consumption	5V ± 10%
Technology	2μ CMOS

A low-power, 10-bit successive approximation differential input converter which uses a combination of ratioed resistors and ratioed capacitors.



DAC10B 10-BIT D/A Converter

A 10-bit ratioed capacitor and resistor string DAC with a deglitched sampled-and-held buffered output. Like the ADC10, it also uses 2 micron technology. In CMOS. All of which makes us a tough act to follow. And gives you a good reason to watch this space in April.

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INSIDE TECHNOLOGY

WORLD'S FASTEST MICROPROCESSOR!

AMD's 32-bit chip uses an enhanced RISC design to run at a sustained performance level of 17 mips; it can hit a peak execution rate of 25 mips

by Alexander Wolfe and Bernard C. Cole

In the high-stakes race to produce ever-faster microprocessors, Advanced Micro Devices Inc. is about to blow past the rest of the field with the first microprocessor ever designed by the company. Using an enhanced reduced-instruction-set-computer design, the Am29000 Streamlined Instruction Processor stakes a claim to the title of the world's fastest 32-bit microprocessor. The Sunnyvale, Calif., company regards the new microprocessor as its most significant product in a decade.

The Am29000 (see fig. 1) operates at a 25-MHz clock rate and a 40-ns instruction cycle time. It can hit a peak execution rate of 25 million instructions per second and a sustained performance level of 17 mips.

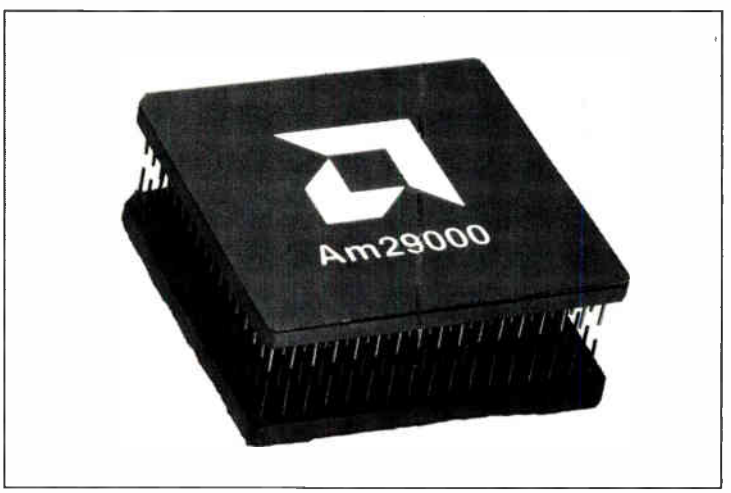
That kind of performance explains why AMD is betting that the chip, set for sample-quantity production in the second half of this year and full production in the first half of next year, will help turn the company's ink from red to black (see p. 64). AMD thinks its microprocessor can be a formidable contender against the swelling ranks of RISC-based chips. The company believes the chip can outrun a whole host of similar products: the popular RISC chip set from MIPS Computer Systems, Sunnyvale, Calif.; the Clipper 32-bit microprocessor from Fairchild Semiconductor; and upcoming releases reportedly on the way from Digital Equipment and IBM Corp. (see p. 66).

Among the applications AMD envisions for the Am29000, embedded controllers lead the list. ISDN networks, for example, may use the Am29000 to provide the switching control. Node controllers based on the chip will give work stations network access to large data bases at 10 times the performance level of existing Ethernets. As for other applications, AMD claims a multifont laser printer built around a 29000 will run four times faster than those printers built with Motorola's 68020 32-bit microprocessor. Beyond that, the sky's the limit: "The Am29000 will allow the creation of markets that we don't even envision yet," says Lyle Pittroff, the director of strategic marketing at AMD.

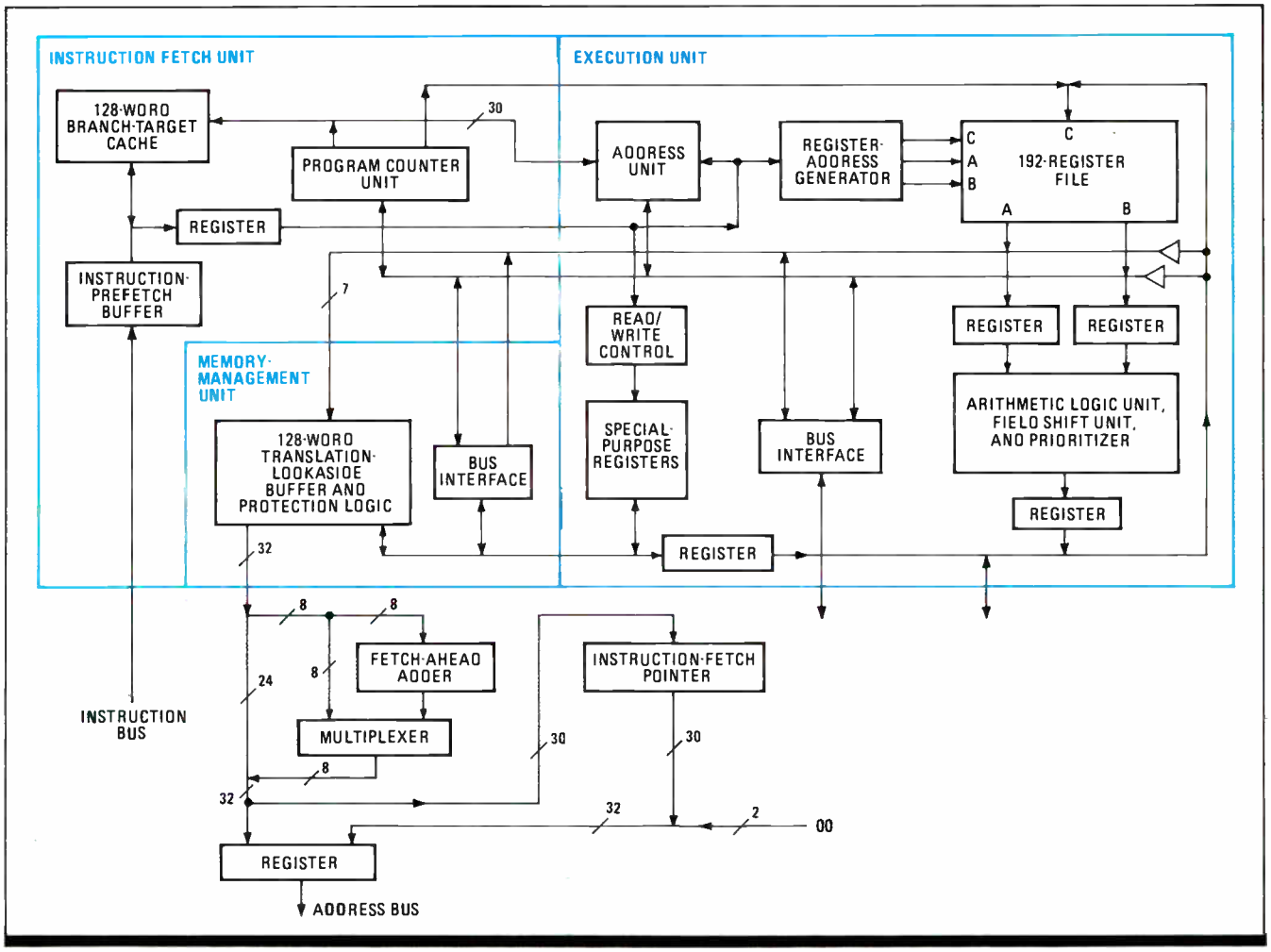
To pack such power into the Am29000's design, the company opted for RISC with a twist. "To aim at RISC-type applications, you need more than RISC," says Paul Chu, AMD manager of programmable processors. So AMD came up with the enhanced-RISC design, combining several key RISC concepts with the best of conventional designs.

Here, streamlining means that the 1.2-μm CMOS chip, packaged in a 169-terminal-pin grid array, includes such key RISC features as a four-stage pipeline and a 128-instruction branch target cache, which increase instruction throughput, and 192 internal registers, which reduce the need for external accesses. The conventional elements include a memory-management unit that is on chip and an interface channel capable of supporting a 200-megabyte/s transfer rate.

One advantage of RISC is that it works with optimizing compilers for high-level programming languages such as C. A RISC ancestry is also



1.FAST CHIP. AMD's 32-bit chip peaks at 25 million instructions per second.



2. UNIFORMITY. The pipeline's instruction-fetch, execution, and memory-management units ensure uniform operation.

evident in the instruction set of the Am29000 microprocessor. The instruction set, defined to ease the building of optimizing compilers that convert C-language programs to compact Am29000 machine code, contains 115 instructions, all of which are executing in a single cycle.

AMD is also introducing the Am29027, a floating-point accelerator that interfaces directly to the microprocessor. The Am29027 performs single- and double-precision floating-point operations and a complete set of integer and conversion operations. Additional speed comes from its ability to simultaneously handle one single-precision operand and one double-precision operand, saving conversion operations.

In RISC architectures, single-cycle execution of instructions is the performance ideal. This is possible because of an instruction pipeline, which, in effect, prepares an instruction for execution before the processor is ready to execute it. On most programs, the Am29000 comes close to its goal: an average of 1.3 to 1.5 cycles per instruction-execution rate has been measured.

The Am29000's pipeline has four stages: fetch, decode, execute, and write back (see fig. 2). In the pipeline, instructions are prefetched up to four cycles in advance of actual execution. During the fetch stage, the location of the next processor instruction is determined, and that instruction is selected for the decode stage. During decoding, the previously fetched instruction is decoded, and required operands are also fetched or assembled. In addition, addresses are evaluated for branches and stores. In the execution stage, the operation specified by the instruction is performed. Finally, during write back, the results of the operation performed during the execute stage are stored in the register file.

In designing the pipeline, special attention was given to uniform operation with minimum contention of resources and interlocks. For example, hardware forwarding is implemented in the pipeline. This is a feature that allows the Am29000 to bypass the register file when the result of an arithmetic-logic-unit operation is needed as a source operand in the next instruction cycle.

Within the pipeline, delayed branching is an important feature because it speeds throughput. Typical pipelined processors must re-establish their instruction-fetch stream and refill their pipeline after executing a branch. In the Am29000, the target of the branch can be stored in the

branch target cache, so the processor can execute those branches in one cycle. Single-cycle branching has a dramatic effect on performance, since roughly 15% to 25% of the instructions executed in a typical application are branches. To keep the pipeline operating at the maximum rate, the instruction following the branch, referred to as the delay instruction, is executed regardless of the outcome of the branch. For 90% of all branches, an optimizing compiler can place a useful operation in the delay-instruction position, further boosting efficiency.

Like branches, load and store instructions running rampant can adversely affect processor performance. The large number of registers built into the Am29000 minimizes this problem: by allowing frequently used data to be maintained on chip, the number of external data accesses that application software must perform are greatly reduced. Indeed, the 192-word register file is significantly larger than the usual 16- or 32-word register files in other microprocessors.

Unlike most microprocessors, which limit certain registers for address, data, or other special purposes, the Am29000's 192 registers are all general purpose. The register file is divided into 128 local registers, which are addressed relative to an internal stack pointer, and 64 global registers, which are addressed by absolute register number. The 128 local registers can be used by a compiler as a run-time stack cache to avoid off-chip data references. As a result, overhead for many procedures is reduced by a factor of 5 to 10. The register file can also be divided into banks of 16 registers to support applications requiring fast context switching.

Memory management is another area in which the Am29000's flexibility is readily apparent. The chip handles its memory management by providing a 64-entry on-chip translation look-aside buffer, which translates a 32-bit virtual address into a 32-bit physical address in a single cycle. The buffer allows the implementation of a demand-paged virtual memory system, so the system designer can choose the virtual memory architecture best suited to a particular design.

When executing applications programs, normal program flow may be preempted by an interrupt that causes a subroutine to take control temporarily. In the Am29000, those interrupts are designed for maximum flexibility. The interrupt mechanism has been defined so that only a minimum, predefined interrupt-processing sequence is required, allowing interrupt response time on the order of 200 ns and a context-switching time of less than 700 ns.

For internal and external communications, the Am29000 channel, or system interface, uses a modified Harvard architecture with three 32-bit buses: an instruction bus that transfers instructions into the processor; a data bus that transfers data to and from the processor to peripheral devices, and an address bus that provides addresses for both instruction and data accesses. Because the address and data buses don't have to be shared, the speed and efficiency of the chip increase. To send signals over these buses, the channel uses three access protocols: a simple access mode, a faster pipelined mode, and a burst mode for the fastest data and instruction access. Transfers across the channel can occur at a maximum transfer rate of 200 megabytes/s. □

TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*

BUILDING THE AM29000: EASIER SAID THAN DONE

The aim of the design team on the Am29000 Streamlined Instruction Processor was simple and to the point: to develop the fastest and most powerful 32-bit central processing unit around that can also serve as a central processor in systems ranging from application-specific embedded controllers to high-performance general-purpose computers.

However, that was easier said than done, says 34-year-old Paul Chu, the product planner and department manager for programmable processors at Advanced Micro Devices. A graduate of Stanford University with master's and bachelor's degrees in electrical engineering, Chu and 33-year-old Mike Johnson, section manager and chief engineer for programmable processors at AMD, headed up the nearly three-year-long effort that eventually would make the Am29000 a reality.

"What we want is a machine and an architecture that will dominate the high-performance end of the 32-bit fixed-instruction CPU marketplace in the same way that the 2900 architecture dominates the micro-programmable building-block side of the business," says Chu.

DESIGNERS. Paul Chu, left, and Mike Johnson.

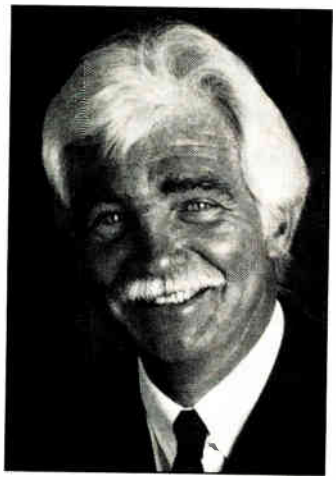
One important element in ensuring the success of the CPU was throughput—sheer computing speed—not just in terms of the highest possible burst speed but also as measured in sustainable performance, according to Johnson, who spent eight years at IBM as part of the development team on ROMP, one of the original reduced-instruction-set computers that eventually emerged as the IBM RT PC. "The majority of the features were defined with the maximum achievable performance in mind," says Johnson. "Compromises, and just small ones at that, were made only when it became clear there was no other way to incorporate the other features necessary to the design."

The result, he says, is a processor with a burst mode that can reach as high as 25 mips at 25 MHz, and, more important, a sustained performance time of 17 mips, which is at least three times faster than any other 32-bit CPU.

A STREAMLINED AMD FIGHTS BACK, LOOKS FOR STRATEGIC PARTNERS

Sanders keeps product development going, says chip maker can turn profitable by June

by Clifford Barney



'GOOD KING JERRY:' 'I'm talking everything from alliances . . . to acquisition or being acquired.'

At a time when lone-wolf, determinedly independent semiconductor companies are considered to be an endangered species, Advanced Micro Devices Inc. is running hell-bent to mutate. The company has streamlined its staff and is prowling for a pack of strategic partners.

The Sunnyvale, Calif., company has dropped $130 million in six straight losing quarters. It can't break even in its process-driving commodity product, MOS memories. It faces fierce competition for sockets for its bread-and-butter line of proprietary products from a score of sharp young design and process houses. It's in danger of losing its grip on the mainstream microprocessor market, since rival Intel Corp. shows no signs of making its hot 32-bit 80386 available for second sourcing. Its prospects are considered in some quarters to be so bleak that one industry research company lists AMD as a prime candidate for acquisition.

AMD has heard it all before. The company's demise has been predicted before, during the 1974 and 1981-82 recessions. Both times it came back strongly, catapulting from $358.3 million in sales in fiscal 1983 to $931.1 million in fiscal 1985. That high-water mark was accompanied by a frenzy of expansion that founder and chairman W. J. Sanders now describes as "ill-disciplined." It left AMD with a half billion dollars worth of capital equipment, including three 6-in. wafer-fabrication lines that are now woefully underutilized, at 25% of capacity, but which are poised for recovery.

AMD has discarded its no-layoff policy and has drastically reduced staff during the past six months. Now, with a new-generation microprocessor, the Am29000, (see p. 61) joining an already impressive list of new products beginning to play a significant role in sales, the company figures it is poised to capitalize on what looks like a genuine industry recovery. Realizing that product development is too costly for AMD to go it alone, Sanders and his seasoned management team are looking for new strategic alliances—and being acquired has not been ruled out—to help bolster its line of products in growth markets. One market dear to AMD, erasable programmable read-only memories, is beginning to grow again, thanks to September's trade agreement between the U. S. and Japan.

A mere two quarters of back-to-back 10% growth, says Sanders, would put AMD in the black; the first of those quarters is in progress. AMD, he contends, can be profitable again by June. The entire product line will figure in this growth, AMD says. MOS microprocessors, particularly the Intel 80186 and 80286 and their peripherals, are one key factor. Sanders concedes, however, that it will be a long time, "certainly not this year," before AMD gets rights to the 386.

In the fall of 1984, Sanders was among the first to predict the downturn when he warned that the Semiconductor Industry Association's rosy forecast for 1985 was not justified by the business from the computer industry. He was more on the mark than he knew. With its personal-computer market melting, the mainframe computer market sagging, and profit wrung out of memories by Japanese lowball pricing, AMD soon found itself able to produce only half of what it could build.

Rather than cut costs, Sanders continued to spend heavily on research and product development, never dropping below $45 million a quarter. He clung to the no-layoff policy to the point where securities analysts were openly sniping at him and hinting that he was on the verge of being forced out.

Sanders stayed, the no-layoff policy went, and with it went Sanders' belief that AMD could afford any such rigid policies. "The concept that you could carry everyone was well-intentioned but perhaps unrealistic," Sanders says. AMD has pared 1,100 workers since August, including 700 who were laid off. Others lost their jobs when they declined transfers from Sunnyvale to Austin.

Another change from the long slump goes even deeper: "AMD is now on the lookout for partners to help develop new products." AMD's basic strategy, Sanders insists, must be to keep manufacturing costs down, maintain a state-of-the-art process technology, and profit from product innovation, but he now concedes that AMD can't do it single-handedly. The cost of doing business is too great. "We'll have to find some new ways," Sanders

says. "I'm talking everything from alliances to mergers to acquisitions or being acquired."

An unfriendly takeover would be "inconceivable," because AMD's veteran management team wouldn't go along with it, Sanders says. Five of AMD's top executives—president Anthony B. Holbrook, 51; operations vice president James B. Downey, 45; treasurer Richard Previte, 51; marketing vice president George M. Scalise, 52; and North American marketing vice president Stephen Zelencik, 51—have been at AMD more than a dozen years. John East, 42, logic-group vice president, is a relative newcomer with eight years service.

Sanders, 50, has been with AMD since its founding in 1969. Asked to define his role, he replies with conviction, "I am the leader." In an industry where prima donnas are not exactly scarce, Sanders still manages to stand out. No other chief executive in the industry could get away with depicting himself, as Sanders did in a company brochure, as "Good King Jerry," a dragon-slaying knight in armor. AMD took it in stride. Sanders' antics may be viewed with amusement, but he is very much in charge of AMD.

SEEKING A GRAND ALLIANCE

Rather than mergers or acquisition, Sanders sees an alliance as the best way to bring out new products with fewer AMD dollars. AMD has long had a connection with Siemens AG of West Germany, which owns nearly 20% of AMD's stock and is a major customer. They have second-sourced a few of each other's chips, but in some sectors they are fierce competitors.

Siemens is often mentioned as a possible candidate for a friendly takeover of AMD. But Sanders says AMD is not for sale, and a Siemens source says the company is not interested in buying a U. S. chipmaker. The current bits-and-pieces trading satisfies Siemens' needs in the U. S. market, the source says, and "a takeover of AMD would not fit our concept."

AMD's newest partner is Sony Corp., which represents an entry into the Japanese consumer chip market just as digital circuitry is becoming important in consumer goods. The two companies have already agreed on a common CMOS process, and their first joint products will be out by the end of the year, Sanders reports.

Among U. S. companies, AMD has an agreement with Intel on the iAPX series of microprocessors, a second-source agreement for gate arrays and standard cells with LSI Logic Corp., Milpitas, Calif., and a technology agreement with gallium arsenide specialist Vitesse Electronics Corp., Camarillo, Calif. Another agreement, with a major programmable-logic maker, will soon be announced.

EPROMs, which AMD executives cannot mention without referring to the "predatory" Japanese pricing that contributed heavily to the company's losses, are rebounding in the U. S., thanks partly to the semiconductor trade agreement with Japan. AMD is the second-largest U. S. producer, although it had to cut production when prices collapsed and the company lost ground to Intel. AMD is also offering a variety of 35-ns 64- and 256-K CMOS static random-access memories, in by-1, by-4, and by-8 configurations.

HOLBROOK: The president of AMD says its product line is no longer tied to the personal-computer market.

AMD's logic parts, such as a compression-expansion processor for office equipment, a powerful graphics chip, controllers, modems, and communications chips, are being accepted on a broad market front not tied this time to the personal computer, notes Holbrook. The products in AMD's year-long Liberty Chip program, in which a new circuit was introduced every week, generated 9% of sales in AMD's September quarter and 11.5% in the quarter ending Dec. 28. "The manufacturing resources are in place," Holbrook says, adding that hiring has continued for AMD's five Austin fab lines, even during last fall's layoffs.

Analysts are skeptical about AMD's ability to turn around, but none doubts that the company will make a fight of it. "They are going to have to outpace the rest of the industry, which is still not growing at 10% a quarter," says Andrew Kessler of Paine Webber. And at least until the current quarter, he adds, AMD's orders have been virtually flat for a year.

Sanders knows it. He won't be satisfied until AMD regains the $250 million in quarterly sales it had reached before the slump. Then, he says, R&D, now at $40 million a quarter, will be a respectable 16% of sales, and normal profit margins will be possible. ❑

VETS. AMD veterans Scalise, Previte, (standing, from left) Downey, and East (seated, from left) would hold the line against an unfriendly takeover.

A SWARM OF RISC CHIPS IS CHASING A FAST-GROWING SYSTEMS MARKET

One forecast calls for the systems market to grow 84% annually for the next five years

by Clifford Barney

The new reduced-instruction-set computer chip from Advanced Micro Devices is not only the company's "most important product ever," (see p. 61) but it reflects a major trend developing in the microprocessor market. For most chip makers, it's too late now and far too expensive to develop a new entry in the standard complex-instruction-set microprocessor market. But another way to compete in the microprocessor market turns out to be the RISC chip, which uses a simpler architecture that executes one instruction every machine cycle. While the RISC approach makes it easier to design the chip, it does put more of the design burden on the programmers writing the compilers.

Easily more than a dozen chip designers are hard at work now on a RISC microprocessor, and the U. S. military is showing great interest. What they are aiming for is a market that some research firms now predict will grow at compounded annual growth rates of 75% or more. For example, the Information Network, a San Francisco market-researcher, predicts a startling 84% growth for RISC machines, from $540 million in 1985 to $16.25 billion in 1991. Nearly half of that market is expected to be for technical work stations, since RISC chips are particularly strong in the areas of compute-intensive engineering and scientific tasks. Because this design approach can be used to emulate the more complex instruction sets of other computers, it can bring greater execution speed to applications where a large body of existing software must be supported. But the first wave of RISC machines will be dominated by embedded computers and controllers, because writing the new software is a less cumbersome task.

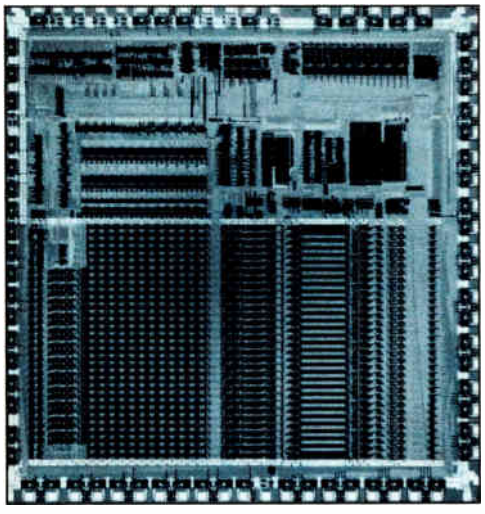
Hewlett-Packard was an early entry into the RISC game with its Spectrum family. Chips and boards from MIPS Computer Systems of Sunnyvale, Calif., are going into systems from the Dana Group, Racal Redac, and Silicon Graphics, the latter in a system for Prime Computer. Fairchild Semiconductor's Clipper RISC chip set is in a work station from Intergraph, and in several board-level controllers. Intel and Motorola Semiconductor, major players in the microprocessor market, both are reportedly working on RISC chips.

Acorn Computer designed a RISC central processing unit for one of its computers, using tools and technology from VLSI Technology, San Jose, Calif.; in turn, VLSI Technology, which was given rights to the chip, targets it for the industrial and controller markets as the VL86C010 (see photo). VLSI Technology's automated design tools make it easy to tailor the chip to run different code efficiently. "We are now offering a generic product," says a company spokesman. "However, if a customer wanted something different, we can quickly come up with a special product."

IBM has designed two RISC chips, and others are now reportedly being developed at Digital Equipment, Cypress Semiconductor, Performance Semiconductor, AT&T, United Technologies (see p. 97), and Japanese chip companies. The U. S. military has become enamored of RISC and has programs for designing embedded RISC computers, implementing the 1750A architecture in RISC, developing gallium arsenide RISC chips, and evaluating RISC-chip performance.

Andrew Bechtolsheim, vice president of technology at Sun Microsystems, Mountain View, Calif., says work stations—from Sun, and probably others—will move to RISC CPUs in the next year. "RISC architecture isn't more expensive than other 32-bit technology, yet its performance is higher," he says.

The ability to emulate more complex instruction sets, one of RISC's key attractions, could have far-reaching implications. "The issue of multiple standards, CPUs, instruction sets, and operating systems is going away," Bechtolsheim says. Through emulation, "a single user can have access to any one of them." In the future, work stations will be able to switch to faster processors as they become available, and run the same software. □



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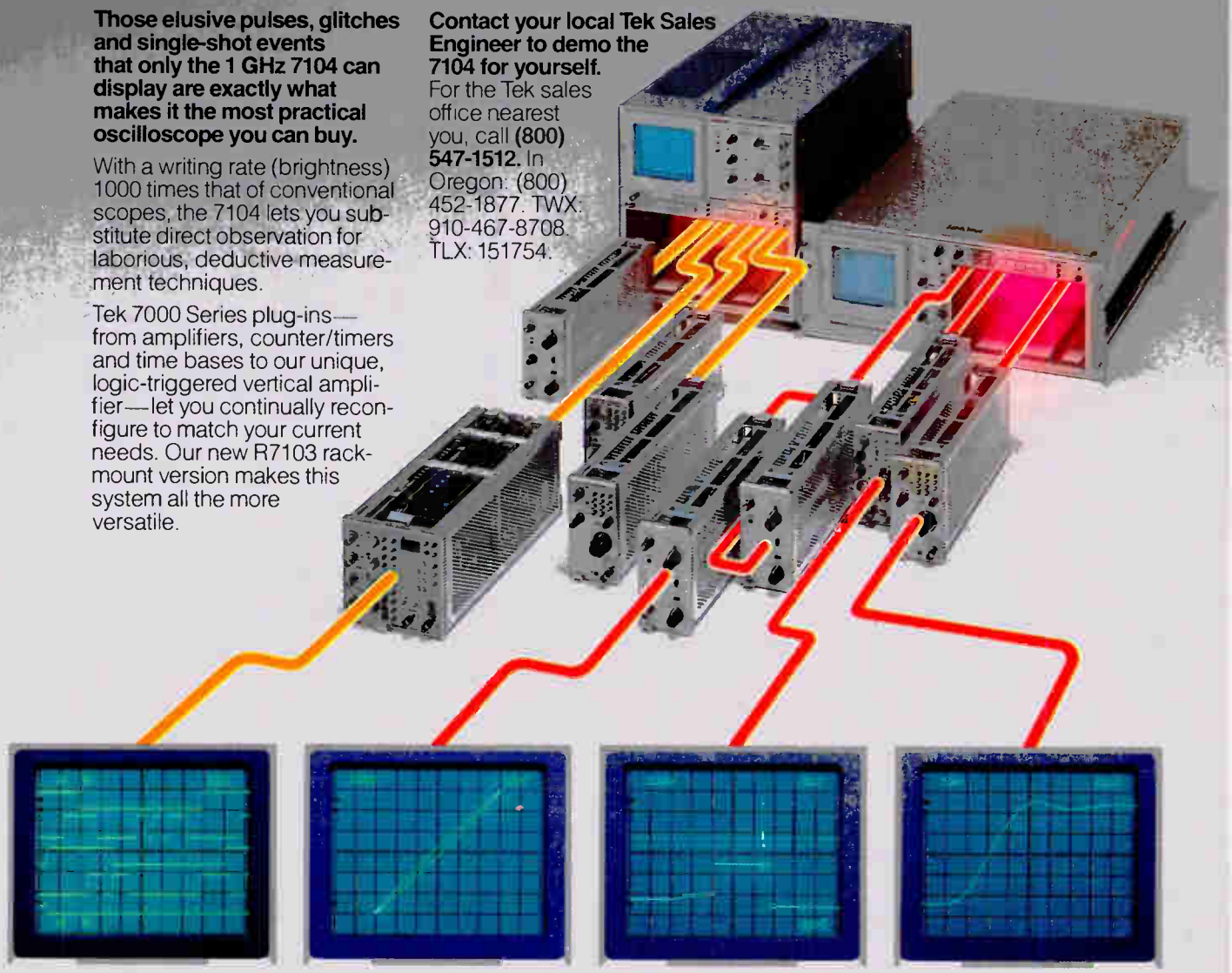

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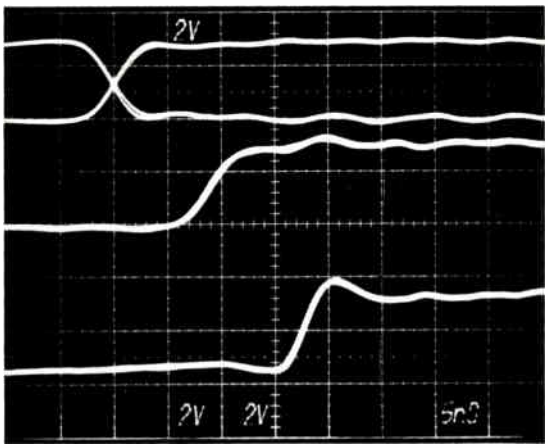
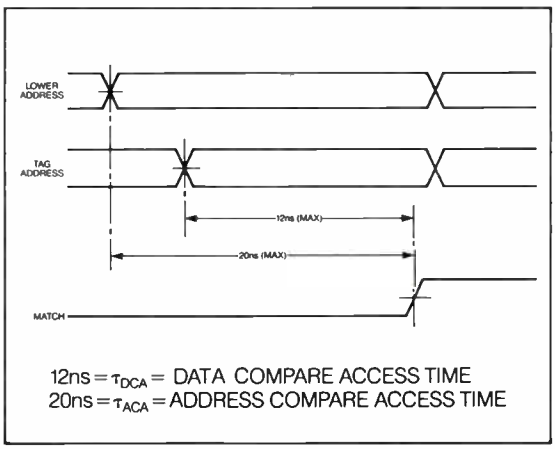
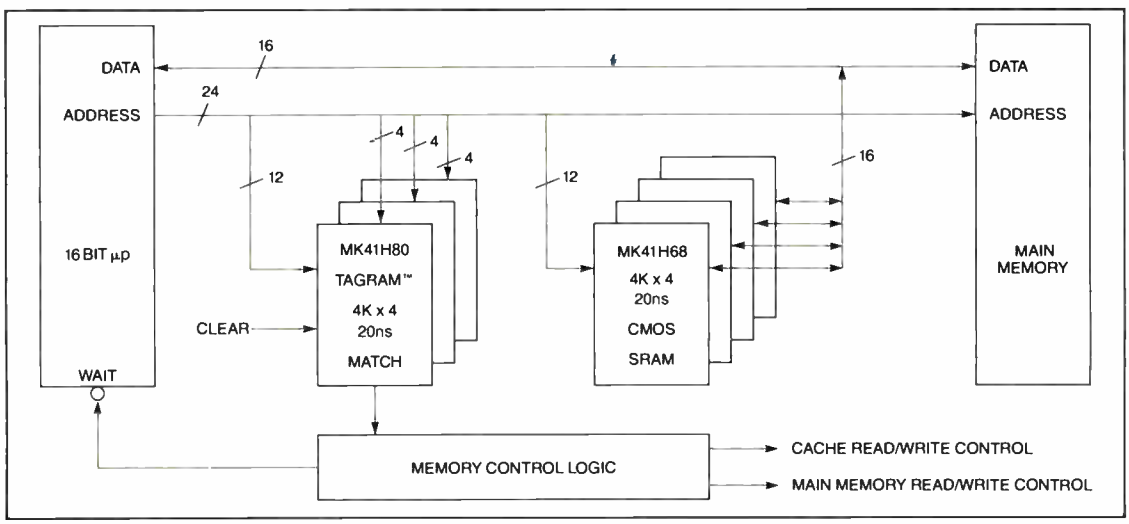


Actual MK41H80 TAGRAM Scope Trace Photograph



Match Access Timing



Direct Mapped Cache System Block Diagram

DEVICE	CONFIG	PINS	$\overline{CE}$	$\overline{CS}$	$\overline{OE}$	$\overline{CLR}$	MATCH
41H68	4Kx4	20	X				
41H69	4Kx4	20		X			
41H78	4Kx4	22	X		X		
41H67	16Kx1	20	X				
41H66	16Kx1	20		X			
41H79*	4Kx4	22	X		X	X	
41H80	4Kx4	22			X	X	X

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Circle 69 on reader service card

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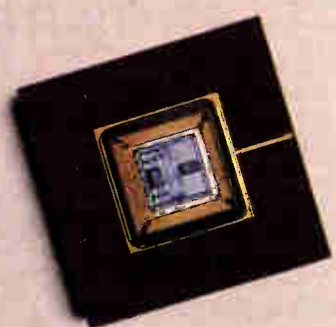

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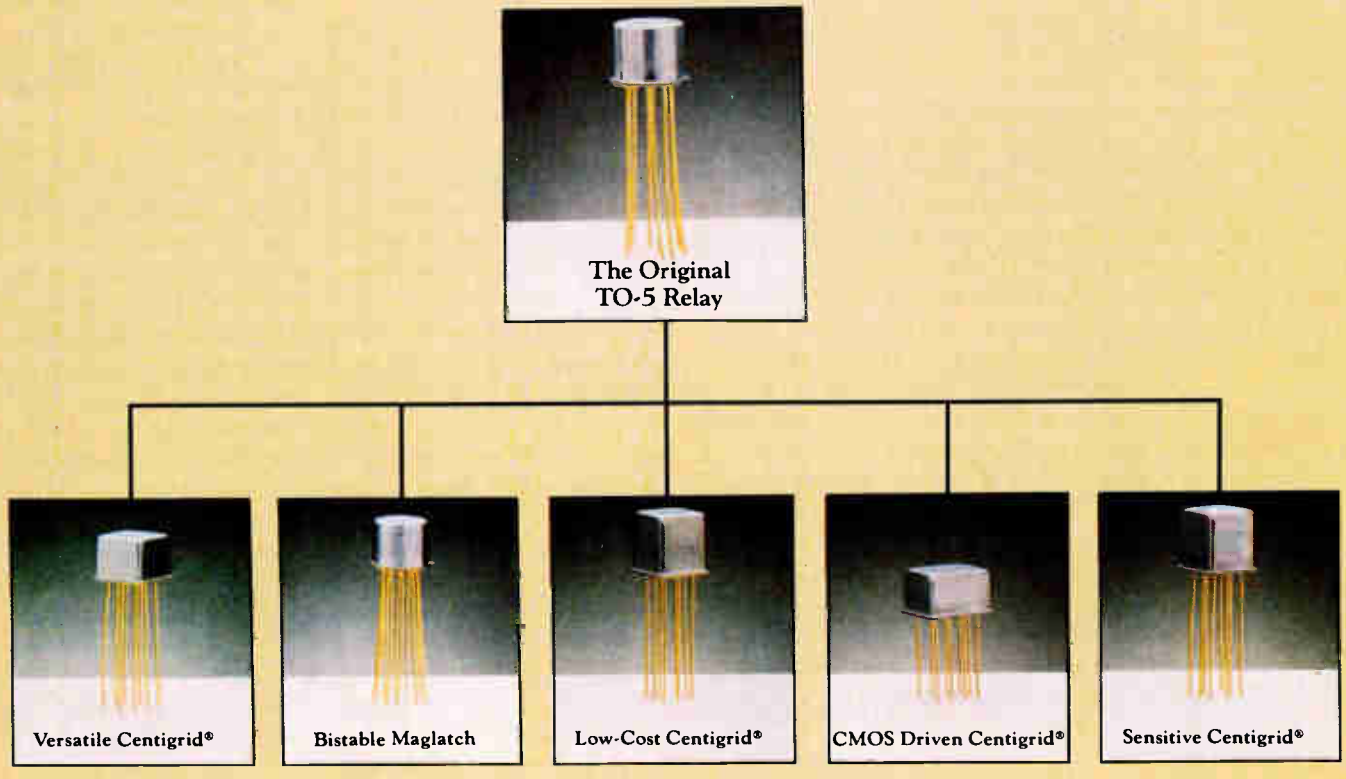

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TI'S ANSWER TO THE NEED FOR FASTER VLSI: ITS ExCL PROCESS

Based on Impact-X, the new ECL process cuts switching speeds to 200 ps and pushes density to 60,000 gates; it also produces highly reliable bipolar VLSI devices

More than ever, the name of the game these days in designing new generations of equipment is more speed! This demand is accelerating a swing in bipolar very-large-scale-integration circuitry from the workhorse transistor-transistor logic to emitter-coupled logic. But this shift requires advanced semiconductor processes that will provide equal measures of performance, packing density, and reliability. Now, after two years of evolutionary steps taken at Texas Instruments Inc., a new generation of ECL process technology—called ExCL—is emerging that can accomplish just that.

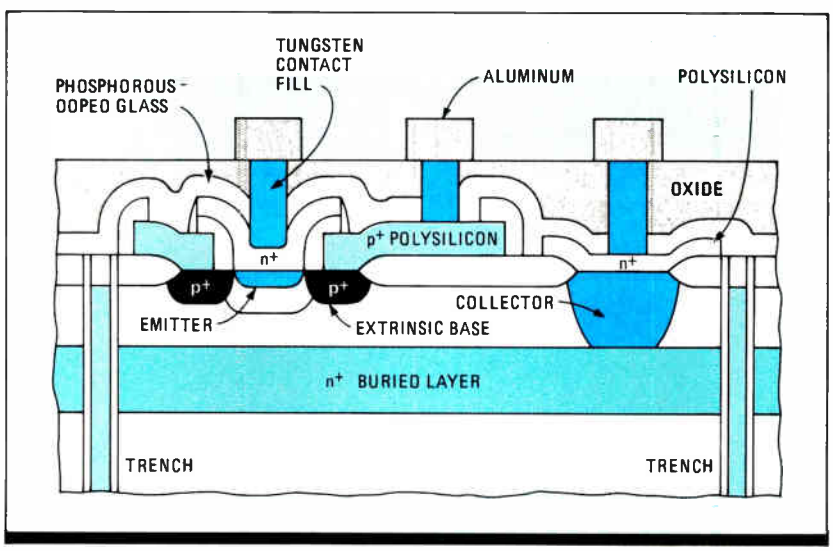
ExCL transistors (see fig. 1) consistently switch at speeds as low as 200 ps; that's 27% to 38% faster than those achieved by transistors built with the process on which ExCL is based, the Implanted Advanced Composed Technology, or Impact-X, an earlier high-speed, polysilicon trench-isolated bipolar VLSI process aimed at speeding up and shrinking transistors [*Electronics*, Dec. 23, 1985, p. 45]. ExCL outdoes Impact-X in transistor speed by reducing the area of the emitter-base region and the spacing between emitter and base contacts.

The process's multilevel interconnect system also increases chip densities and enhances reliability. A novel pillar structure permits chips to be built with three or more levels of metal, using 20% to 30% less chip area than the standard via techniques used in other multilevel-metal systems. With reasonable chip sizes (up to 150,000 mils^2) and four metalization levels, 50,000- to 60,000-gate densities may be attained. The technique for forming the pillars tends to promote reliability by providing a planar surface, one that is unmarred by varying levels.

The result is a high-performance chip optimized for memory and logic—ideal for high-density ECL static random-access memories and gate arrays. TI already is developing both, using ExCL, and could introduce products this year.

The immediate ancestor of ExCL, Impact-X, was itself a breakthrough technology. It replaced conventional oxide isolation in favor of a polysilicon-filled trench to isolate transistors on a chip and made the first production use of polysilicon emitters to boost current gain. Pitch dimensions of just 7 μm were attained. (See table, p. 75).

However, Impact-X fell short of the highest speeds possible with ECLs. One reason is the length of the oxide between the base contact and emitter. This distance affects the base resistance—R_{is}—a key parasitic that affects ECL transistor switching speed. The



1. PACKED. Polysilicon self-aligned bipolar transistors fabricated with TI's ExCL process cut transistor dimensions to get high packing density and performance for ECL VLSI.

emitter-base distance in Impact-X is too wide to reduce R_B to the resistance levels required of ECL transistors.

All of the process and geometry improvements incorporated in ExCL are intended to produce a faster-switching transistor on a smaller silicon area that offers greater reliability than its predecessors. In overcoming R_B limitations and other processing obstacles, TI engineers chose to work with the basic Impact-X process. But along with many of the Impact-X ground-breaking features—trench isolation, polysilicon emitters—ExCL goes farther by reducing the R_B parameter through the use of a silicided polysilicon base contacting layer. Moreover, the distance between emitter and base has been shortened considerably.

A multilevel interconnect system uses metallic pillars for interlevel contacts, taking 20% to 30% less chip area than an etched-via technique would require

In addition to the silicided polysilicon base-contacting layer for lower R_B, ExCL uses polysilicon emitters whose shallow junctions enhance a transistor's gain-bandwidth product characteristic, leading to higher switching speed. Emitter contacts, like those of the base, are covered with silicide to lower resistance.

Polysilicon emitters, in turn, allow the use of buried contacts—contacts under metal—which among other things reduce the need for very tight metal pitch, allowing the designers to pack transistors closer together. Yet another innovation of the process is its highly planar oxide surfaces, which enable ExCl chips to be built with three or more levels of metal.

To use its multilevel metal layers, TI development engineers developed a novel multilevel interconnect system that employs metallic pillars for interlevel contact (see fig. 2). The purpose of the pillar approach was to avoid the restrictive design rules required by the standard etched-via interlevel contact process. In the standard via process, leads must be flared around the top and bottom of the via, restricting the metal pitch and requiring about 20% to 30% more chip area.

The new method involves forming a layer of conductive leads with straight-walled metallic pillars in regions where interlevel contact is desired. Both the lead and pillar metal layers, along with a refractory layer, are deposited in situ and dry-etched with two masking levels. In addition, a tailored interlevel planarization process is used to ensure that the tops of all pillars are etched to clear simultaneously, regardless of size or packing density.

Compared with the traditional via method, pillar interconnections overcome a number of restrictions. First, the process prevents a pillar from falling outside the boundary of a lead, eliminating the need for a flared lead either above or below the pillar, as in the via process. A pillar can be formed on a lead of the same width or on a wider lead. Since flared leads are not necessary, conductor working pitch can be reduced, conserving valuable silicon real estate and enhancing packing density. Moreover, a planar dielectric surface is fabricated over each conductor-pillar level. The surface does not break its planarity to allow interlevel contact.

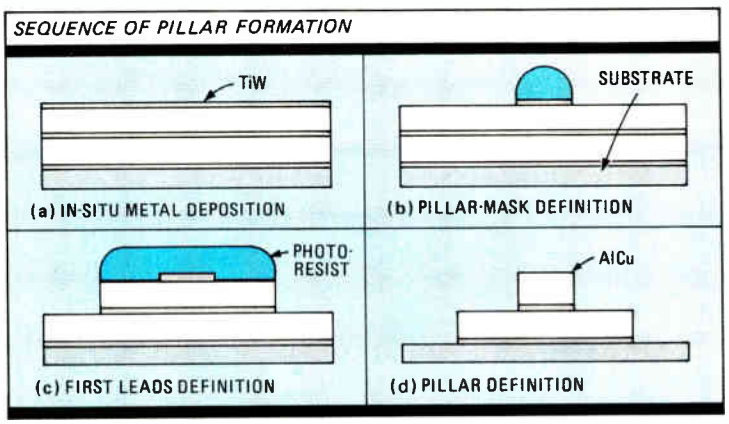
As a result, pillars can be placed directly over previously formed pillars. TI has constructed devices using the pillar technique with metal design rules for a triple-level pitch system having first-, second-, and third-level pitches of 4.0, 4.5, and 7.0 μm respectively, thus paving the way for extremely dense VLSI devices.

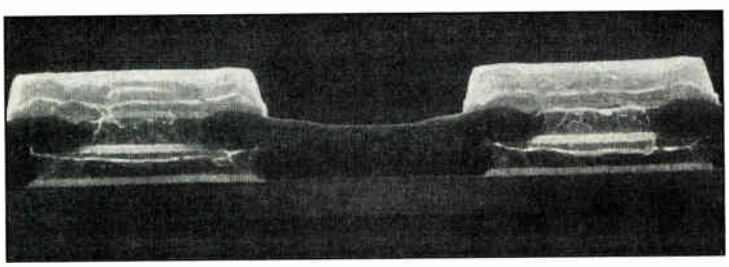
Because of the way in which the pillars are formed, the technique leads to highly reliable chips. To begin, metal is deposited on the surface, followed by an etch for the pillar. Next the lead is etched, and the oxide is deposited over it.

KEEP IT ON THE LEVEL

This process is the reverse of that used in conventional systems in which the oxide is deposited first. The surface resulting from that technique, far from being planar, is pocked by numerous step changes in height, which leads to compromised reliability.

Premetal planarization consists of depositing an oxide on the chip's surface of about l-μm thickness. Much thicker than that of standard processes—which average a few thousand angstroms—it permits interconnections to be run on





2. PILLAR OF STRENGTH. An interconnect method using metallic pillars packs transistors much closer than conventional via connections can.

the first metal level with capacitance that is significantly lower than in conventional devices.

TI uses a technique called contact fill to fill the contacts before planarization, so the metal interconnect plane sits on a very smooth surface, a factor that greatly enhances reliability.

Planarity is also important at the silicon level. It is not affected by the isolation trenches that separate the active transistor areas. During one of the oxidation steps, the top area of each trench is converted to oxide to maintain planarity. Trenches are filled with polysilicon, but their sidewalls are lined with oxide. A thin oxide sidewall coupled with polysilicon fill prevents stress fractures in the silicon and oxide that could occur with a thicker oxide insulation.

Two other key parameters in building faster transistors are the area of the emitter-base region and the spacing between emitter and base contacts; minimizing these parameters results in faster switching performance. In the ExCL process, local oxide isolation of about 4,000-Å thickness, used to define the emitter-base region, reduces the emitter-base area, bringing the nodes into very close contact. The separation between the effective base contact and emitter region is simply the width of an oxide spacer plug. Compared with the distance in Impact-X, the ExCL distance is substantially smaller.

Because the ExCL emitter-base gap is far shorter than in Impact X—3,000- to 4,000-Å oxide width, compared with 2 μm—the base resistance is much lower, on the order of 300 to 400 Ω. Moreover, the inactive base area of ExCL transistors is much smaller than that of Impact-X, a factor that reduces the capacitance between collector and base, and speeds switching.

The speed and power curves of Impact-X and ExCL illustrate the differences in the key specifications for the two processes. Under Impact-X, transistor speed falls in a range of about 275 to 325 ps. ExCL transistors, on the other hand, consistently switch at speeds below 200 ps, and actual device measurements indicate projected switching speeds of 45 to 150 ps, depending on design considerations.

ExCL SHRINKS BIPOLAR DESIGN RULES

Rule	Low-power Schottky	Advanced low-power Schottky	Impact	Impact-X	ExCL
Isolation	Oxide	Oxide	Oxide	Trench	Trench
Isolation pitch (μm)	32	24	20	7	7
Emitter, min. (μm)	4	2.5	2.0	1.5	1.25
Contact, min. (μm)	4	3.0	2.0	2.0	1.5
Metal 1 pitch (μm)	16	11	7 (4)	4	4
Metal 2 pitch (μm)	20	16	11 (7)	4.5	4.5
Via (μm)	6	6	4	3	3
Layers	2	2	2	3	3

Such speeds can be attributed to the process's extremely low capacitance and resistance parameters. The emitter-to-base capacitance is just 20 femtofarads; collector-to-base capacitance measures 5.5 fF. Typical critical base-resistance is at 350 Ω. DC parameters measured a transistor gain between 100 and 200 and a gain-bandwidth product above 10 GHz.

The ExCL process technology has a variety of uses and applications for several classes of products. By design, the process is optimized for high-performance memory and logic. A good example of the former is high-density ECL static RAMS; a good example of the latter is high-density gate arrays. Products addressing these market segments are in development at TI and could be announced during 1987. □

A SEARCH FOR SIMPLICITY ENDED UP ON THE ROAD TO ExCL

"When I sketched out the first ExCL process flow, it was meant to be a simpler and more manufacturable alternative to the complex structures then being researched," says Douglas Verret, bipolar development manager at Texas Instruments Inc. That was in 1983, and TI was exploring the advanced transistor structures that would launch its very large-scale-integration efforts.

Verret first conceived of the process as a version of emitter-down integrated injection logic, which was simpler but slower than emitter-coupled logic. However, that approach proved too slow to be practical, and the thrust of the ExCL development shifted. "ExCL was a natural for ECL all along," says Verret. "We just had our heads turned by the superior packing density of integrated injection logic."

Troy Campbell, who helped start TI's ALS technology, was picked to head the development team. Jeffrey Brighton, a recent MSEE student at the University of Illinois, was recruited as principal engineer. Mixing youth and experience proved to be a winning combination. Working from TI's Impact-X process, the team soon was consistently achieving gate delays far below 1 ns.

But at this point, TI engineers realized that conventional interconnect technology could be a serious drag on ExCL's performance. Verret tapped Ron McMann, an ALS engineer with more than 15 years of interconnect experience, and Mike Welch, a young engineer from the University of Houston. Again, the synergy of youth and experience paid off. "What we got was a sophisticated, high-density interconnect system with excellent reliability that could accommodate the blazing speed of the transistor because of the new system's low parasitics," says Verret.

ExCL DEVELOPMENT TEAM: From left, Ron McMann, Troy Campbell, Mike Welch, Douglas Verret, and Jeff Brighton.

ALTERA MAKES IT EASIER TO BUILD FAST STATE MACHINES

First in a new family of user-configurable microsequencers offers system performance and flexibility that are superior to any other single-chip or to many multichip sequencers

by Bernard C. Cole

Two powerful new CMOS state sequencers that carry on-board microcode based on erasable programmable read-only memories are providing system performance and flexibility superior to any other single-chip—and in many cases multichip—sequencers. Altera Corp.'s EPS444 and EPS448 can be used to build state machines having hundreds of states, compared with only dozens of states that conventional electrically erasable programmable logic devices can have.

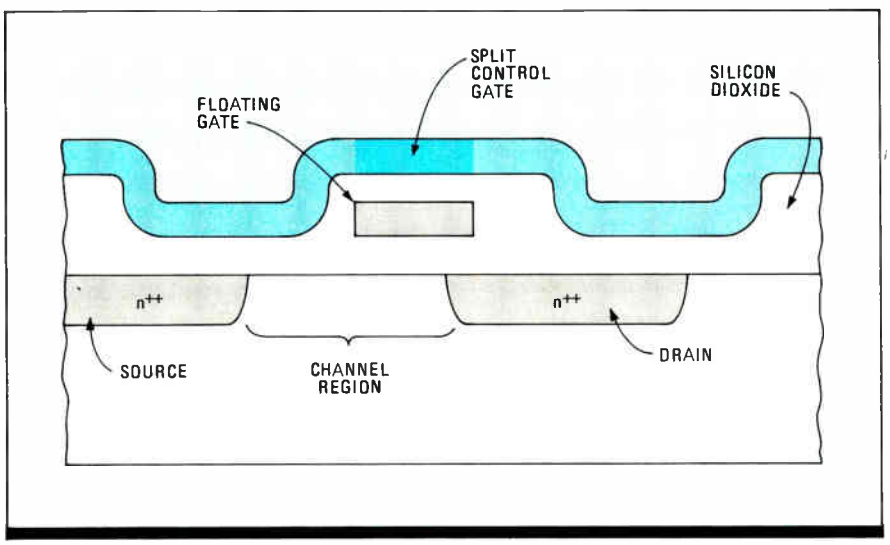
The new devices—the first in a new family of user-configurable microsequencers—will make it easier for designers to build fast state machines. They incorporate an architecture developed by the Santa Clara, Calif., company and are built around a single-transistor, electrically erasable, split-gate structure devised by WaferScale Integration Inc., of Fremont, Calif. The microsequencers will be fabricated with an advanced 1-μm CMOS process by Sharp Corp. of Japan.

Altera uses WaferScale's cell to incorporate on a single chip an architecture which enables users to implement designs that can do very complex multiway branching operations quite fast, using either a truth-table state machine, microcoding, or both. Unlike bipolar state machines, the sequencer is reprogrammable on the fly. And unlike bit-slice-oriented sequencers, the microcode can be stored on-chip, rather than externally. Further, unlike traditional programmable logic arrays, where no more than 400 to 500 product terms are available, this new approach allows implementation of designs using more than 100,000 product terms.

These stand-alone microsequencers, or SAMs, combine three divergent technologies in one chip: CMOS-based electrically erasable programmable logic devices built around Monolithic Memory Inc.'s programmable array logic; state-machine, or truth-table-based, sequencers made with bipolar PLAs, and microcode-based bit-slice sequencers. Currently, PAL-based devices are used primarily to integrate simple glue-logic combinatorial functions on one integrated circuit. Applications requiring the manipulation and control of a sequence of operations are usually done by a control sequencer. For simple two-way branching operations where speed is essential, truth-table-based bipolar PLA-type state-machine sequencers are used. For multiway branching, in which several levels of operations must be controlled, designers usually choose multichip bit-slice microsequencers, which allow control via externally programmed microcode.

The EPS444 and 448 are integrated solutions for state machines and microcode controllers requiring up to 448 states, or words of code, such as memory- and interrupt-controller designs and compact processing engines for floating-point and digital-signal-processing tasks. Combining the EPROM microcode memory and associated sequencing logic—stack, loop counter, and multiway branch block—with advanced CMOS technology on a single chip yields performance better than 35 MHz.

The two chips are scheduled to come to market in mid-1987, togeth-



1. SPLIT GATE. Key to the density and high speed of Altera's stand-alone microsequencer is the use of a split-gate, single-transistor EPROM cell for both read and write operations.

er with development tools. They will be followed by larger (44- and 68-lead) and more complex versions. Altera and WaferScale are pursuing a broad base of controller applications, including VMEbus and Multibus controllers; support functions, such as arbiters, interrupt handlers, and mailboxes; floating-point and industrial-control processors; cache and dual-port memory control, and graphics-transform accelerators.

The SAM architecture and performance theoretically allow the devices to be used as bit-slice controllers for applications with system cycle times as short as 30 ns, if the other system elements can be made to match. In practice, the fastest that can be achieved today is a 50-ns cycle. Even this is twice the performance that can be achieved using traditional multichip 2900-family bipolar components of a year or so ago. The availability of the SAM devices means that the speed of the sequencer no longer determines maximum system performance.

EIGHT INPUTS, BETTER THROUGHPUT

Just as important as the improved performance and flexibility is the incorporation of multiway branch-control logic into the SAM architecture. Multiway branch capability in a single clock cycle greatly enhances throughput over conventional controllers and sequencers that have only two-way branching, says Stan Kopec, Altera's manager of product planning. Eight general-purpose inputs to the branch-control logic are available to modify control flow without external multiplexing, thereby eliminating a major bottleneck. In addition, SAMs may be cascaded in a building-block fashion to achieve designs of higher complexity.

The key to the functional density—100,000 product terms—and the speed of SAM devices is WaferScale's split-gate, single-transistor electrically erasable cell (see fig. 1), which when combined with 1-μm CMOS technology allows speeds rivaling those of bipolar. This is because the split-gate structure yields bit-line read currents in excess of 150 μA, compared with the 50 μA typical of conventional EPROM cells, providing the equivalent of the traditional multiple-transistor EPROM cell without its die-size penalty.

In addition, the use of silicide rather than polysilicon virtually eliminates RC delays associated with polysilicon interconnect lines. This ensures the speed of dual-layer metal without the attendant cost and yield penalties.

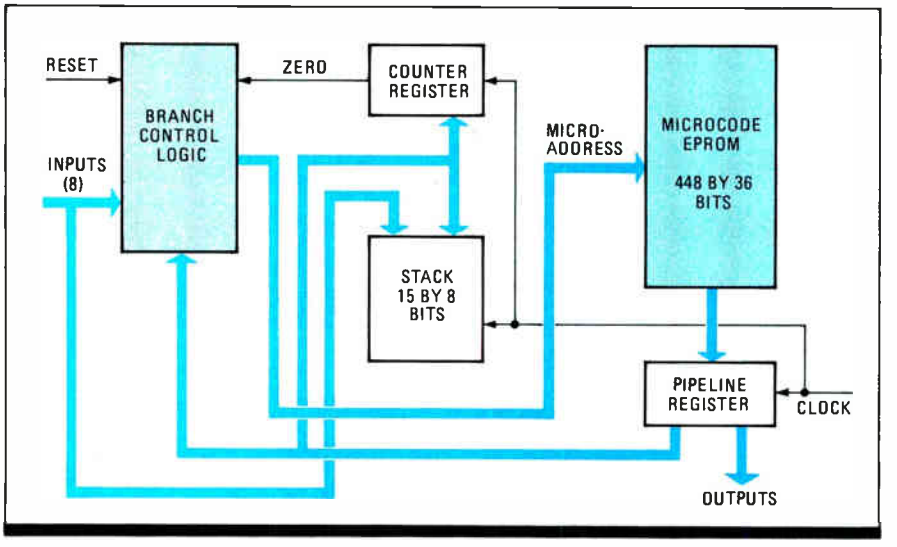
The SAM architecture (see fig. 2) forms a 448-state Moore-machine sequencer having several features not found in the traditional canonical Moore state machine. For one thing, each 36-bit word carries its successor's address, so no program counter is required. In addition, the output of the microcode EPROM is clocked into the pipeline register synchronously on the clock's rising edge. Also, users can define either 12 (on the EPS444) or 16 (on the EPS448) of these bits at device pins as outputs. The state of the lines can therefore be defined on a clock-by-clock basis as a function of current state, forming a Moore-machine architecture.

At the heart of the high-performance sequencing ability of the SAM family is the branch capability. This capability is controlled by the branch-control block, which contains eight dedicated inputs to the device and the current state of the sequencer. The outputs from this block select the destination states of branch locations in microcode memory. A default destination is also provided to easily handle Else constructs in If, Then, Else expressions.

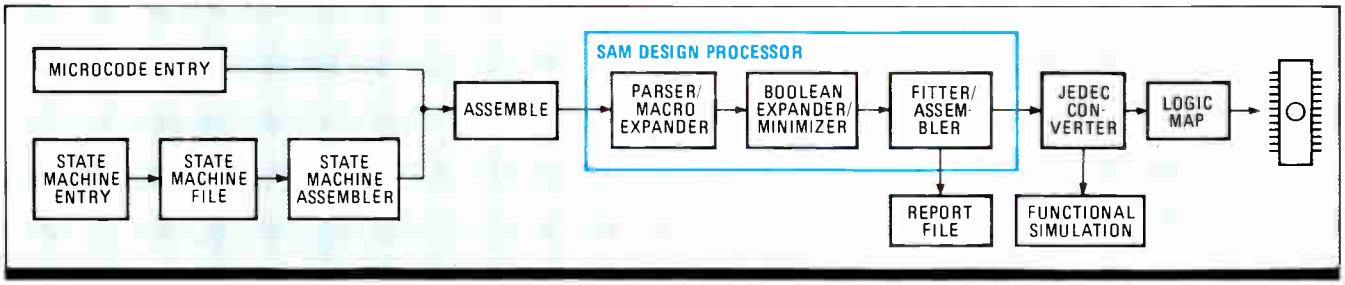
The SAM has a last-in, first-out stack consisting of 15 eight-bit words. The counter register or microcode address may be pushed or popped to or from the stack under microprogram control, making it easy to create nested loops, microsubroutines, and other iterative structures. The eight input lines may also be pushed to the stack to allow external address specification.

Altera's Sequencer Design Software (see fig. 3) gives the user a higher-level view of the branch-control block so that machine or algorithm development can occur at a conceptual, rather than bit, level. This is important, because the capacity of this block is equivalent to 768 product-terms of transition specification in a traditional EPLD. The Altera software generates a standard Jedec programming file, from which the required EPROM cells may be programmed for branch equations.

The SAM instruction set avoids complex high-level instructions, which impose algorithmic constraints, since the device is user-configurable and must cover a wide range of applications.



2. HOT COMBO. Altera's stand-alone microsequencer combines the best features of CMOS EPROM technology, microcoded sequencers, and state-machine architectures.



3. SAM SOFTWARE. Using the SAM design-processor program, users can program the EPROM-based microsequencer using either state-machine truth tables or on-chip microcode similar to that of a bit-slice device.

Devices may be cascaded horizontally to obtain greater output capability. For microcode memory greater than the 448 words provided, devices may be stacked vertically.

Each microcode word contains an output-enable control bit that activates the outputs of the SAM when programmed to a 1. These bits are accessible through high-level constructs in Altera's development software, allowing vertical and horizontal device cascading. By partitioning control functions between two or more devices and activating one device's outputs onto the control bus at a time, microcode of arbitrary depth may be obtained. In addition, multiple devices may be run in lock-step to obtain greater output width. For example, three devices can be used to yield a 48-bit-wide output control word. The microcode of these three devices, along with shared inputs and clock, ensure their synchronization.

SAM devices are supported with a software and programming-adapter upgrade to Altera's IBM Personal Computer-based EPLD development system. The software supports microcode generation through high-level programmatic state-machine entry and sequencer microcode compilation. It will also be available on Digital Equipment Corp. VAX and other computer platforms. This development software provides a high-level method of state-machine or assembly-level entry. Complex state-machine flows may be specified using the If, Then, Else constructs familiar to users of bit-slice sequencers and the truth-table format favored by most users of field-programmable logic devices. □

A BROAD-BASED TEAM DEVELOPED ALTERA'S MICROSEQUENCERS

The concepts behind the SAM family of stand-alone microsequencers represent the efforts of a multidisciplinary team from throughout Altera Corp., including members of the product-planning, applications, silicon-design, and software-engineering groups. In SAM development, for instance, tool definition, rather than being subsidiary to device demands, interacted with and in some cases modified device architecture.

One example of this was the decision to have multiway branching hardware solve the problem of ensuring that only one case selector would come true at a time. The design-description language imposes a priority sequence on the branching conditions; that is, the first condition on the list which evaluates as true is taken. In this way the priority sequence behaves much like sequential "if-then" statements in a software program. In hardware, all of these decisions are made at the same time.

Much of the success of the project hinged on a team that blended expertise in system architecture and development-tool software with traditional integrated-circuit design skills, says David A. Laws, 45, vice president of the Santa Clara, Calif., firm. Kevin Norman, 31, head of the silicon-design team, brings a background in high-performance CMOS logic design and microprocessor architecture gained in the Clipper project at Fairchild Semiconductor Corp. And Stan Kopec, 36, manager of Altera's product-planning activities, brought to the project more than 10 years of microprocessor peripherals definition and design experience at Exel Microelectronics Inc. and Intel Corp.

Clive McCarthy, 40, director of product planning and applications, brought the user's perspective to the task. He was always immersed in hands-on work, from writing a Jedec converter program to alpha-testing a new software release. Also involved in simplifying the software user interface was Michael Glaviano, 37, of the software engineering group, who worked with both silicon designers and applications engineers to ensure an easy transition from the state-machine input specification to programmed silicon.

To smooth the transition from concept to implementation required some engineers to move between disciplines, Laws says. For example, Kerry Veenstra, 25, transferred with the SAM project from applications to the silicon design team. His contributions included device architecture and generation of a software simulator to facilitate design of the device and test programs. Overseeing the SAM effort was Robert Hartmann, 44, vice president of engineering and a founder of Altera, whose insight into the strengths and weaknesses of gate-array design and applications led him to develop the user-configurable IC concept on which the company is based.

MANY TALENTS. Altera's multidisciplinary team includes (from left) Glaviano, McCarthy, Norman, Hartmann, and Kopec.

SONY PACKS POWER INTO LOW-COST WORK STATIONS

Two MC68020 processors allow the machines to handle heavy network loads, with a dedicated I/O processor freeing the CPU to run applications

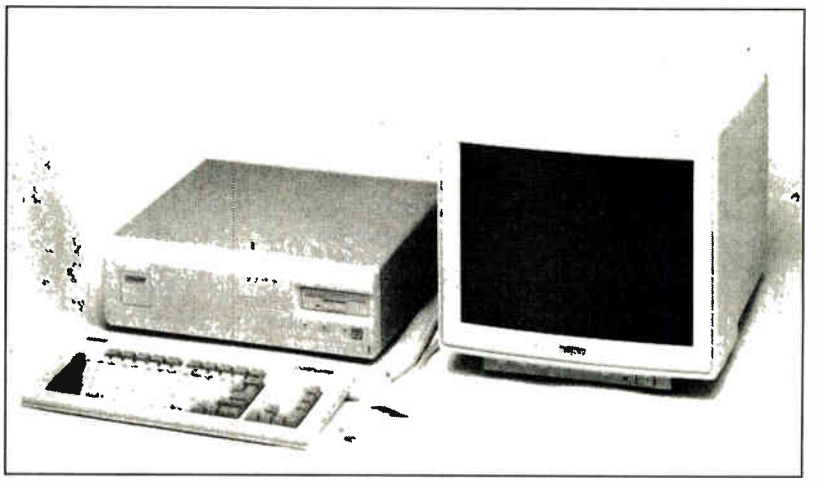
A consumer electronics giant, Sony Corp., has jumped into the work-station market, with a family of powerful but low-cost machines designed for software development. Called NEWS, for network station, the family consists of three work stations introduced recently in Japan that range in price from $6,500 to $17,900 (see fig. 1). They use two 16.67-MHz Motorola MC68020 microprocessors—one for the central processing unit and the other for an input/output processor—and a 16.67-MHz MC68881 floating-point processor.

Sony packed a number of functions into a compact, high-performance package (see fig. 2). Backing up the 68020 CPU is an I/O processor using another 68020. An 8-K-byte instruction cache is included on the top-of-the-line machine. All models are equipped with a memory-management unit designed and built by Sony, plus a standard Small Computer Systems Interface bus for I/O peripherals. Networking for NEWS stations is provided by Ethernet and the TCP/IP upper-level protocol, and all the machines have high-resolution bit-map displays. A VMEbus interface is added for additional I/O flexibility.

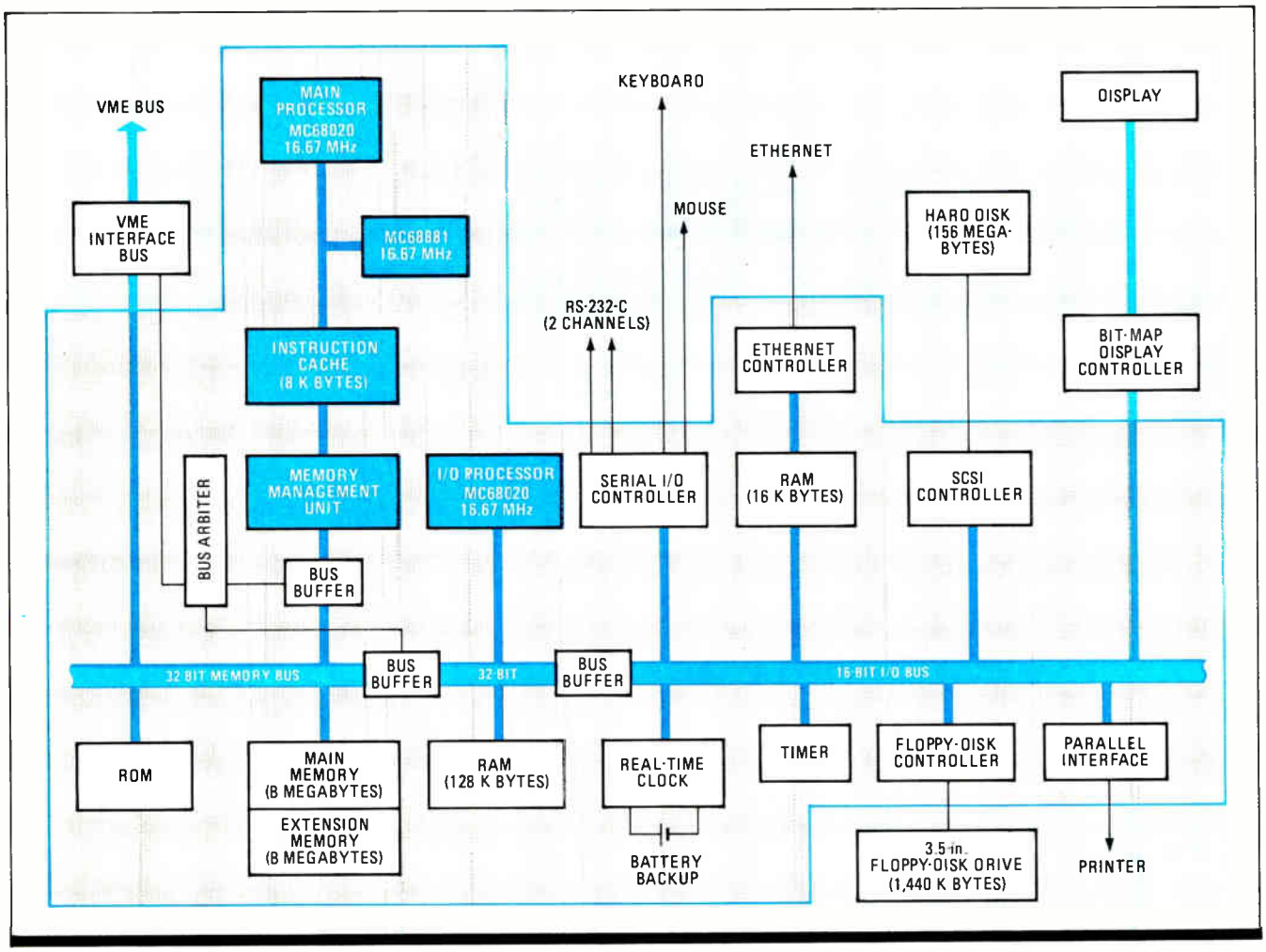
The NEWS offering includes Japanese-language versions of standard software, the 4.2 BSD Berkeley version of AT&T's Unix, Sun Microsystems Inc.'s Network File System (NFS) for file sharing and distributed processing, and the X Windows user interface developed at Massachusetts Institute of Technology and supported by a number of international vendors [*Electronics*, Jan. 22, 1987, p. 58]. The machines, available now in Japan, will be sold in the U. S. by the end of the year.

In general, 32-bit microprocessors can perform well with Unix, but they sometimes run into trouble with heavy I/O loads caused by local-area network connections, bit-map displays, and serial I/O devices. To compensate, a 16-bit processor or a direct-memory-access controller is often used in each peripheral device, but this results in more complicated and expensive hardware. With the NEWS design, the single I/O processor in the host does all the direct-memory-access and I/O processor functions, freeing the CPU's power to run applications.

☐ *This Technology to Watch was adapted from an article written by Masao Hori, Katsutoshi Doi, Hiroshi Tezuka, Takashi Yosida, Nobuyoshi Kimura, and Yasunori Yamashita of Sony Corp., Tokyo. The original article ran in Nikkei Electronics, which is published by Nikkei-McGraw-Hill Inc., a joint venture of McGraw-Hill Inc., publisher of* Electronics, *and Nihon Keizai Shimbun.*



1. CLEAR PICTURE. The 32-bit NEWS station has high-resolution bit-mapped graphics.



2. SQUEEZE PLAY. Sony packed many functions into the compact NEWS system unit, most of them on the main board (shaded area).

Because of the I/O processor's dynamic bus-sizing capability, data can be transferred from both 8-bit and 16-bit I/O devices to the main memory with one Move instruction, which automatically converts the data width. Besides functioning as a direct-memory-access controller, the I/O processor performs other I/O processing, including interrupts. To handle real-time processing, the I/O processor also has a real-time multitask monitor.

Since the I/O-processor program memory and the I/O devices are completely isolated from the main memory bus, operation of the CPU is impeded only during data transfer and communication between the I/O processor and the CPU. The main memory is shared by the two processors.

Part of the 8-K bytes of main memory is reserved for communications between the two processors. Through this area, a command from the CPU is passed to the I/O processor and the response from the I/O processor is returned to the CPU. Either of the processors can enable communications by transmitting an interrupt signal.

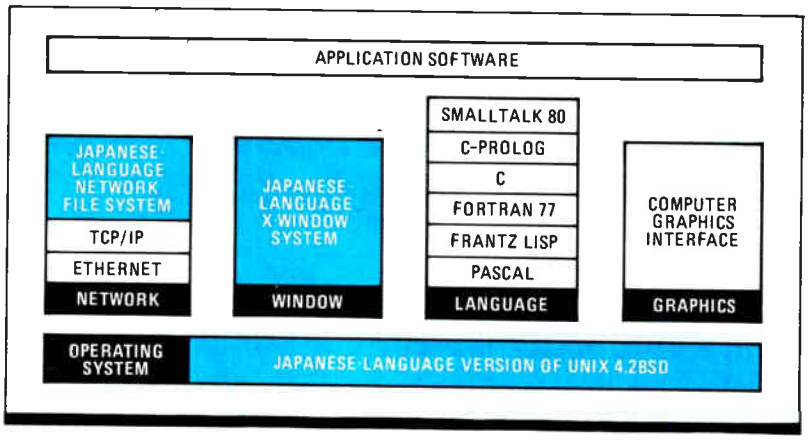
The direct-mapped 8-K-byte instruction-cache memory in the top-of-the-line model 830 is used to achieve the difficult task of no-wait operation of the 68020 at 16.67 MHz. Instructions are cached in a 35-ns static random-access memory so that they can be fetched by the CPU with no wait states. When a cache miss occurs, the system acts as if there is no cache, which speeds up fetching of instructions that are not in the cache. The main memory offers a high-speed one-wait operation, making it possible to maintain nearly the same basic performance, even with programs of a rather low cache hit rate or on the NEWS models that have no instruction cache.

The single-level-paging, virtual-memory architecture of the NEWS is made possible with the Sony-designed memory-management unit. The MMU uses 35-ns SRAM and some standard ICs. It supports demand-paging virtual memory. One-level paging, with a page size of 4-K bytes, is used. The originals of the MMU page-table entries are stored in the main memory, and the MMU serves as the cache for them.

The SCSI interface on the NEWS can accommodate eight peripheral controllers. The protocol of the SCSI interface is not dependent on hardware, making it possible to add new devices without developing new interface hardware—a very desirable feature for a product such as NEWS, which needs to be expandable in an economical way. For

example, hard disks, magnetic tapes, and optical disks can be connected with only a few software modifications.

The SCSI bus is an ANSI-standard daisy-chain bus for 8-bit parallel data transfer between a peripheral device and a computer's main memory. It is capable of 1.5 megabytes/s for asynchronous transmission and 4 megabytes/s for synchronous. SCSI protocol implementation is shared between the CPU and the I/O processor. The I/O processor takes charge of those basic parts that remain unchanged regardless of the device connected—namely, the target select, command send, data send/return, parameter set for disconnect/reselect, and command sequencing. In contrast, the CPU is equipped with drivers unique to individual devices.



3. SOFTWARE LINEUP. Software includes a Japanese-language version of Unix 4.2 BSD, Sun Network File System, and X Windows user interface.

The network interface provided with NEWS is the standard IEEE 802.3 Ethernet. The complete interface, employing the AMD Am7990 Lance local-area-network controller and Am7992 serial-interface adapter chips, resides on the system board, so NEWS can connect directly to the Ethernet transceiver on a coaxial network cable.

The Lance controller is complemented by a 16-K-byte bidirectional transmission and reception buffer between the I/O processor and the network interface. The capacity of this buffer is 10 data packets. In addition to controlling the network interface directly, the I/O processor also controls transmission and reception on the packet level. High-level protocols, such as TCP/IP, are placed under control of the CPU to make it easy to cope with additional protocols, such as XNS.

Realizing a high-speed, versatile multi-window display system requires hardware with the bit boundary block transfer, or bitblt, function. In both the color and monochrome bit-map displays available for NEWS, the bitblt hardware is implemented with a 2,000-gate gate array for high-speed operation. The color display uses one gate array for each color plane, all of which are operated concurrently so that multiwindow processing in color can be done as fast as it can for the monochrome display.

When the optional VMEbus interface board is added to NEWS, VME peripherals can be connected and put under control of the CPU. The CPU operates as the bus master for controlling access to slaves on the VMEbus. Both addresses and data words are 32 bits wide.

In providing software for NEWS, Sony designers gave priority to several features, including a Japanese version of Unix 4.2 BSD, integration into an Ethernet local-area network, a multiwindow user environment, Japanese versions of other key software, support for several programming languages, and graphics (see fig. 3).

NFS was chosen to provide distributed processing among networked NEWS work stations. With NFS, users can mount the file directories of a remote machine to their local machine. Thereafter, the files on the remote machine referenced in the directories mounted on the local machine can be accessed just like local files. To take advantage of NFS, as well as to cope with different file systems such as MS-DOS, the software engineers added a new layer called VFS (virtual file system) in the upper part of the Unix file system. The differences between processors, such as a VAX and a 68020, are absorbed by the lowest layer of the NFS protocol, the external data representation.

Early in the development of NEWS, Sony decided to adopt the X Windows system, Version 10, Release 3 and translate it into Japanese. This system not only is independent of the network used, but also offers a library to help the user work with a window tool of his choice. In these respects, it satisfied the two requirements the engineers had in mind for the NEWS multiwindow environment: establishing a flexible environment that meets every user's needs, plus increasing efficiency in software development.

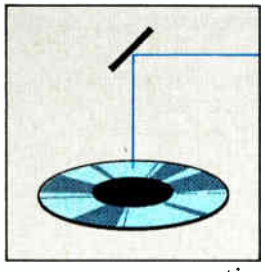
Interprocess communication via a socket is used for interfacing the window server with the window tool. The socket can accept an X Windows tool from a work station using a different CPU. The operating system handles the X Windows system as two different processes: the server process and the window-tool, or client, process. X Windows is activated in two steps. First the server and the log-in window are started by the "xinit" Unix command, and then the log-in window starts the necessary clients.

NEWS is only the first step in Sony's effort to develop work stations for software engineering. To provide a sophisticated software-development environment, Sony says, it intends to continue to develop a variety of tools and application software, including software development tools, artificial-intelligence tools, management tools, business software, and a scientific/technical calculation package. Sony also plans to strengthen the family's peripheral-equipment lineup to enable its work stations to expand into other applications.□

THE OPTICAL-DISK INDUSTRY GROPES FOR STANDARDS

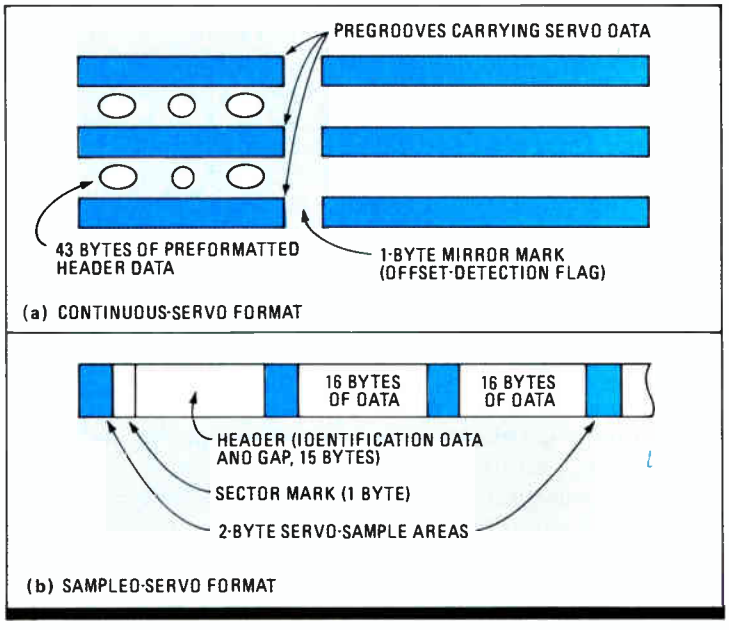
If it fails, the chaos in 12-in. write-once disks could spread to the emerging 5¼-in. products

by Jonah McLeod



Systems integrators simply can't resist the lure of optical disks for bulk data storage. That's why many of them have walked the extra mile to put the disks into systems despite the almost complete lack of standards in this fledgling industry.

And for vendors of 12-in. write-once optical disks—also called write-once, read-many, or WORM, disks—the situation approaches chaos. The industry has no recording- or logical-format standards; the only thing drive makers have been able to agree on is disk size. Makers of the newer 5¼-in. write-once disks have been trying to avoid creating the same kind of chaos that afflicts the 12-in. world. However, there are still two strong recording-format contenders vying for the 5¼-in. standard: the continuous-servo format and the sampled-servo format. The American National Standards Institute's X3 B11 Optical Digital Data Disk committee is looking at both formats, hoping to choose one as an industry-wide standard (see fig. 1). But it may be forced to accept both.



1. FORMATS. Some makers of 5¼-in. optical-disk drives prefer the continuous-servo recording format (a); others support the sampled-servo format (b).

The market for write-once drives will grow some 80% per year during the next five years, mostly because of the opportunity to replace paper and microfilm data storage, says Raymond C. Freeman of market analysts Freeman Associates Inc., Santa Barbara, Calif. About 95% of the world's information is still in forms not readable by computers—mainly on paper. For many paper applications, especially documents that may be used for legal purposes, the nonerasability of write-once disks is an advantage. Furthermore, optical-disk storage has a volumetric efficiency nearly 10 times that of ½-in. tape.

Although the number of read-only drives shipped will exceed the write-once machines, the write-once drives will make up 74% of wordwide optical-disk revenues in 1991, Freeman predicts—up from $181 million in 1986 to $1.14 billion in 1991. Write-once drives with capacities less than 1 gigabit—including 5¼-in. types—will constitute 61% of the units sold in 1991, but 1-to-3-gigabyte 12-in. drives will capture 83% of the revenue because of tighter competition at the low end of the market.

A BLOCKED PATH

However, without an industrywide development effort to produce a standard product and a set of common applications, the path to rapid technical development and declining product costs remains all but blocked. The optical-disk industry has been left floundering about, looking not only for standards, but, in their absence, for profitable market niches and ways to integrate optical disks into existing systems.

The lack of standards has severely hampered the efforts of system integrators to incorporate the drives into computer systems. They have managed to find a number of applications by replicating existing magnetic-tape and Winchester-disk storage formats. And they have written complex software routines to hide the write-once nature of optical disks from such host-computer operating systems as MS-DOS, used by IBM Corp.'s Personal Computers and compatibles, and VMS, from Digital Equipment Corp. Unisys Corp. of Blue Bell, Pa., has added the necessary software driver to its Univac operating system to handle its new optical-disk drive. Another ANSI effort seeks to set up a logical-format standard for 12-in. write-once disks so that systems can view the drives in a consistent fashion, even

if the disks are still not interchangeable.

The optical-disk industry's lack of direction has also been manifested in its attempts to sell the devices for the wrong applications. System users have been unwilling to give up established and reliable tape and Winchester disk drives for a newcomer that not only is expensive, but also asks them to adapt to nonerasable media. Besides, Winchesters are much faster in terms of access time.

But there is at least one potentially important niche developing for write-once disks: in document storage and retrieval systems that use optical drives and disk "jukeboxes" for storage of copies of paper documents. Document storage and retrieval systems, such as one offered by FileNet Corp. of Costa Mesa, Calif., have replaced many paper-based filing systems. Other systems, such as the Kodak Information Management System, are supplementing or replacing microfilm archives.

Currently, document storage and retrieval is done most frequently with 12-in. disks for big jobs at corporations like banks and insurance companies, which have significantly greater volumes. For 5¼-in. drives, document storage and retrieval systems mean markets where the volume of data to be stored is relatively low, down to minicomputer and personal-computer markets. Within those markets, acceptance of 5¼-in. drives is expected to come quickly—once standards are set.

THE BATTLE OF THE FORMATS

The divisiveness of the proposals before the ANSI X3 B11 committee reflects the fact that no single large supplier has a big enough installed base to influence the standards-making process. As a result, neither of the opposing format factions has the power to push the other out of the 5¼-in. picture.

The continuous-servo recording format derives servo information from what are called the pregrooves, V-shaped valleys in the space between data tracks (see fig. 1a). In the sampled-servo approach, on the other hand, two bytes of servo information are written at the start of each sector, and in between every 16 bytes thereafter (see fig. 1b). Each spiral track for either format is divided into 17 or 32 sectors, depending on the number of bytes per sector. Different Winchester magnetic-disk drives use both continuous- and sampled-servo approaches, but disks are not removable from a Winchester drive, so format compatibility is not that important.

A comparison of the two alternatives for 5¼-in. disks (see table) gives no clear indication as to which might have an advantage. Both require about the same overhead, and both offer about the same amount of storage capacity.

Supporting the continuous-servo approach is Gordon Knight, director of optical products at Maxtor Corp. in San Jose, Calif. "After looking at both schemes, Maxtor decided to support the continuous-servo format," he says, "because it will be easier to build drives with faster access times and disk rotational rates, and greater storage."

Backing up this view is the fact that the continuous-servo approach is better adapted to self-clocking modulation codes. The clock for timing the writing or reading of data from a disk is extracted from the data itself. Continuous-servo proponents have settled on a 2,7 run-length-limited (RLL) code, which makes possible an increase in density with no increase in the number of bits written on the disk. Double-density recording can be added in the future with pulse-width recording techniques, in which information is contained in the width of the written bit, as well as in the absence or presence of a bit.

Hitachi America Inc. officially supports both servo approaches, but a spokesman says that the self-clocking feature of the continuous-servo scheme adds to data reliability, because it eliminates data shifts resulting from changes in the media. In the sampled-servo approach, clocking data is contained in the servo burst in the sector header and interspersed within the data field.

OPTICAL-DISK RECORDING FORMATS: THERE'S NO CLEAR WINNER

Parameter	Continuous-servo recording format		Sampled-servo recording format	
Sector size, bytes	1,024	512	1,024	512
Number of sectors per track	17	32	17	32
Bytes per sector	1,360	727	1,368	702
Bytes per track	23,120	23,264	23,256	22,464
Linear density, μm/bit	1.02	1.01	1.01	1.05
Servo data, bytes per track	0	0	1,292	1,248
Format overhead, %	32.8	42.0	33.6	37.1

SOURCE: AMERICAN NATIONAL STANDARDS INSTITUTE

Another advantage of the continuous-servo approach is that the read/write head is always supplying feedback as to its position on the disk surface, the Hitachi spokesman says. As the head moves over the disk surface from one track to another, it is constantly reading servo data.

In the sampled-servo approach, the read/write head has to settle on a track and capture an intermittent burst of servo data. But because the continuous-servo head always has servo data, its supporters claim that the drive can accelerate and decelerate the head faster.

The opposing view is taken by Martin de Haan, vice president of research and development at Laser Magnetic Storage International, a Colorado Springs, Colo., joint venture of Philips International NV of Eindhoven, the Netherlands, and Control Data Corp., Minneapolis, Minn. "We selected the sampled format because we felt it was better for accommodating future systems," he says.

The sampled-servo technique does not require pregrooves, which are built into the media be-

fore the disk ever enters a drive. These pregrooves are particularly troublesome in the case of magneto-optic media, making it much more difficult build a reliable drive-media combination. Drives built for the sampled-servo format "can more easily handle a wide variety of different media, including disks that will result from future advances in the technology," says Haan.

ANSI's X3 B11 committee may have to select both of the recording formats, because if it chooses just one, the losers will simply ignore the standard

This is also important because at this stage, nearly every media supplier takes a different approach to optical media.

The sampled-servo format will help drive-makers build the multifunction drives they are planning for the future. "With the multifunction drive, the user can have mass storage using an erasable optical disk, and he can load programs and databases using optical read-only memory (OROM)—the equivalent of the CD-ROM, but on a disk with a 5¼-in. diameter," says Lawrence Fujitani, director of marketing at Optimem of Sunnyvale, Calif. The write-once disk would be used for archival storage in this type of product.

To accommodate read-only, write-once, and erasable magneto-optic media requires a drive with broad operating characteristics. Read-only types "have a reflectivity of between 70% and 80%, while magneto-optic disks have a reflectivity on the order of 30% to 40%," says Fujitani. Write-once disks fall in between these two extremes.

The continuous-servo camp has arrived at a unified standard format on track and sector focusing, as well as tracking data and modulation code, says Gary Lee, manager of advanced development at Scientific Micro Systems Inc., Mountain View, Calif. They settled on 2,7 RLL and the long-distance Reed-Solomon error-correction code developed by Neal Glover, president of Data Systems Technology of Broomfield, Colo., which has become a de facto standard thanks to its implementation as an integrated circuit by Scientific Micro Systems.

The sampled-servo camp has achieved less accord, Lee reports. They have not agreed on modulation and ECC type. Optimem is holding out for 2,7 RLL with the Reed-Solomon code, while Sony Corp. of America, Park Ridge, N. J., and Laser Magnetic Storage International want 4,15 modulation code with product-code error correction.

The ANSI X3 B11 committee has reaffirmed the goal of having one standard, says Joseph Zajaczkowski, chairman of the committee and executive vice president of Cherokee Data Systems in Boulder, Colo. But he concedes the possibility still exists that there will be two, because if the committee selects one of the two proposals the losers will simply ignore the standard.

The lack of standards has not stopped enterprising companies from building products that use optical disks, although they have taken more time to develop. The petroleum industry, for instance, has been willing to offload seismic data from magnetic tape, a highly standardized storage medium, onto nonstandard optical disks.

In this application, a single user must access a large amount of data on-line for a long time, which used to mean tying up a large computer system with multiple reels of tape. With optical disks this application is now performed on a work station. One integrator innovating in this market is Landmark Graphics Inc. of Houston. On Landmark's system (see fig. 2), each optical-disk cartridge can contain the equivalent of twelve 6,250-b/in. magnetic-tape reels—enough for an average three-dimensional seismic survey.

Users, however, are concerned about going from the highly standard ½-in. tape medium to a largely nonstandard optical-disk medium without second sources. That's why an ad hoc ANSI committee has started to set up some logical format standards for 12-in. optical disks. "Even if you do not have a physical format that is compatible, if there is a logical format, then the media can appear transparent to the operating system," says Larry Fujitani of Optimem. "The logical standard gives the system integrator a stake in the ground that says 'here is an interface' between the host software and what the integrator has to provide in the form of a software driver."

In one approach, the optical disk is treated as a file server for a Wang system. "We decided not to treat the optical disk as an alternative to tape," says Charles Bennett, executive vice president at Image Management Systems Inc. of Providence, R. I. The company makes a

2. DATA BASE. An optical-disk-based work station from Landmark Graphics gives the user access to a huge data base containing a three-dimensional seismic survey, freeing up a mainframe.

12-in. optical-disk-drive subsystem, the Office Archiver 2000, that is integrated into a Wang personal computer. The computer is connected to a larger Wang running under the Wang VS operating system.

"Our system does not use the operating-system commands of Wang VS to access the optical disk," says Bennett. "Rather, we wrote our own software, which stores files on the optical disk just as they appear on a magnetic disk."

"The next version of our system will make the optical disk a true file server in a networked environment," says Bennett. This version will tie the optical disk to a 3200 work station from Sun Microsystems Inc. of Mountain View, Calif. A Winchester will be used to cache frequently accessed files from the optical drive, and users will access the server over an Ethernet.

A system with this kind of capabilities, the 7250 Series, is already available from Tallgrass Technologies Corp. of Overland Park, Kan. (see fig. 3). "We devised three ways of putting data on the disk," says Michael Kaufman, optical-products manager at the company. One way is for the system to directly write, or capture, to the disk, which is good for gathering data. A second way is to write data to the magnetic-disk cache. Information being frequently updated can be changed on the magnetic disk and then automatically offloaded to the optical disk when accesses to it become infrequent.

A third method is to place files on the magnetic disk and let the user determine when to capture data onto the optical disk for backup purposes. Like most other system integrators, Tallgrass tried to keep the software that accesses the optical drive as transparent as possible to the host operating system, which in this case is PC-DOS. "We had to add only one command—capture—to the basic DOS commands to accommodate our optical drive," says Kaufman.

But the software for accessing optical-disk drives is, like the disks themselves, still not standardized. Add-on systems builders offer their own solutions. "On the LX400 optical storage subsystem we offer, we write software drivers that make the optical disk look like a magnetic-disk drive in the DEC environment," says Don Murray, product manager at Emulex Corp. of Costa Mesa, Calif.

One of the first computer companies to begin providing software drivers for write-once drives is Unisys, the company formed out of the merger of Burroughs Corp. of Detroit, Mich., and Sperry Corp. of Blue Bell, Pa. The Unisys 5071 optical disk system, which uses the Hitachi drives, ties directly to the company's 1100 mainframe block-multiplex channel, just as a magnetic drive would.

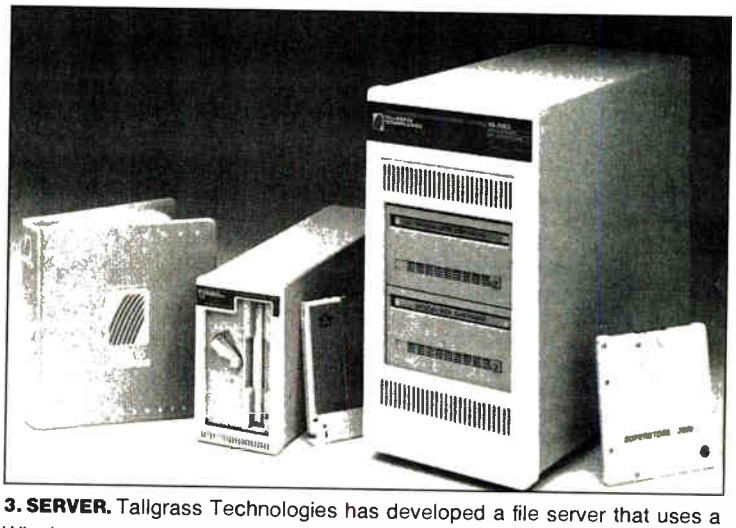
The software package allows the user to provide the basic functions to access a removable optical disk. It can provide random access to records on the disk, but a faster method of accessing such data is to move the file containing the record onto magnetic disk and make all accesses to the file from there.

Optical disk systems have had their best successes in an area not usually associated with data processing: office automation. Optical drives have made inroads into document storage and retrieval, where paper filing has been the standard method and where microfilm also thrives. Large systems, such as the disk jukebox from FileNet Corp. of Costa Mesa, Calif., that is capable of loading one of many optical disks into one of several drives, are typical of those going into insurance and financial institutions.

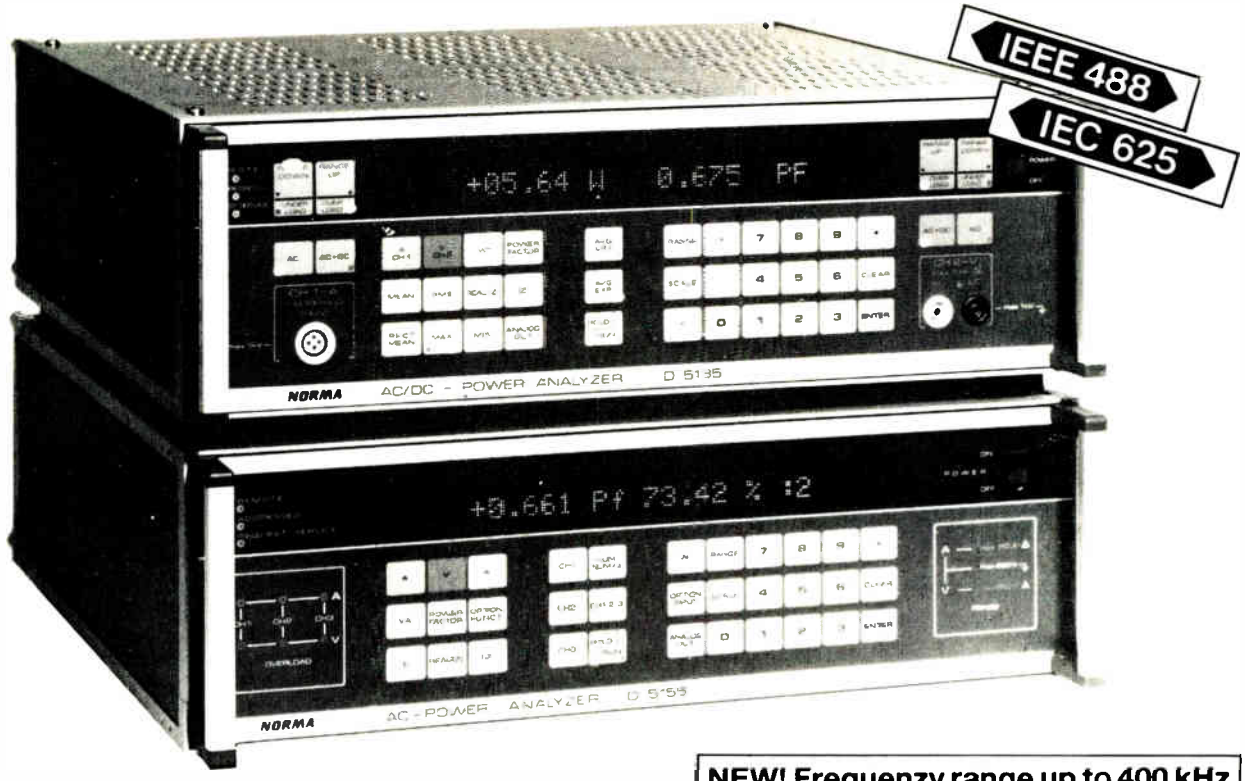
Optical-disk systems are having their biggest impact in document storage and retrieval, especially with the 'jukebox' type of disk handlers

Systems like those FileNet sells serve other types of mass-storage applications that require rapid access to large amounts of data: files of fingerprints in law-enforcement agencies, for example. De La Rue Printrak Inc. of Anaheim, Calif., for example, sells an optical-disk-based fingerprint storage system.

Jukebox systems are particularly suited to huge data bases such as fingerprint systems and document systems for big companies. In addition to FileNet, Cygnet Systems Inc. of Sunnyvale, Calif., makes optical-disk jukebox systems. "De La Rue Printrak uses our Series 1800 expandable jukebox," says Eva Marsh, product marketing manager at Cygnet Systems. Cygnet also sells its jukebox system to Kodak Corp., Rochester, N. Y., which integrates it into the existing Kodak Information Management System. KIMS can combine existing microfilm data bases with optical-disk data bases. Kodak's newest KIMS, introduced in March, uses 14-in. disks. □



3. SERVER. Tallgrass Technologies has developed a file server that uses a Winchester drive as a cache between the user and the optical-disk drive.



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WHAT'S NEW IN SINGLE-BOARD COMPUTERS?

A SPATE OF BETTER MODELS SPARK AN EXPLODING MARKET

Instead of building their own machines, customers are buying board computers; vendors offer faster, lower-priced models that are uncoupled from their buses

by Alexander Wolfe

A decade ago, engineers who needed a special-purpose, microprocessor-based computer got it the old-fashioned way. They built it. Today, they reach for a single-board-computer catalog. By packing more and more computing power into their products, single-board-computer companies have built a multimillion-dollar market serving engineers who'd rather write applications software than put together the right machinery to run it.

The significant products in that market are Intel's Multibus I and Motorola's VMEbus, with STD bus, the IBM Corp. PCbus, and the proprietary Digital Equipment Corp. Q-bus also holding large shares. A sixth contender, Multibus II, is coming on strong, fueled by products from companies such as Intel Corp. and Heurikon Corp.

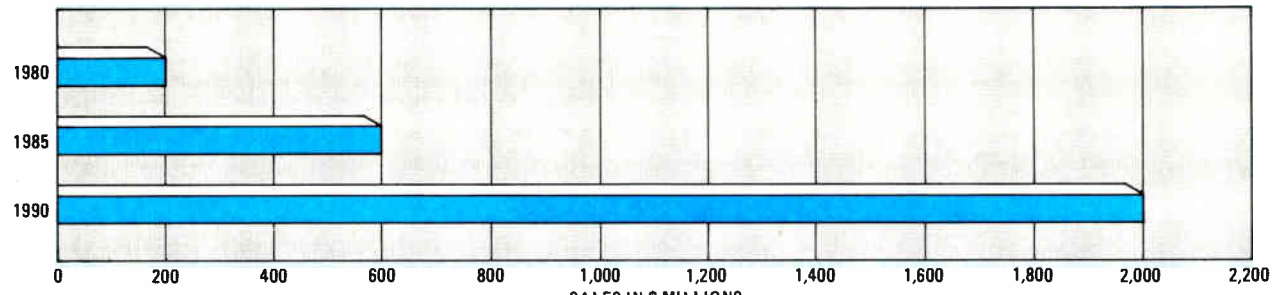
Those products are competing for a market that will climb from about $600 million in 1986 to $2 billion in 1990 (see bar chart, opposite), according to Zebu Research Corp. VMEbus sales will tally $460 million in sales by 1990; Multibus II, $400 million, and Multibus I, $540 million, says the Sunnyvale, Calif., market tracker. The remaining $600 million will be shared by STD bus, PCbus and the various proprietary buses, including Q-bus (see pie chart, opposite).

The growth in the market will be fueled not only by the introduction of faster board computers, but also by the increasing trend toward uncoupling microprocessors from the buses for which they originally were built. The trend is already picking up steam: last year, Force Computers Inc. mated Intel's 80386 with VMEbus, supported by Motorola Inc. Similarly, Heurikon, of Madison, Wis., and Microbar Systems Inc., Sunnyvale, Calif., have announced Multibus II boards featuring Motorola's 32-bit 68020 microprocessor. The Heurikon product is also pushing foward in speed, running at a 25-MHz clock rate, one of the first to pass the 20-MHz mark.

As they get faster, board computers' price/performance ratio will favor consumers, assuming the historical trend of falling unit prices continues. According to market researchers Dataquest Inc., San Jose, Calif., the average selling price has dropped from $1,480 in 1982 to an average

BUILDING STEAM. Single-board computers have become the engineer's choice for turbocharging a variety of systems and will be a $2 billion market by 1990.

RAPID GROWTH PROJECTED WORLDWIDE FOR SINGLE-BOARD COMPUTERS



SOURCE: ZEBU RESEARCH CORP.

of about $1,000 today. The most powerful products command prices in the $4,000 to $6,000 range. Alternatives with lower prices will be available from mature product lines such as Multibus I, particularly when those products are based on 16-bit processors.

And now emerging are new categories of single-board computers. These products offer capabilities beyond simple computing power, based on compatibility with personal computer software. They are paving the way for a class of application-specific single-board computers, dedicated to particular functions.

At the moment, high-performance, 32-bit Multibus II and VMEbus products are grabbing much of the limelight. The interest in them is spurred by users' desires to take advantage of the power of Intel's 80386 and Motorola's 68020.

Multibus II multiplexes addresses and data on its master parallel system bus and uses a synchronous communications protocol. VMEbus, with both 16- and 32-bit data paths, is nonmultiplexed and uses asynchronous protocols. Multibus II is generally considered best for multiprocessor applications; VMEbus for process control.

Intel has combined the 80386 and Multibus II in the iSBC 386/100, a building block for multiprocessing systems. The iSBC 386/100 serves as master to other board computers connected to the parallel system bus.

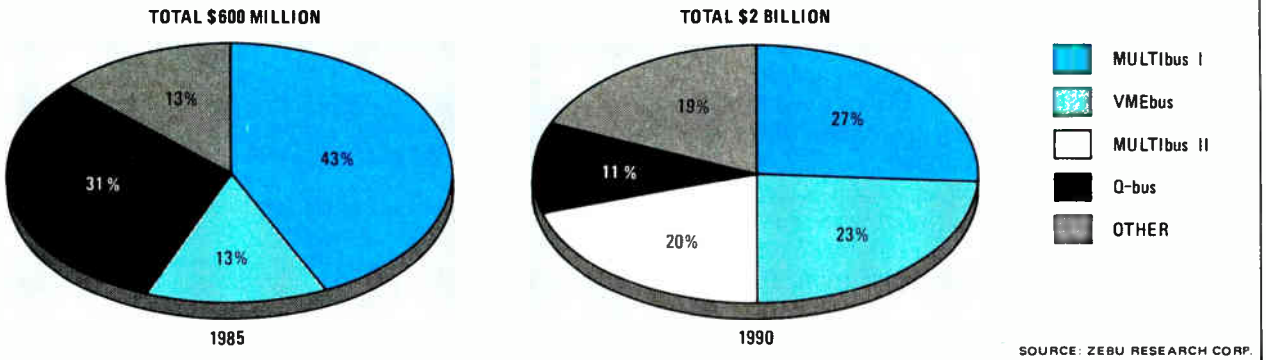
Standing alone, the iSBC 386/100 offers impressive performance, with a 64-K-byte memory cache helping achieve zero-wait-state operation at 16 MHz for memory input/output cycles. Dual-port dynamic random-access memory in expansion boards is available up to 4 megabytes. Programs are stored in the 128-K bytes of electrically programmable read-only memory.

The first 80386-VMEbus combination comes from Force Computers, Los Gatos, Calif. (see fig. 1). The SYS80K/CPU-386 is Force's first venture not based on Motorola's 68000 family. The CPU-386's 2 megabytes of high-speed DRAM make possible zero-wait-state operation for memory I/O. Address pipelining is used for both local memory and VMEbus access for improved performance. Four EPROM sockets for 512-K bytes are available for user-supplied firmware. To aid firmware development, Forcebug/386, a debugging package with an assembler/disassembler, benchmark routines, macro facilities, and floating-point coprocessor support is included.

Heurikon stayed with Motorola processors in its Multibus II product. Its 68020-equipped HK68/M220 has four 32-bit direct-memory-access channels, allowing transfer rates of 16 megabytes/s in 16.5-MHz systems. Up to 4 megabytes of RAM, 256-K bytes of EPROM, and 128-K bytes of nonvolatile RAM are available.

Microbar Systems also went with a 68020-Multibus II combination. Its MT68020 can be equipped with either a 12.5- or 16.67-MHz 68020. It has 1 megabyte of high-speed dual-ported DRAM. Memory expansion modules can increase

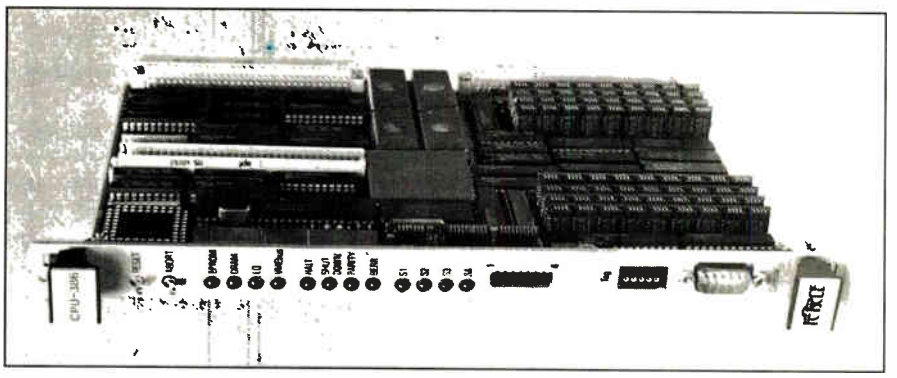
WHAT MAKES UP THE WORLD MARKET FOR SINGLE-BOARD COMPUTERS



SOURCE: ZEBU RESEARCH CORP.

that amount to 16 megabytes.

The Motorola chip's popularity extends to both Multibus II and VMEbus—more than 20 companies use the 68020 for 32-bit VMEbus products. Fastest is the 25-MHz VMPU-4M from Dual Systems Corp., Berkeley, Calif., executing some 7 million instructions/s. A 68851 memory-management unit and 68881 floating-point coprocessor supplement that power. Zero-wait-state operation is obtained through a software-selectable logical data-instruction cache. Four megabytes of memory can be accessed within 115 ns; the cycle time is 200 ns. A board-to-board mailbox interrupt lets multiple boards interrupt one another and transfer data and control.



1. FULL FORCE. The SYS80K/CPU-386 from Force Computers has 2 megabytes of high-speed DRAM, allowing zero-wait-state operation in a VMEbus format.

Dual's speed title will be challenged by General Micro Systems Inc. in the third quarter of 1987 with a 30-MHz version of its GMSV07. Based on the 68020 and VMEbus, it now operates at 16-, 20-, or 25-MHz clock speeds. It has 1 megabyte of zero-wait-state static RAM selectable for either dual-port or processor-only use, on-board expansion ports for another 4 megabytes of DRAM, and seven-level interrupt handling to support multiprocessing applications.

Also in the high-speed VME class is the latest offering from PEP Modular Computers Inc., Pittsburgh, Pa. Running at a choice of 16.7-MHz or 12.5-MHz clock speeds, the VMPM68KC consists of two circuit boards piggybacked to create one single-height microcomputer board set. One board contains the main central-processing-unit circuitry; the second houses memory chips. That split results in higher system performance, because the CPU and memory card communicate over a local bus, reducing the number of accesses that would be made to the VMEbus if an external memory card were used. In addition to the basic 68020 CPU, the boards also feature a 68881 floating-point coprocessor; 1 megabyte of zero-wait-state, dual-port static RAM; and four 32-pin sockets holding up to 512-K bytes of ROM.

Motorola's own offering in VMEbus boards is the 20-MHz MVME133A-20, an all-in-one microcomputer board combining the 68020, a 68881 floating-point coprocessor, and 1 megabyte of RAM. Two RS-232-C serial ports, one serial debug port, three 8-bit timers, a real-time clock, and four sockets for EPROM or ROM round out the list of hardware features. Software developers will be interested in the board's Versados real-time operating system, which incorporates drivers for Motorola's companion line of VMEbus peripheral controller boards.

As impressive as the 32-bit chips are, many users will want lower-cost products. For them, Intel's 16-bit 80286 and Motorola's 68010 microprocessors are widely used by designers. The VMEx 286 from Iskra Electronic Inc., Farmingdale, N.Y., is billed as the first high-performance VMEbus product based on the 80286. Running at 8 MHz, it features 512-K bytes of dual-port memory with no wait states, on-chip memory management, a real-time clock, two bootstrapped EPROM sockets for up to 64-K bytes of program storage, and two RS-232-C serial communications ports. An 80287 coprocessor provides added mathematical muscle.

The VMEx 286 comes complete with full operating system support. For single-user applications, Microsoft Corp.'s MS-DOS and iRMX are available. Xenix is supplied as the multiuser operating system. Software support in the form of development tools is also available.

QUICK TESTING

Mizar Inc., St. Paul, Minn., bases its offering on support for hardware designers. Its VME8115 contains a 16-bit 68010 microprocessor operating at 10 or 12.5 MHz, 512-K bytes of zero-wait-state, dual-port DRAM, 128-Kbytes of ROM, two RS-232-C serial ports, and a full system controller. During prototyping, engineers can add their own components on an expansion board for rapid testing of new designs. Tied together by a 96-pin DIN connector, the VME8115 and expansion board share a non-buffered interface for speedy transfer of data and control commands.

Though less glamorous than Multibus II and VMEbus, Multibus I is still going strong. A nonmultiplexed and asynchronous design built to handle 8 bits, it has since been upgraded to 16 bits. And recently several new products have brought 32-bit microprocessor power to the Multibus I world.

Among them are four new 80386 Multibus I introductions from Intel itself. The boards, designated the iSBC 386/21, /22, /24, and /28 offer 1, 2, 4, and 8 megabytes of memory, respectively. All run at 16-MHz clock speed. Each can expand its memory to 16 megabytes via add-on modules.

STD bus, another mature contender, also still holds considerable commercial sway. Since its introduction in 1978, the bus has kept pace with each generation in processor design, moving from the 8-bit Zilog Corp. Z80 to Intel's 8-/16-bit

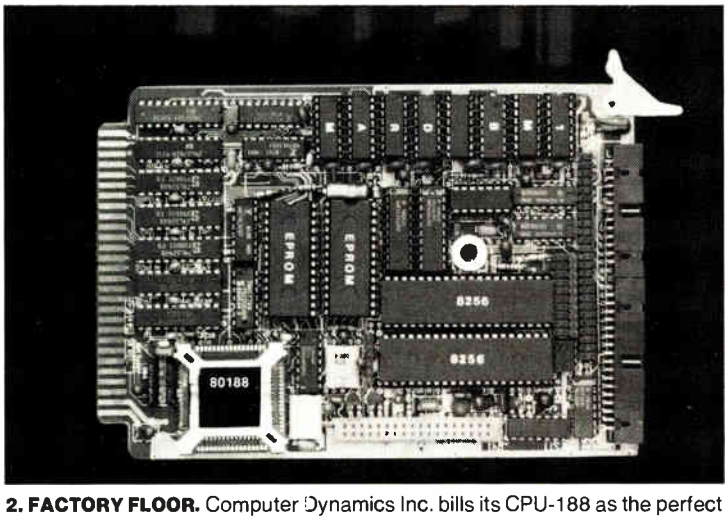
8088. Designed for factory floor applications, STD bus has long been considered rugged and reliable. Today, it has perhaps the broadest range of products of any available bus standard, with support from more than 150 vendors.

To make their products stand out, STD manufacturers are looking to easy applications development. One recent example of that trend is the 890 CPU card from Octagon Systems Corp., Westminster, Colo. The board comes complete with STD Basic, featuring floating-point commands for use in real-time control and data acquisition.

Board computers increasingly will move from general-purpose microcomputers toward those tailored to functions such as communications or network control

The 890 CPU hardware is based on the 4-MHz Zilog Z80A microprocessor. Also featured are two fully independent asynchronous serial I/O channels and a countertimer with four 8-bit channels. Memory consists of four sockets that can hold 64-K bytes of RAM and EPROM.

Another STD bus standout comes from Thomson Components-Mostek Corp. The Carrollton, Texas, semiconductor maker offers no less than six board computers. Built around Z80-compatible microprocessors, the boards are aimed at minicomputer designers. Leading that lineup is the MDX-CPU4. On-board are five 28-pin sockets that can accept a wide range of EPROM, SRAM, or ROM chips, a Centronics printer interface as well as a full-handshake RS-232-C I/O port. Also included are bidirectional power-on-reset, allowing operation with power-fail controllers and two programmable 8-bit timers. Mostek's MDX-CPU3, CPU2B, and CPU1A contain differing combinations of those features. Its MDX-MATH board, based on the AM9511A Arithmetic Processing Unit, brings high-powered number-crunching to the STD bus. At the low end, the MD-SBC1 is a complete Z80-based microcomputer on a tiny 4.5-by-6.5-in. module, though it is not bus-expandable.



2. FACTORY FLOOR. Computer Dynamics Inc. bills its CPU-188 as the perfect control link between the factory floor and the engineer's desk.

Computer Dynamics Inc., Greer, S. C., is bringing compatibility with software for the IBM Personal Computer to the STD bus with its CPU-188 (see fig. 2). The CPU-188, boasting a 16-bit 80188 microprocessor and 1 megabyte of on-board RAM, is billed as the perfect control link between the factory floor and the engineer's desk. In a typical application, a design engineer will develop software on the PC, download and test the program on the CPU-188, then burn the program into EPROM. The EPROMs are installed on a CPU-188, which then assumes the factory-control task.

PCs are the foundation for another bus competitor's success. PCbus has become a potent force by virtue of the IBM PC's success. Expansion cards—providing enhanced graphics, video, and disk storage capabilities—plug into the PC bus using edge connectors inside the machine. Since PCs already have a CPU as their central element, board computers for the PCbus must provide more than simple computing power.

One such PCbus product comes from Alloy Computer Products Inc., Framingham, Mass. Its PC-Slave/16 is an add-in board fitted with an 80286 microprocessor and 1 megabyte of RAM. The board enables users to create clusters, or a network-like group, of terminals that share data and peripherals with a host IBM PC. This clustering approach offers a low-cost alternative to establishing networks of fully configured PCs. Machines are added to the cluster by installing a PC/Slave-16 and connecting an asynchronous terminal to the board. Clusters of up to 31 users can operate from a single PC.

In designing microcomputers, PCbus manufacturers are also offering alternatives to the standard PC AT motherboard. Faraday Electronics, Sunnyvale, Calif., has introduced one such option, the FE3010. Intended as a CPU, the board contains only 40% fewer components than a typical AT motherboard. As a result, it is 80% smaller and 70% less power-hungry than those boards. Using proprietary ICs, the FE3010 has equivalent power to an 80286-equipped board and supports 6-MHz, 8-MHz, and 10-MHz clock speeds. It can accommodate both 256-K and 1-Mb DRAM and includes 15 interrupt channels, three timer channels, and seven direct-memory-access channels.

Both the PC/Slave-16 and the FE3010 are examples of a trend which will solidify over the next few years: the development of the application-specific board. A result of the ability of semiconductor manufacturers to integrate more and more functions onto silicon, future product introductions will move away from general-purpose microcomputers and toward those tailored to functions, notably—as in the case of the PC/Slave-16—communications or network control. □

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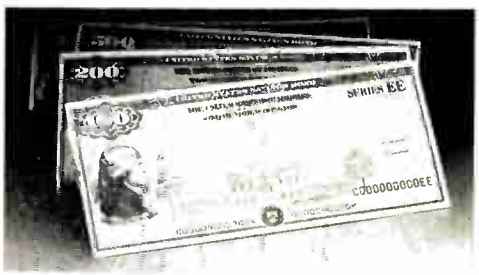

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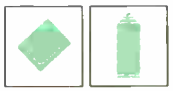

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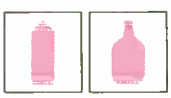

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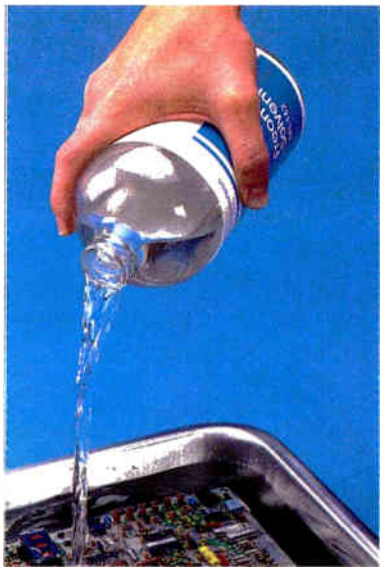

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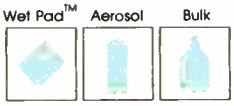

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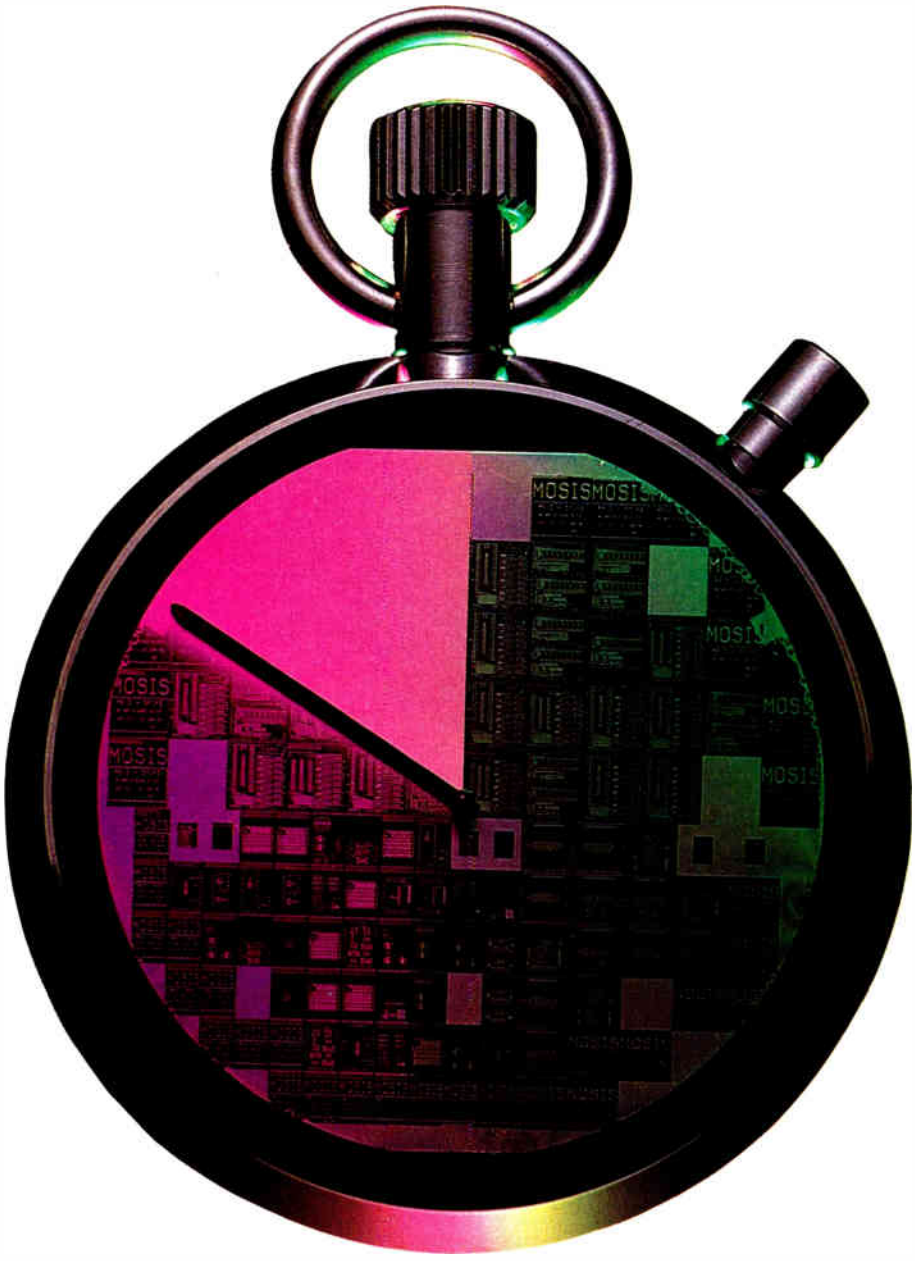

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TI PUTS ITS LISP CHIP INTO A SYSTEM FOR MILITARY AI

Packing complex artificial-intelligence applications into the tight spaces within military equipment is now possible thanks to a new chip and a new system from Texas Instruments Inc. Billed as the first microprocessor designed for executing software written in the AI language Lisp, TI's 32-bit Lisp processor chip is the heart of the Artificial Intelligence Embedded System, or Aries—a set of system modules now under development at TI that form a shoebox-sized computer with the power to handle real-time symbolic processing.

The Lisp chip is a slimmed-down and souped-up version of the central processing unit in TI's Explorer work station, a popular AI system. It is fitted into a 6.58-by-5.88-in. military-style module that forms the Aries processor (see fig. 1), one of its five function modules. The others, also 6.58-by-5.88 in., are the memory, memory mapper and cache, MIL-STD-1553B bus interface, and maintenance and diagnostic modules. A power supply and system-interconnect card complete the system.

The modular design enables Aries systems to be customized for a wide variety of processing needs. For example, they can be fitted with multiple processor modules, as well as circuit boards containing conventional microprocessors. In addition, multiple Aries can be tied together in a network to handle applications requiring distributed computing. The modules themselves are built to withstand the rugged environmental requirements of military specifications. They make extensive use of mil-spec chips as well as conventional surface-mounted integrated circuits and components.

The Lisp processor chip (see fig. 2) integrates more than 60% of the circuitry of the two-board CPU of the Explorer, but TI managers say it is five times more powerful than the Explorer's CPU. TI used a 1.2-μm double-level-metal CMOS process to cram 553,687 transistors onto a 1-cm^2 piece of silicon. Packed in a custom, 264-pin grid array, the Lisp chip is the densest microprocessor ever produced, according to TI.

The first prototype chip will operate with a clock cycle of 40 ns; that will improve to 30 ns in the next version. Controlling that operation is a microcoded architecture compatible with the Explorer system. Microcode resides in an off-chip 32-K-by-64-bit writable control store.

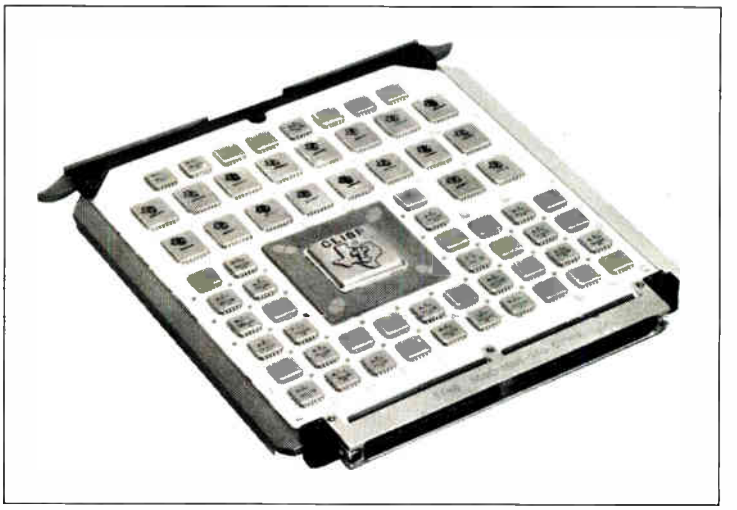
In the Aries system, the processor module incorporates a four-stage pipeline to allow the execution of one microinstruction per clock cycle. Two pipeline stages perform microinstruction fetches, allowing sufficient time for off-chip accesses. The third pipeline stage reads the internal memories, while the fourth performs the actual computations. Since the single-ported memories, designated A and M, and the PDL, or push-down list, memory can be read every cycle, the results of the calculations cannot be directly written back into these memories. Instead, they are written into 4-word associative buffers until a free write-cycle is available.

The chip also includes a macroinstruction prefetch queue. This queue further speeds operation by allowing frequently used routines, which consist of several microinstructions, to be called and executed at one macroinstruction per clock cycle.

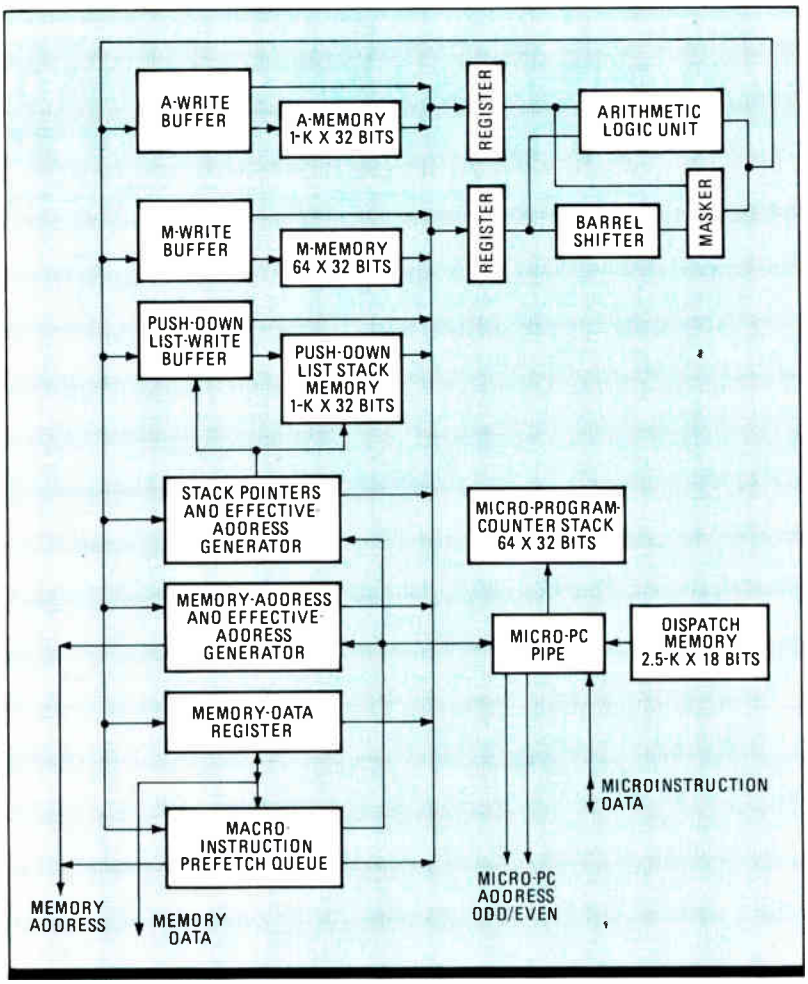
Because Lisp programs are memory-intensive, memory occupies a relatively large portion—233 μm^2—of the CPU chip. On chip, there are six random-access memories providing a total of 114 K of cache and intermediate storage, as well as 16 K of read-only memory used for microcode and initialization software. The RAMs are supported with individual refresh counters as well as a master refresh-period timer.

The remainder of the chip is occupied by control logic and the data path. The control-logic section is implemented by a regular array of domino and static gates. A novel design for the arithmetic logic unit was used in the data path, resulting in faster ALU throughput. The ALU and a 32-bit barrel shifter/masker make up the execution unit. The 1-K-by-32-bit A memory provides one source for this execution unit, while several registers, the 64-word-by-32-bit M memory, and the 1-K-word push-down-list stack memory drive the other input.

Main memory for the Aries system is provided by the memory module. A single Aries memory module contains eight megabytes of storage. Up to eight of these modules can be attached to a



1. COMPACT LISP. The processor module is one of the five basic 6.58-by-5.88-in. military-style modules in Aries.



2. LISP CHIP. TI's 1.2-μm double-level-metal-CMOS Lisp processor chip crams 553,687 transistors onto a 1-cm² piece of silicon.

system, providing a total of 64 megabytes of memory space. Provision for Aries operation in tough military environments comes in the form of error-correcting features built into the modules.

Help for memory operation comes from the memory mapper and cache module. One half of this module contains a high-speed data cache that provides intermediate storage for memory data requested by the processor, reducing traffic on the Aries bus and thereby increasing processor throughput. The other half is devoted to the memory mapper. Using an address map, the mapper translates virtual addresses generated by the processor into physical addresses used to access memory.

The MIL-STD-1553B bus interface module allows Aries to interface to external devices that communicate over a data bus using the MIL-STD-1553B bus standard. Because of its wide use in military electronics, MIL-STD-1553B is necessary if Aries is to connect with other machines typically present on an aircraft, ship, or tank. In addition to managing normal data transfers, this module can handle "exception" conditions such as asynchronous events or errors without intervention by the Aries processor. Internal communication among the Aries modules is done over the 32-bit NuBus, a standardized bus structure developed at the Massachusetts Institute of Technology and also used in the Explorer work station.

The maintenance and diagnostic module implements a key requirement of the military environment—the ability to isolate system faults so that failed boards can be located and replaced rapidly. In operation, the maintenance and diagnostic module connects to an external host computer, which can be either an Aries or an Explorer, that controls the test sequences. The maintenance and diagnostic module also allows Aries applications programs to be debugged from the host computer.

To control the execution of AI applications, Aries is equipped with a complete software environment geared to military computing. At the heart of that software is the Aries run-time support environment. Providing real-time control flexibility, the run-time support allows the Aries to respond to software interrupts within 100 μs. Rapid response to interrupts is critical in real-time systems, where literally thousands of interrupts can occur during every second of CPU operation.

Also included in the run-time support is extensive support for garbage collection, on which Lisp-based systems rely heavily, as a means of freeing the vast amount of memory they need to store information used to track and manage the operation of an applications program. Without speedy garbage collection, that memory would soon fill up, and the applications program would grind to a halt. Besides handling garbage collection in a timely fashion, the Aries software is designed to run without causing any interruption to the operation of the Aries applications program, a particularly difficult feat given the real-time requirements of the system.

Applications software intended for execution on Aries will first be developed on the Explorer system and then down-loaded into Aries through the maintenance and diagnostic module. The system's capabilities are intended to benefit applications developers who need to "put militarized AI into a real-time system," according to Marvin Applewhite, TI's manager of military computing systems at the company's Data Systems and Engineering Group. As such, it will run expert systems for diagnostics and maintenance of aircraft as well as electronic warfare applications.

A demonstration Aries is scheduled for late this year, with the first production prototypes slated for early 1989. A complete system, weighing in at between 26 and 30 lbs., will cost roughly $100,000, though prices are expected to decline after production gears up. *–Alexander Wolfe*

BOOSTING MIL-SPEC CHIP PERFORMANCE WITH RISC

An ongoing challenge to companies that build equipment conforming to MIL-STD-1750A, the instruction-set standard governing embedded computers for military systems, is how to boost performance without losing 1750A compatibility. To meet that challenge, the United Technologies Microelectronics Center in Colorado Springs has come up with a high-performance 1750A microprocessor based on a reduced-instruction-set-computer architecture.

The UT1750AR (see fig. 1) is the first high-performance, 32-bit RISC processor that supports the complete MIL-STD-1750A Instruction Set Architecture. It is the first member of a planned family of 1750A and B processors and support peripherals from United Technologies, with all the processors designed to take advantage of the RISC approach to design. Using RISC, which provides a simple, efficient, and easily built architecture, is fast becoming an effective and increasingly popular way to emulate older architectures and at the same time increase their performance and lower their cost.

The processor, constructed from 1.5-μm CMOS gate arrays, operates in two modes—as a 1750A emulator and in its native RISC mode. Executing a benchmark using a mix of the standard, digital, avionics-instruction-set operations, the 12-MHz UT1750AR delivers a throughput of 0.75 million instructions/s. In its RISC mode, it runs 6 mips. The performance of the native RISC machine is available to the 1750A systems designer through the MIL-STD-1750A built-in-function opcode.

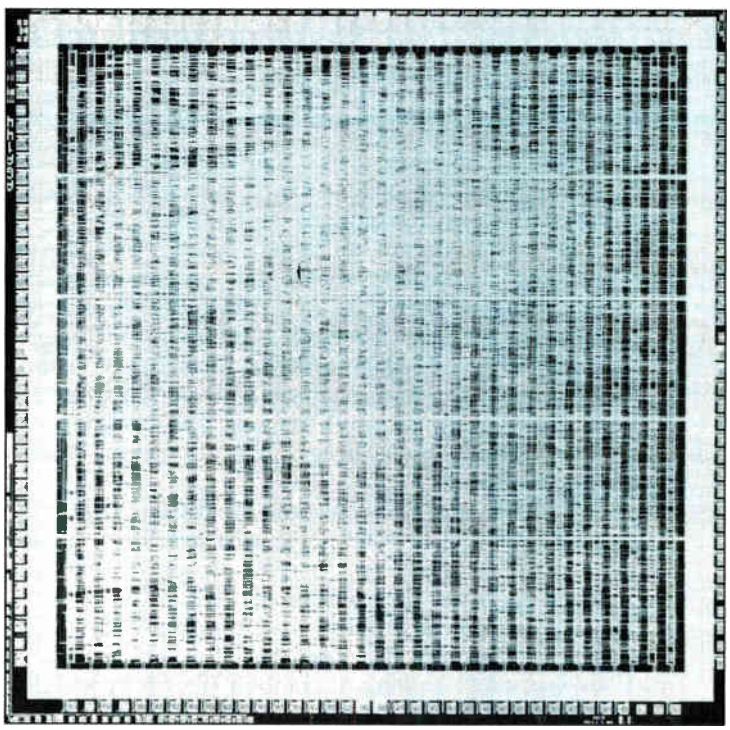
The processor supports normal bus-cycle operation, direct memory access and arbitration operation, and extensive exception handling. The exception handling is accomplished through 16 levels of vectored interrupts. In the 1750A mode, the machine supports the standard instruction-set and data formats. In its native RISC mode, it has three basic instruction formats for both 16- and 32-bit instructions—register-to-register, register-to-short-immediate, and register-to-immediate instructions.

Operating in the MIL-STD-1750A mode, the UT1750AR requires 8-K bytes (4-K by 16 bits) of read-only memory to map the 1750A instruction set into the native RISC machine language instructions. Each MIL-STD-1750A opcode has a RISC-code macro in the external ROM. When this macro is executed by the microprocessor, it performs the function of the standard 1750A instruction that is being emulated. In a general system architecture, the emulation ROM is isolated from the system's instruction and data memory, and it can be accessed only by the microprocessor (see fig. 2).

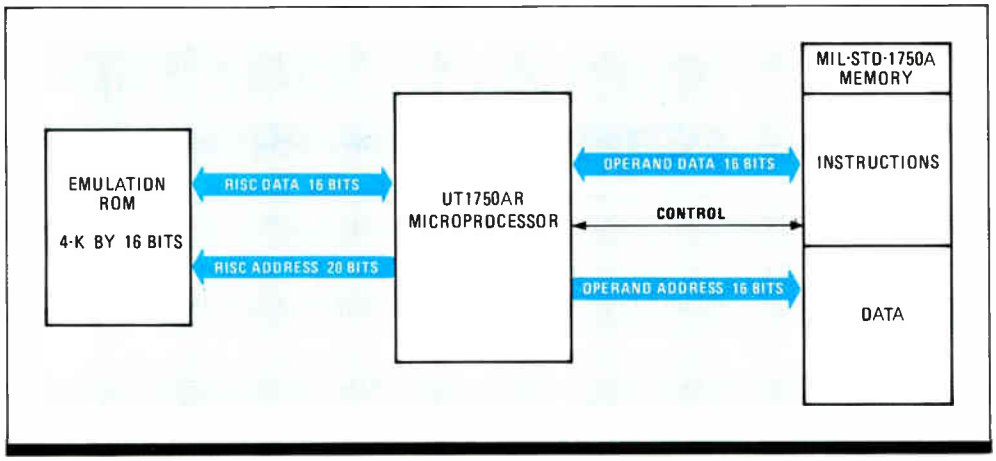
The native RISC mode of the UT1750AR executes most RISC instructions in two clock cycles. Its peak speed of 6 mips is an effective execution rate for real-time applications. This native RISC mode performance is usable in two ways. In the 1750A emulation mode, 1750A source-code programs can call the built-in-function opcode to access RISC code for fast real-time processing when required. In addition, the processor can be programmed and operated purely as a RISC machine.

The UT1750AR's register-based architecture provides extensive register support, with 16 general-purpose 16-bit registers, four 16-bit accumulators that can also be used as general-purpose registers, and 16 special registers. The large register set available to the instructions reduces the memory references required. Programmers will typically use these registers for such activities as temporary storage in arithmetic and logical functions, program-flow control, fault detection, monitoring processor status, controlling the built-in universal asynchronous transceiver, and controlling exception handling.

Register flexibility is provided by allowing the concatenation of the 16 general-purpose registers and the four 16-bit accumulators into eight 32-bit registers and two 32-bit accumulators. All of the registers can be used either as the source



1. MILITARY RISC. The UT1750AR from United Technologies uses a RISC architecture in a CMOS microprocessor to boost performance.



2. MAPPING. To run MIL-STD-1750A computer codes, the UT1750AR requires a 4-K-byte-by-16-bit ROM to map the 1750A instructions into the RISC machine language instructions.

or the destination for any register operation.

The 16 specialized registers on the chip include a stack pointer, instruction counter, instruction-counter-save register, instruction register, status-word register, fault register, interrupt-mask register, pending-interrupt register, configuration register, UART transmit and receive registers, and five 1750A special registers for the MIL-STD-1750A mode of operation.

The 1750A registers are a 16-bit register to hold the prefetched 1750A instruction, a program register for holding the current instruction, a program counter for the address of the current instruction, and two 1750A timer registers. The timer registers, TA and TB, are 16-bit interval timers as defined in the military standard.

The UT1750AR provides extensive register support: 16 general-purpose 16-bit registers, four 16-bit accumulators, and 16 specialized registers.

However useful a large register set is for keeping operations within the processor, many operations still require external access or control through memory references, input/output operations, or handling interrupts. The UT1750AR microprocessor handles these external operations in three ways: through normal bus cycle operation, direct-memory-access operation, and exception handling.

During normal bus-cycle operation, the bus performs one of four possible operations: memory read or write or I/O read or write. The bus cycle requires three clock periods.

Direct-memory-access operations are used for bus arbitration functions when more than one device needs control of the bus. This is especially important when multiple processors are in the system. There are four control signals for managing the bus and preventing contention. These signals are the bus-request input, the bus-grant-acknowledge output, bus request, and bus-grant signals.

When, during a bus cycle, the processor first requests access to the data bus, the bus-grant signal is sampled on every rising edge of the clock until it is asserted, indicating that the bus is free. The processor becomes the new bus master and locks out all other contenders by asserting the bus-grant-acknowledge-output signal—the bus-busy signal. While the processor controls the bus, a series of normal bus cycles can occur. It retains control until another device (or processor) asserts the bus-request-input signal and takes over as the new bus master.

When priority operations have to take place, the processor's interrupt- or exception-handling system comes into play. Of the 16 prioritized interrupts, 10 interrupts are external, with eight of these interrupts open to definition by the user. The six internal interrupts are used by the processor. The UT1750AR interrupts are controlled by software.

An interrupt can be enabled at any time during processor operation. As long as it is masked, its corresponding bit in the interrupt-mask register is set, and it is ignored. The highest priority interrupts—the power-down sequence and executive-call interrupt—cannot be masked nor disabled.

The UT1750AR has three basic instruction formats that support both 16-bit and 32-bit instructions—register-to-register operations; register-to-short-immediate instructions, in which a 5-bit immediate field is the source; and a register-to-immediate format with a 16-bit immediate-value data field. The first two types are 16-bit instructions, and the third type of format is 32-bit instructions.

The United Technologies engineers have shown just how much functionality can be stuffed onto a board when parts like the UT1750AR microprocessor are available. They have built a MIL-STD-1750A-emulation board product that consists of a UT1750AR chip, emulation ROM, a memory-management unit, and a MIL-STD-1553B bus controller and remote-terminal interface on one VMEbus-size card.

The design is an example of the types of products that a chip like the UT1750AR can make possible. It illustrates that the 1750A RISC microprocessor chip is a likely candidate to become the CPU of choice for board-level MIL-STD-1750A embedded computers. *–Tom Manuel*

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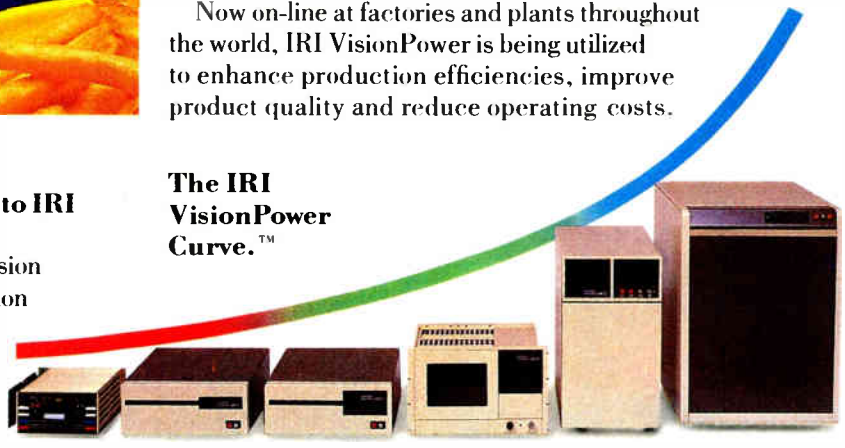

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MILITARY/AEROSPACE NEWSLETTER

ARMY SIMULATORS USE COMMERCIAL-GRADE COMPONENTS

Four tank-battle simulators that have rolled off the assembly line at Perceptronics Inc. are not only a trailblazing way to train Army personnel, but also are among the first U. S. military projects to use commercial-grade components throughout. The Woodland Hills, Calif., company built the simulators under a $67 million contract awarded last year by the Defense Advanced Research Projects Agency, which is encouraging contractors to employ off-the-shelf integrated circuits for non-battlefield applications, instead of more expensive devices that have to meet stringent military specifications. Doing so cuts both hardware costs and development time, according to Perceptronics managers, who say the simulators' price—$250,000 each—would have been far higher otherwise. The four Perceptronics simulators are the first production units for a large-scale Simulation Network, or Simnet, a prototype system that the Army will use to train tank commanders and crews. The simulators pit crews against each other in a video-game format, complete with computer-generated graphics and sound effects, enabling the crews to learn realistic battlefield tactics faster and cheaper than they could in actual maneuvers [*ElectronicsWeek*, March 11, 1985, p. 32]. □

A DRIVE BEGINS TO CREATE A CAD/CAM MILITARY MARKET

Some 50 companies and standards-setting agencies involved in computer-aided design and engineering are working with the Pentagon to produce a report on how the military can shift from its reliance on paper designs and documentation to CAD/CAM and related electronic systems. The group's interest is being spurred by the Defense Department's Computer-Aided Logistics Support program. CALS requires that all U. S. military services use digital data to support logistics by 1990, a requirement that is expected to spark a major military market in hardware and software for storing and processing technical data. The Yankee Group, a Boston market research and consulting group, estimates that the five Naval Systems Commands alone will spend almost $2 billion on CALS for hardware, software, training, documentation, and maintenance. Stand-alone work stations for 10% of the Navy's engineering personnel could ring up $100 million, says the Yankee Group. Another reason the companies and agencies are eager to get involved in the Pentagon's planning is self-defense. The military, and particularly the Navy, which does far more of its own design and engineering than the other services, will almost certainly use its buying power to enforce a set of standards. The group contributing to the report wants to have a say in what standards are adopted. The report is scheduled to be published by the National Computer Graphics Association by the end of April. □

NASA TRIES TO CLEAN UP BACKLOGGED SATELLITE LAUNCHINGS

The National Aeronautics and Space Administration is negotiating with the Air Force to acquire two Titan 3 missiles, even before NASA releases the results of its own study on using unmanned—or "expendable"— launch vehicles [*Electronics*, Jan. 22, 1987, p. 96]. NASA will use the missiles to launch backlogged scientific experiments. NASA is also talking to the Air Force about the acquisition of one and possibly two Titan 4s, which are newer than the Titan 3s. The space agency, however, must ask Congress for supplemental funding for the Titans or redirect some of its spending, because expendable launch vehicles are not in its fiscal 1988 budget proposal. Meanwhile, NASA will carry two "extremely high priority" Pentagon programs on its next shuttle flight, scheduled for next year, says Dudley McConnell, NASA's assistant associate administrator for space science and applications. The space agency would like to launch six shuttles a year, he adds. □

MILITARY/AEROSPACE NEWSLETTER

GETTING A HANDLE ON HOW MUCH AND WHEN TO RETRIEVE SPACECRAFT DATA

The National Aeronautics and Space Administration is banking on a new program, the Civil Space Technology Initiative, to give NASA telecommunications specialists a better handle on two of the oldest problems in its space-flight program. The program is aimed at determining what kind of data should be downloaded for real-time analysis, and what data can remain aboard a spacecraft for later study. NASA will also look at how to download or store the data—it is researching high-rate and high-capacity data acquisition and processing techniques and developing and evaluating onboard processing and storage systems. Among other things, NASA scientists are examining optical-storage techniques for the large amount of data downloaded from orbiting spacecrafts. As now funded, CSTI will help boost the agency's budget for space research and technology programs from $171 million to $250 million. □

WANT TO OPEN AN AI OFFICE IN DAYTON, OHIO? TALK TO THE AIR FORCE

Any artificial-intelligence vendor willing to take a five-year flyer with the newly established Air Force Aeronautical Systems Division's AI office could wind up with a neat commercial AI business as well. ASD is looking for a company willing to provide quick-response AI studies; to put together training and education for students, engineers, and program managers; and to develop programs for rapid transfer of AI technology to Air Force systems. However, the vendor must establish a full-time AI center in the Dayton, Ohio, area—near the Wright-Patterson Air Force Base, home of the ASD. The winning vendor could pick up additional AI business from military, commercial, and university operations in the Dayton area, says Robert Barthelemy, technical director of ASD's Air Force Wright Aeronautical Laboratories. The ASD's annual AI budget is $25 million, but Barthelemy says, "we're increasing our level of effort and likely will double our budget for this type of research within the next few years." The ASD's new office already is working on AI applications for F-16 mission planning. Contract proceedings will start soon, and the contract will probably take effect in September. □

IEEE CLAIMS SPACE STATION MAY COST TWICE NASA'S ESTIMATE

A space station that the National Aeronautics and Space Administration wants to build could end up costing twice as much as NASA has estimated, according to an IEEE analysis of proposed federal research and development funding for fiscal 1988. NASA's estimate is that the station can be built for $8 billion. If the budget balloons as the analysis predicts, the IEEE says, the project could become a target for Congressional budget-cutters. The space station already is set to get the biggest chunk of NASA's total 1988 R&D budget, growing by almost 83% to $767 million. □

INFUSION OF FOREIGN STUDENTS WORRIES PENTAGON

The already high level of foreign student enrollment in graduate programs at electrical engineering and physics schools in U. S. universities is continuing to grow. A Pentagon official says that this has become an "issue of increasing concern to the Department of Defense," which directly and indirectly employs some 14% of all scientists and engineers in the country. Because a large number of these foreign students return to their native countries after graduating, the DOD expects a shortage of engineers in many critical areas, says Ted Berlincourt, director of research and laboratory management. To help alleviate the shortage, some 75% to 85% of all undergraduate Reserve Officer Training Corps scholarships are now earmarked for science and engineering majors. □

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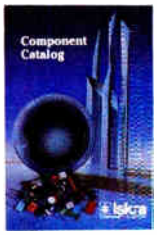

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NEW PRODUCTS

PERIPHERAL CONTROLLERS BURST DATA AT MULTIBUS II MAXIMUM

NEW CHIP KEY TO 32-MEGABYTE/SEC BUS RATE

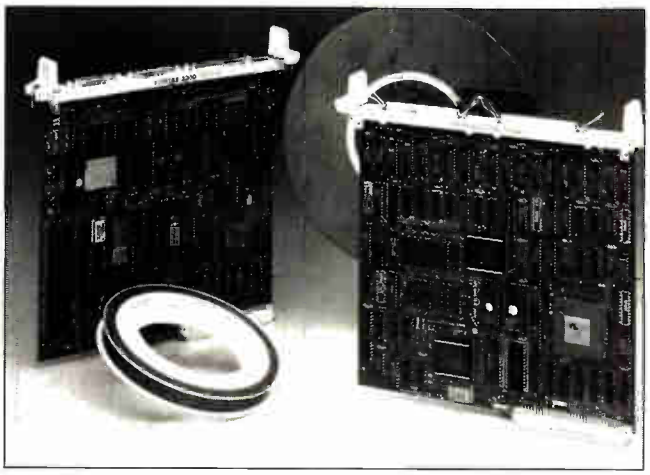
Two controllers can boost the performance in systems by bursting 32-byte data packets at the maximum Multibus II rate of 32 megabytes/s—double the burst rates of many high-performance 32-bit VMEbus controllers. Ciprico Inc.'s Rimfire 2200 disk-drive controller and the Tapemaster 2000 tape controller do this by using a recently introduced Multibus II message-passing coprocessor chip. The two products are believed to be the first Multibus II-compatible disk- and tape-drive controller boards not designed by Intel Corp., the main backer of the Multibus II 32-bit bus standard.

The development of the two boards was made possible by the arrival of single-chip silicon that can handle communication functions for Multibus II. Both controllers rely on the chip, called the Message Passing Coprocessor, which was codesigned by Intel Corp. and VLSI Technology Inc. [*Electronics*, April 21, 1986, p. 17]. The MPC was first introduced last spring, but it is only now becoming available. Ciprico has begun receiving the devices from VLSI Technology Inc. in sufficient quantities to support a product ramp-up, says William D. Moren, Ciprico engineering marketing manager.

DATA BURSTS. By bursting data across the bus at maximum Multibus II speed, the MPC chip consumes only minimal bandwidth. That contributes to overall system performance by freeing the bus for other critical operations.

Both controllers feature 512-K cache memory under control of an Intel 80186 processor for intelligent data management that increases disk or tape system throughput. Transfer rates can be sustained at 4 megabytes/s for the Rimfire 2200 disk-drive controller and at 6 megabytes/s with the Tapemaster 2000, says Moren.

The Tapemaster 2000 will handle up to eight formatted start/stop or streaming ½-in. tape drives, as well as group-coded-recording, phase-encoded, or non-return-to-zero-inverted ½-in. drives; all conform to the Pertec standard interface. The Rimfire 2200 will support up to four SMD-E (for storage module drive with ECL drivers and receivers) compatible disk drives, as well as SMD, high-speed SMD, and extended-SMD variations.



FAST ACCESS. Ciprico's controllers' command-queueing interface lets them take operating-system driver requests without handshaking.

To exploit the fact that programs tend to request sequentially stored data, the Rimfire 2200 prereads more data than needs to be supplied to meet a specific request. Subsequent program requests for the sequential data can then be accommodated from cache, avoiding longer disk-access times.

Data stored in the cache is sent over a 4-megabytes/s direct-memory-access channel to the coprocessor, which formats it into 32-byte packets and bursts it onto the Multibus II. The cache-to-MPC direct memory access channel in the Tapemaster 2000 can hit speeds of 6 megabytes/s.

Both Ciprico products also feature a command-queueing software interface that lets them receive requests from the operating system driver asynchronously, without handshake timing restrictions. With access to all pending disk requests, the Rimfire 2200 employs techniques such as command sorting and combining, and overlapped execution of commands, to optimize disk-head motion and minimize the number of times an actual access of a disk is performed. This improves performance by minimizing disk latency time and seek and rotational delays, Moren says.

The Tapemaster 2000 is available now from the Plymouth, Minn., company, and is priced at $2,495. The Rimfire 2200, which will sell for $3,395, will be available late this month in evaluation unit quantities. *–Wesley R. Iversen*

Ciprico Inc., 2955 Xenium Lane, Plymouth, Minn. 55441.
Phone (612) 559-2034 [Circle 341]

VMEBUS CONTROLLER HIKES MEMORY ACCESS BY 100%

Xylogic Inc.'s disk controller for VMEbus-based computer systems bundles multiple sectors into large bus packets, a technique that vastly improves system throughput. The controller achieves an 18-megabyte/s direct-memory-access rate—double that of the current Xylogics controllers—by employing a new direct-memory-access technique and a read-ahead concept that anticipates future data requirements.

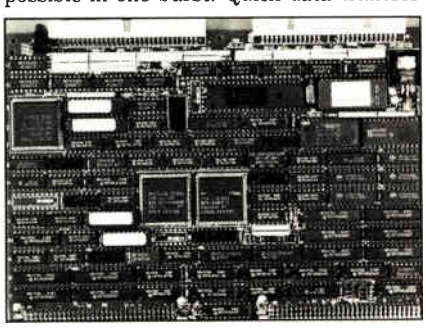
The new Dynathrottle direct-memory-access design increases throughput up to 60% by using an 8-K-byte first-in, first-out buffer and a scheme for condensing multiple disk sectors into large packets that hold up to 6,144 bytes of data.

In addition, the read-ahead technique, which also makes use of the large FIFO buffer, brings the total increase in throughput up by as much as 100%, according to the Burlington, Mass. compa-

ny. Besides its blazing direct-memory-access rate, the new Xylogics 752 VME HSMD (for high-speed storage-module drive) controller can handle up to two drives, each at a maximum data-transfer rate of 2.4 megabytes/s.

The 752's maximum packet size of 6,144 bytes is considerably larger than other controllers, which typically use either 32- or 512-byte packets. By squeezing data from several disk sectors into one large packet for transmission on the bus, the Dynathrottle eliminates the intersector dead time—bus and central-processor time wasted waiting for the disk drive to find sectors—by 50%.

The controller dynamically assembles packets of one to six sectors worth of data, depending on the amount of data in the FIFO buffer, to send as much data as possible in one burst. Quick data transfer leaves the bus free for other operations.



Dynathrottle provides continuous transfers through its large word-wide fast buffer instead of the two-step process used in other controllers, where small blocks of data (32, 256, or 512 bytes) are staged from slow dynamic RAM to a small buffer that requires a substantial overhead to refill.

The 752's intelligent read-ahead capability also adds to performance. Using its buffer much like a cache memory, the controller reads more data blocks from the disk than are requested by the read command—continuing to read until the buffer is filled. Many times, a program will eventually issue requests for sequential sectors. When it does, the data will already have been stored in the controller's buffer.

The controller, which is integrated on a standard VMEbus board, supports the full VME 8-, 16-, or 32-bit address and data modes, with the word-size selection being made by software. Besides the 8-K-byte FIFO data buffer, the 752 also has a 2-K-byte command buffer and is driven by microcode. The controller costs $2,695, and it is available immediately. *–Tom Manuel*

Xylogics, Inc. 144 Middlesex Tpk., Burlington, Mass. 01803.
Phone (617) 272-8140 [Circle 340]

BOARD GIVES PC ATs PHOTO-LIKE DISPLAY

By taking full advantage of a high-performance Intel Corp. display-controller chip and squeezing 4 megabytes of video memory on a single board, Univision Technologies Inc. has produced a display controller with 2,048-pixel-by-1,536 line resolution and a blistering fast 200 MHz display rate.

The near-photographic quality of the UDC-800's images is believed to be the highest 8-bit resolution yet for IBM Corp. Personal Computer ATs and compatibles.

SPEED TRIPLED. Pushing resolution above the 1,280-by-640 standard meant adding more memory capacity and designing high-speed circuitry to keep the display screen refreshed. Instead of refreshing a screen of 1 million pixels—a job that can be handled at 60 or 70 MHz—the new controller refreshes 3 million, says Julius Perl, engineering vice president of the Burlington, Mass., company.

Intel's 82786 display controller had to be interfaced with glue logic designed with fast ECL parts to maintain system

performance at 200 MHz. Packing 4 megabytes of memory—a total of 104 memory chips are on the board—posed another problem. Univision Technology solved it by utilizing ZIPs—for zig-zag in-line packaging—which staggers device pins so that even though chip output pins are on 100-mil centers the pin contacts on the board are on 50-mil centers.

CMOS memory chips were used to minimize power consumption and heat production, Perl says. In another space-saving move, designers used surface-mount technology for non-memory chips, says Perl.

The controller's high resolution will open important new applications in the medical-imaging market, by bringing photographic quality to personal-computer screens. "[Resolution of] 1,000 by 1,000 is just not good enough for a doctor to make a diagnosis of a chest X-ray off the screen," Perl says, but "at 2,000 by 1,500, that resolution makes it look like a real X-ray."

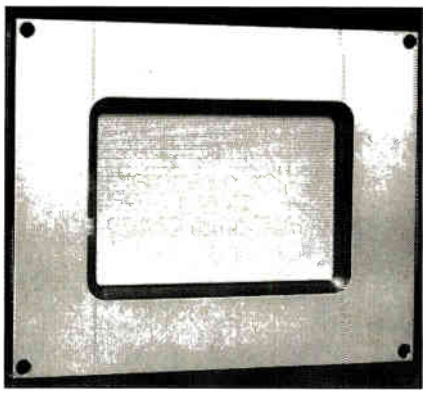
Single-quantity pricing is $6,995 and includes initialization, diagnostics, and a driver for Microsoft Corp.'s MS-DOS operating system. The boards are available now. – *Craig D. Rose*

Univision Technologies Inc., 12 Cambridge St., Burlington, Mass. 01803.
Phone (617) 273-5388 [Circle 342]

THIN-FILM DISPLAYS CAN BE CUSTOMIZED

Two thin-film electroluminescent flat-panel displays from Sigmatron Nova Inc. can be adapted to specific applications. Aircraft cockpit displays, for example, can be customized so they are easily read in bright sunlight.

The MDS-23 is a 2-by-3-in. unit and the MDS-35 is a 3-by-5-in. model. Both



have contrast ratios of better than 20:1, a viewing angle exceeding 160°, and better than 2 lumens/W efficiency. Thickness is 0.65 in.

The MDS-23 has a 50-lines/in. resolution and a 96-by-160 dot matrix. The MDS-35 has 64 lines/in. resolution and a 192-by-320 dot matrix. In 100-unit quantities, the MDS-23 costs $350 and the MDS-35 $675. Both are available now. Customization takes six to eight weeks from receipt of order.

Sigmatron Nova Inc., 1901 Oak Terrace La., Thousand Oaks, Calif. 91320.
Phone (805) 498-4504 [Circle 345]

TWO-IMAGE DISPLAY GIVES 3-D GRAPHICS

A new graphics display system from Tektronix Inc. gives a viewer three-dimensional perception with liquid-crystal-shutter stereoscopic technology that provides two images, one for the right eye and one for the left.

The SGS 430 system consists of stereoscopic viewing glasses, a graphics adapter card that creates a 512-pixel-by-512-line display, a 3-D color monitor, a modulator-driver, and software for creating stereo views.

Tektronix is targeting applications in computer-aided design, molecular modeling, architectural design, and medical imaging. Available now, the complete SGS 430 system costs $9,800.

Tektronics Inc., Liquid Crystal Shutter Marketing Div., P. O. Box 500, MS 48-300, Beaverton, Ore. 97077.
Phone (503) 672-5000 [Circle 346]

COMMUNICATIONS

LAN ANALYZER SNIFFS OUT ETHERNET BOTTLENECKS

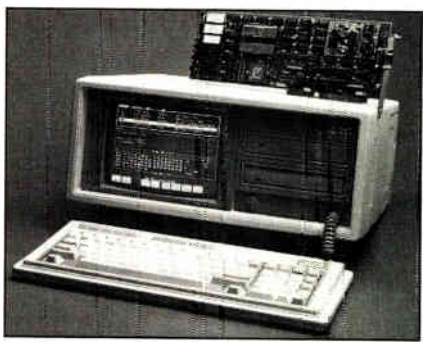
NETWORK GENERAL UNIT CHECKS EACH BYTE AT 10-MB/s SPEED AND DISPLAYS RESULTS WITHOUT DEGRADING LAN PERFORMANCE

A protocol analyzer for Ethernet local-area networks boosts LAN efficiency by pinpointing abnormalities—such as software mismatching—that cause delays. Network General Corp.'s Sniffer monitors each byte of information passing a port, captures frames or partial frames at full network speed without affecting LAN performance, and displays time-stamped descriptions at several levels of complexity.

Built to operate with a Compaq Computer Corp. Portable Computer II based on Intel Corp.'s 80286 central-processing unit, the Sunnyvale, Calif., startup's Ethernet Sniffer consists of a plug-in 16-bit direct-memory-access board with its own Intel 80186 CPU, 512-K of random access memory, and an Intel 82586 Ethernet adapter, plus six software suites matching various implementations of upper-level protocols.

FAST LANS. Sniffer was introduced last fall for analysis of IBM Corp.'s 4-Mb/s Token Ring networks. The new version is for 10-Mb/s Ethernets. Until recently, LANs have offered such high bandwidth that network usage has not been a problem. But as more users come on line, maximizing network performance becomes more important.

Network General's president, Harry Saal, says that the Sniffer has discovered numerous instances of networks being slowed down by mismatched software that nonetheless met protocol specifications. Also, he says, many networks create too much overhead for themselves, sending a great number of empty packets. Others generate errors. Saal cites one case of a network that reads records from a multiuser data base before locking it. "This error is very clear on the screen, but it would be almost impossible to find by trial and error," he says. The Sniffer handles real-time collection, filtering, and analysis of network data. It can also be used as a development tool for applications using IBM Corp.'s Netbios. Arpanet Corp.'s TCP (transmission control protocol), or other communications protocols.



SLEUTH. Sniffer uses Compaq's Portable Computer II to uncover LAN problems.

As a development tool, the Sniffer "takes six months of debugging and reduces it to an afternoon," Saal says. As an analyzer, it displays abnormalities in network traffic so that users can spot parts of their systems that generate delays or errors.

The Ethernet Sniffer Model PA-402 costs $19,000. A dual Token Ring/Ethernet version, model PA-403, costs $24,000. An upgrade from present Token Ring Sniffers is available for $5,500. In addition, Network General is introducing protocol interpreters for TCP/IP, ISO IP and TP protocols, and Sun Microsystems Inc.'s NFS protocol. Protocol suites cost $995. All products are available now.

Network General Corp. 1296B Lawrence Station Rd., Sunnyvale, Calif. 94089.
Phone (408) 734-0463 [Circle 440]

LAN CONNECTS PCs TO CAE SOFTWARE

DashNet, a local-area network from Data I/O Corp., gives as many as 25 IBM Corp. Personal Computers access to the full family of DashNet computer-aided-engineering software. It can also be used with Digital Equipment Corp. VAX computers.

DashNet is an adaptation of Ethernet. It connects the computers and CAE tools through a central file server composed of a 70-megabyte disk drive, 960-K of system memory, and a 60-megabyte backup tape-cartridge unit. Called the DN3-Server, it costs $11,950.

Another DashNet component, the DN Station, consists of all the software and hardware needed to connect the PCs or VAXs to the LAN. It costs $650 for each work station.

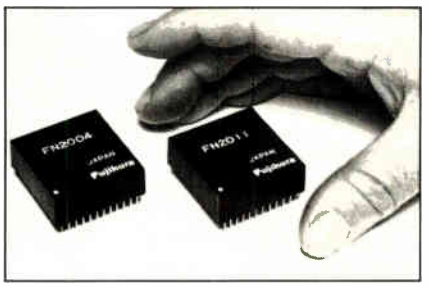
The DN-Cabl component of DashNet is the cable/connector package that forms the physical linkage between file server and computers. It costs $45 for a 7-meter cable; $200 for a 100-m cable.

FutureNet, 9310 Topanga Canyon Blvd., Chatsworth, Calif. 91311.
Phone (818) 700-0691 [Circle 447]

LAN TRANSCEIVER MOUNTS ON PC

Fujikura America Inc.'s transceivers for local-area networks mount directly on the printed-circuit board of a personal computer. They save original-equipment manufacturers the time and money that would be required to design a transceiver of their own.

The transceivers meet IEEE 802.3 local-area-network specifications. Two versions are available: the 12-V FN2004,



which supports Ethernet, and the 5-V FN2011, for personal computers that use other protocols. Available now, both cost $90 in 1,000-unit purchases.

The Ethernet version also comes as a molded package that incorporates not only the transceiver but also a tap and cable. It is available now in sample quantities with a 15-, 30-, or 60-ft. cable for $270.

Fujikura America Inc., 455 One Allegheny Sq., Pittsburgh, Pa. 15212.
Phone (412) 323-9696 [Circle 445]

CONCENTRATOR LINKS PACKET NETWORKS

The Advanced Network Processor 1220 concentrator from Siemens Data Switching Systems permits several terminals to use a single CCITT X.25 packet network, regardless of whether or not they are X.25-compatible terminals.

The ANP 1220It ensures X.25 compatibility with IBM Corp.'s BSC 3270, BSC RJE, SNA/SDLC, asynchronous, and X.25 attachments.

When installed at a host site, the concentrator funnels multiple data streams into a single port. When installed remotely, it can concentrate data streams from different sites before they are sent to a host site, thereby reducing network link requirements.

Data communications software is stored on a number of exchangeable firmware modules. Each version provides support for a different IBM synchronous protocol and allows the selection of an X.25 or asynchronous port.

The unit costs about $5,000, depending on configuration, and is availabile four weeks after order.

Siemens Data Switching Systems Inc., 110 Ricefield La., Hauppage, N. Y. 11788.
Phone (516) 435-4000 [Circle 446]

TRANSISTOR ARRAY CHIPS ACHIEVE 350-MHz SPEEDS

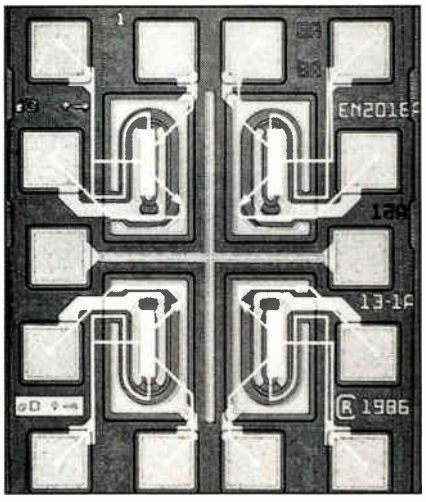
ELANTEC USES GLASS LAYER TO TOTALLY ISOLATE FOUR MATCHED NPN DEVICES; A WAY TO REPLACE DISCRETE BIPOLAR TRANSISTORS

A line of transistor arrays from Elantec Inc. achieves high-speed performance—up to 350 MHz—by using four independent npn devices that are dielectrically isolated on a single chip. The dielectric isolation creates devices with a low collector-to-substrate capacitance, which, in turn, permits very high-speed performance and complete dc isolation.

The line includes two commercial arrays, the EN2016C and the EN2016AC, and two military models, the EN2016 and EN2016A, that can all operate at up to 350 MHz. They are the industry's first monolithic quad arrays with matched npn transistors that provide total isolation of each transistor, the Milpitas, Calif., company claims. The arrays target hybrid and board-level designs in which designers now use discrete bipolar transistors to build devices such as current sources and multipliers.

GLASS LAYER. The transistors are electrically isolated from one another by a layer of glass, according to vice president of marketing Dean Coleman. The resulting low collector-to-substrate capacitance eliminates the need for substrate biasing in normal operation, as is required in conventional devices.

The new arrays are designed to complement the company's 350-MHz EP2015 and EP2015A arrays, the industry's first dielectrically isolated vertical pnp quad-transistor arrays.



CHOICE. Elantec's quad-array transistors come in commercial and military versions.

"These devices feature excellent parametric matching and high-speed performance up to 350 MHz," says Coleman. They are pin-compatible and similar in performance to nondielectrically-isolated arrays from Sprague Electric Co. and Motorola Corp. Moreover, he says, the product family specifies base-emitter voltage matching to 1 mV and beta matching to 5%.

The EN2016C is specified to run at 25°C, while the EN2016AC is even more tightly specified and guaranteed over the commercial temperature range from –25°C to 85°C. The two military versions, the EN2016 and the more tightly specified EN2016A, are tested over the full military temperature range from –55°C to 125°C.

The EN2016C and EN2016AC are available in either 14-pin plastic or ceramic dual in-line packages. The military versions are available in either ceramic packaging or in chip form for hybrid applications. The chips incorporate large bonding pads for easy automated manufacturing.

The EN2016C costs $1.40 each in 100-piece quantities, and the military versions start at $7.50 each in 100-piece quantities.

–Bernard C. Cole

Elantec Inc., 1996 Tarob Ct., Milpitas, Calif. 95035.
Phone (408) 945-1323 [Circle 360]

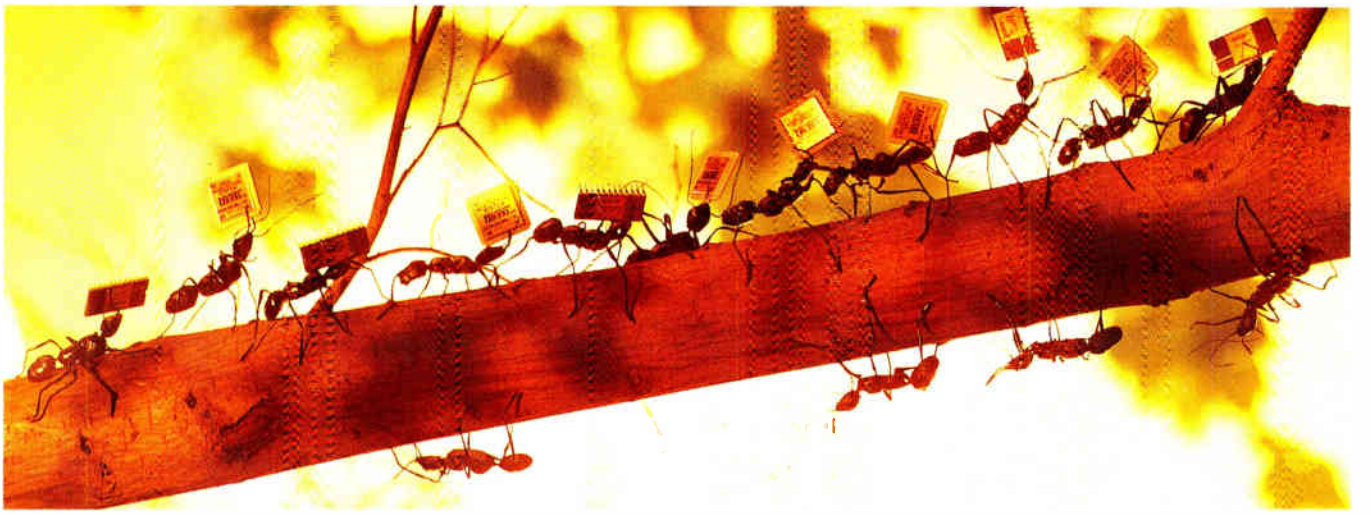
VIDEO DACs DRIVE HIGH-POWER TERMINALS

Two versions of an 8-bit, digital-to-analog converter from Integrated Device Technology Inc. offer 125 MHz performance—fast enough to drive 75-Ω video terminals with resolutions of 1,280 pixels by 1,024 lines.

For most applications, the IDT75C18 and IDT75C28 DACs do not require any additional registration, buffering, or deglitching. Power dissipation for the devices is 400 mW.

The 75C18 has ECL-compatible inputs and is both pin-compatible and functionally compatible with TRW Inc.'s TDC1018.

The 75C28 has TTL inputs for systems with lower clock rates. Output levels correspond to the RS-170 and RS-343 monitor standards. Production quanti-



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ties are now available. The price of the devices is set at $27.50 each in 100-unit quantities.

Integrated Device Technology Inc., 3236 Scott Blvd., P. O. Box 58015, Santa Clara, Calif. 95052.
Phone (408) 727-6116 [Circle 365]

CMOS 16-K EPROM IS BIPOLAR-COMPATIBLE

A byte-wide 16-K CMOS electrically programmable read-only memory from Texas Instruments Inc. is pin-compatible with 2-K-by-8-bit bipolar PROMs and has access time of 35 ns.

The TMS27C292 has a power dissipation of 394 mW from 0°C to 70°C and is available in a windowed 600-mil ceramic dual in-line package. TI plans to introduce 300-mil ceramic packaging, 300- and 600-mil plastic packaging, and a plastic leaded-chip-carrier version. The windowed model can be reprogrammed.

Latchup immunity is provided beyond the level of current voltage transients possible at a minimum of 250 mA on all inputs and outputs.

It is suitable for use in bit-slice systems and for digital-signal-processing applications.

Prices depend on access speed and voltage tolerance. The 35-ns version with ±5% voltage tolerance has a 10- to 12-week delivery time and costs $9.25 each in 100-unit quantities.

Texas Instruments Inc., Semiconductor Group (SC-713), P. O. Box 809066, Dallas, Tex. 75380.
Phone (800) 232-3200 [Circle 366]

POWER IC DRIVER HITS PEAK OF 7 A

A multichannel power IC driver from Sprague Electric Co. that has four outputs, each rated at 6 A or 7 A peak, can drive high-current solenoids, relays, motors, and incandescent displays. The UDN-2948W array replaces discretes in current-source applications and comes in a 12-pin single in-line package.

The driver eliminates the need for buffers when discrete npn emitter-followers, pnp drivers, or MOSFETS are used with low-level logic. Built-in level-shifting circuitry eases interfacing with the logic. Input current is 220 μA.

The device is rated at 60 V minimum breakdown voltage and 35 V sustaining. Two supply pins allow each pair of outputs to drive loads with a different supply voltage.

Delivery takes 10 to 12 weeks after receipt of order. The drivers cost $4.48 each in 100-unit quantities and $2.68 each in 50,000-unit quantities.

Sprague Electric Co., 41 Hampden Rd., P. O. Box 9102, Mansfield, Mass. 02048.
Phone (617) 853-5000 [Circle 367]

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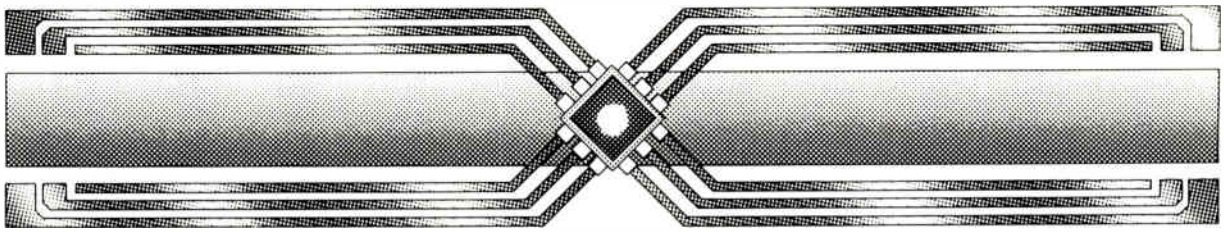

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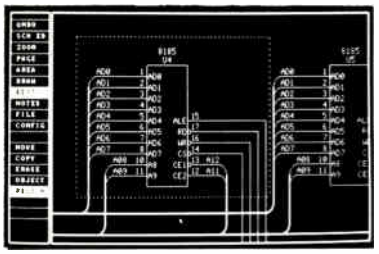

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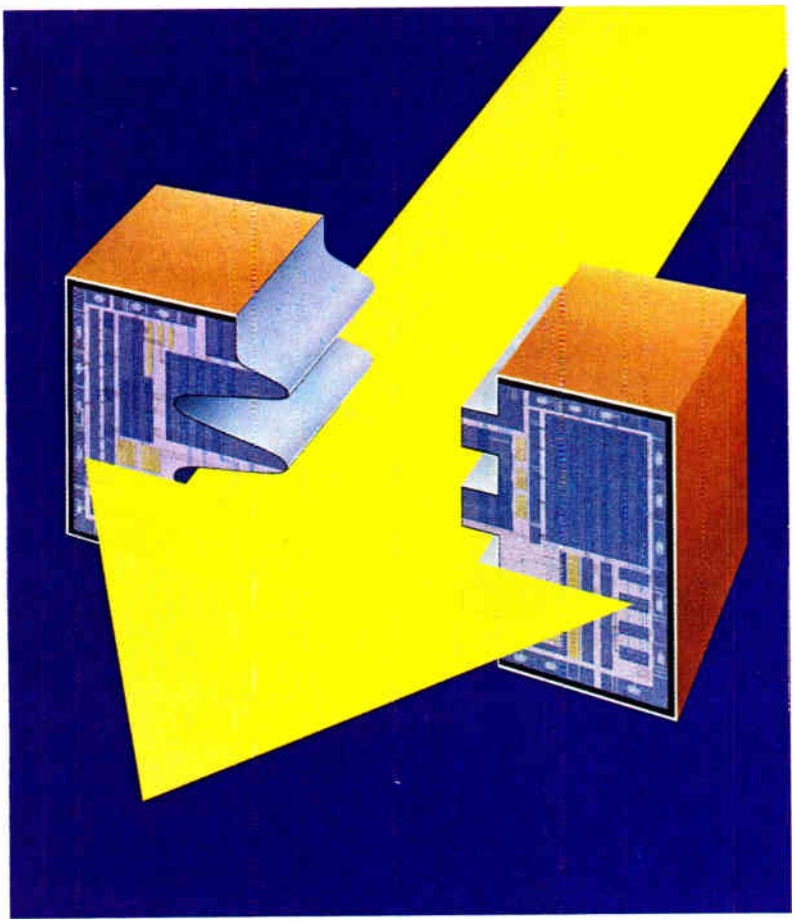

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Excerpted from an exclusive article in the January 22, 1987 issue.

ELECTRONICS WEEK

NEC INSISTS JUDGE BE DISQUALIFIED

NEC Corp. is not giving up on its contention that the judge who ruled against it on a key point in a suit against Intel Corp. should be disqualified because he owned some Intel stock at the time. San Jose, Calif., District Court judge William A. Ingram has already ruled that microcode may be copyrighted. At issue is whether the Japanese company illegally copied Intel microcode in a NEC microprocessor. Although a U.S. District Court in San Francisco this month denied NEC's move to oust Ingram, the Japanese firm says that if it loses on appeal, it will raise the issue in any further appeals after a final decision.

HERE'S A MARKET THAT'S EXPLODING

Semiconductor technology is giving explosives a shorter fuse—a few tens of microseconds, versus the few thousandths of a second it takes a conventional hot wire to ignite a charge. Scientists at Sandia National Laboratories and the University of New Mexico, in Albuquerque, say the new device, called a semiconductor bridge, improves control of blasting in the mining, construction, and engineering industries. It may also find service in rockets and missiles, for precision ignition of propulsion and course-correction thrusters. The bridges are smart devices that require a coded signal to trigger them.

MCC NAMES A NEW CHAIRMAN

The Microelectronics & Computer Technology Corp. finally has a new chairman and chief executive officer. In July, Grant A. Dove, a retiring executive vice president at Texas Instruments Inc., will assume these posts, which have been vacant since the departure last December of B. R. (Bobby) Inman. Dove, who is taking early retirement from TI after 28 years there, will act as a consultant to the Austin, Texas, consortium while he phases out his duties at the Dallas company.

VITESSE IC DIVISION GOES INDEPENDENT

Vitesse Electronics Corp.'s Integrated Circuits Division, Camarillo, Calif., has become an independent company called Vitesse Semiconductor Corp., says its president and now chief executive officer, Louis R. Tomasetta. The restructured firm has acquired $10 million in second-round funding from a group of investors headed by Sequoia Capital of Menlo, Calif. The new funding will enable Vitesse to develop additional products and expand into higher-volume production, Tomasetta says.

NEW SUPPORT FOR INTERACTIVE CDs

Sun Microsystems Inc., of Mountain View, Calif., and the Dutch multinational Philips International NV will cooperate to build a "multi-media authoring system" for interactive compact disks, teaming Sun's work stations with Philips' disk technology. Aimed at entertainment, education, and information markets, the authoring system will allow developers to integrate audio, video, data, and text on the disks.

FUJITSU, GTE FORM VOICE/DATA VENTURE

Fujitsu America Inc. and GTE Communications Systems Corp. are forming a joint-venture company to develop and market voice-and-data business communications systems in North America. The venture, called Fujitsu GTE Business Systems Inc., will begin operations in Tempe, Ariz., on April 1. It will be owned 80% by Fujitsu America and 20% by GTE. GTE Business Systems will transfer its Tempe Business Systems division to the joint venture.

SATELLITE CHANNELS GO BEGGING

Because it cannot find customers for many of the 16 satellite transponders it leases, Equatorial Communications Co. of Mountain View, Calif., has took a $45 million writeoff and reported a $67.8 million loss for the fiscal year ended last Dec. 31. The firm's sales were off 9.3 per cent at $50.9 million. Contel ASC, a subsidiary of the Contel Corp., has provided some help by agreeing to buy $10 million worth of Equatorial equipment, guarantee the satellite leases, and lend the company $6 million, in return for the right to buy $11.7 million in Equatorial stock.

BOOK-TO-BILL RATIO CONTINUES TO RISE

The end of the March quarter may give solid evidence as to whether the semiconductor industry's apparent recovery is real. The bellwether book-to-bill ratio crept from 1.12 to 1.13 in February, the fifth straight monthly increase—while three-month average bookings and billings themselves were virtually flat, each up less than 1% from January. The Semiconductor Industry Association, which released the figures, attributed the increase to continuing improvement in electronic equipment sales.

DEC, ALDUS SIGN PAGEMAKER DEAL

Aldus Corp., the developer of PageMaker desktop publishing software, is teaming up with Digital Equipment Corp., which will offer the IBM PC version of PageMaker for its VAXmate personal computer. DEC, of Maynard, Mass., will sell a version of the Seattle company's desktop publishing program that includes a filter to allow it to import DEC's WPS-PLUS word-processing files. The VAXmate runs PC software and also accesses VAX resources.

CONCURRENT SIGNS DEAL WITH APOLLO

Concurrent Computer Corp., the Tinton Falls, N.J., manufacturer of high-performance parallel processors, will sell Apollo Computer Inc. work stations as peripherals in large-memory real-time processing systems. Apollo, of Chelmsford, Mass., signed a similar agreement a little over a year ago with Alliant Computer Systems of Littleton, Mass., another maker of parallel processors.

U.S., JAPAN FIRMS SET AUTOMATION PACT

Matsushita Electric Industrial Co. of Osaka, Japan, and Westinghouse Electric Corp. of Pittsburgh, Pa., will establish a joint venture for factory automation equipment in the U.S. this summer. Matsushita will supply technology for automating consumer-products and light industrial manufacturing, and Westinghouse will supply technology in the heavy-industrial electrical field.

AEA: U.S. SALES END '86 ON HIGHER NOTE

In the fourth quarter, U.S. electronics manufacturers sold $61.1 billion of domestically produced goods and services, matching a sales record that was set way back in the fourth quarter of 1984, reports the American Electronics Association. It was enough to bring an otherwise sluggish 1986 up to a total of $226.5 billion—only 1% less than 1985's $228.7 billion, according to the group. New orders hit $60 billion in the quarter, the highest level since early 1985, and December saw a 12% gain in orders over November, to $22.9 billion, it says.

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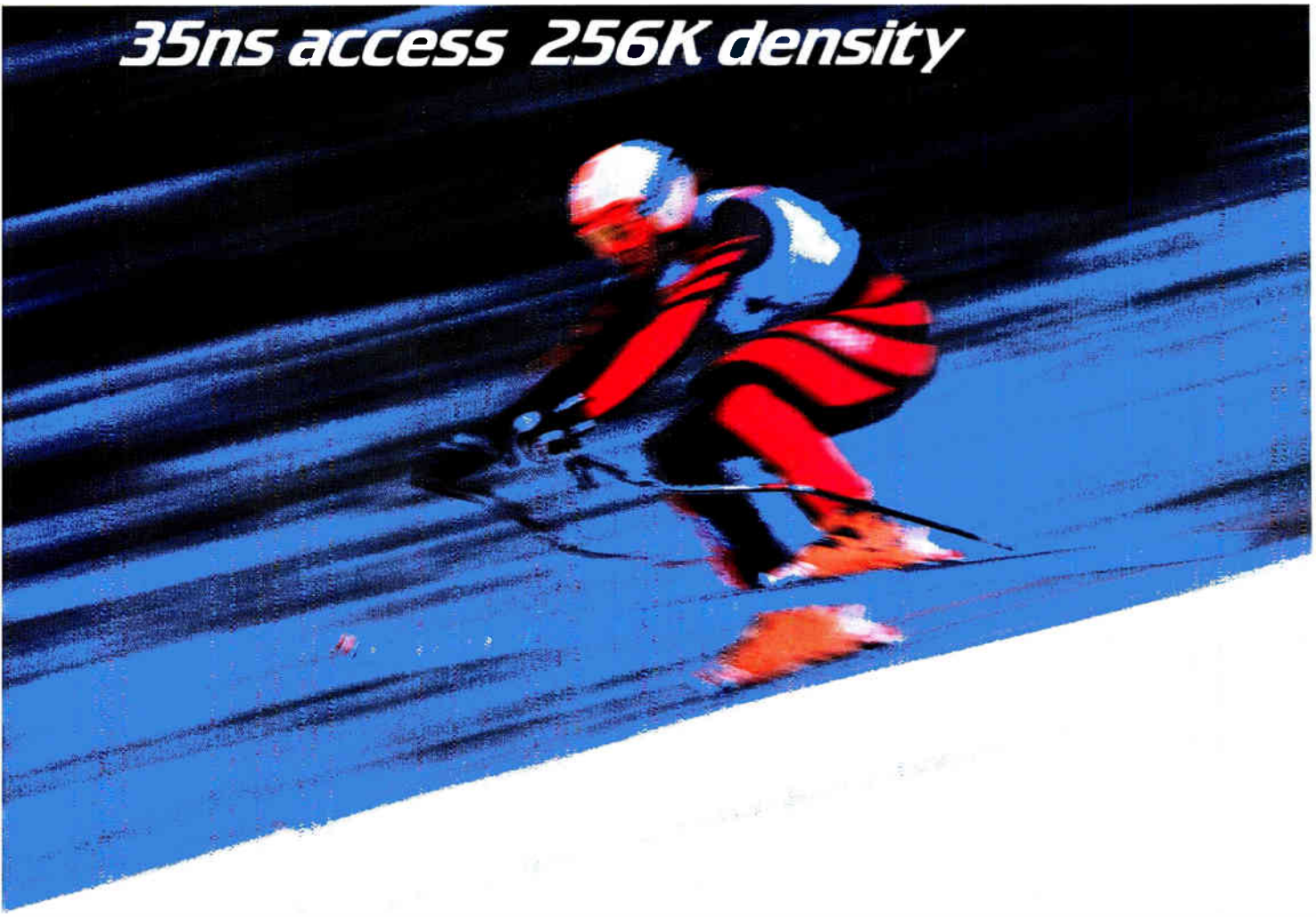

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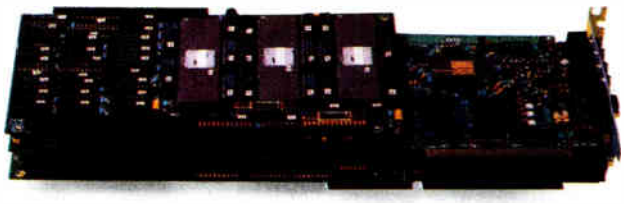

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