DATA GENERAL'S 88000 RISC CHIPS WILL HIT 100 MIPS/32

SMART-POWER IC SET ALL BUT ELIMINATES CIRCUIT DESIGN/93

A VNU PUBLICATION

Electronics®

APRIL 28, 1988

RISC SLUGFEST

IS MARKETING MUSCLE GETTING MORE IMPORTANT THAN CHIP PERFORMANCE?

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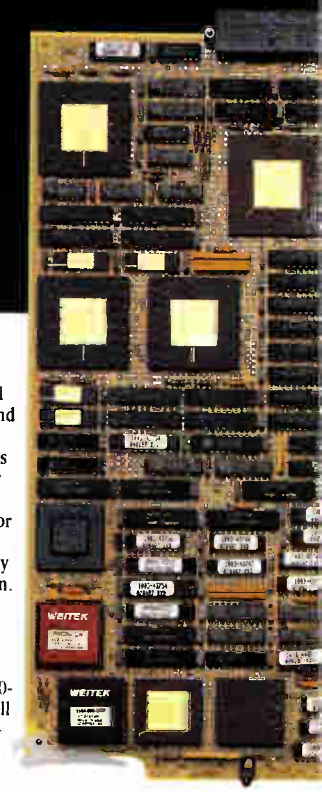
A CLOSE LOOK AT MOTOROLA'S 88000/75

CHOOSING A RISC CHIP: WHAT DRIVES CUSTOMERS?/85



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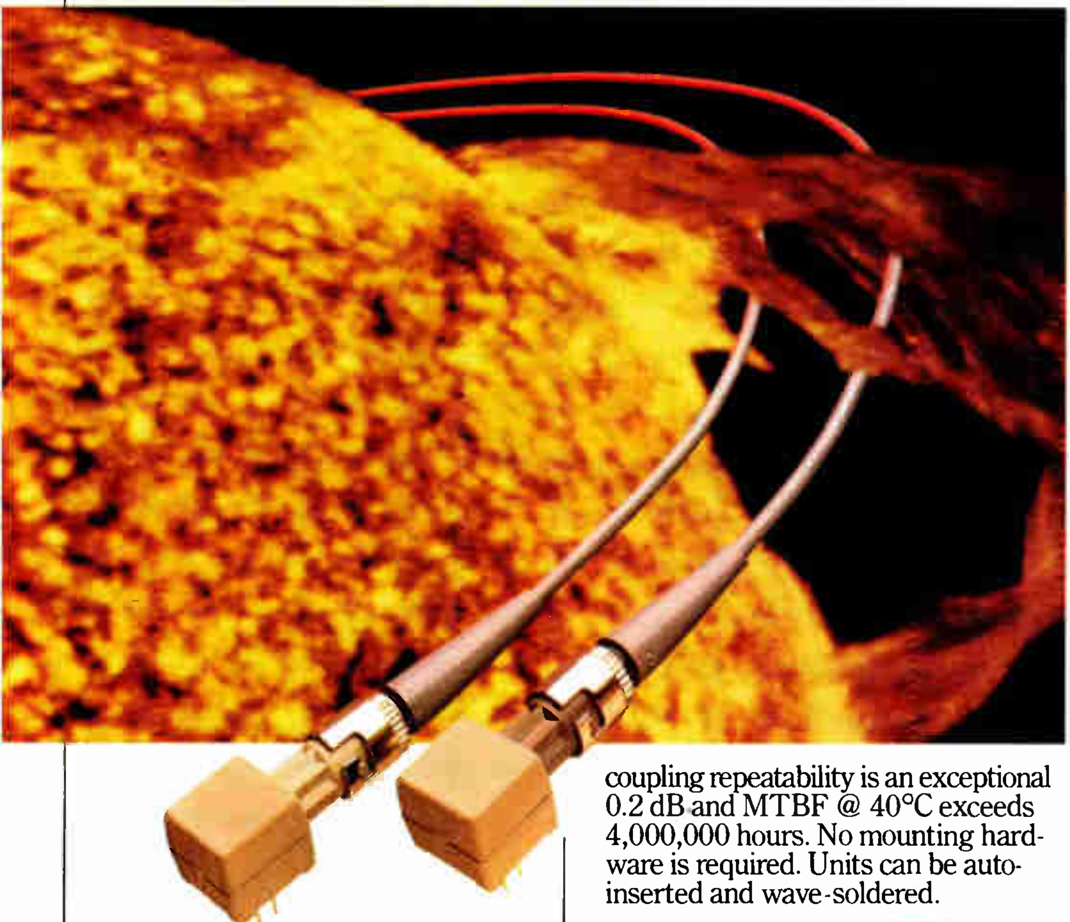

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ELECTRONICS MAGAZINE JOINS A NEW TEAM

Like Fairchild and National, we've become partners with a major competitor—now all we need to do is figure out how to get to New Jersey

Now I know how Don Brooks and the Fairchild Semiconductor gang felt last year when they were sold to National Semiconductor. Suddenly, the guys they'd been battling in the marketplace for years became their partners. That's what has happened to *Electronics*; for those less sharp-eyed readers, we were sold in March. But Charlie Sporck seems to have done a fine job in packaging those two cultures together into an even stronger competitor, and I know we can do it too.

A few years ago, I ignored my college adviser's advice to get an MBA, because I wanted the fun and excitement of a career in journalism. I don't know about the fun part, but it sure can't get much more exciting. At the same time we're going all-out to put out this magazine, we're also trying to move from McGraw-Hill's Manhattan headquarters to New Jersey's VNU Business Publications. It's the U.S. subsidiary of a Dutch publishing giant that wants to make it big in the U.S. market. VNU has already made it big outside the States. With projected sales of more than $2 billion this year, it's larger than McGraw-Hill.

While *Electronics* no longer fits into McGraw-Hill's long-term strategic plans, it does fit well into VNU. Last year, the Dutch became a major player in the U.S. electronics and computer trade press by purchasing Hayden Publishing, which published our biggest competitor (now our partner) *Electronic Design*. Also fitting well at VNU is the bulk of *Electronics'* veteran staff. We've got exciting plans for both publications, each of which will continue to do what it does best: *Electronics* as the leading worldwide magazine for managers and *ED* as its counterpart for design engineers.

I do have a personal problem. I can no longer make my usual half-hour commute: walking from the Upper East Side to Rockefeller Center. Wearing out shoe leather instead of burning gasoline has not only helped our balance of trade, but it has always been one of those job perks that's kept me here in Manhattan for two decades. Now I have to buy a car for my new commute to the wilds of New Jersey. Don't tell anyone, but my commute will actually take less time. Of course, that's hitting Mach 0.8 out over the Hudson. To get up to speed, I've decided I'll need something a little extra; Honda's Acura Legend, for example, but I surely will hear from my son for not buying American.

ROBERT W. HENKEL

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PEOPLE

HOW HONEYWELL'S MINO WILL SPEED TECHNOLOGY TO MARKET

COLORADO SPRINGS, COLO.

In an era of shortening semiconductor product-life cycles, the speedy transition of technology from the development labs to the manufacturing line is increasingly important to a company's competitiveness. And at Honeywell Inc.'s Solid State Electronics Division in Colorado Springs, Thomas D. Mino is the man charged with making it happen.

"I'm trying to build stronger bridges between the R&D people and the actual operations people," says Mino. "Probably the biggest single challenge I see is reducing the cycle time from technology development to its introduction in the marketplace."

The 41-year-old Mino was named vice president of operations, a new position at the Honeywell division, last December. He moves up to the post from vice president of manufacturing, and in his new spot picks up added responsibility for the division's research and development operation in Plymouth, Minn.

Mino concedes that having development and production facilities located 750 miles apart in Minnesota and Colorado, though not necessarily unusual, does make an already complex job tougher. But it is manageable, Mino says. His focus now is on the transfer of Honeywell's advanced, submicron CMOS, and bipolar technology developed under the Defense Department's Very High Speed Integrated Circuits program. And he's already making some moves.

"Probably the major thing we've done is really formalize the transition process," Mino says. "We've established some networks and standards for the two organizations, as to what each is responsible for with the start-up of a new technology, when it's ready for transfer into manufacturing, what kind of information has to flow with it, and how it has to flow," he explains.

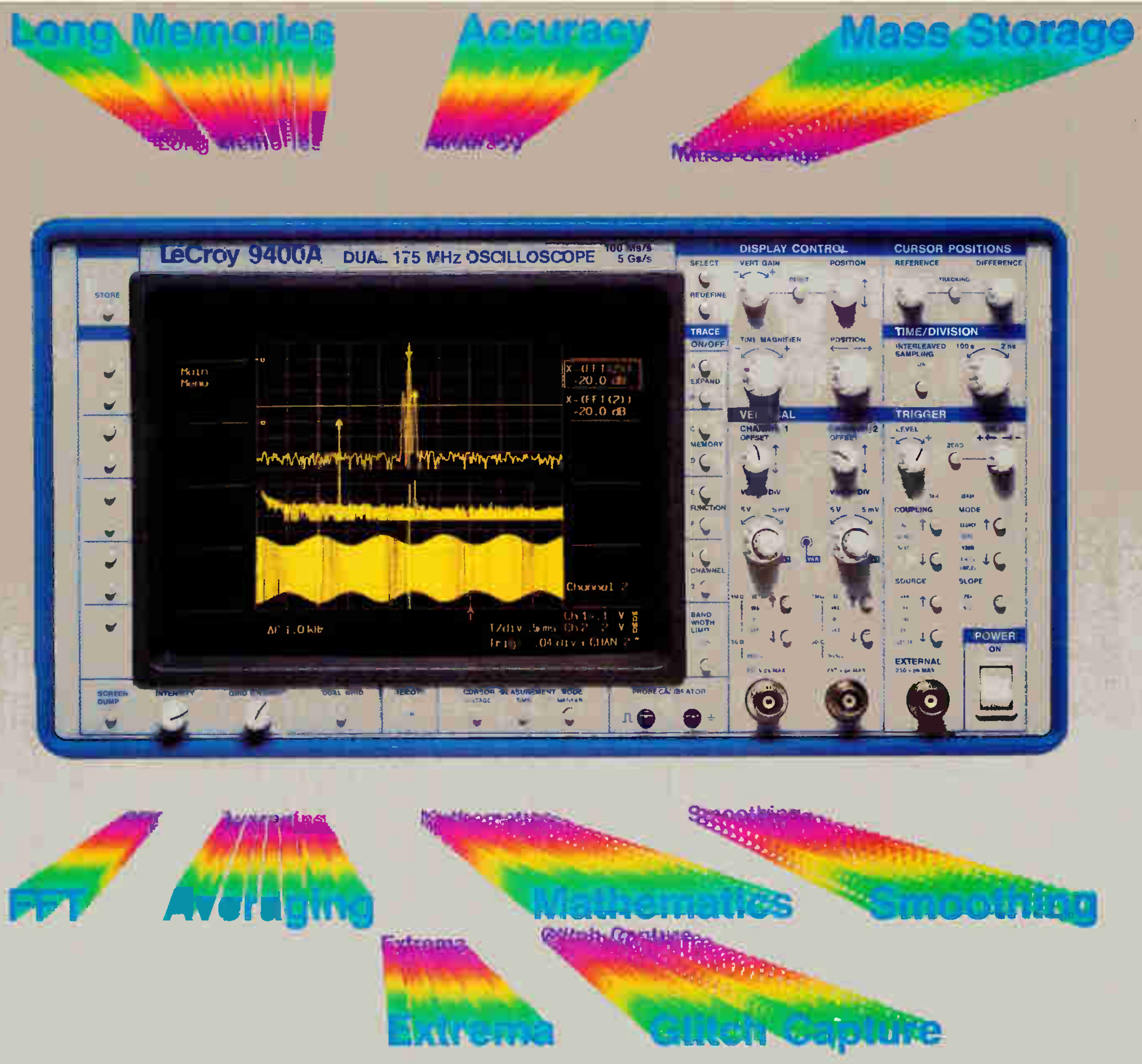
NOW, A CONTRACT. Teams consisting of both production and development engineers now make the decisions as to when a process or product is ready for transition to manufacturing, for example. "Before, it was sort of like somebody called us and said it's about time to put this into manufacturing, and we're going to send the stuff down, and if you have any problems, call us," Mino observes. "It was sort of a handshake before, and now we've got more of a contract."

Mino brings strong technical and chip-manufacturing credentials to the job. Before joining Honeywell in 1986, he spent 18 years in a variety of positions at AT&T Corp. Mino was the first manager of AT&T's Orlando, Fla., chip plant. Then, as director of MOS engineering and operations, he had engineering responsibility for all of AT&T's MOS production locations and manufacturing responsibility for the company's Allentown, Pa., plant. He holds BSEE and MSEE degrees from the University of Pittsburgh and Lehigh University, respectively.

Thomas D. Mino must coordinate the work of operations that are 750 miles apart.

"Tom brings a manufacturing professionalism to the position, and at the same time, he is quite technical, so he is able to create respect for the two different viewpoints, both research and development and manufacturing," says Brian Hegarty, vice president and general manager of the Honeywell chip division. "He's really got the background to be able to knit these two organizations together."

For Mino's part, the immediate goal is to bring Honeywell's submicron-VHSIC technology to the marketplace within 24 to 30 months after its development was begun. Honeywell is currently shooting for late 1989 to begin 0.5-μm production in Colorado. Beyond that, Mino hopes to apply what he learns to shorten the development-to-market cycle on future technology jumps. "Right now, we're probably looking at two-year kinds of windows," he says. "But we'd like to establish goals where we improve that by, say 20%, whenever we move to a new technology." *–Wesley R. Iversen*



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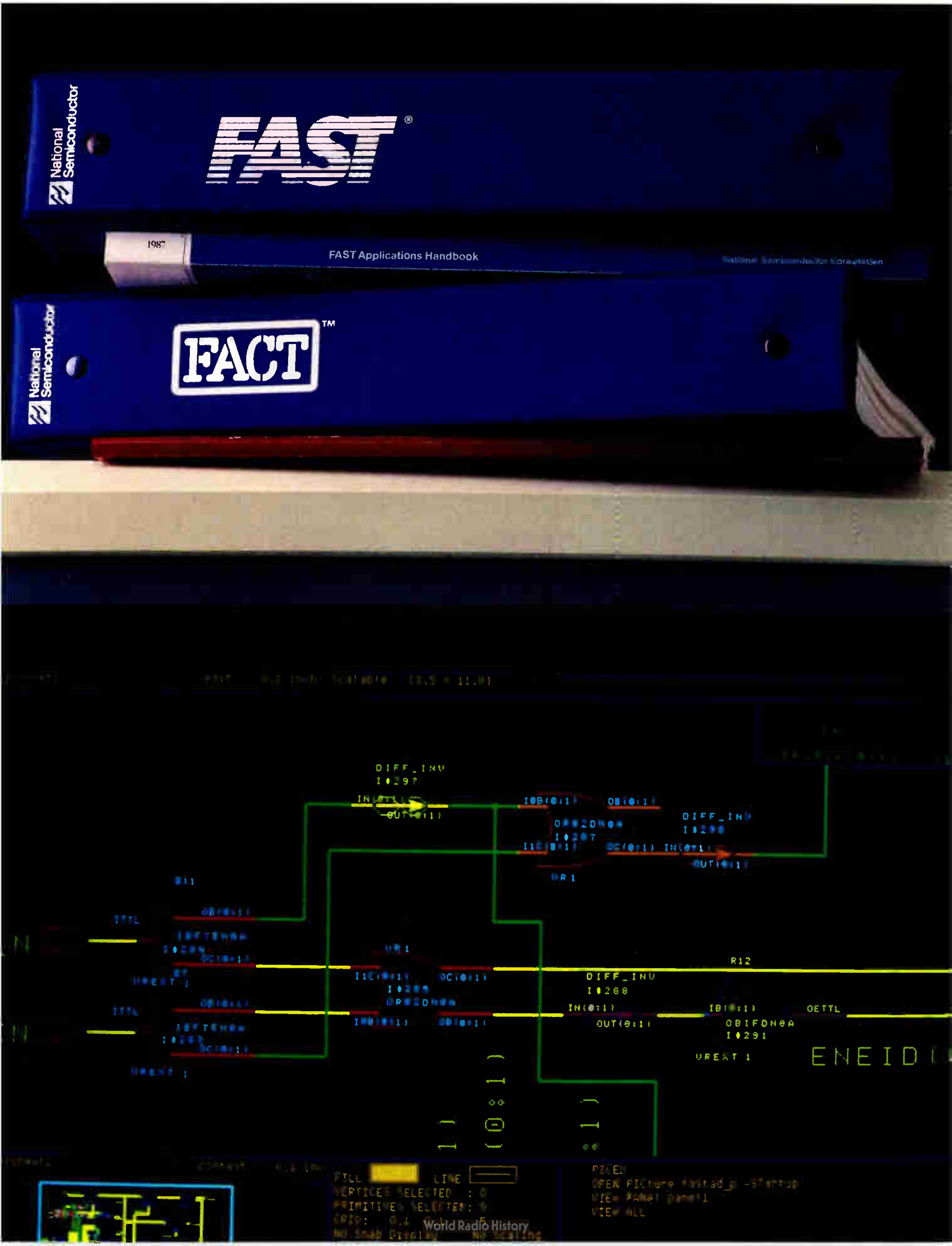
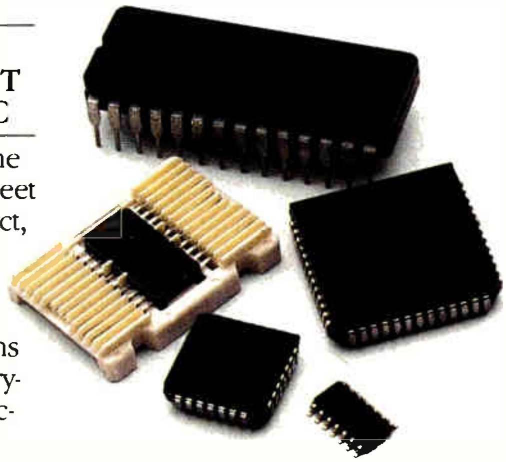


The logic in choosing National.



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User-configurable supercomputing

To the editor: I was delighted to receive your special issue on supercomputers [*Electronics*, March 3, 1988, p. 51]. I was disappointed, however, that Computer System Architects was not included in the table of different machines now on sale.

As a part of another article, a copy of one of our Mandelbrot-Set scenes appeared on p. 75 without reference to CSA. The photo reference said "... computers made visible to scientists' eyes the behavior of poorly understood mathematical systems, such as the one that produces the fractal geometries of the Mandelbrot set discovered by IBM Corp. researcher Benoit Mandelbrot."

Mandelbrot should receive the credit for giving the world the function $z \leftarrow z^2 + c$ and for pointing out how fascinating various regions of that function appear when its rate of divergence is color-mapped. But CSA was the source of the actual image you printed. Our own Scott Lloyd wrote the software, which allowed him to explore the Mandelbrot Set, find this particular region, and then color-map it.

Many fractal buffs spend hours upon hours computing images within the Mandelbrot Set, taking from 20 minutes to 2 hours per frame on a large-model DEC VAX or the like. The one you printed took only 35 seconds to produce, using eight Inmos transputers on a pair of our PC add-in boards. What's more, CSA PARTS (for parallel transputer series) systems can be selected from a family, and mixed and matched within arbitrarily large networks of processors, hosts, and peripherals—bringing user-configurable personal supercomputing to the desktop at prices well under those quoted by your writers for equivalent performance.

The PARTS family has a price range of $1,200 to $6 million, the top end of which has 4,192 processors and 1 Mbyte of RAM per node (actually, even larger systems can be configured). Its peak rate is over 4 gigaflops, based on an even mix of 64-bit scalar adds, subtracts, multiplies, and divides. Other numbers that would have been on your chart are 0.37 megaflops/processor on the 100-by-100 Linpack benchmark, 51 systems shipped, and under 10 major application packages.

Duane B. Call
President
Computer System Architects
Provo, Utah

☐ Electronics *regrets omitting Computer System Architects from the chart and not giving proper credit for the photo.*

DSP's FFT benchmark in question

To the editor: In your article on Analog Devices' new ADSP-2101/02 digital signal processors [*Electronics*, March 31, 1988, p. 70], the 1,024-point FFT benchmark quoted for the Motorola DSP56000/01 is inaccurate. Even the most simplistic 1 K FFT written for the DSP56000/01 is faster than the quoted 6.4 ms. Our best published performance on this benchmark is 3.4 ms with the current 10.25-MHz instruction-rate DSP56000/01. This is easily justified since the DSP56000/01 executes a radix 2 butterfly loop in only six instructions (with or without scaling) versus the ADSP-2100's 9 instructions (without scaling) or 12 instructions (with unconditional scaling). Although scaling is free on the DSP56000/01, it is rarely needed because of the larger 24-bit data size.

For a broader perspective, consider that a 13.33-MHz instruction-rate version of the DSP56000/01 will be available in 1988. Given the time frame that is being quoted for ADSP-2101/02 availability, the 75-ns DSP56000/01 FFT benchmark will be 2.6 ms versus the 80-ns ADSP-2101/02's 4.4 ms.

As you can see, we are proud of the FFT performance of the Motorola DSP56000/01. The recently announced Motorola DSP96001/02 IEEE-754 standard floating-point DSP [*Electronics*, March 17, 1988, p. 64] is a good example. The DSP96001/02 can execute a radix 2 butterfly loop in just 4 instructions, yielding a 1 K FFT under 2 ms at a 13.33-MHz instruction rate. This is almost twice as fast as published FFT benchmarks for other recently announced DSPs, which are not IEEE floating point.

Kevin Kloker
Principal Staff Engineer
Motorola Inc., Corporate Research
Schaumburg, Ill.

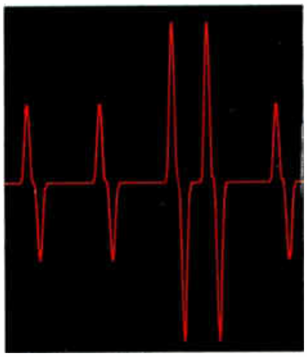
Updating smart-power forecasts

To the editor: In response to Mr. Selven's reply to my letter published in a recent issue of your magazine [*Electronics*, March 31, 1988, p. 12], I would just like to say that I could not agree more with Mr. Selven's point of the need to update forecasts.

BIS Mackintosh Inc. has updated its smart-power forecasts and they do constitute a significant part of the analysis contained in our Automotive Electronics Multi-client Study, which was delivered to client firms in September 1987.

George I. Stojsavljevic
Consultant
Continuous Information Services
BIS Mackintosh Ltd.
Luton, England

Correction: A recent item in an *Electronics* newsletter [*Electronics*, April 4, 1988, p. 25] incorrectly identified the headquarters location of Microchip Technology Inc. The company is based in Chandler, Ariz.



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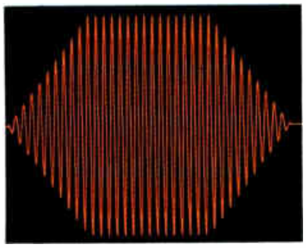

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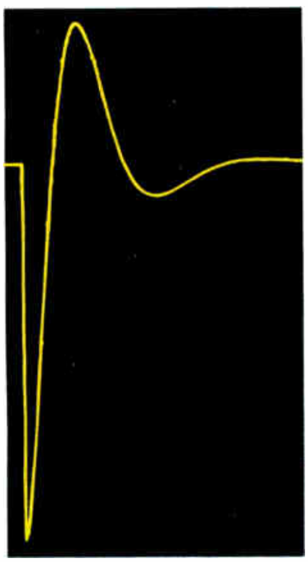
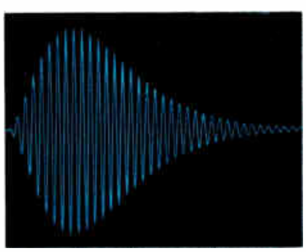


Neuron Impulse



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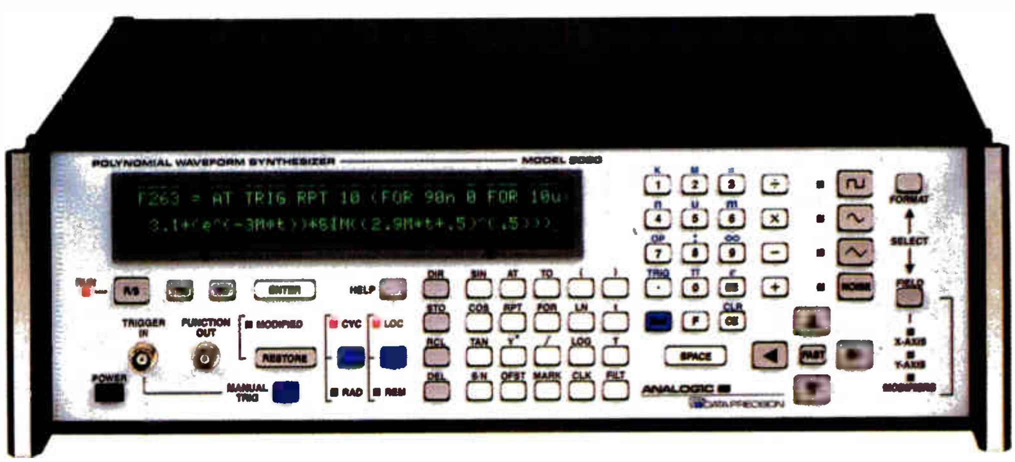

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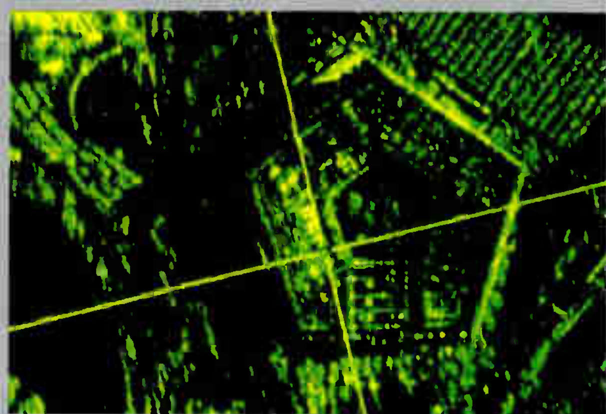
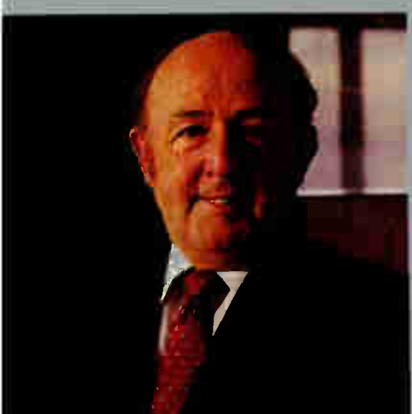


While developing software for the B1-B Bomber radar system, Westinghouse Defense landed on a tough problem – integrating its computer resources. "We needed a complete network that would allow hundreds of software engineers across the country to interact, create, enhance and modify the software," says Ron Clanton, Manager of Software and Information Systems.

The solution was a network from Digital.

Remarks Clanton, "The network is so comprehensive, it extends even to the air in our Flying Software Lab. Giving us real-time, in-flight software testing and development capabilities. The Software Lab alone provides a cost savings of up to 98% versus traditional in-flight testing in the B1-B Bomber."



"A networked software engineering environment that helped Westinghouse Defense zero in on ways to cut in-flight test costs by 98%."

"But our savings don't stop there," continues Clanton. "With the VAX™ architecture and the VMS™ operating environment, engineers both on the ground and in the air can react instantly to each other's modifications." He adds, "That's sharing their knowledge and expertise faster and more productively than they ever thought possible. Which, of course, provides for a better end product."

Clanton sums it up this way, "Our Digital network and The Flying Software Lab allow us to cut software development time and costs across the board. And that's increasing our productivity and ability to compete for similar projects."

To find out how Digital can give you a competitive edge, write: Digital Equipment Corporation, 200 Baker Avenue, West Concord, MA 01742. Or call your local Digital sales office.

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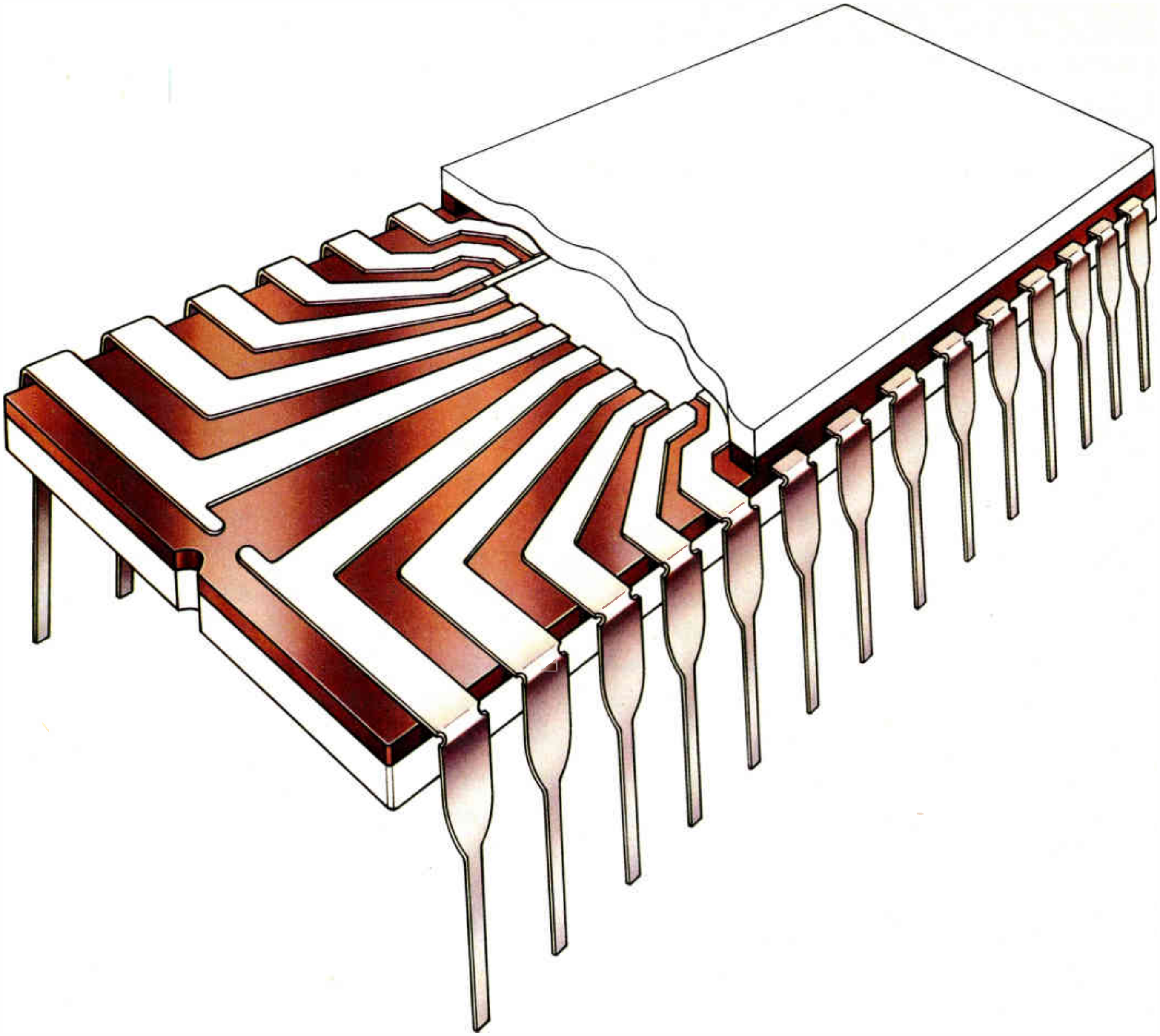

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Hitachi:	6301R, 6301V1, 6301X, 6301Y, 6303R, 6305V, 63705, 6309, 6309E, 64180R0, 64180R1
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Circle 20 on reader service card

ELECTRONICS NEWSLETTER

THE KOREANS ARE COMING! THE KOREANS ARE COMING!

Korean chip producers are reaping the reward for the massive expansion in chip-making capacity they made in the mid-1980s, by grabbing large chunks of the world chip market. The Korean growth is coming fast, and it's mostly at the expense of the Japanese. The biggest part of the Korean expansion was in dynamic random-access memory capacity, where the Japanese have led. South Korea will sell about $400 million worth of DRAMs in the U. S. this year—four times last year's total, estimates William J. McLean, a market researcher with Integrated Circuit Engineering Corp., Scottsdale, Ariz. It's poetic justice, says Dan Hutcheson, executive vice president of VLSI Research Inc., a San Jose, Calif., semiconductor equipment consultant: "The Koreans are doing the same thing to Japan that the Japanese did to the U. S. 10 years ago." South Korean giants Samsung Electronics Co. and Hyundai Electronics Co. invested heavily in new fabrication equipment in 1985 and 1986 when U. S. and Japanese chip makers were cutting back, he says. □

CAN A STANDARD UNIX EMERGE FROM THE TUG-OF-WAR BETWEEN POSIX AND AT&T?

The drive for a standard, open Unix is gaining steam. By the end of the year, the IEEE's Posix Open Systems Environment Committee—which held its first meeting just last month—expects to have draft guidelines published on a variety of key issues including languages, networking, relational data bases, and user interfaces. That's an ambitious goal, says committee co-chairman Kevin Lewis of Digital Equipment Corp., but one that needs to be met. The Unix user community is demanding action, he says, and there are lingering fears that the alliance between AT&T Co. and Sun Microsystems Corp. will make Unix more proprietary and less universal [*Electronics*, Jan. 21, 1988, p. 33]. Sun and AT&T added to the worry with the mid-April introduction of Open Look—a graphical user interface for Unix System V-based computers. □

TANDY CHALLENGES THOMSON IN RACE TO MARKET ERASABLE CD SYSTEMS

Tandy Corp. will challenge Thomson CSF to be the first to market with an erasable/recordable compact disk system. The Ft. Worth company announced plans for THOR—Tandy High-density Optical Recording system—late in April. TI says its first products—audio/video systems for the consumer market—will cost under $500 and should hit Radio Shack stores in time for the 1990 Christmas rush. The technology's key is a secret coating material on which Tandy has six patents pending, but it won't disclose what's special about the material. Thomson's Consumer R&D Laboratory in Villingen, West Germany, has developed a competing system [*Electronics*, March 17, 1988, p. 42], but won't say when it plans to offer products. □

NETWORK SYSTEMS READIES AN OPEN NETWORK ARCHITECTURE

Look for Network Systems Corp. to make a splash in May when it announces a new network architecture that is media- and protocol-independent. The Hyperchannel DX product line will be built around a central adapter, based on Motorola Inc.'s 68020 chip and equipped with 1 to 16 Mbytes of memory, that will handle processing for a variety of standard protocols, input/output buffering, diagnostics, and network management. Hyperchannel DX will work initially at speeds up to 100 Mbits/s—twice as fast as the Minneapolis company's 11-year-old Hyperchannel line. The system will accommodate the emerging 100-Mbit/s Fiber-optic Distributed Data Interface standard, and will eventually handle higher speeds. Hyperchannel DX will work with systems equipped with direct-memory-access channels. □

ELECTRONICS NEWSLETTER

IT'S HITACHI VS. HP AND SONY IN A BATTLE OF DIGITAL AUDIO TAPE FORMATS

The first products using digital audio tape technology for computer data storage will reach U. S. shores late this year—and they will arrive amid almost as much controversy as audio DAT players did last year. This time the debate is over formats, says Dennis Waid, an analyst with Peripheral Strategies Inc., a Santa Barbara, Calif., data-storage consultant. The fight pits Hitachi Ltd. against the team of Sony Corp. and Hewlett-Packard Co. Waid says Hitachi got a boost in March when 33 companies chose to use its format as a working document, even though the HP/Sony format offers higher density and faster data transfers. The company's ace in the hole is that it's promising to offer its format free of charge, while HP and Sony are seeking a large licensing fee. Hitachi's prototype is a 1-gigabyte cartridge that transfers data at 133 Kbytes/s; HP and Sony counter with a 1.3-gigabyte unit with a 180-Kbyte/s transfer rate. □

WESTINGHOUSE DEVELOPS A SOLID-STATE REPLACEMENT FOR LASER PRINT ENGINES

Westinghouse Electric Corp. says it's got a low-cost, all-solid-state replacement for the lasers used in today's high-performance, nonimpact printers. By turning electroluminescent thin film on its side, and taking light from the film's edge rather than from its face, scientists at the Westinghouse Research and Development Center in Pittsburgh have refined a high-brightness light source to replace lasers in some applications. Unlike lasers, printer-image bars made from linear arrays of the thin-film emitters require no scanning mirrors or other moving parts. Now Westinghouse is searching for partners to commercialize the technology. Prototype systems are printing 10 pages a minute at a resolution of 400 dots/in., but scientists say 1,000 dots/in. and 20 ppm are within easy reach. □

HAPPY DAYS WILL CONTINUE FOR CHIP MAKERS, PREDICTS TI

The semiconductor industry can expect its recovery to continue through 1988, says Texas Instruments Inc. Dallas-based TI expects the U. S. chip market to grow by 20% to $12.4 billion in 1988, based on the strongest demand for electronic systems in four years. TI predicts worldwide sales will grow 25% for the year to $40.5 billion, and also disclosed its own plans to boost spending on research and development and related capital equipment. TI will hike 1988 capital expenditures to $600 million, up from $450 million in 1987, with the bulk going to semiconductor and defense-equipment plants. TI's R&D totals will grow $32 million to $460 million this year, mostly for advanced semiconductors and new products. □

PHOTONIC ICs: HERE COME THE FIRST FRUITS OF A U. S.-JAPANESE STARTUP

Photonic Integration Research Inc., a joint venture recently formed by Japan's NTT Corp., Mitsubishi Corp., and the Battelle Memorial Institute, is getting ready to market its first product—a family of photonic integrated circuits. The devices are initially aimed at applications in telecommunications, including local-area network and Fiber-optic Distributed Data Interface communications, broadcast and cable TV, intracomputer links, automobiles, airplanes, and telemetry. The Columbus, Ohio, company's technology uses a thin layer of silica—the material that optical fiber is made from—deposited onto a silicon substrate. Waveguide patterns are then put down on the silica using conventional photolithography and etching techniques. The first devices, which will be limited in scope, could be called very-small-scale ICs. Among them are optical branching circuits, directional couplers, multiplexers and demultiplexers, and optical-gate matrix switches. □

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PRODUCTS NEWSLETTER

TOSHIBA'S 3½-IN. DRIVE STORES 4 MBYTES—FOUR TIMES THE COMPETITION'S

Floppy-disk memory capacities in the 3½-in. format are making a fourfold leap over the standard 1-Mbyte (unformatted) systems now that Toshiba Corp. has released its PD-210 drive. Besides an unformatted capacity of 4 Mbytes, the new system features compatibility with current 1-Mbyte 3½-in. systems—something the Tokyo company's first 4-Mbyte, 3½-in. system lacked. Toshiba achieved compatibility by incorporating two logic chips and one gate array to control read/write and erase of both 1-Mbyte and 4-Mbyte disks, and by using an extra wide-gap erase head for the 1-Mbyte mode. The PD-210 employs a perpendicular recording method, which enables it to record more than double the capacity on a barium ferrite-based coated-type floppy disk. Using IBM Corp.'s PC format, it provides 2.95 Mbytes formatted capacity in 4-Mbyte mode and 737 Kbytes in 1-Mbyte mode. It weighs 430 g and measures 102 by 25 by 150 mm. Samples are available now, for $320. □

SIEMENS' CMOS POWER IC DISSIPATES 10% THE POWER OF BIPOLAR PARTS

A CMOS power-supply chip from Siemens AG gives designers of telephones and Integrated Services Digital Network equipment 10 to 15 times better power dissipation than the bipolar supply circuits it replaces. The PSB2120P consumes less than 10 mW in operating mode. Designed as a pulse-width modulator, it boasts an efficiency of 85%, and its low consumption makes it suitable for line-powered terminals requiring a stabilized supply. It can also be used in ISDN terminals, priority terminals—which remain operational even under emergency conditions—and for network terminations for 60 V. Samples of the PSB2120P are available now from the Munich company. In quantities of up to 1,000 pieces, the price is around $3.50 each. □

DEC'S VAX 6200 GOES HEAD-TO-HEAD WITH IBM'S 4300 FAMILY

Taking dead aim at IBM Corp.'s 4300 computers, Digital Equipment Corp. has introduced four new systems, a new version of its VMS operating system, and a Fortran compiler that gives the VAX a strong multiprocessing ability. The VAX 6200 series is priced from $131,600 to $653,200, features a CMOS central processor, and comes in configurations of up to four central processing units. Performance ranges from 2.8 times the VAX 11/780 for the single-processor system to 11 times for the four-processor model. The Maynard, Mass., company says the series provides performance similar to the IBM 4381 at prices comparable to the lower-priced 9370. The hardware is available immediately. VMS Version 5, a symmetric multiprocessing operating system that enables all processors to work on a task, is priced at about $900 for the VAXstation II and will be ready this summer. Early summer is also the target for the VAX Fortran compiler, which enables parallel multiprocessing by allowing programmers to share execution of a single program among several processors. Compiler licenses are priced from $780. □

PLANAR BOOSTS EL DISPLAY BRIGHTNESS 50%

Planar Systems Inc. has boosted the brightness of its electroluminescent flat-panel displays—already the brightest—by 50%, to 30 foot-lamberts. The Beaverton, Ore., company's improved design and manufacturing technologies have also reduced power consumption of the EL panels by an average of 30%. The EL8358HR 640-by-400-pixel display, for example, previously used at 22 W and now uses 10 W. Also, the specifications for luminence reduction over time have been improved from an expected 30% reduction in 10,000 hrs. to only a 10% reduction. The panels offer contrast ratios of 20:1. They are available now at the same price as existing products. □

PRODUCTS NEWSLETTER

MASSCOMP'S UNIX SYSTEMS RUN MATH FOUR TIMES FASTER

MassComp Corp.'s real-time, Unix-based 6000 family of computers performs scalar operations more than twice as fast as competing Hewlett-Packard Co. systems and betters the HP machines at floating-point operations by 4 : 1. That translates into 10 milion instructions/s, 15 million Whetstones/s, or about 3 million floating-point instructions/s for a single-board version that sells for about $9,000. Based on Motorola Inc.'s 68030 microprocessor, the family runs RTU, MassComp's real-time version of Unix. The highest-performance entry from the Westford, Mass., company is the MC6700, which ranges in price from $59,000 to $120,000 and supports up to five central processing units, each of which has a floating-point coprocessor and optional floating-point accelerator. Using four vector accelerators, the MC6700 operates at up to 56 megaflops. The systems will be available in June. □

TEKTRONIX LOGIC ANALYZER GIVES USERS A WIDER CHOICE OF CHANNELS

Modularity is the key feature of Tektronix Inc.'s latest logic analyzer, the model 1230. Instead of having to opt for either a 32- or an 80-channel box—as offered by the competition—users can configure the 1230 in 16-channel increments up to 64 channels. Besides modularity, the Tektronix unit offers four time bases for simultaneously observing data from different parts of a system, a feature usually found only in expensive analyzers. The time bases allow the user to inspect data from different nodes in the system under test by clocking the signals from each node individually. The 1230 also comes with four memories of 2 Kbytes each for every channel to help ferret out problems in more complex system architectures. Pricing begins at $2,795 for the 16-channel version and goes to $6,395 for the largest configuration. All will be available within four weeks of order. □

EESOF'S TOOL KIT HELPS SOLVE THE RIDDLES OF MMIC

A software/work-station package from Eesof Inc. provides a set of integrated computer-aided-engineering tools for designing chips for the Department of Defense's Microwave and Millimeter-wave Integrated Circuit program. The MMIC Design Workstation is the first such computer-aided-design package in the industry, according to the Westlake, Calif., company. It runs on either Apollo Computer Co.'s DN 3000/4000 or Sun Microsystems Inc.'s Sun 3 platforms. The design station performs schematic capture, linear and nonlinear simulation, full-custom layout, and design verification. Other key featues include seamless work flow between programs, powerful multitasking capabilities, and a consistent user interface, says the company. Pricing for the MMIC Design Workstation starts at $35,000 for a basic system, and goes up to $150,000. It will become available in June. □

PLUS DEVELOPMENT'S DETACHABLE WINCHESTERS HANDLE PC AT BUS AND MICRO CHANNEL

Plus Development Corp.'s removable 3½-in. Winchester disk drives for IBM Corp. Personal Computers, PS/2s, and compatibles let users take just their data with them and leave the keyboard, display terminal, and computer behind. The Milpitas, Calif., company's Plus Passport 20- and 40-Mbyte drives feature host adapters for the IBM PC AT bus and Micro Channel, and a housing that inserts into a 5¼-in. half-height bay on PC/XT, AT, PS/2, or compatibles. The Passport boasts an effective access time of 28 ms and can copy 40-Mbytes in less than 5 min. Passport is scheduled to ship in June, with suggested retail prices of $1,250 for a complete 20-Mbyte system and $1,450 for a 40-Mbyte version. Extra removable hard disks are priced at $595 for 20 Mbytes and $795 for 40 Mbytes. □

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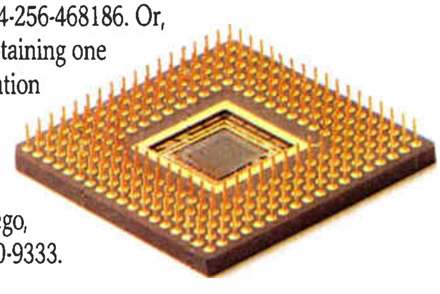

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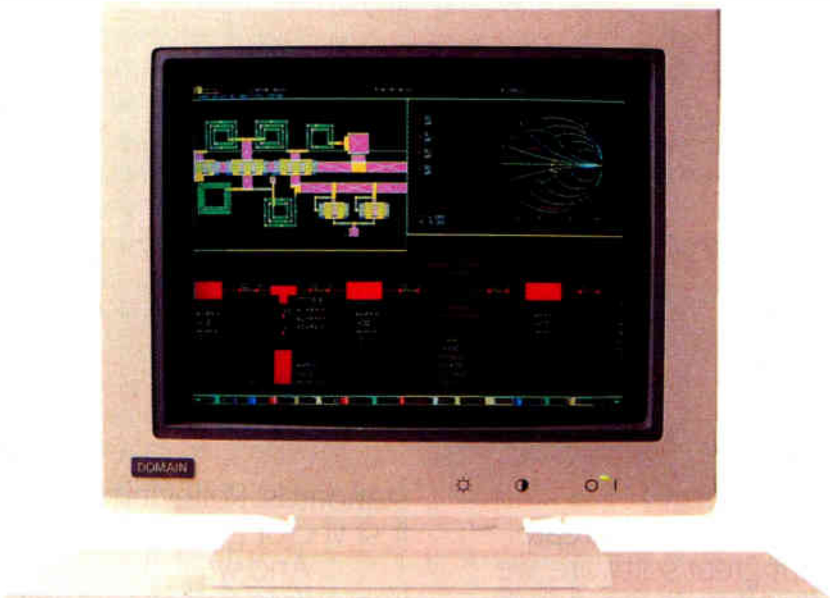

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Electronics

APPLIED MATERIALS BETS ON MAGNETICS AS THE WAY TO MAKE ULTRA-LARGE-SCALE ICs

Market leader's backing could tip the scales in favor of the technique

SANTA CLARA, CALIF.

The 64-Mbit dynamic random-access memory and other ultra-large-scale integrated circuits are still a decade and two generations of products away, but process engineers now have to start making the hard decisions on how to build them. A debate is starting to heat up on the role of magnetics and dry etch in the submicron process. Proponents say it's the best method to shape and smooth the deep trenches and holes needed for such chips; opponents say magnets are overrated. What will do it, they say, are dramatic breakthroughs in chemical etching. Now the market leader in dry-etch manufacturing equipment, Applied Materials Inc. of Santa Clara, Calif., is putting its considerable weight behind this technique.

Applied Materials cast its vote on April 27 when it introduced a multiple-chamber electromagnetically enhanced plasma system. Called the Precision 5000 Etch, the equipment marries low-pressure reactive-ion technology to a unique electromagnetic system; this system, say company officials, enhances plasma properties at wafer surfaces for smooth sides in deep holes and fine-line trenches. Such profiles are necessary for advanced three-dimensional circuits.

Using single-crystal wafers, the system has etched trenches with rounded bottoms and 21:1 aspect ratios: 0.2-μm wide by 4.2-μm deep. That feat should allow the industry to make 64-Mbit dynamic RAMs and dense logic chips well into the next century. The system is initially aimed at filling two key applications: excavating small, deep holes for posthole storage capacitors in DRAMs, and grooving fine-line trenches to isolate adjacent devices on dense bipolar or biCMOS chips.

TOUGH TEST. "We have it characterized on what we think is the toughest application that the industry has been able to throw at us," says Peter R. Hanley, vice president of Applied Material's Etch Products Division in Santa Clara.

Analysts believe Applied Material's market prowess in dry etch can swing confidence behind the technique as a way to control plasma ionization and dissociation efficiencies. Backers of magnetically enhanced plasma systems say wafer-etch rates jump dramatically and dc bias voltages can be reduced to lower the risk of damage to silicon crystals from ion bombardment. Higher grade material can result in faster circuits.

Skeptics at such companies as Texas Instruments Inc. in Dallas downplay the advantages, though. There, dry-etch researchers contend that magnets can't cut the mustard; passivation chemistry is the only way to get smooth sidewalls and rounded bottoms for vertical integration and trench isolation in advanced circuits.

The skeptics may be fighting a losing battle. Managers at Applied Materials report the benefits of magnetics on plasma discharges have been demonstrated simply by switching the feature off. In addition, Applied Materials has seen etch rates increase by a half to one order of magnitude with the electromagnets switched on.

At the same time, other U. S. equipment makers are starting to bank more heavily on magnetically enhanced ion-etch concepts. Materials Research Corp. of Orangeburg, N. Y., has been pioneering the use of magnetrons in dry etch, and introduced a prototyping system for process labs in 1983. The company says it no longer is dealing with labs and is now shipping its Aires production systems, mostly to Japanese-based chip makers.

Unlike Applied Materials, Materials Research is promoting magnetics as only a method of boosting the etch rates of its low-pressure equipment to the levels that are typically seen in high-pressure plasma gear. The magnetron is used to raise etch rates nearly 100 times by raising the density of the reactive species—the ions—in low-pressure plasma.

Soon to join the movement is Tegal Corp., a subsidiary of Motorola Inc. in Novato, Calif., which plans to move its magnetically enhanced plasma work from the lab to market next year. "Because the magnetic technology is still in the development stage, there is controversy about exactly how much good it does and what it does," concedes Elliott Philofsky, president. "But the level of activity in the industry indicates that it does offer some advantages."

The trench, with its 21 : 1 aspect ratio, in 0.2-by-4.2-μm, is etched into single-crystal silicon.

For its part, Applied Materials has gone the electromagnetics route in the 5000 Etch to create a volumetric field at the wafer surface. This magnetic field is rotated slowly by the system's controllers to produce uniform vectors. While the vectors change direction in the process, the scalar value of the field remains constant over the whole plasma discharge. The system has also been designed for multiple wafer-processing chambers that can run up to four wafers in parallel for high throughputs, and uses low-pressure reactive-ion etch, known as RIE (under 100 milliTorr) for anisotropic etching to achieve tight control of uniformity and critical dimensions.

Applied Materials has shipped 10 systems to silicon-processing laboratories in the U. S., Europe, and Japan. Costing $800,000 to $1.3 million, the 5000 Etch is considered to be so advanced that it is not likely to be deployed for volume production until the mid-1990s. *–J. Robert Lineback*

WHY DG IS TEAMING WITH MOTOROLA ON RISC

NEW YORK

The dust had barely settled last week after Motorola Inc. announced its CMOS MC88000 reduced-instruction-set-computer microprocessor (see p. 75) when it dropped another bombshell: the chip maker has teamed with Data General Corp. to jointly develop an ultra-high-speed version of the 88000 implemented in emitter-coupled logic.

The deal is a coup for Data General. The Westboro, Mass., company beat its rivals to the punch simply by volunteering to design the five-chip ECL set, which is intended to operate at more than 100 million instructions/s in a single-processor configuration. (The initial CMOS 88000 is rated at 14 to 17 mips). It was an offer Motorola was more than happy to accept, given Data General's ECL expertise.

KEY TO STRATEGY. Data General regards the 88000 family as a crucial ingredient in its important transition from a solely proprietary computer architecture to Unix-based industry-standard platforms for the 1990s. "The 88000 is a key to our future strategy," says Thomas West, vice president in Data General's System Development Division. That's why Data General has joined the 88open consortium, the group of companies supporting and promoting the 88000 [*Electronics*, April 14, 1988, p. 31]. "We want a union—a consortium—that is big enough to appeal to all the suppliers of shrink-wrapped applications software."

Data General has evaluated all available RISC microprocessors "and even built a few of our own to see how fast they'd run in a system," West says. "But we saw that the merchant semiconductor manufacturers were on a fast track. Motorola had built hundreds of thousands of 68000s, so we decided to go with them." The CMOS 88000 will probably debut in Data General systems in a year or more.

The ECL chips defined to date are an instruction-set processor, including the floating-point function; a memory-management unit; a cache controller; a system controller that may incorporate the system timing; and a system bus-interface device. The ECL design team "has been in place for some time and the design is well under way," says West. And Data General is no neophyte in ECL design. "We've designed more than 30 Motorola-built ECL gate arrays that are shipping in our MV supermini line," he adds.

Motorola holds the basic patents on ECL and has been the leading producer and advocate of the high-speed bipolar logic since the 1960s. It's significant that the semiconductor giant would yield to any other company to design such a prestigious product. Jeff Nutt, technical marketing manager for the Motorola Microprocessor Products Group, says Data General was selected because of its ECL design experience and because the company volunteered to do the job.

"They got so excited about the ECL 88000 that they offered to assist us by using their [design] resources," Nutt says. "This development is very important to their future," he adds.

Thomas West, Data General's vice president, says, "The 88000 is a key to our strategy."

The ECL 88000 design will initially be aimed at applications in superminicomputer, mainframe, and supercomputer systems, Data General says. "Running memories fast enough to keep up with a 100-mips processor is a problem that has to be addressed," West says. "We have to think about all aspects of the design in terms of their impact on the system, and that's where we're strong."

For Motorola, say industry watchers, the arrangement kicks a hole in its competitors' sales pitches. Both Sun Microsystems Inc., creator of Sparc, and MIPS Computer Systems Inc., which offers the R3000, have been harping on the fact that their RISC microprocessors are the products of system designers. Motorola can now say the same thing.

SECOND-SOURCING. But that's only part of it, says Alice Leeper, senior industry analyst in Dataquest Inc.'s semiconductor industry service in San Jose, Calif. Along with the systems issue, she says, "Sun and MIPS had made second-sourcing important in the RISC business. Perhaps this move will also put to bed the second-sourcing question, because it shows that Motorola is open about sourcing. They can make a plausible case that Data General has the capability to be a foundry." Data General has a plant for semiconductor prototyping in Sunnyvale, Calif.

This teaming isn't the first time the Motorola microprocessor group and a customer have joined in device development. "We've had joint relationships before but not disclosed them," Nutt says. Neither company is ready at this point to provide extensive details about device density, performance, or process technology. West says he understands that two of the chips—probably the instruction processor and MMU—will be fabricated in a new process technology, with the others to be done in Motorola's Mosaic III ECL 10K process.

Motorola will fabricate the ECL 88000 chips in Phoenix, with first silicon expected sometime in 1991. It will sell the ECL version worldwide the way it is going to sell any 88000 part: through its Microprocessor Products Group in Austin, Texas. *–Lawrence Curran*

MICROCONTROLLERS

TI MAKES ANOTHER STAB AT 8-BIT MICROCONTROLLERS

NEW YORK

Texas Instruments Inc. yielded the bulk of the 8-bit microcontroller market to Intel Corp. and Motorola Inc. over the last decade or so through a series of marketing blunders. Now it is storming back with a new product line, a new strategy, and a new goal.

The Dallas-based chip maker's new family of programmable controllers, called TMS370, was commissioned by Delco Electronics in 1985. It includes six standard parts, but TI is hoping to capitalize on more than just a standard product line. Rather, the company is pushing a sort of application-specific capability built around product flexibility and premium performance—and aiming it at the high end of the market. The goal is for TI to be one of the top two 8-bit controller suppliers by 1994.

TI likes the market potential. "Most of

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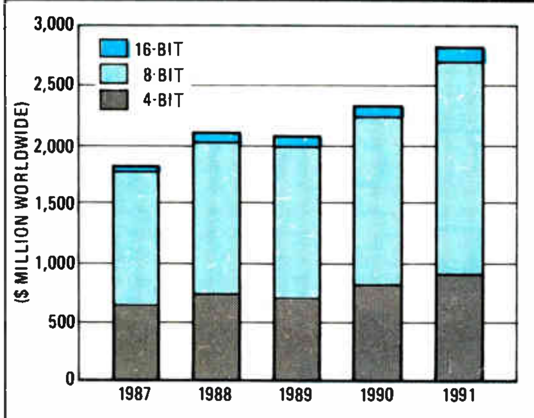

SOURCE: DATAQUEST INC.

the market will remain 8-bit," says Mike Polen, microcontroller marketing manager in Houston. According to figures from Dataquest Inc., the San Jose, Calif., market researcher, 8-bit parts made up 64% of the $1.8 billion worldwide microcontroller market in 1987, and will account for 65% of a $3.1 billion market in 1992 (see figure). "That's where the business is," Polen says.

And within the 8-bit market, the growth is at the high end, adds Willie Fitzgerald, another TI marketing manager. TI estimates that the premium 8-bit market, now dominated by Motorola's 68HC11, will be worth about $56 million in 1988, roughly 4% of the total 8-bit market. TI projects that figure to grow to about $475 million by 1992, or 23% of the total 8-bit market.

The 370 is TI's second shot at regaining a share of the market it once dominated. Trying to leapfrog the competition, TI tried to play off its early lead in 4-bit controllers by offering a 16-bit device while others were just getting to 8 bits. When the market didn't respond, TI withdrew the product and introduced the TMS7000, which though still offered, has not won a major following.

Now TI figures to lure this business with performance and flexibility. Fitzgerald says the TMS370's register-to-register architecture is about 20% faster than the HC11's, which uses an accumulator-based design that requires it to process more instructions to do a task. And in terms of flexibility, Fitzgerald says TI will customize a 370 on orders as small as 50,000 units.

DIFFERENT SIZES. TI's family includes modules offering different sizes of read-only memory—in mask-programmable, electrically programmable, and electrically erasable programmable technologies—as well as up to 512 bytes of random-access memory, two serial interfaces, two timers, an expansion bus, and an analog-to-digital converter. In all, there are 16 modules to go along with the core processor.

TI's strategy—to use a high-performance core developed for Delco's audio systems, heating, ventilation, and air-conditioning division in Kokomo, Ind., and build a standard-cell environment around it—is remarkably similar to that of rival Motorola and its HC11, which in 1987 took 1.5% of the 8-bit controller market.

At Motorola's Microcontroller Division, Austin, Texas, marketing manager Steven Marsh claims he's been offering that environment for over a year with the HC11, which was also developed in conjunction with Delco. "We have a chassis that's easily modifiable," he says, plus 10 standard parts, compared with TI's current family of six.

Both companies claim comparable turnaround time for a custom configuration, and both say they have all the development and emulation tools needed to start designing a specially configured part into a system before that part actually exists. TI is hoping that higher density memories, made possible in part by a 1.6-μm CMOS manufacturing process, will be its drawing card.

Motorola's Marsh says the HC11 can be configured with up to 1 Kbyte of RAM, 12 Kbytes of ROM, and 2 Kbytes of EEPROM. And although TI's 370 has less RAM—just 512 bytes maximum—it offers up to 16 Kbytes of standard ROM, 16 Kbytes of EPROM, or 4 Kbytes of EEPROM. Having more EEPROM capacity could be key for TI, as both companies go to great lengths to describe not only the value of EEPROM—it's particularly useful in prototyping, when algorithms may need to be repeatedly changed—but also the difficulty each had in incorporating the technology into an otherwise standard CMOS process. *–Tobias Naegele*

MILITARY

THE PENTAGON WILL SETTLE FOR NOT-SO-SUPER VHSIC SUPERCHIP

REDONDO BEACH, CALIF.

Superchip never made it out of the phone booth. The chip, the flagship part in Phase 2 of the Pentagon's Very High Speed Integrated Circuit program, would have been one of the most complex devices ever built [*Electronics*, July 10, 1986, p. 49], packing 28 million transistors in a 1.4-in.^{2} area. But processing problems encountered by TRW Inc. and Motorola Inc. have forced them to lower the sights of their ambitious and closely watched program.

Replacing it is a considerably scaled-down version, called the CPUAX. Essentially consisting of the smaller central-processing unit at the heart of the superchip, the new version does manage to incorporate what is probably the most exciting feature of the original chip: a form of on-chip redundancy that makes it self-correcting.

The changes have been approved by the two firms' customer, the VHSIC program office in the Department of Defense, which revealed the problems and solution in some detail in its just-released 1987 annual report. The report also says that despite the delay, chips should be ready late this year in time for a brassboard module to be working in September 1989, roughly on track with original scheduling.

The chip's fabrication woes stem from subpar performance of the Aeble-150 electron-beam lithography machine, say the companies and the VHSIC report. This e-beam unit, supplied by Perkin-Elmer Corp., was to play a key role in fabrication of patterns in the 0.5-μm CMOS process required to build the devices. Not only was the Aeble-150 about a year late in delivery in late 1986, which wiped out the planned experimentation and testing period, but also its accuracy did not meet the submicron specifications developed to fabricate the key overlay pattern levels. Motorola's Austin, Texas, plant is responsible for the CMOS development.

The most critical failure "was in patterning the isolation trenches between the individual devices on the chip, which led to excessive current leakage," says Thomas A. Zimmerman, manager of VHSIC programs at TRW's Electronic Systems Group in Redondo Beach. The VHSIC 2 team had chosen the trench-isolation technique because it was "thought to be very proven, and could work at the submicron level," he says.

TOO SOON. But others in the business "warned [that] we would find surprises," says Zimmerman, and they proved prophetic. Among those skeptical about trench isolation was one engineer at a company that was a VHSIC Phase 1 participant. The engineer, who declines to be identified, says, "By trying to insert trench isolation into a VHSIC design, they were trying to run before they could walk." In a survey done after the fact, TRW and Motorola found no successful examples of repeatable submicron trench isolation fabrication, says Zimmerman.

To replace it, Motorola's Semiconductor Products Sector in Phoenix, Ariz.,

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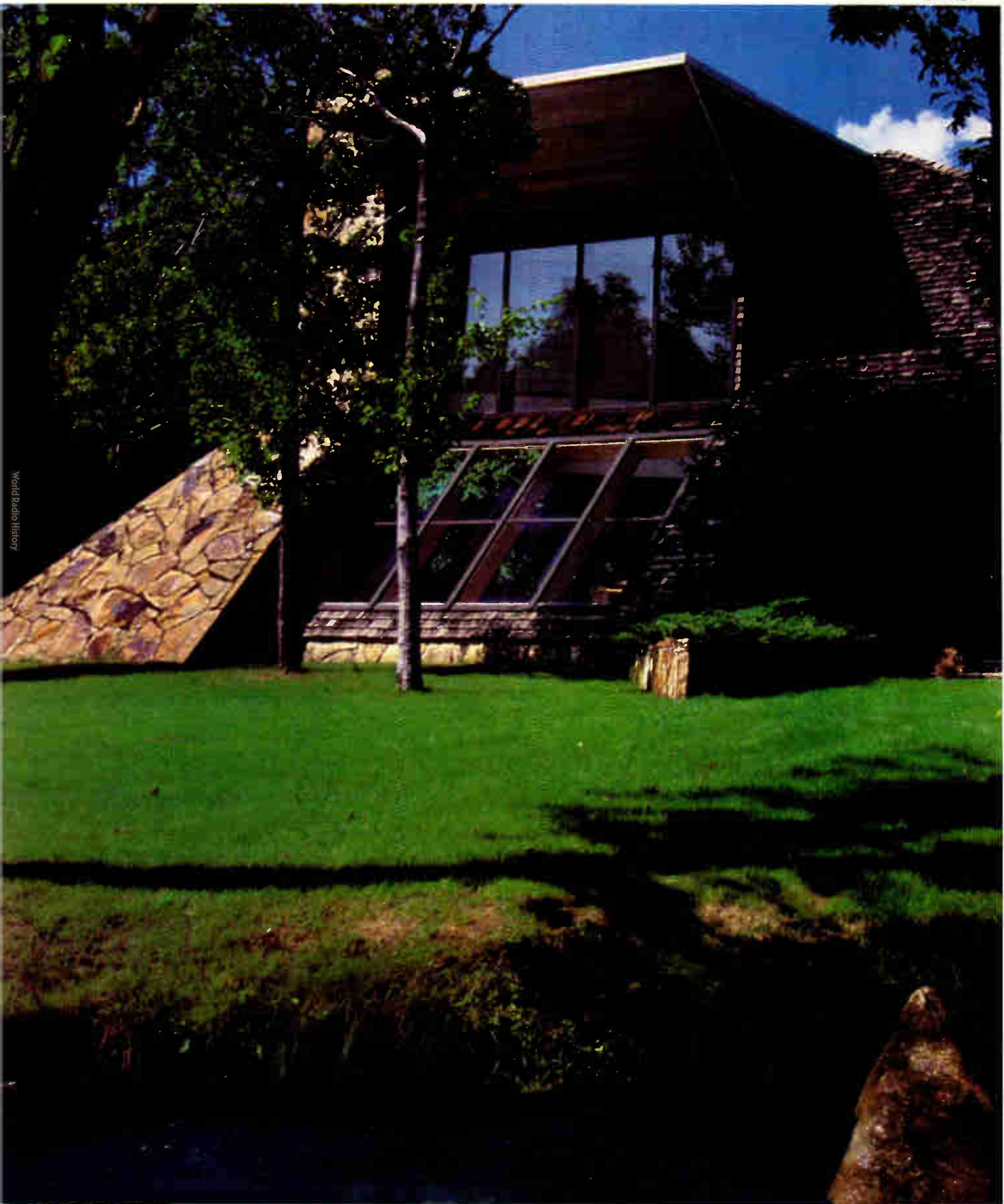

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chose Locos (for localized oxidation of silicon), an isolation process that works well in small geometries and uses advanced but tried-and-true optical lithography instead of e-beam. But the tradeoff sacrifices the density envisaged with trench isolation—the oxidation process used in Locos tends to cover line walls and make them wider than the backfilling procedure used in trench isolation.

This density tradeoff, says the VHSIC report, "jeopardized the probability of yielding a superchip" on 4-in. wafers since not enough time remains to redesign and test the 29 types of macrocells it requires. Instead, eight macrocell types have been resized with Locos for the CPUAX. The new chip has about 150 macrocells, containing nearly 4 million transistors, with 64 macrocells active at one time and the remainder available as backup. It measures 1.3 in. by 1 in., dissipates 10 W, and is designed to perform 200 million floating-point operations/s, about the same as the superchip. But it uses off-chip memory.

Although TRW and Motorola engineers are disappointed in not completing the ambitious superchip as planned, outsiders point out that the CPUAX appears to be more of a general-purpose device, with wider potential than the specialized superchip. *–Larry Waller*

GALLIUM ARSENIDE

THE UK's JOINT GaAs EFFORT MAY NOT FLY

LONDON

Plessey Ltd. is sitting in the eye of a storm of controversy over the future of the fabrication of gallium arsenide integrated circuits in the UK. The row revolves around the British government's attempts to encourage Plessey and General Electric Co. plc to collaborate on a GaAs IC foundry. The affair could shoot down the government's plan, leaving Plessey the only GaAs producer in Britain.

The flap started after the Department of Trade and Industry decided that it should promote GaAs IC development in the UK with cash: about $46 million. The idea was to build a facility jointly operated by Plessey and GEC.

But figuring it has little to gain, Plessey now says says it does not want to participate. The firm claims that it was asked only to take part in a feasibility study for the project, and withdrew because it believes the project is commercially unviable. The move forced GEC to let go 60 of the 100 engineers working on GaAs at its Hirst Research Centre, and GEC is claiming that Plessey has wrecked the nation's GaAs chances.

For its part, the government is amazed that industry would refuse money, and annoyed because its offer has apparently been spurned. Besides, a Trade and Industry spokesman says, "The concept came from industry in the first place." To determine what to do, the department will reconvene its Industry Strategy Committee, which came up with the original joint-development plan.

Meanwhile, despite a shower of criticism, Plessey is unrepentant. "Plessey has invested more than [$55 million] in gallium arsenide research, development, and production over the last decade," says Pat McGuire, managing director of the Plessey 3-5 Group Ltd. "We have already built a foundry with sufficient capacity to meet foreseeable demand for GaAs ICs and discrete devices until the mid-1990s." Another UK plant would just lie idle, McGuire adds.

Plessey itself is anything but idle in GaAs. Its foundry opened in 1986 at Towcester, Northamptonshire, just a few miles from Plessey's Alan Clark Research Laboratories at Caswell, where most of its GaAs materials research, process development, and applications work is done. Currently it is being tuned to run Plessey's 18-GHz F2 GaAs process, for which it claims 80% to 90% yields. "Now we are characterizing the process so it can be offered to foundry customers," says McGuire. Standard parts are running through the line, and some specially designed parts have been delivered.

Some years ago, Plessey concluded that there was no future for digital GaAs ICs, and concentrated its efforts on linear circuits. To date it has concentrated on developing a robust production process. Now the company has moved on to the next phase and is working hard to increase the complexity of GaAs linear ICs, and has devised some new component structures such as on-chip electronically adjustable inductors and delay lines based on the polyimide isolation technique it has perfected.

The objective is to reduce size and cost for the IC it sees as providing the high-volume market in the 1990s. This is a transmitter receiver cell for phased-array radar antennas. The radars, now under development, could use up to 1,000 such cells on each of their five faces. Already an earlier design has been reduced in the laboratories from a 12-by-4-by-1-in. module to a ceramic-based hybrid less than 4 by 4 by 0.5 in. Now a fully integrated device is being designed for a module less than 1 by 2 in., with a cost dropping from $1,200 to a few hundred dollars.

McGuire also sees significant civilian markets in the mid-1990s. He says that the low power consumption and low noise of GaAs linear circuits will make the technology ideal for application in handheld cellular and digital mobile telephones and in domestic and mobile satellite terminals. *–Peter Fletcher*

BUSES

CAN ARDENT MAKE ITS BUS A SUPERCOMPUTER STANDARD?

SUNNYVALE, CALIF.

What the world needs is a standard supercomputer bus. At least that's what the people who run Ardent Computer Corp. of Sunnyvale, Calif., believe—and that's what the company is out to supply. And at least one expert thinks Ardent might have the right idea, although there is competition.

The reasoning at Ardent is that the advent of desktop supercomputers such as those from Apollo, Stellar, and Ardent itself makes such a standard necessary. The bus would provide third-party hardware suppliers with a market for add-in boards for use in the high-powered systems, much as VMEbus and Multibus now do for microcomputer systems.

Since Ardent happens to have exactly that kind of bus in its Titan supercom-

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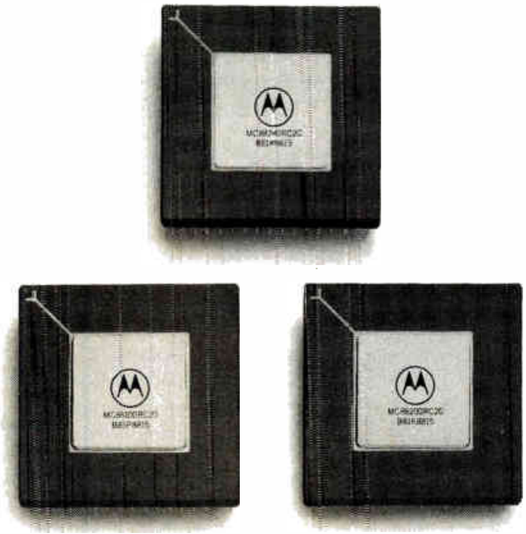

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puter, the next step in turning the bus into a product is to make an offer that no one can refuse. To do that, the company is taking a simple approach: offering the bus at a rock-bottom price. Takers will be able to license the Titan bus's timing and pinout specification, bus-interface circuit schematics, and protocol definition for $250, and buy the

The price is right: $400 to license the bus architecture and buy one required chip

bus-arbitration chip for another $150—a total of just $400. The only additional cost would be incurred if the third-party supplier plans to build a dual data-path bus, for which two bus-arbitration chips are needed.

Steven Blank, vice president of marketing at Ardent, expects the deal to appeal to manufacturers of equipment that requires high I/O-to-memory transfers. These include signal processing, image processing, high-speed networking, and mass storage products.

In making the bus specifications public, Ardent is aggressively pursuing an open-architecture strategy not unlike the one that made Sun Microsystems Inc. successful. In February, for example, Ardent announced it would license its supercomputer graphics software package DORÉ—for Dynamic Object-Rendering Environment—under similar terms [*Electronics*, Feb. 4, 1988, p. 69].

Blank says that his company will submit the Titan bus to the newly formed SuperBus Study Group of the Institute of Electrical and Electronics Engineers for consideration as a base for standard supercomputer buses. Jon Rubinstein, the Titan computer and bus's architect, will be a member of the group.

The Titan architecture has a chance to become a de facto standard, says Paul Sweazey, chairman of the SuperBus group and a system architect at National Semiconductor Corp. in Sunnyvale, Calif. However, he adds, Ardent doesn't have the field to itself—he singles out as a possible competitor the latest Futurebus 896.1 IEEE standard.

The Ardent bus was designed with high-performance parallel processing in mind. With a sustained data-transfer rate of 256 Mbytes/s, "it offers performance 10 times that of a VMEbus," says Blank. "And that's a sustained, not peak, rate."

According to Rubinstein, "The bus is unique in that the third party adding boards to the bus actually gets to use the entire bus bandwidth, because the board can transfer data at the full transfer rate."

In addition, the bus operates with

very low bus overhead, the time required to switch from one bus user to another. In fact, the bus can be handed off every clock cycle. There are no dead cycles in its operation: it is a synchronous, split-transaction, or disconnect bus. That is, one request can go on the bus and another be initiated before the first request is completely serviced.

Another way the bus does away with overhead is that it eliminates the possibility that, say, a processor will tie up the bus because it must wait to use a resource that is already being used. For example, say a processor on the bus wants to use a communications controller. Before the processor gets control of the bus, the controller must be available for use. In addition, to eliminate the possibility of one processor hogging the bus, there is an arbitration mechanism that ensures each processor gets an equal share of the bus bandwidth.

By making a high-performance supercomputer bus available at a reasonable cost, Ardent hopes to build support for its bus architecture at the expense of its competitors Stellar and Apollo. Both companies have a proprietary buses and do not appear to be making them generally available. *–Jonah McLeod*

RESEARCH & DEVELOPMENT

TURF WAR ROILS EUROPE'S VERSION OF SEMATECH

PARIS

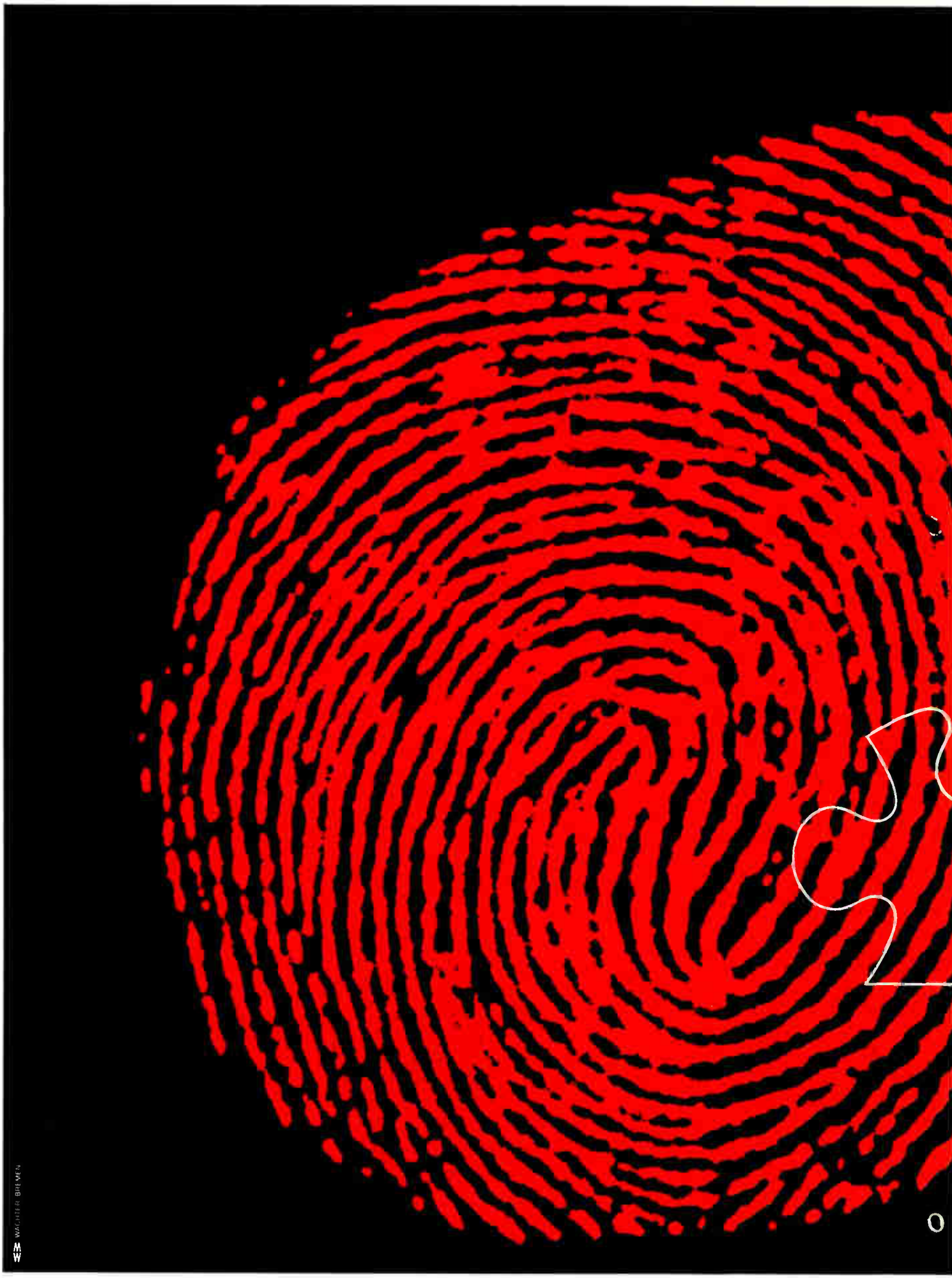
Like many a seemingly sound scheme for international industrial cooperation, the Joint European Submicron Silicon Initiative—Western Europe's potential counterpart of the U. S. Sematech effort—is becoming embroiled in clashes of national self-interest. And if Jessi doesn't jell, European chip makers' chances of standing up to Japanese and U. S. competition in world markets in the years ahead will take another turn for the worse.

West Germany's Siemens AG and Philips of the Netherlands launched Jessi in 1986, aiming to develop a process technology for the submicron features that will mark high-density memory and logic chips in the 1990s. They expect the project eventually will cost about $2 billion.

Now the Franco-Italian chip maker SGS-Thomson Microelectronics wants a full share in the action. But Siemens says no way.

In early April, the Munich firm went public with a statement that SGS-Thomson would be restricted to only a supplementary membership in Jessi. Siemens is working with Philips in a binational effort, known as Mega, to develop 4-Mbit chips; it has an edge on SGS-Thomson in fine-line memory technology. Apparently the company fears that with know-how from Jessi, SGS-Thomson could become a formidable competitor in static and dynamic random-access memories, eating into Siemens' and Philips' market share.

The Siemens pronouncement caused tempers to flare at SGS-Thomson. "If somebody is at risk about sharing technology without getting returns, it is us," snaps Philippe Geyres, SGS-Thomson's corporate vice-president for strategic planning. Noting that SGS-Thomson has supplanted Siemens as Europe's No. 2 integrated-circuit producer (behind Philips), Geyres says that neither the German nor the Dutch company can come close to matching its technology in megabit electrically programmable read-only memories. SGS-Thomson announced a fully working 1-Mbit CMOS EPROM chip with enhanced verification at the 1988 ISSCC conference in San Francisco in February. "Ours is purely



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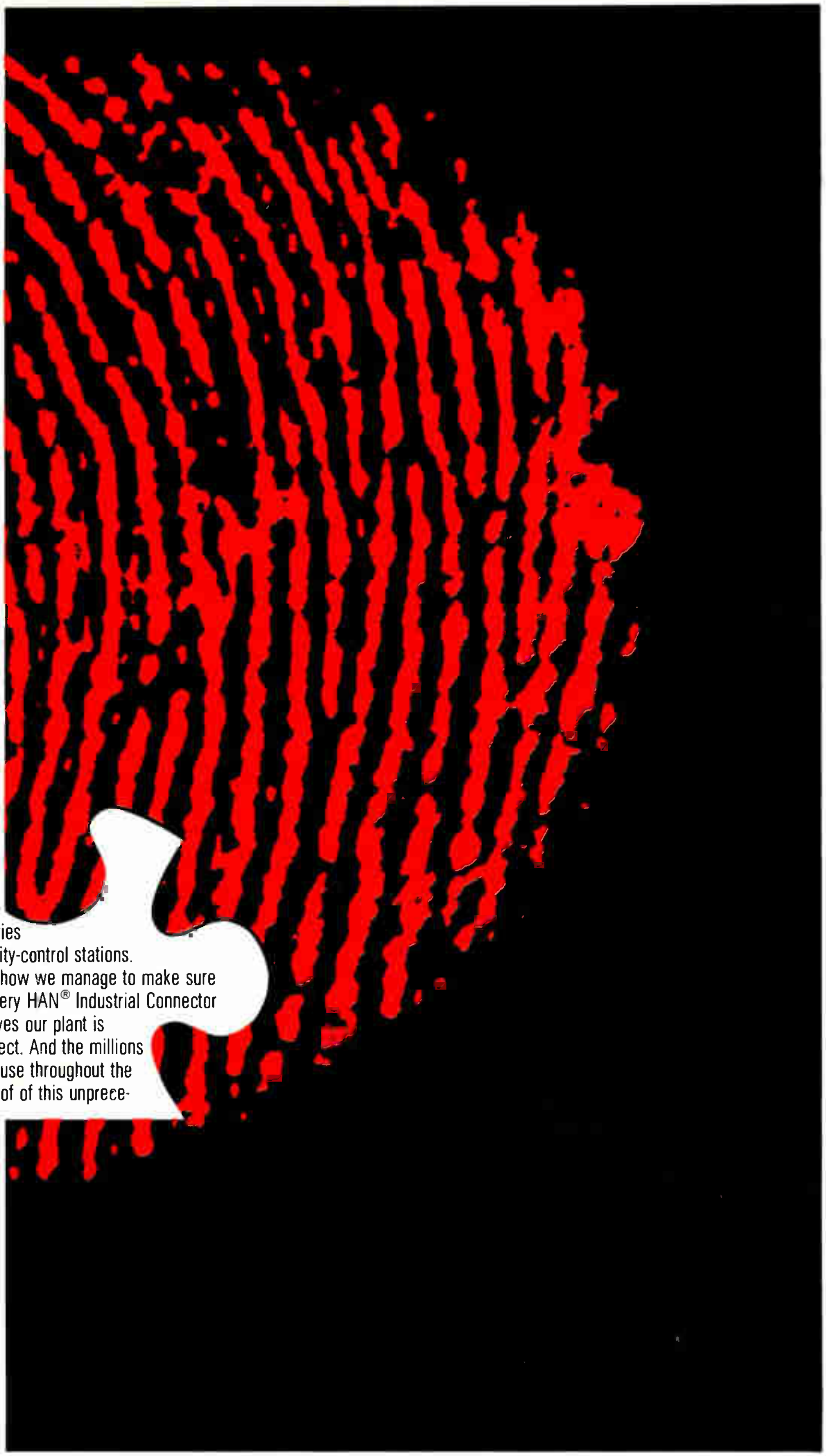

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Circle 45 on reader service card

European technology; we don't buy technology from Toshiba like Siemens did," says Geyres, referring to Siemens' efforts in megabit memories.

But if Siemens keeps SGS-Thomson out of Jessi, the Franco-Italian company may follow Siemens' lead and buy technology from the Japanese, says a former top executive at SGS-Thomson. "If that happens, the whole European Community loses," he comments.

Geyres hasn't indicated that he wants to go that route. "Our position is simple: a European cooperation including all the major companies—Philips, Siemens, SGS-Thomson, and Plessey—is mandatory because we are facing the Japanese challenge and the American challenge," he says. "Semiconductor sales by the No. 1 Japanese company—NEC Corp.—are bigger than Siemens, Philips, and SGS-Thomson put together. So it is evident that we all have to work together for a full European cooperation—and that this cooperation must be on an equal basis between partners."

SGS-Thomson threatens to buy Japanese technology if Siemens bars it from Jessi

To that end, Geyres has been flying back and forth between Germany, France, and Italy trying to make his company's position clear. Earlier, with French government backing, he had publicly threatened to file a complaint to the European Economic Community. But SGS-Thomson now is taking a wait-and-see attitude, preferring to try to smooth things out in private meetings rather than continue slugging it out in the European press.

Complicating the situation is the possibility that coordination of the project might ultimately be taken over by Eureka, the European advanced research program. If Siemens decides to stick by its decision to lock out SGS-Thomson, Eureka could be prevented from playing any role with Jessi. Eureka's guidelines mandate that Siemens and Philips would have to provide details on their planned research program to all 19 member nations (some non-EEC countries have joined Eureka). Interested companies would have the right to ask to join, and if they were refused or not given equal status they would have to be given a valid explanation.

If Siemens and Philips keep it to themselves, Jessi would most certainly end up with a much narrower focus than originally intended. Catching up with the Japanese leaders is likely to continue being an uphill, nearly impossible struggle for the Europeans for a long time to come. *–Jennifer Schenker*

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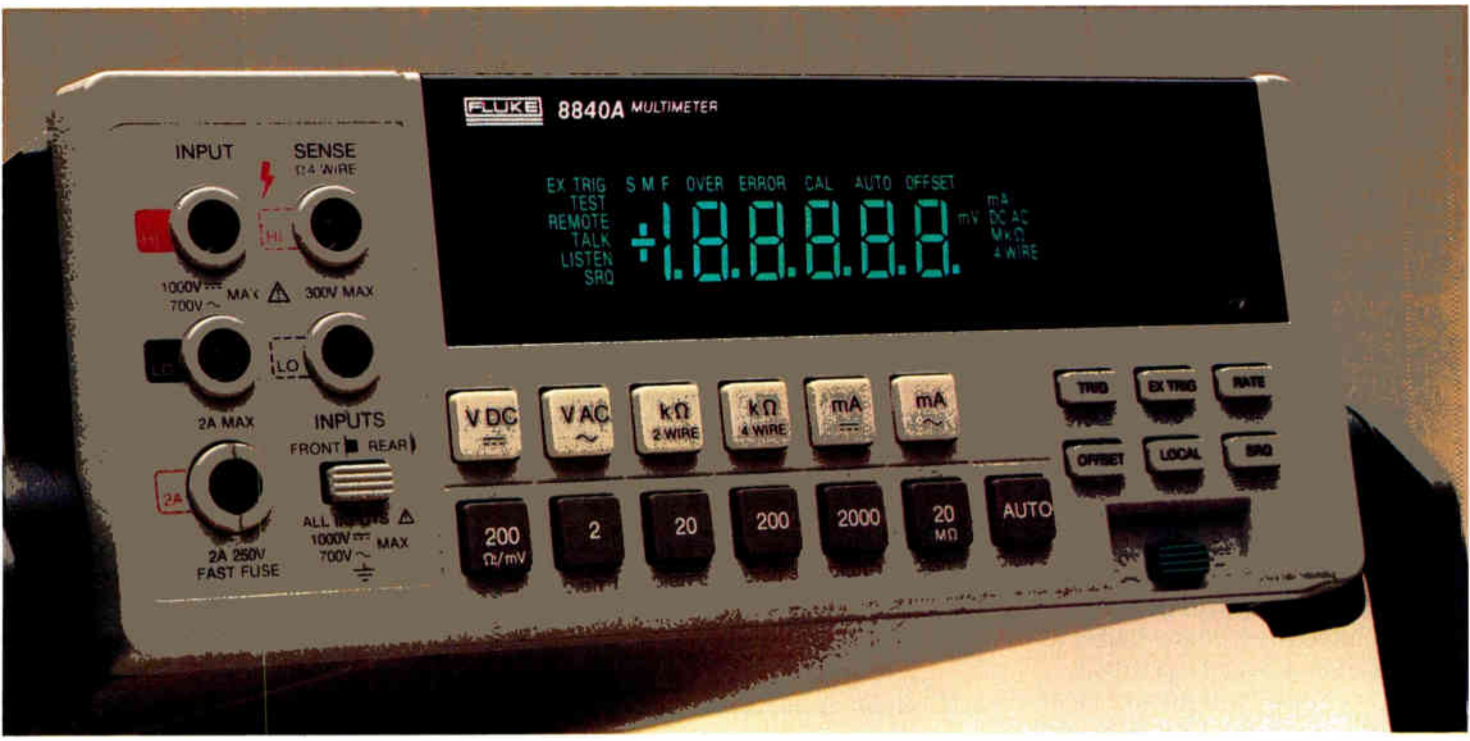

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Resolution to 1 μV, 10 μA, 1 mΩ	Resolution to 100 nV, 1 μA, 100 μΩ
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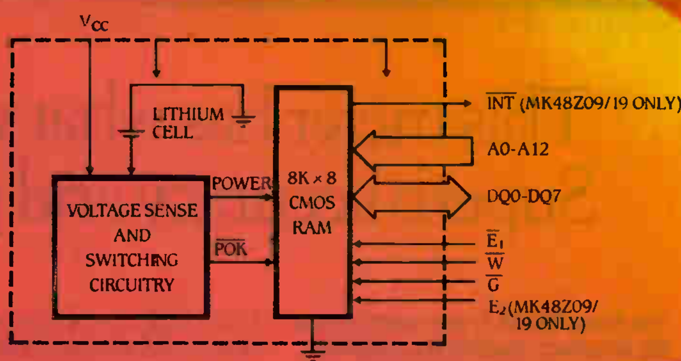
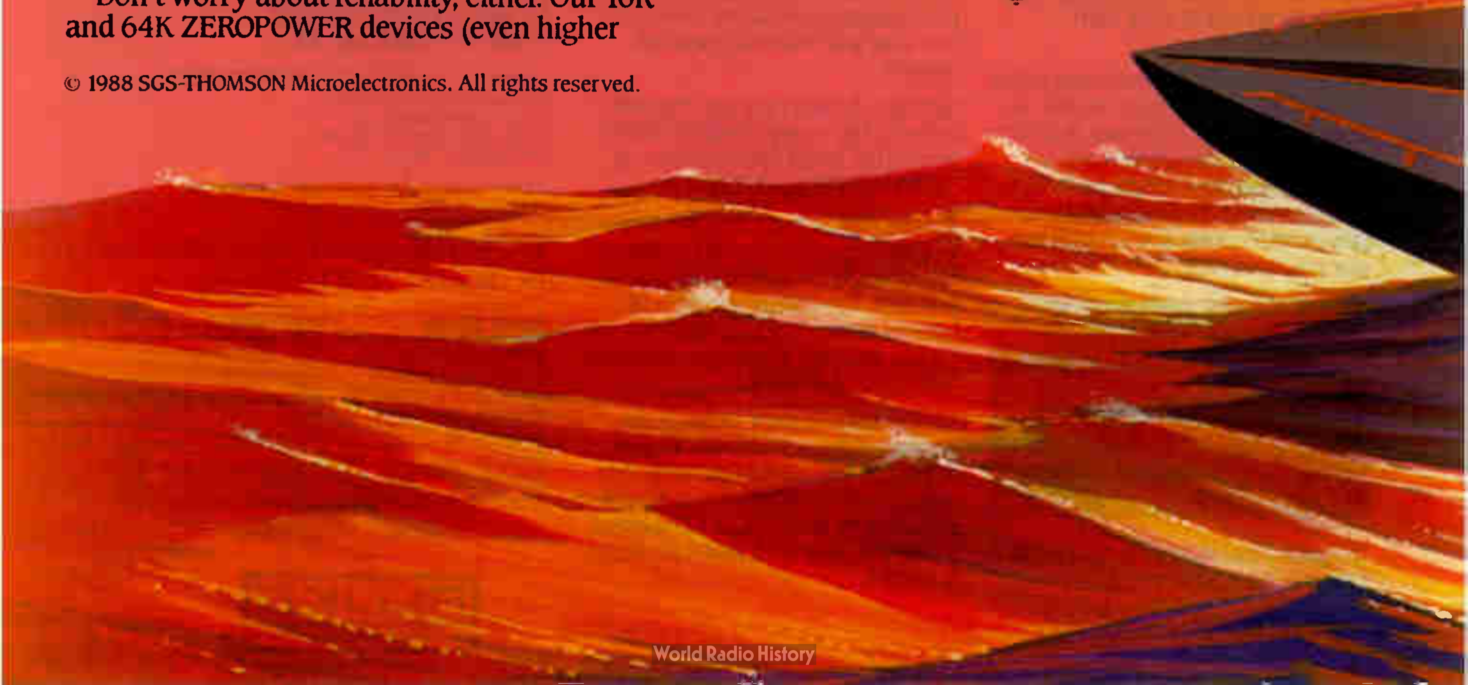
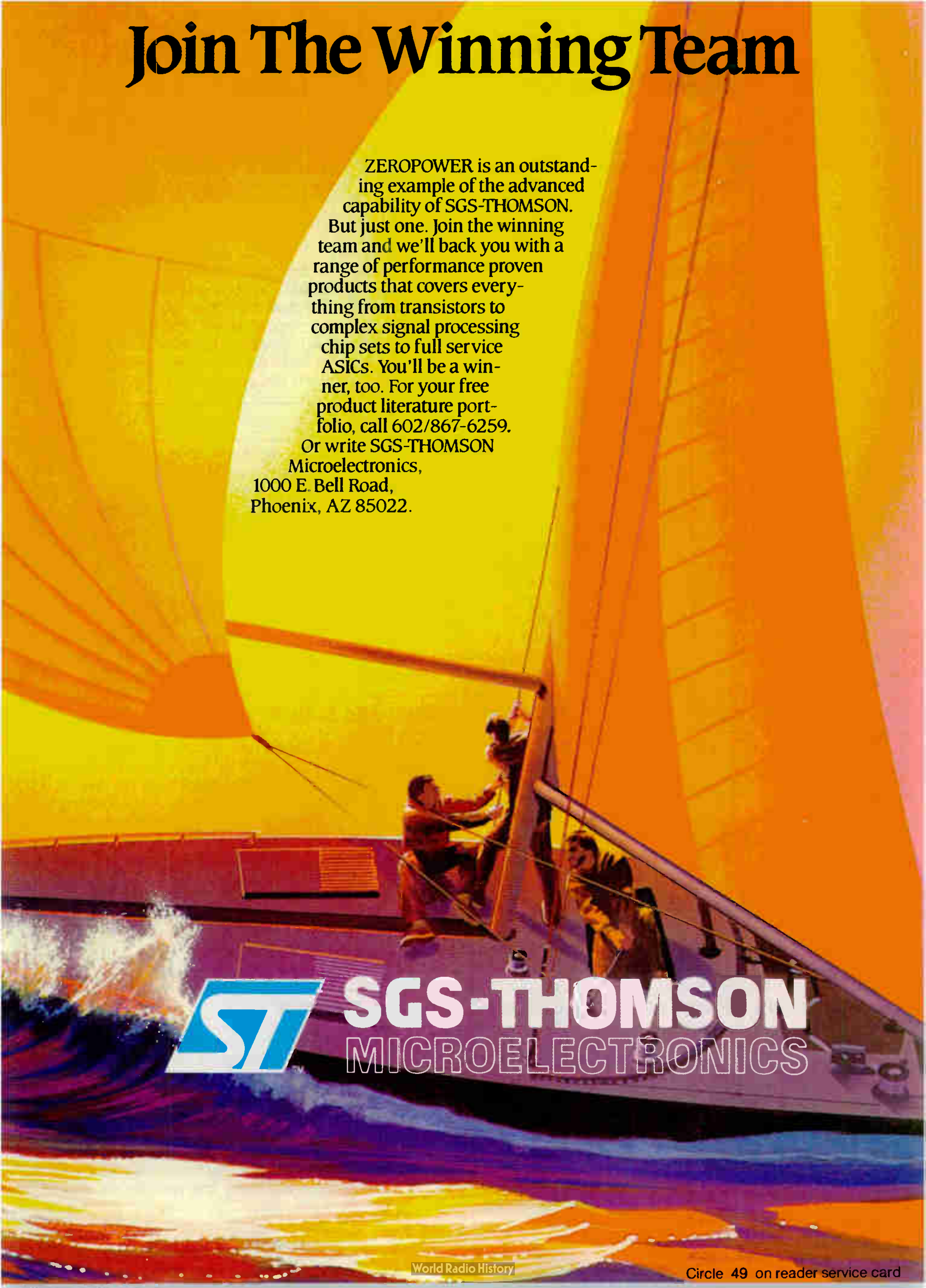
DEVICE	TEMP RANGE	WRITE PROTECT VOLT.	BATTERY LIFE OVER TEMP	U.L. RECOG	SPEED	KEY FEATURES
MK48Z02	0-70 C	4.75V	11 yrs.	Yes	120-250ns	2K × 8 SRAM unltd. write cycles
MK48Z12	0-70 C	4.5V	11 yrs.	Yes	120-250ns	2K × 8 SRAM unltd. write cycles
MKI48Z02	-40-85 C	4.75V	6 yrs.	Yes	120-250ns	2K × 8 SRAM indust. temp. range
MK148Z12	-40-85 C	4.5V	6 yrs.	Yes	120-250ns	2K × 8 SRAM indust. temp. range
MK48T02	0-70 C	4.75V	11 yrs.*	Yes	120-250ns	2K × 8 SRAM w/realtime clock
MK48T12	0-70 C	4.5V	11 yrs.*	Yes	120-250ns	2K × 8 SRAM w/realtime clock
MK48Z08/09	0-70 C	4.75V	11 yrs	Yes	150-250ns	8K × 8 SRAM w/additional CE and power fault flag (– 09)
MK48Z18/19	0-70 C	4.5V	11 yrs.	Yes	150-250ns	8K × 8 SRAM w/additional CE and power fault flag (– 19)

*3.3 yrs. minimum clock operating in battery backed mode.



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INTERNATIONAL NEWSLETTER

DAI NIPPON POINTS THE WAY TO SHARPER LIQUID-CRYSTAL DISPLAYS

Much sharper liquid-crystal color displays for portable TV sets and office-automation gear are in sight. Dai Nippon Printing Co. is offering samples of a high-resolution LCD color filter that features picture elements only 10 by 10 μm, located with an accuracy of ±2 μm. Current high-resolution filters have pixel sizes of 100 by 150 μm or more. Key to the improved resolution is a pigment-dispersed manufacturing technique that lays down a fine pattern of red, green, and blue plastic material on a glass plate; the Tokyo firm says the technique cuts the number of processing steps to only a fifth or a sixth of the number needed to turn out a conventional dyed filter. Dai Nippon is sampling 5- and 6-in. filters and plans to get into mass production by October. Larger sizes are in the works: there's already a 14-in. prototype. □

SIEMENS IS FIRST WITH AUTOMATED MASK-PRODUCTION CENTER

Siemens AG has installed what it believes to be the world's first robotized mask-production center. Now used for pilot runs at the company's chip-fabrication facilities in Munich, the center has two Siemens-made mobile robots that unload and load magazines of masks for a Perkin-Elmer Corp. Mebes III electron-beam write system. During the pilot operations, a single person observes the mask-making process. But the center could conceivably run without personnel around the clock for seven days a week, says project leader Andreas Oelmann. At the moment, though, the e-beam system runs around the clock all week to expose masks but only two shifts for five days a week can handle the finishing operations necessary for enough masks to fill the company's needs. Pilot operations will continue for another two months; after that, the center will be put into regular service. Besides cutting personnel costs, robotized mask-making pays off with a reduction in mask defects. □

IBM JAPAN UNVEILS PCs THAT SPEAK BOTH JAPANESE AND ENGLISH

IBM Japan Ltd. is moving to tap into a peculiar Japanese demand: the demand for personal computers that run English-language software. Many Japanese PC users want to run English-language software because there is much more variety on the market than the world of Japanese-based software offers, and leading-edge programs generally appear in English long before Japanese translations are ready. The Tokyo-based IBM subsidiary is introducing a line of Personal System models that run Japanese-language software written for IBM Japan's Japanese versions of the MS-DOS and OS/2 operating systems, like earlier PCs from IBM Japan, but that add the capability to run English-language software under the standard American versions of MS-DOS and OS/2. The new 5550-S, 5550-T, and 5570-T models are built around the Intel Corp. 80386 processor running at 16 or 20 MHz. Their hard-disk capacities range from 30 to 230 Mbytes. □

ERICSSON'S OPTICAL SWITCHES WORK WITH NON-POLARIZED LIGHT

Sweden's L. M. Ericsson expects to have commercial versions of a four-by-four optical switch that can handle non-polarized light and thus work without special high-cost optical fiber on the market in about a year. The Stockholm firm reports that it has already turned out a handful of the switches, which have 24 two-by-two elements on a 49-mm-long slab of lithium niobate. "They worked the first time," says Lars Thylèn, who heads Ericsson's integrated-optics development group. "The crosstalk was so low we couldn't measure it—in the order of minus 50 dB." Ericsson has found a way to ease temperature and geometry constraints, which make the switches relatively easy to produce. □

INTERNATIONAL WEEK

JAPAN–U. S. TEAM TO DESIGN SUPERDISK

Hoya Corp., a leading Japanese optics manufacturer, has teamed with three U. S. companies to develop a glass-based magnetic disk with 10 times the storage capacity of aluminum-based disks. Hoya and Xidex Corp., Fremont, Calif., will engineer the required sputtered-type magnetic film and Applied Magnetic Corp., Santa Barbara, Calif., will help develop the magnetic read head. A U. S.-based magnetic-disk-drive manufacturer—whose name Hoya would not disclose—will design the drive. Increased capacity is possible because the glass-based disk has better dimensional stablity. Hoya expects to commercialize the disks—in both 3½- and 5¼-in. formats—in one or two years.

ITALIAN TELECOM TALKS STALLED

Negotiations on a three-way telecommunications alliance involving AT&T Co., Ing. C. Olivetti & C. SpA, and STET SpA, a holding company for the Italian government telecommunications operations, are at an impasse. Citing "significant basic differences," Olivetti refuses to allow AT&T to up its equity stake in the Ivrea, Italy, company from the present 22% to 40%. This leaves up in the air STET's plans to restructure by hooking up with AT&T because the deal includes a three-way equity swap. Meanwhile, three other companies—Alcatel, Ericsson, and Siemens—are all waiting to take AT&T's place should the deal fall through.

PHILIPS MOVES TUBE UNIT TO TAIWAN

To achieve a more cost-effective supply of monochrome tubes and deflection units to monitor manufacturers, Philips has moved its entire tube operation to Taiwan. The Dutch company's International Product Group's Monitor Display Components is the world's largest tube operation and relocating to the Far East puts it right at its customers' doorstep because that's the region of most monitor production.

CELLULAR PHONE CONTEST HEATS UP

Siemens AG and Société Anonyme de Télécommunications, a Paris-based telephone-equipment maker, will form the newest consortium to bid on contracts for two digital mobile-phone networks in France. The networks—one in the Paris region and the other in the Grenoble/Lyons area—will be used to acquire data and know-how for the pan-European mobile telephone network planned for the 1990s. Competing with the SAT/Siemens group in France are two other consortia, one comprising France's Alcatel NV and Finland's Nokia, and the other France's Matra and Sweden's L. M. Ericsson.

SANYO TO FABRICATE A U. S. EPROM . . .

A U. S. semiconductor company, Atmel Corp., will have its design of a 1-Mbit erasable, programmable read-only memory manufactured in Japan. The San Jose, Calif., company has licensed the CMOS design to Sanyo Electric Co., Osaka, which will use it to gain a foothold in Japan's specialty-memory integrated-circuit market. The chip delivers a 100-ns access time and the two companies have a 70-ns version under development. Production schedules for the products have not been disclosed.

. . . AND HELP DESIGN A 32-BIT RISC CHIP

Meanwhile, Sanyo Electric Co. has also been busy teaming up with another American firm on a microprocessor design. It signed an agreement with VLSI Technology Inc., San Jose, Calif., to jointly develop and market 32-bit reduced-instruction-set-computer chips. The new RISC processor will be a one-chip version of VLSI Technology's current multichip VL86C010 family, which will also be marketed by Sanyo in the domestic market under the same agreement. Sanyo and VLSI expect to complete the development of the one-chip processor in one year. Moreover, VLSI Technology provides Sanyo with rights to manufacture the new version, which will be the world's first one-chip RISC 32-bit processor, says the Osaka company.

NTT TO PURCHASE AT&T MULTIPLEXERS

Following up on a promise to purchase more U. S.-made products, Nippon Telegraph and Telephone Corp. (NTT), Tokyo, will use AT&T Co. multiplexer systems for its commercial services in the Kanto and Tokai areas. NTT chose AT&T's DDM-1000 multiplexers because of a subsystem—which Japanese multiplexers lack—that lets them directly multiplex 1.5-Mbit/s electrical signals with 90-Mbit/s optical signals or 100-Mbit/s electric signals. Japanese multiplexer systems currently in use employ a three-step process to transmit the same volume of information. NTT plans to buy about 600 DDM-1000 systems before 1990.

FRANCE, BELGIUM TEAM ON MISSILES

The European arms industry has forged a cross-border link with the merger of the military rocket units of a subsidiary of France's Thomson-CSF and a firm partly owned by Belgium's Société Générale de Belgique SA conglomerate. Forges de Zeebrugge SA, which produces 2.75-in. and 5-in. air-to-ground missiles, will merge with Thomson-Brandt Armement, which produces 68-mm and 100-mm missiles. The as-yet-unnamed company will be formed in June or July. More inter-European cooperation is seen as being necessary for Europe to remain competitive in a shrinking international military market.

FRENCH TO LAUNCH INDIAN SATELLITES

France's Arianespace consortium's position on the commercial market got another boost recently when it won two contracts to launch India's multirole telecommunications satellites INSAT IIA and IIB. They will be placed into orbit in 1990 and 1991 by Ariane 4, the newest and most powerful version of the Ariane launch vehicles. Arianespace's order book now shows 44 satellites, worth about $2.50 billion.

ITALTEL LICENSES TECHNOLOGY TO CHINA

Italtel SpA, the Italian communications equipment maker, has signed a $24 million licensing agreement with the Chinese government for manufacturing the company's digital switches. Made at two plants near Beijing, the annual output of switches will handle 100,000 subscriber lines. Italtel, a subsidiary of STET SpA, Italy's telecom authority, will train Chinese personnel and supply the production equipment.

GREEKS OPT FOR ERICSSON SWITCHES

The Hellenic Telecommunications Authority of Greece has ordered $28 million worth of AXE digital central office switching systems from L. M. Ericsson, making Greece the 71st country to order AXE systems from the Stockholm company. The equipment will be installed in nine local and transit exchanges to be put in service in late 1988.

INTERNATIONAL PRODUCTS

PC-BOARD TOOL KIT GENERATES CODE FOR INDUSTRIAL CONTROLLERS

Sinorg's Easymitis cuts errors by describing factory systems in high-level language

Programming industrial controllers has taken a big leap forward with Sinorg SA's computer-aided-design tool based on a proprietary high-level structured language. Easymitis allows design engineers to describe directly how they want the production system to work, avoiding the tedious manual work programmers now do by writing executable code from the process-flow diagrams that are generated by present-generation graphics-based tools.

Running on an IBM Corp. Personal Computer AT or compatibles powered by Intel Corp. 80286 or 80386 microprocessors, Easymitis supports front-end programming with two modules: a control-description module and an object library. Control descriptions are written in a language similar to Pascal or C, but with additional control structures. The Grenoble, France, company has not yet named the language.

DATA FLOW. The object library allows programmers to tailor general control functions to specific manufacturers' equipment. This information flows into a precompiler with an attached errors list and documentation sections that produce an intermediate, present-generation, graphics-based code, which flows through another compiler. This produces an executable code, which is then transmitted to the controller.

Sinorg's initial commercial version of Easymitis will be available at the end of 1988. It is compatible with Modicon controllers from Gould Modicon Inc., Andover, Mass. The company plans additional versions to interface with more programmable controllers, such as those from the French companies Télémécanique SA and April SA, says Bruno Demarez, project engineer.

Easymitis "automates the first part so that there are no more errors in that phase," Demarez says. "For somebody who knows computers, this sounds very common and basic but for programmable controllers it is not." Users can save money because the design cycle is shortened and accuracy improved.

For about the same 100,000 French-franc price of less powerful software now on the market, Sinorg's software will make it far easier to order and carry out more sophisticated assembly line directives and to pinpoint and fix problems faster, Demarez says.

As things stand now, each programmable controller has its own operating system. "This is an economic and strategic problem for customers because the suppliers have chosen to remain incompatible," he says. To start the design process, engineers create a system on paper in natural language, which is more ambiguous than straightforward computer language.

As a result, the programmer who must translate it into excutable code may not understand all the directives and subsequently makes a guess. Or the programmer may follow the directions to the letter only to find out that the design engineer's theory was defective in practice. At that point, Demarez says, "you can never find the person who did the programming, the documentation is lost, and you don't know what is in the machine so you have to go back to the 1s and the 0s."

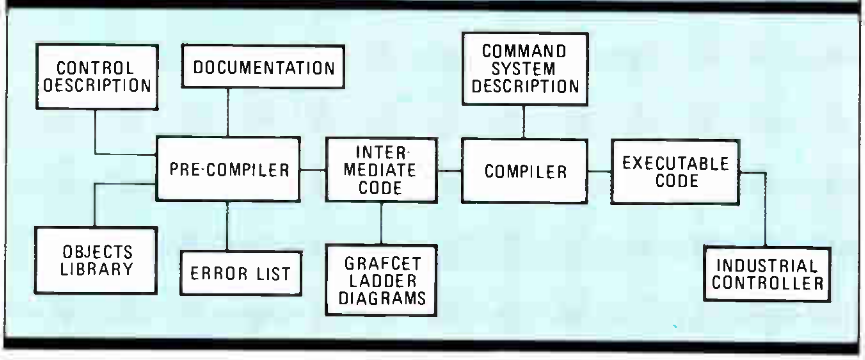
GRAPHICS. Controllers are already handling slightly more sophisticated functions, thanks to the introduction of Grafcet—a method of graphics programming adopted by the International Electrotechnical Commission—that has been used increasingly over the past two years. Although Grafcet allows controllers to do more, finding a glitch in a graphics program is "like trying to search for a needle in a haystack," says Demarez.

Sinorg, which specializes in data processing and computers, began with the premise that "language is more natural than graphics," says Demarez. "Even the designers of Grafcet know that the biggest thing lacking in Grafcet is structure because when you want to design something sophisticated with reliability you need structure."

In a chemical factory application, for example, the commands involving a complex cycle of combining, heating, agitating, and transporting a variety of chemicals will take up about a half a screen using Easymitis and be written in clear language. Although Grafcet can accomplish the same thing, its directions would take up at least five screen pages of complicated ladder diagrams, meaning that, should something go wrong, modifying the program would be much more difficult, says Demarez.

"The control design has to be linked to the product cycle," says Demarez. "On an automobile manufacturer's assembly line, parts arrive and are assembled and then the red cars go off on one track and the white on another. It is far more complex than this but if you try to to the same thing with Grafcet, you are going to end up with graphics going in all directions." Demarez says that automobile manufacturers and chemical plants as well as other companies are

MAKING INDUSTRIAL CONTROL SIMPLE



By using two compilers, Easymitis integrates Grafcet's graphics-based programming, which depends on ladder diagrams, with a high-level language that is similar to Pascal or C.

also potential customers.

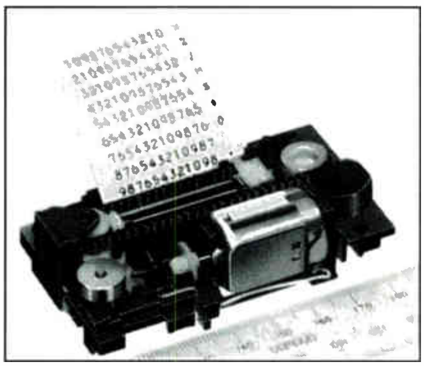
France's Rhone-Poulenc, one of the world's 10 largest chemical companies, has partially financed Sinorg's research on Easymitis and will be one of the first firms to use the system. Sinorg has no competition for this type of CAD software; its patent is about two years old. Sinorg, best known in the U.S. for its Morpho Systems SA subsidiary, which makes automated fingerprint identification systems, is considering the sale of licensing rights for Easymitis to programmable controller manufacturers in the U.S. and Japan. – *Jennifer Schenker*

Sinorg SA, Centre de Transfert de Technologie, 46, Avenue Felix-Viallet, 38031 Grenoble Cedex, France.
Phone 33-7657-4597 [Circle 500]

MODULE HAS INK TO PRINT 1 MILLION CHARACTERS

The model PTMFL55 micro printer module from Alps Electric Co. Ltd. boasts an ink roll that delivers an operational life of up to 1 million characters. The ink, which produces purple copy, can be replaced, just as in present models.

For integration into handheld calculators and other applications where a 38-mm. paper width is sufficient, the module operates on standard manganese batteries. Based on serial impact static



printing technology, it prints 14 characters per line.

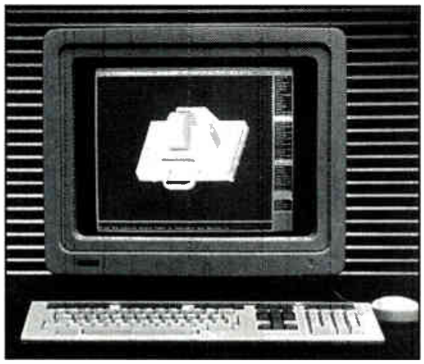
The PTMFL55 offers a printing speed of 1.15 lines/s and runs on 4.5 V dc power supplies. It weighs 55 g and is available now. Price depends on importing country.

Alps Electric Co. Ltd., 107 Yukigawa-Otsukacho, Ota-ku, Tokyo, Japan.
Phone 81-3-726-1211 [Circle 701]

SOLIDS MODELER MAKES CHANGES DYNAMICALLY

The Pro-Engineer software package from Ferranti Infographics Ltd. delivers a solid-modeling tool that lets engineers dynamically construct and modify their designs.

The feature-based data structure provides the capability to add to and delete from the base model without having to



change several data bases. Parametric descriptions are used to capture the general shapes of models, so the need for exact dimensional information is eliminated.

Dimensions can be altered either by inputting a value, establishing a relationship to another parametric dimension, or defining the relationship in a table.

Pro-Engineer runs on a variety of popular work stations, including products from Apollo Computer Co., Digital Equipment Corp., and Sun Microsystems Inc. It is available now for about £10,000.

Ferranti Infographics Ltd., Bell Square, Brucefield, Livingston, West Lothian, EH54 9BY, UK.
Phone 44-506-411583 [Circle 703]

PLASMA DISPLAY PANEL OFFERS 8 GRAY SHADES

The Thomson-CSF TH7622 plasma-panel display screen is capable of generating eight levels of gray scale on each pixel of its 512-by-512-pixel matrix. The display can also be driven—without modification or special interface—by a standard digital video signal.

The display comes complete with drive electronics. It simply connects to a power supply and any TTL-compatible video signal generator to produce graphics or alphanumerics.

Video input includes three data bits that determine the luminance level for each dot, and horizontal and vertical synchronization that allow formatting and clock speeds up to 20 MHz.

The TH7622 can also work in a single-tone mode, in which it achieves high luminance levels.

Thomson-CSF, 38 rue Vauthier, 92100 Boulogne, France.
Phone 33-1-4604-5209 [Circle 702]

CONTROLLER DOUBLES ON-BOARD MEMORY

The PCB83C652 general-purpose 8-bit microcontroller from Philips of the Netherlands features an I²C (for inter-integrated circuit) bus and twice as much on-board memory as the industry-standard 80C53 part with which it is compatible.

Fabricated in CMOS, the microcontroller has 8 Kbytes of program read-only memory and 256 bytes of data random-access memory. Both memories are expandable to 64 Kbytes off-chip.

The PCB83C652 is a control-oriented central processing unit suitable for real-time industrial equipment, public phone systems, and instrumentation. It communicates with ICs over the I²C bus interface—a two-line serial bus that transmits at 100 Kbits/s.

The PCB83C652 is available from stock priced around 18 DM each in lots up to 50,000.

Philips Components Division, P.O. Box 523, NL-5600 AM, Eindhoven, the Netherlands.
Phone 31-40-757319 [Circle 704]

MITSUBISHI'S SRAMS USE 50% LESS SPACE

Designers who need high-speed static random-access memories in their applications can get a 50% saving on board space with Mitsubishi Electric Corp.'s new 256-Kbit SRAMs.

The devices come packaged in 300-mil long, small-outline J-leaded packages that are specifically designed for high-density mounting.

The Tokyo-based company achieved the size decrease by implementing the new chips in its 1-μm CMOS silicon technology and a complementary packaging technology.

The chips come in six models. Three M5M527J series chips have access times of 35, 45, and 55 ns, and are organized in a 256-K-by-1-bit structure. The other three M5M5258J series devices have the same access times but are organized with a 64-K-by-4-bit structure. Samples are available now for a price of 10,000 yen each.

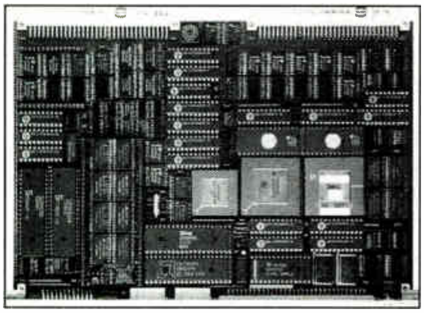
Mitsubishi Electric Corp., 2-2-3 Marunouchi, Chiyoda-ku, Tokyo, 100 Japan.
Phone 81-3-503-6451 [Circle 705]

VMEBUS CONTROLLER TRANSFERS 6.6 MBYTES/S

The SBC8230 VMEbus controller board from Creative Electronics Systems SA accepts data across a vestigal sideband or VMEbus, processes on the fly, and transfers it at up to 6.6 Mbytes/s to other processors on a distributed multiprocessor system.

The board integrates Motorola Inc. 68020, 68881, and 68882 processors, a VSB connection, a high-speed first-in first out-memory, and 1 Mbyte of zero-wait state random-access memory with four 32-bit direct-memory-access channels.

Processing nodes can be separated by distances of up to 100 m, and switching between tasks takes just 100 μs. Up to



15 nodes can be supported by a single controller board.

Software is available to connect the board directly to Digital Equipment Corp. VAX or microVAX hosts as well as Sun Microsystems Inc. work stations for on-line imaging.

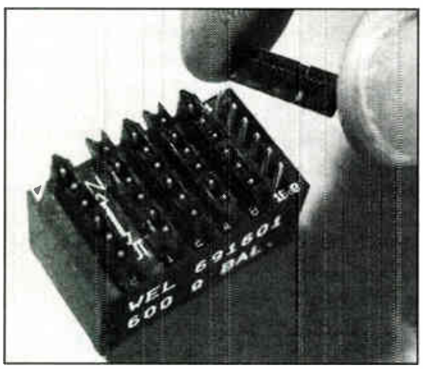
The SBC8230 is available now. Depending on options, it carries an export price of $4,500 to $6,000.

Creative Electronic Systems SA, 70 route du Pont Butin, Case Postale 107, 1213 Petit-Lancy 1, Switzerland.
Phone 41-22-92-57-45 [Circle 706]

ATTENUATOR CAN BE RESET WITHOUT SOLDERING

The 6900 series of adjustable attenuators from Welwyn Electronics Ltd. deliver programmable insertion loss of up to 31½ dB.

Six pads in the attenuator contribute ½, 1, 2, 4, 8, or 16 dB. An arrow-shaped link in each pad shows at a glance whether or not it is enabled. This allows attenuation values to be set and reset without soldering—a major benefit to



installation and service engineers.

The 6900 series is available now. Price depends on importing country.

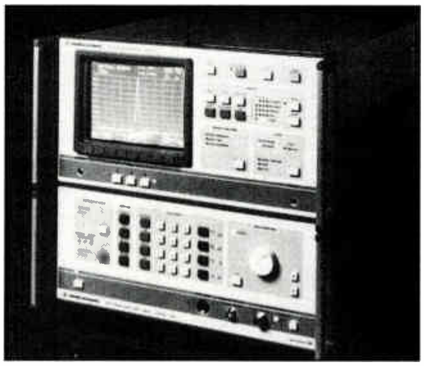
Welwyn Electronics Ltd., Bedlington, Northumberland, NE22 7AA, UK.
Phone 44-670-822-181 [Circle 707]

SPECTRUM ANALYZER HAS WIDE BANDWIDTH

The FSA Spectrum Analyzer from Rohde & Schwarz offers precise synthesized tuning from 100 Hz to 1.8 GHz, 100 dB of on-screen dynamic range, and a total measuring range between −145 and +39 dBm.

Accuracy for low-frequency measurements is enhanced by resolution bandwidths as small as 6 Hz and frequency steps down to 0.0003 Hz. High-frequency measurements are enhanced by resolution bandwidths up to 3 MHz, uncorrected frequency response that is flat to 0.6 dB, and a 150-V overload immunity to pulses.

Single-function keys, menu-driven soft keys, parameter entry by keypad, and automatic test routines contribute to ease of operation. An IEEE-488 bus is standard.



Available now, the model FSA carries an export price of about $39,500.

Rohde & Schwarz, P.O. Box 801469, D-8000 Munich 80, West Germany.
Phone 49-89-41292625 [Circle 708]

FILM SCANNER DELIVERS ULTRA-HIGH RESOLUTION

The LS-3500 35-mm Film Scanner converts images on standard 35-mm color or black-and-white film into digital data at resolutions of 24 million pixels—2.5 to six times the resolution of the film.

Designed to be used with a personal computer or work station acting as its controller, the film scanner targets applications in original-equipment-manufacturer products such as image processing systems.

The scanner is compatible with IEEE RS-232-C serial communications ports as well as the GP-IB interface widely used in instrumentation systems. It measures 288 by 384 by 141 mm and weighs 6 kg. Available now in sample quantities, the LS-3500 costs 10,000 yen.

Nikon Corp., Fuji Building, 3-3-2 Marunouchi, Chiyoda-ku, Tokyo 100, Japan.
Phone 81-3-216-1034 [Circle 709]

2-BY-1.3 METER SCREEN DUPLICATES PC DISPLAY

A 2-by-1.3 m multicolor display from ComFuture Ltd. plugs directly into the RGB output of an IBM Corp. Personal Computer or compatible to provide a large-screen 640-by-200-pixel reproduction of the PC screen.

Based on light-emitting diodes, the MegaLED displays screens in parallel with the PC monitor in real time. A display can be created with any software package that runs in low or high resolution Color Graphics Adapter mode and uses up to four colors.

Each LED is 5 mm in diameter and can display a red, green, or orange dot. Applications include animation and text advertising, and public displays of financial information, time-tables, or schedules.

The MegaLED is also available in 4-by-1.3-m size. Price depends on importing country.

ComFuture Ltd., 7 Habonim St., Ramat-Gan, Israel.
Phone 972-3-7510940 [Circle 710]

FLOURESCENT DISPLAY OFFERS 3 ENTRY MODES

Pulseview Ltd.'s PVM3·vacuum-flourescent-display module has a 40-character width and three data-entry modes—serial, parallel, and asynchronous.

It includes a 505-nm blue/green display with drivers, a power supply, and multifunction microprocessor that handles scanning of display grids and setting of dot patterns.

Characters are 5 by 3.5 mm displayed in a standard 5-by-7-pixel dot matrix. A full 96-character upper- and lower-case ASCII is preprogrammed into the system. The module is available now. Price depends on importing country.

Pulseview Ltd., Unit 1, Suffolk Way, Drayton Road, Abingdon, Oxon OX14 5JY, UK.
Phone 44-235-34909 [Circle 711]

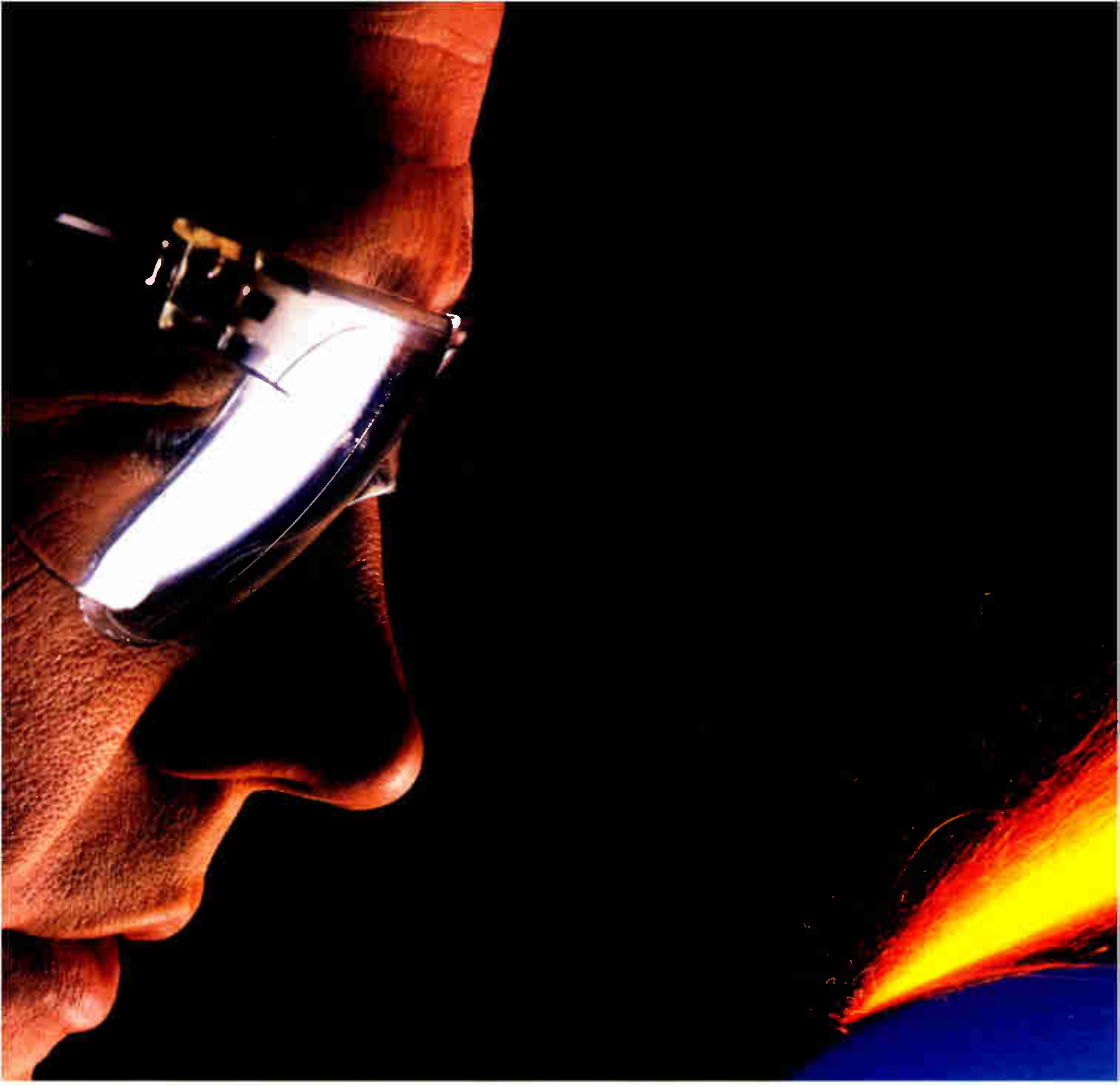
MULTIMETER HANDLES 530 READINGS/S

The multimeter model B1046 from Siemens AG offers measuring rates of up to 530 measurements/s. The frequency can be selected in three steps as a function of the display range.

The meter measures voltages, currents, resistance, and temperatures. It is guarded to suppress interference and handles voltages up to 1,000 V by using a floating-input technology that withstand high voltages. The B1046 multimeter is available now. Price depends on importing country.

Siemens AG, P.O. Box 103, D-8000, Munich 2, West Germany.
Phone 49-89-2341 [Circle 712]

Gould has features you won't find at the ordinary ASIC house.



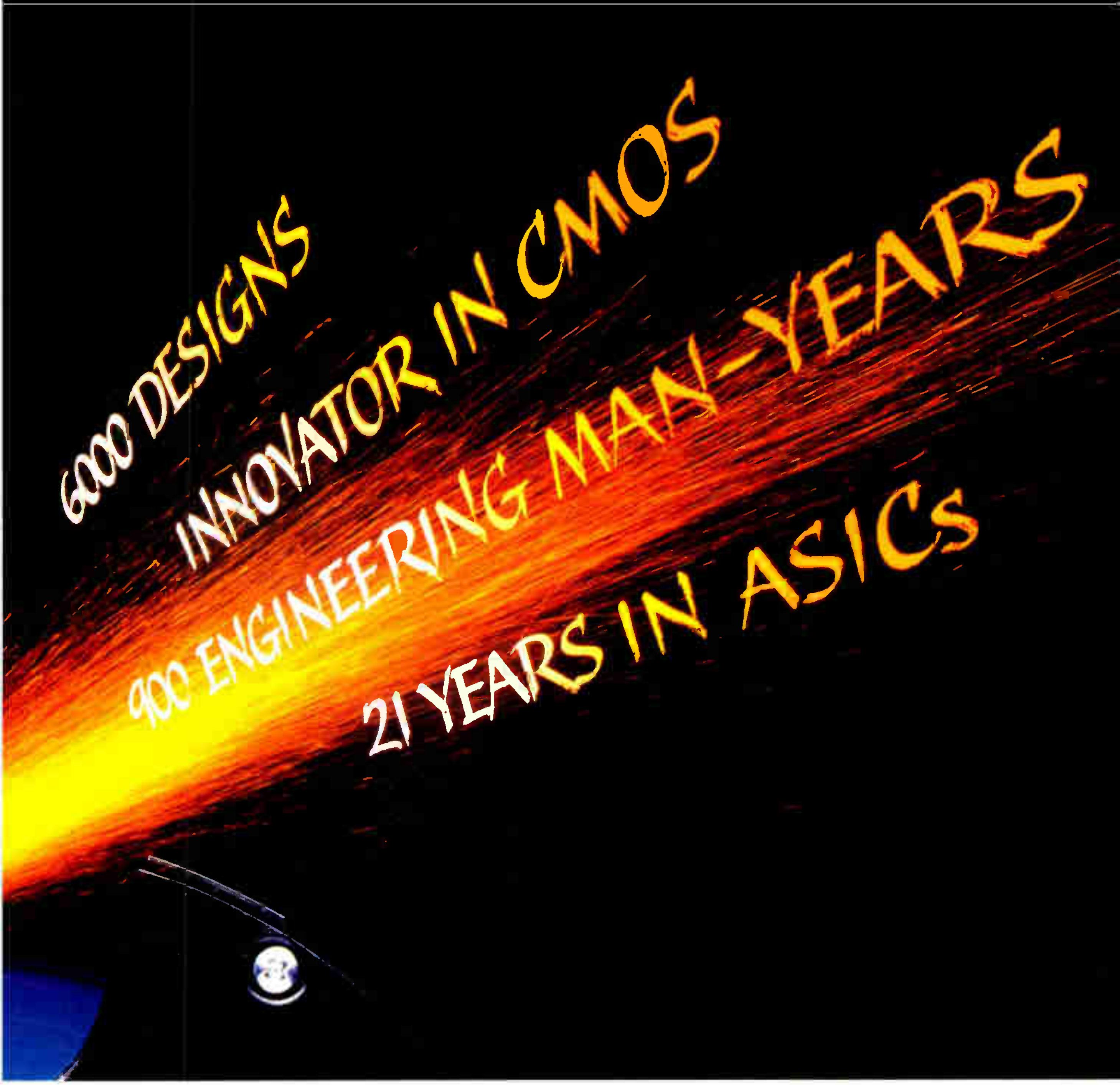
A nose to the grindstone.

What do twenty-one years as an ASIC vendor do for your customers? A lot.

Two decades give you the time you need to develop and manufacture over 6000 successful designs. The time you need to accumulate 900 man-years of engineering experience. The time you need to learn things not found in the textbooks.

That's the kind of experience Gould Semiconductors can put to work for you on every circuit you do.

Gould recognized early how valuable the combination of CMOS processes and CAD/CAE technology would be for our customers. We have been an innovator in both of these areas.



We've also had time to fully develop application-specific IC techniques that still frustrate other vendors. For instance, Gould is an acknowledged industry leader in analog/digital circuit combinations. Many ASIC producers can't even offer them.

The most important advantage to you, though, is that Gould has probably produced a design similar to yours already. We know the problems to look for and how to avoid them. In many cases, we can recommend easily incorporated features that add value to your system.

That's what twenty-one years of hard work can do for you.

Manufacturer of Gould AMI Semiconductors.

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An ear for your problems.

All ASIC customers want essentially the same things: better system performance, lower system cost, quick development and production cycles. But every ASIC project has a different set of priorities.

Your only guarantee of success is the vendor's sensitivity to your individual needs. For two decades, Gould has listened and responded with strategies to provide the best system solution. The ASIC Continuum is one such strategy.

The ASIC Continuum provides a design solution effective for any application. There are low-cost E^2PLDs for instant prototypes and small volume production applications. Also gate arrays for fast prototyping

and cost-effectiveness over a broad range of volumes.

More advanced implementations get standard cell or cell-based custom circuits. These are ideal for analog/digital combinations, high-density systems and other circuits requiring special performance characteristics.

We are also meeting your needs with expert-based design aids. Extensive cell and macro families for PCs and workstations. A full-service design group. And more comprehensive programs to give you the best ASIC solution.

Manufacturer of Gould AMI Semiconductors.

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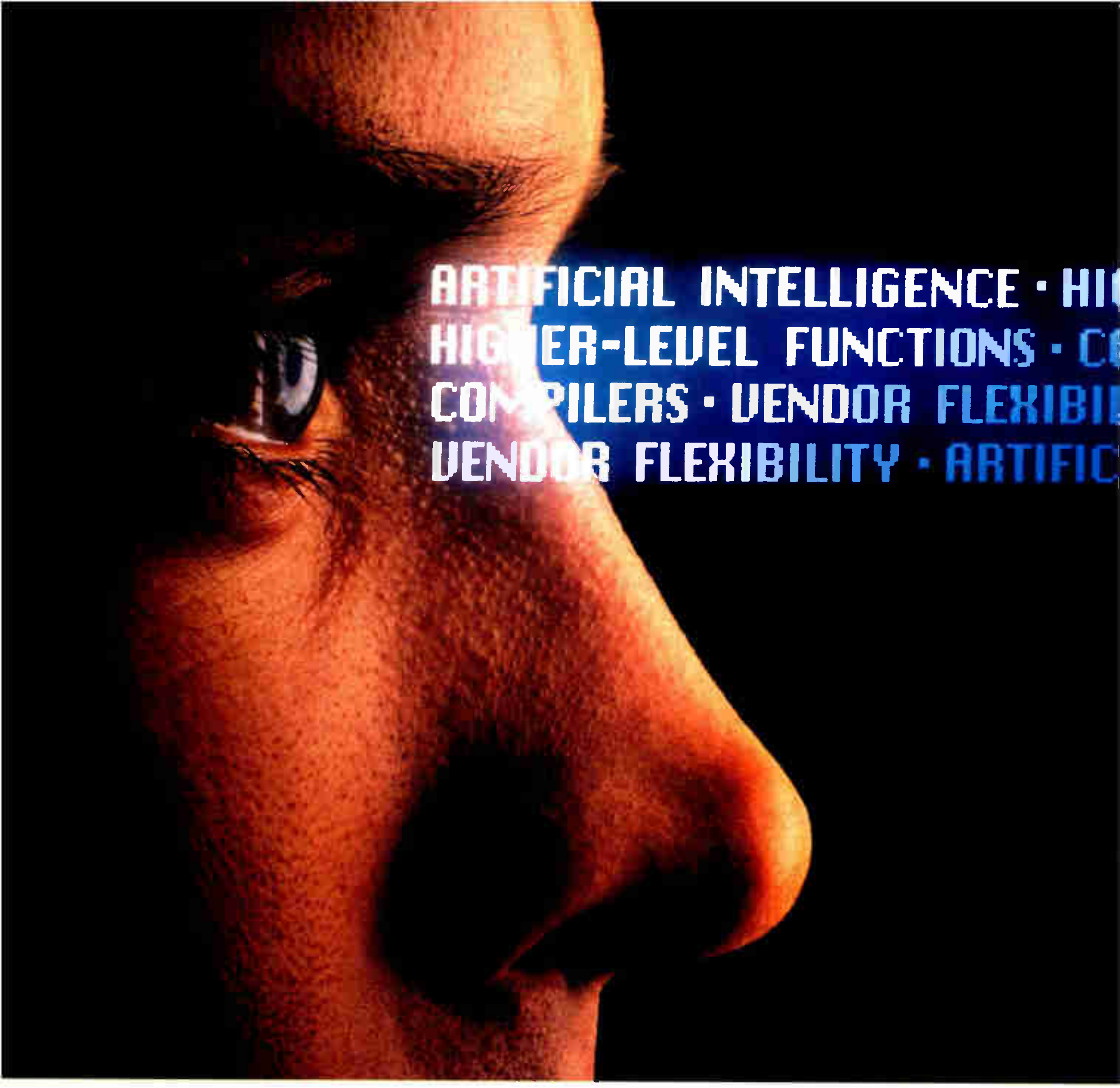

An eye on the future.

The pressure on system designers will continue to be intense. Gould has responded by cutting development spans, increasing functions and performance. And now we're using artificial intelligence (AI) to go even further.

Already Gould Expert Systems™ tools are adding value for system designers.

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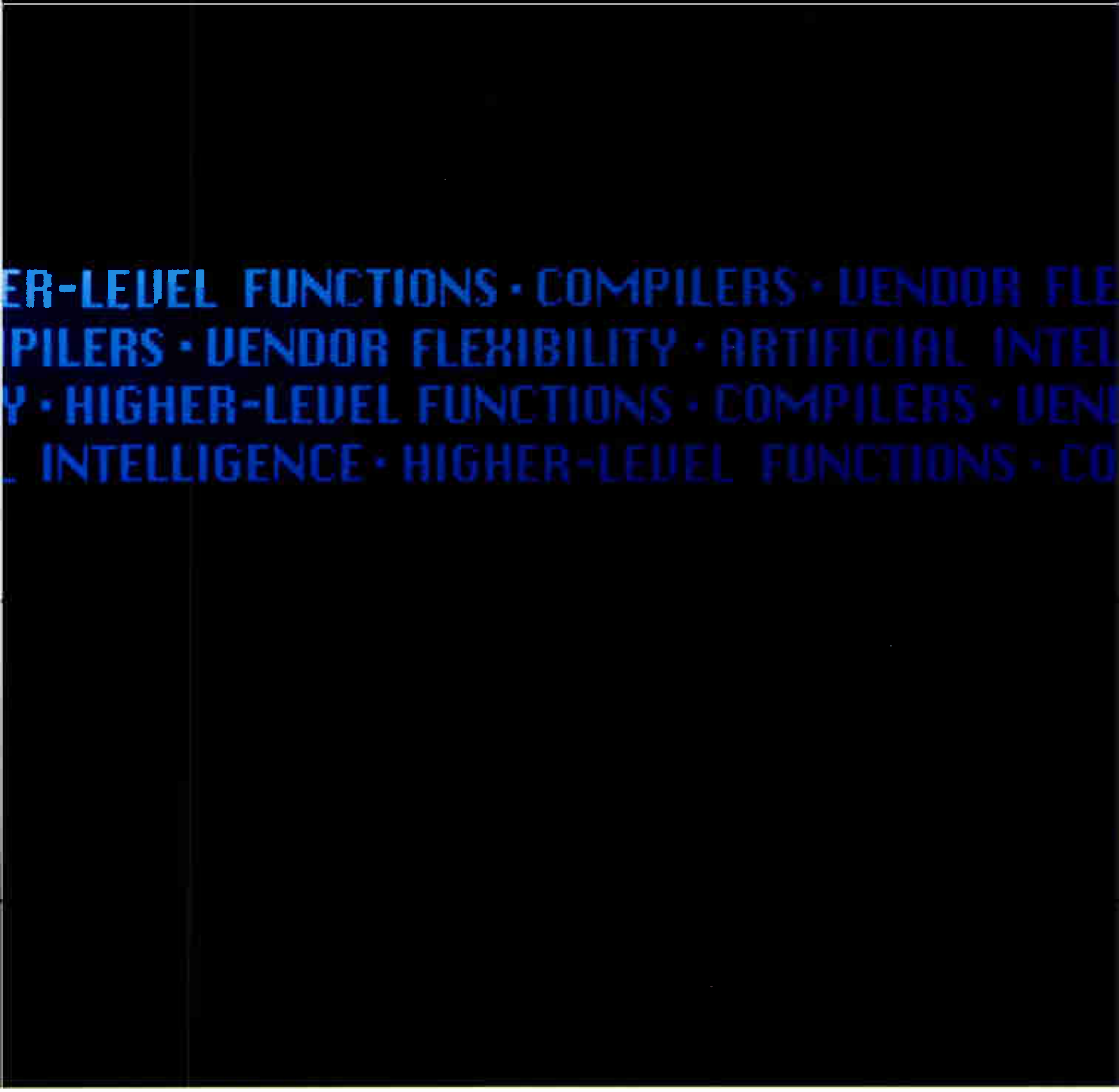

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Come see how Gould's Expert ASIC tools can play a major role in your future.

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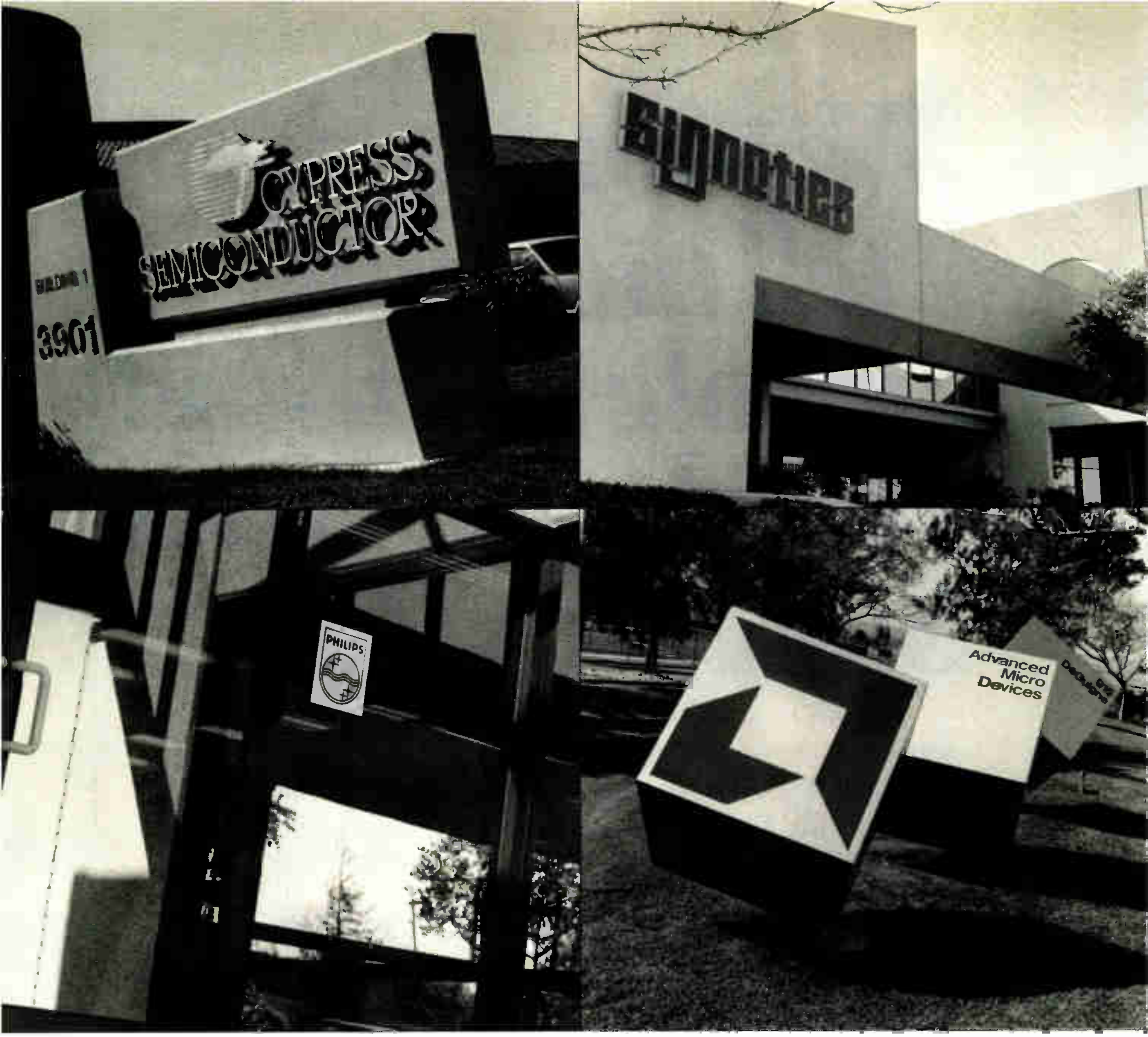
Circle 61 on reader service card



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Circle 62 on reader service card

RISC SLUGFEST: IS MARKETING MORE IMPORTANT THAN PERFORMANCE?

Performance is the main reason to use RISC processors, but RISC vendors are also enticing potential customers with families of peripheral chips, alliances with second sources and software houses, development support, and other services

by Bernard C. Cole

Motorola Inc. is putting on an impressive show as it slowly brings its 88000 RISC processor out from under wraps. A gradual, public striptease of leaks and announcements reveals more and more product details, full-page ads run in major newspapers, a parade of orchestrated customer announcements begins, and a consortium of supporting hardware and software vendors meets—all this is in addition to the normal activities of its large sales force. It's big-time marketing, and the Schaumberg, Ill., company has strong marketing muscles. It's flexing them hard in its late-entry attempt to carve out a piece of the merchant market for 32-bit microprocessors based on the design philosophy called the reduced-instruction-set computer.

Motorola clearly regards its marketing extravaganza as critical to success in the RISC arena—and it's not alone. Chip performance now is not enough: Motorola has that too, in spades, but will not rest on that fact. High performance, although long the central argument for RISC processors, at this point has become just one of the tools wielded by the marketeers. As RISC chips proliferate and their manufacturers push the technology aggressively to higher speeds, the big four—service, support, software, and second-sourcing—are rapidly becoming as important in the buying decision as performance and architectural features.

The market for 32-bit RISC chips is still small but industry observers now are sure that they are not a flash in the pan—that RISC architectural products will encroach steadily on the market share held by complex-instruction-set-computer chips. Many new players have entered the game during the past year and most of these upstarts already see that the winning strategy will necessarily involve a lot of teamwork.

Companies without the resources of an Intel Corp. or a Motorola are banding together to provide multiple sources of the silicon in an ever-increasing range of price-performance choices, plus software and other forms of customer support. They are hoping to strengthen their hands with these alliances so they can offer customers more peripheral chips, software like Unix ports and real-time operating systems, development hardware such as emulators and PC plug-in cards—as well as a bigger team of salesmen and engineers who can help customers design systems. And as the entrenched microprocessor vendors such as Motorola, Intel, and Advanced Micro Devices Inc. play their hands, the competing RISC teams spearheaded by MIPS Computer Systems and Sun Microsystems are scrambling for share of mind by accelerating the announcement of plans for upcoming chips—chips that counter the performance claims of the latest products but that may not be available for months or even years. Standard industry practice is to avoid announcing chips long before they are available: the RISC teams are pushing these pre-announcments as a marketing ploy. They are selling future technology because they want customers to know about the growth path that will be open to them if they buy into a given architecture now.

Thus prospective RISC-chip users now not only need to evaluate the architectures on the market, but the entire spectrum of technology both offered and promised by the opposing camps—and their ability to deliver on those promises. Evaluating the technology is far from easy, in part because the industry has not had time to run benchmarks on the major processors that are just hitting the sampling stage. All the vendors have figures in megahertz and millions of instructions per second, but there is considerable disagreement on the value of the numbers: all mips are not the same, as CISC-processor vendors point out, so comparisons are difficult, and competing claims are far from equivalent. From the customer point of view, this makes it even less likely that decisions will be based entirely on performance.

The customer confusion is made worse by the sheer number of choices. From a handful of vendors 18 months ago, it's become a free-for-all, with RISC vendors and CISC vendors slugging it out toe-to-toe. To muddy the waters even more, CISC chips may be evolving to be more like the RISC insurgents.

As more products are unveiled, the marketing energy is building up. "It's the 1970s all over again," says Andrew Kessler, industry analyst with the Technology Group of New York-based PaineWebber Inc. "Then it was 8-and 16-bit microprocessors and microcontrollers," he says; "now it is 32-bit microprocessors and embedded controllers." While some of the players are the same who fought it out then, there are many new ones as well: Acorn Computer Systems, Bipolar Integrated Technology, Cypress Semiconductor, Intergraph, Integrated Device Technology, LSI Logic, MIPS Computer Systems, Performance Semiconductor, Sanyo Electric, Sun Microsystems, and VLSI Technology.

The makeup of the 32-bit market is changing too. No longer will it be dominated by CISC processors—they must now share the wealth with a variety of RISC upstarts (see graph, below), says Alice Leeper, industry analyst at Dataquest Inc., San Jose, Calif. From a virtually nonexistent postition in 1983, the RISC share of the 32-bit processor market is expected in 1988 to hit almost $60 million in sales, out of a total of $636 million, she says. By 1992, it is estimated that annual sales of RISC chips will reach $443 million, about 25% of the total 32-bit market, she adds.

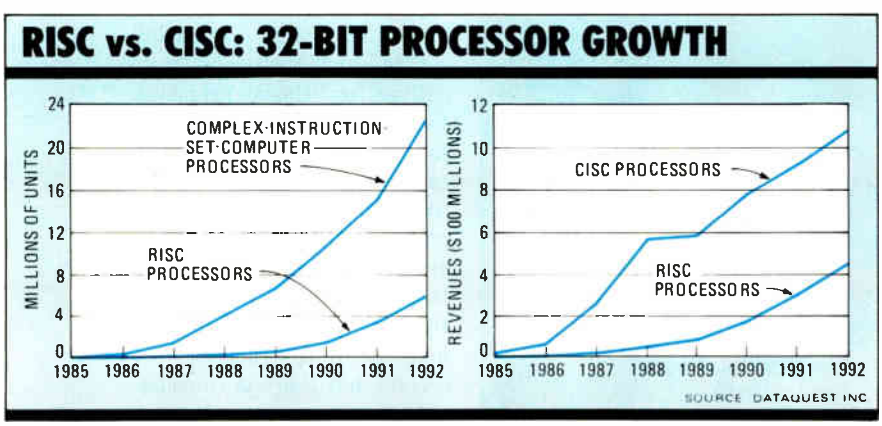
Responsible for the growth of RISC architecture is its simplicity, says Michael Slater, editor and publisher of Microprocessor Report of Palo Alto, Calif. "Take a standard CISC machine such as the 68020 and remove the microcoded control store, the instruction decoders, state-machine logic, clock-phase generators, branch-control circuitry, interupt logic, and bus control. What you have left in the purest sense of the term is a RISC machine," he says, "with instructions that execute in one cycle, greatly simplified design, smaller chips and fewer transistors (tens of thousands versus hundreds of thousands) and apparent performance improved by several orders of magnitude over CISC machines."

The end result is a reduced cost of entry. Even the smallest of startups can design a processor and bring it to production at a fraction of the cost and with a design time that is measured in months rather than years, Kessler says. "What it means is that even traditional users of CISC processors can go away and design their own processor with proprietary and value-added features, freeing themselves from the lock-step-development cycle they were forced into when they had to use one of the standard CISC machines," he says.

Another factor that makes it easier to enter the RISC-processor market is the increasing market growth in systems based on AT&T Co.'s Unix operating system, and the ready availability of Unix to all comers. Unix has become the de facto standard in high-end work stations and scientific computers. In the personal-computer world, software is linked very closely to the architecture of the particular processor on which it must run. But this is not the case for Unix and most Unix application programs, because they are written in the C high-level language, and are relatively easy to port once a good optimizing compiler has been developed for a new architecture. Indeed, most of the concepts for RISC originated not from groups working on CPU design, but from software groups aimed at developing advanced compilers optimized for implementing such high-level languages as C.

To make it even easier to get software going on RISC-based systems, new standards called application binary interfaces are being developed that simplify the process of porting software between systems based on the same processor architecture. Sun Microsystems Inc., Mountain View, Calif., has worked closely with AT&T in developing such a standard for the Sparc. Not to be outmaneuvered, Intergraph, Intel, and Motorola are all working on binary standards for their RISC architectures.

MIPS Computer Systems Inc., Sunnyvale, Calif., is also working with AT&T on a binary standard for both the R2000 and the newer R3000, but it has gone one step further in generating software support for them. It has joined with its second-sourcing partners to form a software company, Synthesis Software Solutions Inc., specifically aimed at acquiring, porting, supporting, and distributing third-party software for the MIPS processors.



Thus both hardware and software factors have contributed to the growth in the number of RISC-chip vendors. It was not long ago that only a handful of companies shared a $16 million RISC market that barely shipped 60,000 to 100,000 units, according to Dataquest. Fairchild Semiconductor's Advanced Processor Division in Palo Alto, Calif. (now owned by Intergraph Corp.), was targeting the high-end work-station market with its C100 Clipper chip set. So was MIPS Computer Systems with its 8 to 12 million-instructions/s 2-μm CMOS R2000/R2010 RISC chip set. VLSI Technology Inc. of

San Jose, Calif., was shooting for the low-end 4-to-10-mips embedded-controller with the VL86C010 RISC processor—a design that originated at the UK's Acorn Computer Systems Ltd.—and associated controller chips built with in a 2-μm CMOS process.

But beginning in March 1987, the industry was hit with a volley of RISC introductions starting with AMD's new 29000 [*Electronics*, March 19, 1987, p. 61]. Then Sun announced its Sparc architecture, along with plans to license it to both systems and chip houses, the first of which were Cypress Semiconductor Corp. and Fujitsu Microelectronics Inc., both of San Jose, Calif., and Bipolar Integrated Technology Inc. of Beaverton, Ore. This was followed later in the year by RISC pioneer MIPS Computer Systems, which announced second-sourcing agreements on its R2000 RISC machine with Integrated Device Technology Inc. of Santa Clara, Calif., LSI Logic Corp. of Milpitas, Calif., and Performance Semiconductor Corp. of Sunnyvale, Calif.

The pace is not letting up. In anticipation of Motorola's 88000 announcement, activity has accelerated to a feverish pitch, with announcements coming back-to-back from Intel, LSI Logic, MIPS and its team of chip makers, Sun and its partners, as well as from AMD, Intergraph, and VLSI Technology. The latest news is from Data General Corp., Westboro, Mass., which has signed a deal with Motorola to jointly develop an emitter-coupled-logic version of the 88000 by 1991. Motorola will be free to sell the 100-mips chip set to other customers (see p. 32).

LSI Logic surprised the industry in late March by announcing that in addition to its agreement to second-source the RISC chips from MIPS, it is entering into a long-term relationship with Sun Microsystems covering technology, manufacturing, and marketing. LSI's president, Wilford Corrigan says the company has the right to make, modify, and enhance the Sparc processor, peripherals, and software.

Sparc processors and peripherals will be offered by LSI as standard products as early as mid-1988, and later as building blocks for application-specific integrated circuits, Corrigan says. LSI Logic also plans multiple versions with different levels of price and performance. The first one, built in the company's HCMOS process, which has a 0.9-μm effective channel length, runs at 25 MHz and achieves about 15 mips, some "three to four times the power of a 386 or 68030," Corrigan says.

In addition, "we will be pushing very hard for military versions of these chips," says Corrigan, "including rad-hard versions." What's more, he says, one of LSI Logic's future chip versions will use the company's new biCMOS process, which will allow the company to push performance up to 40 to 50 mips within approximately the next 18 months. "We expect to have enhanced versions occurring every 6 to 12 months.

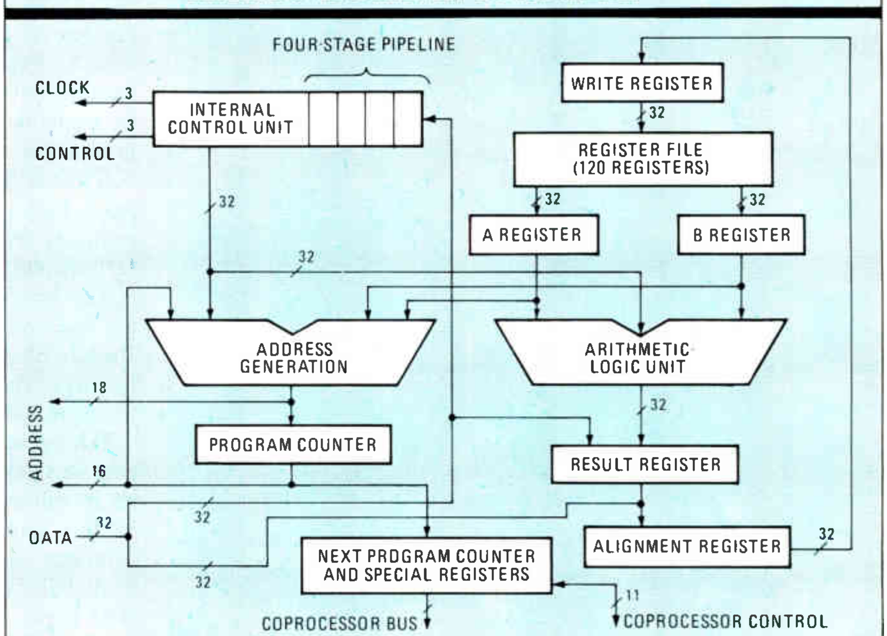
"RISC is a fork in the road," says Corrigan. "It gives a computer manufacturer the option to make a multi-source decision." What Corrigan is driving at is that a new generation of 32-bit processors is coming based on RISC, and in facing this new generation, system manufacturers don't have to choose a single-source part like the 80386 or 68030. Multiple sourcing, he says, is needed particularly to establish a new standard when you're going against entrenched architectures like Motorola and Intel.

Furthermore, RISC processors start with a clean slate: they don't need to maintain binary-level compatibility with software from earlier generations. The promise of future RISC performance increases is strong, too. "We have reached the point of diminishing returns on optimizing CISC architectures," he says. "There is little room now for performance improvement. The chips are already heaviliy pipelined. Complex designs make it hard to increase clock frequency."

LSI is not alone making chip-upgrade plans public. Following its success as the manufacturer of the first 10-mips Sparc chips for Sun using a 2-μm CMOS 20,000-gate array (see fig. 1), Fujitsu has also revealed an aggressive strategy for future RISC chip sets, to reach 40 mips by mid-1990. Full-custom design of a new integer unit is underway and Fujitsu is planning CMOS cores for semicustom processors, a powerful new 64-bit Sparc-oriented floating-point unit, and a memory-management unit.

Starting in July, Fujitsu will introduce a 1.3-μm standard-cell-based integer unit, which, along with a Sparc-specific floating-point controller from another party, will run at 15 mips. The new 25-MHz part, to be called S-25, will be housed in a 179-pin plastic-pin-grid

SPARC ELEMENTS WORK IN PARALLEL

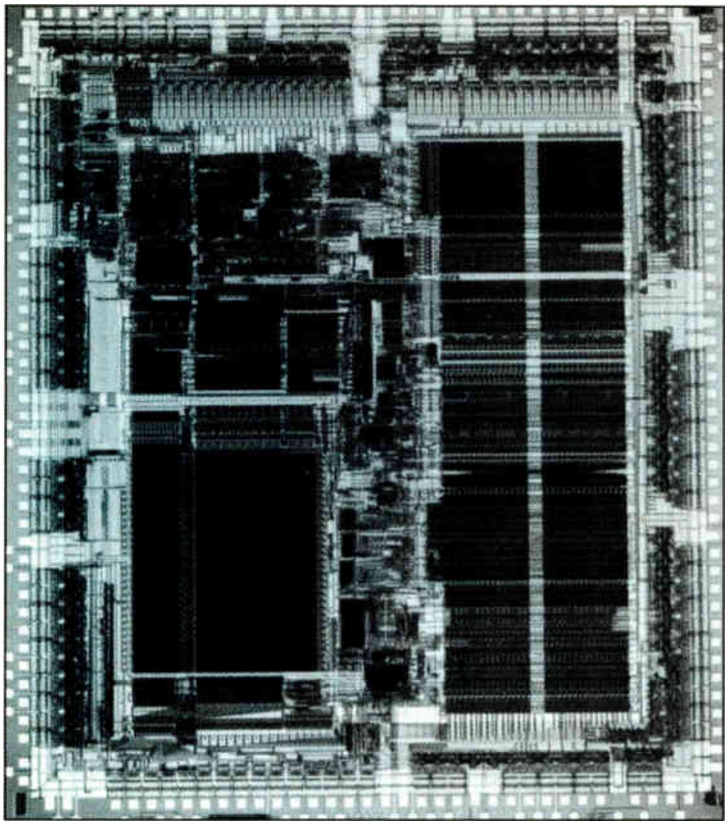


1. The pipelined internal implementation of Sun Microsystem's Sparc processor may be modified in future versions to improve performance without requiring changes in software.

array and is expected to be lower in cost than the current 256-pin 10-mips part, which requires a separate 20,000-gate-array floating-point controller chip. Fujitsu plans to introduce a 20-mips three-chip set, running at 33 MHz, in March 1989. It is also working on a high-performance floating-point controller and its own floating-point coprocessor compatible with IEEE math standards. Within a year, Fujitsu is expected to also introduce an MMU for Sparc. A 40-mips Sparc product, expected to run at 40 to 45 MHz, is now in the design- and process-technology-definition stage; introduction is scheduled for the summer of 1990.

Another Sparc partner, Bipolar Integrated Technology, is planning to introduce Sparc chips built with emitter-coupled logic in the first quarter 1989 or sooner. The parts (an integer unit and a controller for the company's two-chip floating-point set) will offer more than 40 mips. "It will be closer to the 50-mips range," says vice president of marketing Les Soltesz, adding that the 40-mips figure is calculated on conservative estimates of what programs will do and cache hit rates. The company will not disclose the clock speed of the parts, however. The floating-point controller in the chip set is optimized for its emitter-coupled logic floating-point chips, which can do a double-precision multiply in 50 ns and an add or subtract in 25 ns.

On the CMOS side, Cypress Semiconductor is moving into production with its version of the Sparc. Using its 0.8-μm CMOS process, company will soon be selling a 33-MHz, 20-mips set including a RISC chip, a floating-point controller, an MMU, a special cache-tag device for solving large-cache problems, and a family of special-cache static random-access memories, the first of which will be 64 Kbits in size, says Dane Elliot, director of applications engineering.



2. The R3000 from MIPS Computer Systems doubles the performance of the company's R2000, in part by cutting the number of cycles per instruction.

Upping the ante for any potential competitor in the RISC market, MIPS Computer Systems four weeks ago announced availability of its second-generation 32-bit RISC chip set. The R3000 central processing unit (see fig. 2) and the R3010 floating-point coprocessor boast twice the performance of the R2000-R2010 offering, the company says. It speeded up the new chips by scaling from a 2-μm CMOS process down to 1.2 μm (achieving 0.8-μm effective gate lengths) and by revamping the internal architecture to reduce the average number of cycles per instruction from 1.5 to 1.25. The result is a 25-MHz machine that can run at sustained rate of 20 mips, twice what the previous-generation 16-MHz parts could manage.

Key architectural improvements include 512 Kbits of on-board cache, twice that of the R2000, and a modified cache-refill technique that operates in a burst mode, says William Jobe, the company's executive vice president. Other innovations are the use of instruction-streaming procedures that allow access to on-chip cache memory at the same time it is being refilled, modified cache-control circuitry that allows it to use slower 25-ns external SRAMs at 25 MHz rather than shifting to more expensive and less dense 15-ns SRAMs, and a modified floating-point-unit interface that is more tightly coupled to the main CPU, allowing it to run at the same 25-MHz clock rate.

One of the first of MIPS Computer Systems' partners out of the gate with a second-sourced version of the R3000 set is Performance Semiconductor Corp. of Sunnyvale, Calif. The company is now shipping 20-mips, 25-MHz parts fabricated using its 0.8-μm CMOS process and designated the PACE3000/3010, says president Thomas Longo.

Close on its heels is Integrated Device Technology Inc. of Santa Clara, Calif., which will introduce its version of the second-generation MIPS chip set next month. Fabricated using the company's 1.2-μm Enhanced CMOS process, the IDT79R3000 RISC CPU will be available in sample quantities in June, followed by production quantities in September. Samples of the IDT79R3010 floating-point accelerator will be out in July, followed by production units in October. The company will also introduce a write-buffer circuit, the IDT79R3020, designed to enhance the CPU's performance by allowing it to perform write operations during run cycles, says vice president of marketing Larry Jordan. System performance improves by 10% to 15%, he says. Both MIL-STD-883C and radiation-hardened versions will be available in early 1989.

Taking up the challenge on both performance and cost is AMD, which next week will announce availability in volume quantites of the 25-MHz, 20-mips version of the Am29000 enhanced RISC processor it began sampling last year. In addition, AMD will announce availability of sample quantities of cheaper 16- and 20-MHz parts, as well as a faster 30-MHz, 25-mips part. As part of the same announcement, AMD will disclose details on two of its peripherals, which it will begin sampling in the fourth quarter of 1988: the Am29041 data-transfer controller and the Am29062 integrated cache unit (see p. 87). The data-transfer controller is designed to act as a gateway between the Am290000 and a slower external peripheral bus (see fig. 3), says Michael Wodopian, Am29000 program manager. It also contains a four-channel buffered direct-memory-access controller that can act as a bus master and transfer blocks of data to and from memory without the intervention of the CPU. Considerably speeding up data transfers, in the burst mode the Am29041 can achieve data-transfer rates to the CPU of up to 200 Mbytes/s.

Going its own way is VLSI Technology Inc. of Milpitas, Calif. In an attempt to counter moves by competitive RISC makers to boost performance and link up with strategic partners and second sources, VLSI last week announced a broad-based agreement with Sanyo Electric Co. of Osaka, Japan, for the manufacture and marketing of its 2-μm CMOS RISC chip set. The chip set consists of the VL86C010 processor (see fig. 4) and three peripheral controllers for memory, video and input/output and features, as well as higher speed and other derivative devices within the family.

The RISC chip set was originally developed by Acorn Computer Systems—using VLSI Technology's design tools—for use in its family of educational computers and medium-performance work stations. Known by Acorn Computer as the Acorn RISC Machine, the chip set is currently capable of sustained operation at 6 mips using a 12-MHz clock, says Douglas Bartek, vice president and general manager of VLSI Technology's logic and government products division in Phoenix, Ariz. The set has also been marketed by VLSI Technology in the real-time embedded-control market in such applications as disk drives, graphics subsystems, and networking hardware, as well as laser printers. In 1987 alone, VLSI sold 30,000 chip sets for laser printers, about a third of the total market for RISC processors, Bartek says.

Using more advanced sub-2-μm processes, Sanyo and VLSI Technology will develop faster versions and a variety of application-specific variations, says Bartek. Already envisioned are a laser-printer engine, a raster-graphics processor, and network-specific derivatives of the VL86C010, he says.

All this product activity has added to customer confusion. With the number of players exploding, "it is going to be a bloody brawl all over again" says Slater of the Microprocessor Report. He underlines the fact that buying decisions will be based as much on software, support, and second-sourcing as on performance and architectural features. Despite moves to strengthen their positions in the RISC market, the various chip vendors can be expected to have a tougher time with the entry of traditional microprocessor makers such as Intel [*Electronics*, Apr. 14, 1988, p. 97] and Motorola into the market, with the 80960 and 88000, respectively, according to many industry analysts.

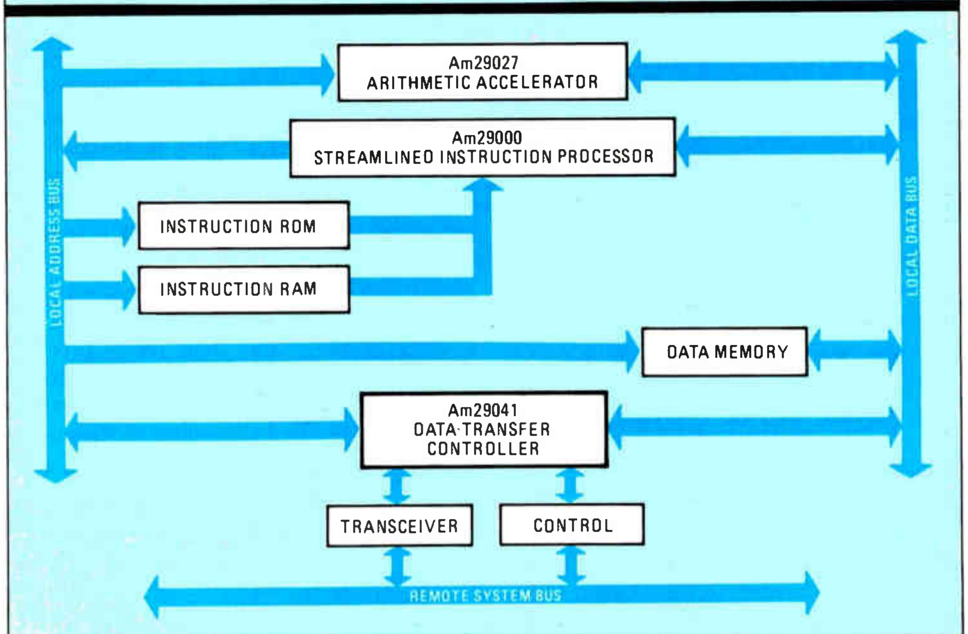
"In this kind of market, with conflicting claims as to performance and a confusing variety of architectures, the established companies have an advantage because customers are familiar with them," Slater says. "Newcomers to the market have to offer more than just speed. They have to offer some sort of security or advantage customers cannot get with the traditional suppliers."

Although Motorola and Intel are only now gearing up for production, they will probably be the strongest players in the market from here on, says Dataquest's Leeper. "Motorola has the top spot because of its experience, reputation, customer connections, and success with the 68000 family as well as other 8-bit processor products," she says. "The same is true of Intel. If you look at the whole RISC picture, most of the firms are not conventional microprocessor players. And the only ones now in the RISC competition recognized as long-term microprocessor innovators are Motorola and Intel. AMD comes in as a close third, but again the 29000 marks a brand-new venture for them," she says.

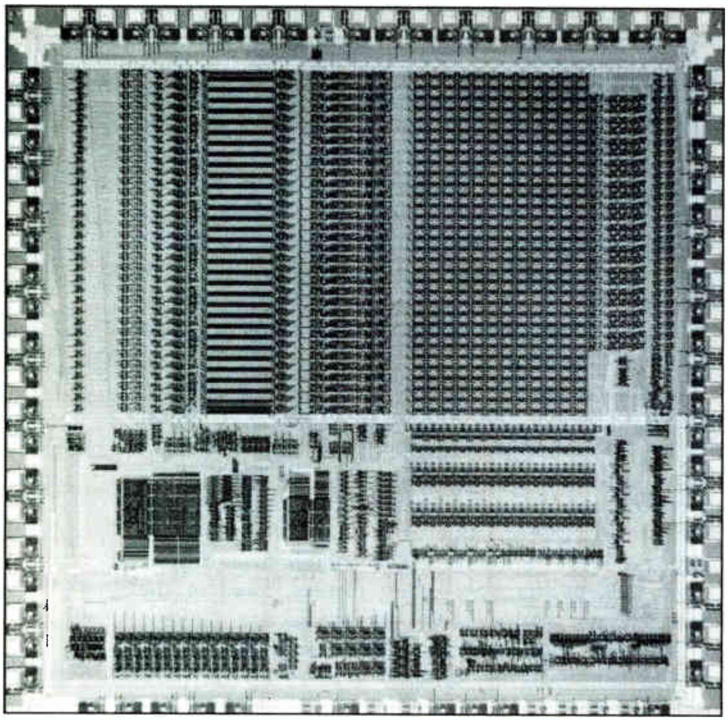
Kessler, of the Technology Group, notes that "because of the much simpler RISC architecture, the development costs to Intel and Motorola to enter this market were a small fraction of what they had to expend on their 32-bit CISC offerings. What this means is that they have even more [available resources] to devote to software support, marketing, and promotion," he warns.

As the RISC market grows, new factors will deter-

AMD BUILDS A SYSTEM



3. Peripheral chips that aid the system designer, like AMD's arithmetic accelerator, data-transfer controller, and integrated cache unit (not shown), are a vital part of the support for a RISC architecture.



4. Both a core standard cell in a VLSI Technology's ASIC library and a standard chip, the Acorn RISC Machine puts out 6 mips.

mine how the technology fares against its CISC competition, says David Schanin, chief scientist and 32000 microprocessor technical director at National Semiconductor Corp., in Santa Clara, Calif. "The RISC makers will no longer be able to sell purely on the basis of quantity, on pure mips," he says. "Customers are already beginning to look at the quality and complexity of the instructions being processed. And when they do, many of the traditional CISC machines come off looking very good."

In addition, mips may no longer be a reasonable measure of system performance, says Kessler. "Mips figures really measure how many instructions a given processor can execute in a given time, which may have nothing to do with how long it takes for it to do a given task," he says. "The most important parameter to consider is the elapsed time per task, which may be less a matter of the number of instructions being processed per second and more a function of the quality and complexity of the instruction set."

Trying to come up a new way to measure performance, Kessler has developed what he calls an "instruction quality multiplier," based on a benchmark analysis of both CISC and RISC instruction sets. A number between 0 and 1, this multiplier normalizes the mips rating to an adjusted mips figure that reflects overall system performance instead of the number of raw instructions that can be executed every second (see table). Based on this analysis, the gap dividing various CISC and RISC machines becomes much narrower, Kessler says.

Moreover, with all of this activity in the RISC arena, designers of traditional CISC machines will not be standing still. In fact, says National's Schanin, RISC and CISC may become more alike. "What everyone must remember is that RISC is a technology, a philosophy of design, not a product," he says. "Virtually every [design technique] that has been applied to RISC machines can be applied to a CISC architecture to improve performance." An example, Schanin says, is the company's 32532 CISC processor, which incorporates many RISC features. It has on-chip data and instruction caches, direct-mapped cache for stack access, pipelining, and branch-prediction logic; it uses microcode for only the most complex instructions and hard-wired logic elsewhere. The result is a 25-MHz, 10-to-12-mips, 1.25-μm CMOS design that can execute an average instruction in about 2.4 cycles, down from 6 in previous generations and close to the 1.25 to 2 cycles claimed for most RISC machines, he says.

The 32532 may be the harbinger of a new class of microprocessors, Kessler predicts, the ultimate winner of the microprocessor wars: Crisp, for complexity-reduced-instruction-set processor. Crisp will have complex instructions but RISC-like characteristics such as as cycles-per-instruction figure of close to one. Indeed, says National's Schanin, a 1.0-μm scaled version of the 32532 is in development, expected out by mid-year, which will reduce the cycles per instruction below 2 and increase the clock rate to 33 MHz for performance of 20 or more mips. And the next-generation 80486 and 68040 processors, expected out next year from Intel and Motorola, will incorporate more RISC-like features to push the number of cycles per instruction below 2, Kessler says.

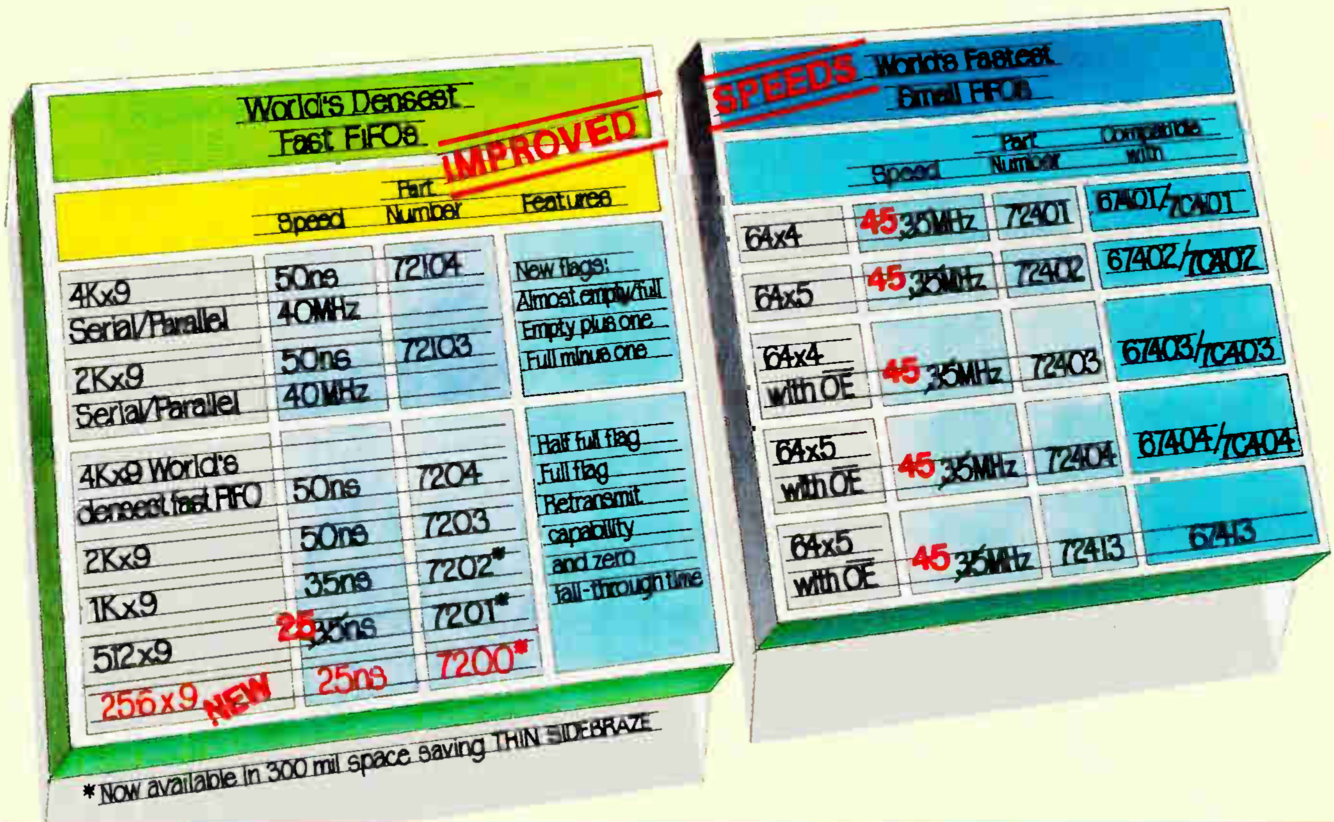
In fact, the market window for RISC to make its mark as an independent architecture is small, if manufacturers of traditional architectures such as National Semiconductor act wisely, says Schanin. "If they do not manage to establish themselves within the next two to three years, many of the independent vendors of RISC processors may find themselves on the outside looking in as CISC architectures begin to adopt many of the attributes of a RISC architecture." □

ADJUSTING MIPS TO THE REAL WORLD

Processor	Speed (MHz)	Cycles/ instruction (average)	Millions of instructions per second	Instruction quality multiplier	Adjusted mips
DEC VAX 780	5	10.6	0.47	1	0.47
DEC VAX 8800	22	2.0	11.0	1	11.0
Intel 80386	24	4.5	5.3	1	5.3
Intel 80960	20	2.7	7.5	n.a.	n.a.
Intergraph Clipper	33	6.7	4.9	n.a. (below 1)	n.a.
National 32532	33	2.4	13.8	n.a. (near 1)	n.a.
Motorola 68020	25	6.3	4.0	1	4.0
Motorola 68030	25	3.7	6.8	1	6.8
Motorola 88000	20	1.25	16.0	n.a. (below 1)	n.a.
Acorn RISC Machine	12	2.0	6.0	n.a. (below 1)	n.a.
AMD 29000	25	1.5	16.7	n.a. (below 1)	n.a.
MIPS 2000	16.7	1.4	11.9	0.8	9.5
MIPS 3000	25	1.25	20.0	0.8	16.0
Sun Sparc	16.7	1.4	11.9	0.5	6.0

SOURCES: PAINE WEBBER INC. AND *ELECTRONICS*

World's fastest FIFOs



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Thinking of getting into bed with RISC?

If you're looking for a cost-effective way to add a commercial high-end multiuser computer to your product line, you're probably looking at RISC. Should you be?

After all, how can you leverage your present investment in 680X0 family software with a non-compatible RISC product? You can't.

Better take a real close look before you leap into bed with RISC technology. Those powerful teeth you think RISC can put into your product line just might eat you alive.

RISC could devour your software investment, your company's profits, maybe even your company. RISC will force you to spend an enormous amount of time, energy and money porting new software. All the while, you'll be supporting and maintaining two separate product lines. Not to mention the fact that you'll be losing market share for every extra year it takes you to bring out your RISC product.

What about the inevitable RISC shake-out? Today, more and more RISC processors are appearing on the market. Tomorrow many of them will be history. Which processors will survive the shake-out? And what happens to those computer manufacturers who pick the wrong ones?

The consequences are obvious. A lot of companies who get into bed with RISC now will someday find themselves sleeping out in the cold. Alone.

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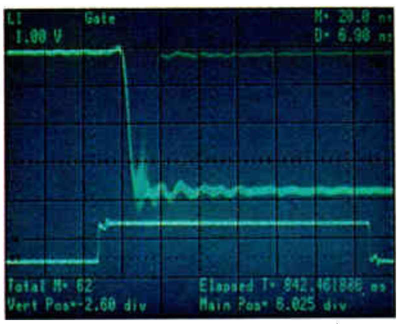
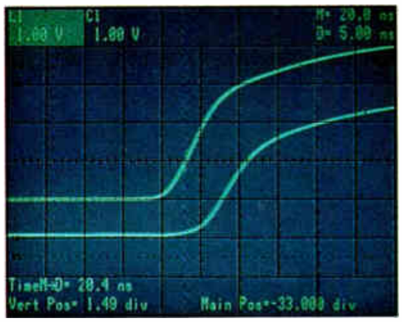
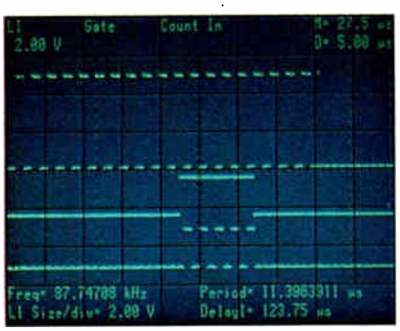


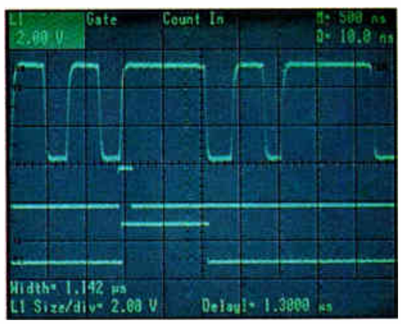
Microchannel CRT makes metastable events visible. Counter shows total number of events during elapsed time.



Built-in counter helps make propagation delay measurements with unprecedented accuracy and repeatability.



Gated frequency: top trace is pulse burst input; center is counter gate; bottom is view of what's being counted.



Make gated pulse width measurements with counter accuracy. Center is counterview trace, bottom clearly shows pulse width measured.

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TAKING A CLOSE LOOK AT THE MOTOROLA 88000

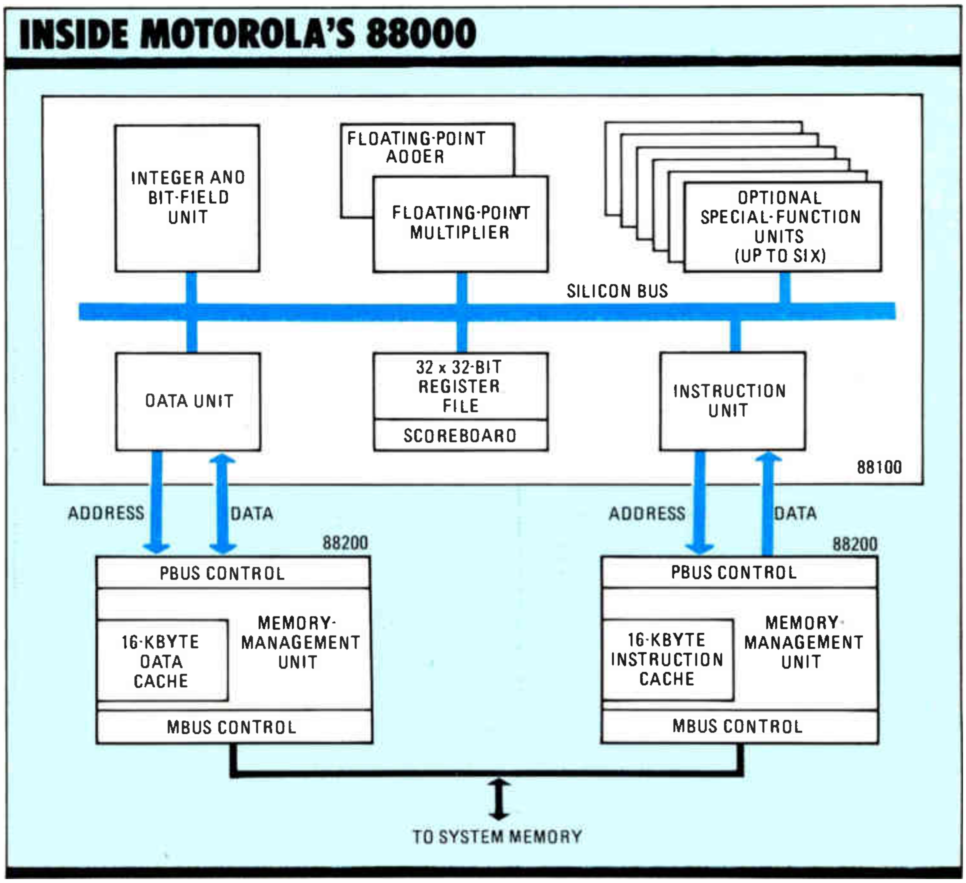
The 88000 architecture puts floating-point and integer units on board a processor and combines a memory-management unit with a cache memory in a three-chip set—a configuration that Motorola is proclaiming the third generation of RISC

by Tom Manuel

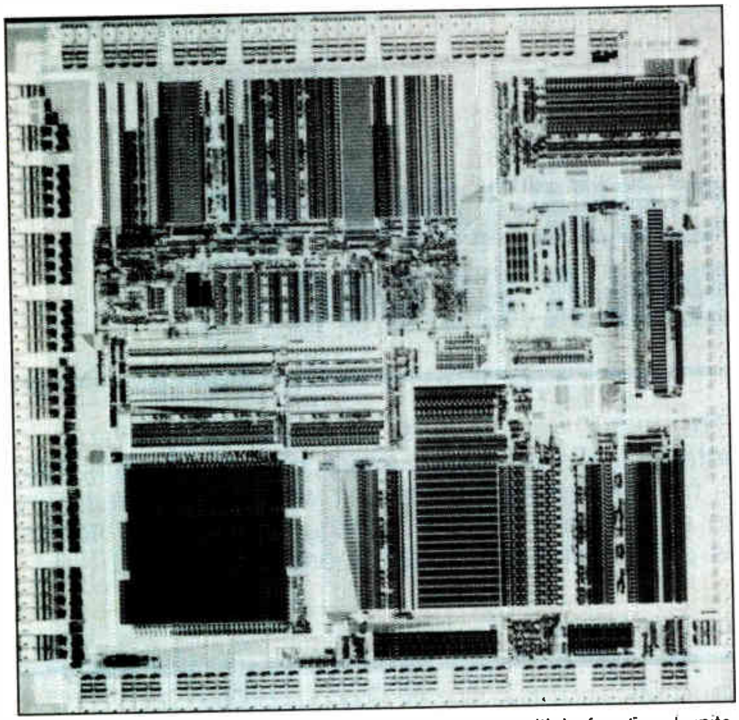
The carefully conducted buildup is over and Motorola Inc. is finally giving the world the first detailed look at its 88000, the latest entry in the RISC race [*Electronics*, Feb. 18, 1988, p.83]. And what the company is showing off is an impressive three-chip set that offers a full systems solution for a reduced-instruction-set architecture—what Motorola is calling the third generation of RISC technology.

The basic MC88000 architecture consists of a processor chip and two identical cache chips, one for data and one for instructions. The processor is the 88100, which has a small, efficient, scoreboarded register file at its heart and both integer and floating-point computational units. Running at 20 MHz, it is rated by Motorola at 17 VAX mips—that is, 17 times the performance of a Digital Equipment Corp. VAX-11/780, as measured in millions of instructions per second—and 34,000 Dhrystones performance, making it one of the fastest RISC processors around. The cache chip is the 88200, which comes with a built-in memory-management unit (see fig. 1).

What makes this a third-generation RISC architecture, Motorola claims, is the combination of on-board integer and floating-point units for the 88100 processor and the use of the 88200 cache subsystem with a memory-management unit. The first generation of RISC, according to Motorola, were crude research machines—IBM Corp.'s 801 project and the projects at Stanford University and University of California at Berkeley. The second generation consists of the RISC products now on the market—which lack the on-chip features and cache memory of the MC8800. The great advantage of the 88000 architecture is its capability for many concurrent operations. The data unit on the processing chip can transfer data between the data cache and the register file while the instruction unit transfers instructions between the instruction cache and the register file. At the same time, the integer and bit-field unit will execute instructions in parallel with an operation underway in the two-part floating-point unit. The emphasis on concurrency helps the chip set deliver twin capabilities that Motorola claims are unavailable with any other RISC processor: multiprocessing and fault tolerance.



1. The 88000 consists of one 88100 processor chip and two identical 88200 cache/memory-management-unit chips—one for instructions and one for data.



2. Motorola's 88100 processor uses multiple functional units controlled by a scoreboard register file.

The heart of the architecture is the processor's register file. "This is a key distinction between this and other RISC designs," says Roger Ross, manager of advanced microprocessor operations and the leader of the design team at Motorola's Microprocessor Products Group in Austin, Texas. "By first designing the type of register file we knew an advanced RISC processor would need, the architecture is enhanced by the register file, not encumbered by it."

The size of the register file is very important. It must be large enough for the computer's needs, but not so large that its average response time becomes too long. The need for a good, ultra-fast register file was in this case especially urgent, because the file must serve multiple functional units operating concurrently.

The designers decided on a small, efficient register file, and turned to a supercomputer architecture similar to that in Cray machines for the design. The 88100 (see fig. 2) has a file of thirty-two 32-bit registers with scoreboarding circuitry built in, which keeps track of register states so software writers don't have to. The register file triggers the execution of operations on the various function units when all the necessary information arrives.

Next, the Motorola engineers built an on-chip internal bus, the silicon bus, which connects the register file to the concurrently operating special-function units. Each special-function unit in the 88100 processor has an address on the bus. For input/output, they opted for a full Harvard architecture. That means that there are completely separate I/O units for data and instructions and each I/O unit has a full 32-bit path for both addresses and data.

The silicon-bus address tied to an instruction determines which special-function unit is to execute the instruction. Special-function unit 0, the integer and bit-field unit, is used to execute all single-clock instructions.

Floating-point operations require more than one clock cycle, and to do them the 88000 team deviated from one of the old ideas about RISC—the idea that floating-point instructions should be excluded from the processor's architecture. The early RISC designers chose to ignore floating-point instructions because they could not be handled in single cycles. Ross and his design team decided that floating-point instructions and, therefore, a floating-point unit, belongs on the register data path of a RISC machine. So they built a concurrent FPU, calling it special-function unit 1, in two parts: a multiplier and an adder.

The FPU is an integral part of the RISC processor design, with equal access to the register file, silicon bus, and the data and instruction units. Two floating-point instructions, one addition and one multiplication, can be started every cycle. No performance penalty is incurred by having to go off-chip to do floating-point instructions.

The 88000 architecture is unusually extensible. For example, Motorola has reserved 256 operation codes for each special function unit and has set aside enough silicon-bus addresses for six future special function units—numbers two through seven. Because the 88000 chips were designed using silicon-compilation tools (see p. 77), it is easy for Motorola to add special-function units as the need arises, by recompiling the chip. New operation codes are implemented in the reserved spaces; the old op codes remain unchanged, so the new version remains binary-code compatibile with earlier versions.

Customers can add special-function units themselves, by defining a unit with their own instructions and having Motorola implement it. Motorola reports that it is already working with one customer, which it declines to name, as a test case to produce the first such add-in unit.

Users can also design a special-function unit and implement it in software to try it out, because if a program uses one of the reserved op codes not yet implemented in hardware, it traps to software control. In other words, they can include the new unit's instructions in their programs. Until the new hardware has been compiled onto the chip the programs will run using software-implemented versions of those instructions.

The 88100 processor is one half of Motorola's RISC effort; the 88200 cache subsystem with its MMU is the second, equally important half. It is designed to work with the four-port Harvard architecture of the processor, with the 32-bit address and data ports of the data unit connecting to a bank of up to four cache/MMUs. The two corresponding sets of 32-bit lines from the instruction unit connect to their own cache subsystem, which can also hold up to four cache/MMUs. The limit of four cache chips is a physical limit imposed by the CMOS/TTL circuitry. When the chip set is implemented in other technologies, the number of chips can increase—the architecture allows up to 128 per side.

Motorola chose to make the 88200 a set-associative cache, rather than a direct-mapped cache. In the former, every main-memory address can be mapped into two or more cache locations. In the latter, every main-memory location is assigned to a cache address.

The set-associative configuration greatly reduces thrashing, which occurs in a direct-mapped cache when two sequentially used addresses have collided in the cache memory.

The 88200 is a complete four-way set-associative cache and MMU subsystem with 16 Kbytes of fast static random-access memory cache per chip. A complex memory-bus control section automatically handles cache coherency for multiprocessing configurations. The set-associative configuration gives every main-memory location four homes in cache, which helps lesson collisions in the cache between main-memory addresses. The 88200 is also a physical cache as opposed to a logical cache, which some RISC-chip users implement. The difference is that a physical cache does not have to be completely flushed between task switching, as a logical cache must be.

The MMU handles address translation, which can run at the same time data is looked up in the cache. A part of the logical address is fed to the cache when the complete address goes to the MMU. When there is a cache hit, the cache delivers all four candidates from the four-way association, but because it has used only part of the logical address, it does not know yet which one is the correct one. At this point, the translated physical address from the MMU is also ready because it has beeen calculated in parallel. But since all four cache values have been found and presented at once, the correct one can be quickly selected.

Another concurrent operation is the on-going cache-coherency control. A dedicated processor on each 88200 chip, called the memory-bus controller, takes care of the cache coherency. The controller continuously watches the memory bus to find out what changes are being made to locations in memory and in

HOW MOTOROLA DESIGNED AND BUILT ITS RISC CHIPS IN ONLY 20 MONTHS

Motorola's 88100 chip was designed and rendered in silicon in only 20 months. This is quite a feat—the 88100 is a RISC microprocessor with an integrated floating-point unit on a chip containing 180,000 transistors. But what makes it really impressive is that at the same time Motorola also built the companion 88200 chip, a cache memory and memory-management unit containing 750,000 transistors—and did it in only 11 months. This contrasts strongly with the three to five years previously needed to design and build a single, far simpler microprocessor.

Motorola managed the feat by using silicon design methodology—specifically, the Generator Development Tools from Silicon Compiler Systems Corp. of San Jose, Calif.

Included in the GDT tool set is a front-end simulator which allowed Motorola to optimize the 88100 instruction set for C language operation. The instruction set contains those instructions used most frequently by a C compiler. This optimization is one way the chip achieves its high instruction-execution speed—17 million instructions/s.

Also in the tool kit are the back-end automatic procedural layout tools—the silicon compilers themselves. These allow the designer to alter the chip layout to achieve the best possible performance and best possible use of chip space right up to the moment he commits the design to silicon.

Early in the design cycle, Motorola designers created a simulation of instruction execution, using the GDT multimode simulator, called Lsim. In effect, they were simulating, very early in the design cycle, the operation of registers and the flow of data between the registers as instructions are executed.

In designing the instruction set of the 88000, one of the key concerns was to minimize the time needed to perform a subroutine call, which compilers rely on heavily. Jumping to a subroutine and performing a context switch was to be done as quickly as possible.

The design team's solution was to use scoreboard registers, a complete set of central-processing-unit registers, for each subroutine. This means that when the computer switches tasks, it doesn't load and unload registers—it simply stops using one set of registers and starts using another. This occurs in one clock cycle.

After the design had been completely simulated, it was given to the procedural layout tools. Motorola provided Silicon Compiler with a behavioral model of the static random-access memory cells for the 882000. These cells came from Motorola's SRAM designers. Motorola contracted with Silicon Compiler Systems to create the complete cache and MMU chip. When the time came to build the chip's memory array, the Silicon Compiler design team used a highly optimized SRAM memory cell that had been hand-designed on a Calma GDS-II layout system. The layout was converted into an L language description. The L language describes all components in the GDT environment. Then, to create a 16-Kbyte SRAM memory array, 8 bits wide by 16 Kbits deep, Silicon Compiler Systems simply specified the array size and the compiler did the rest.

One of the most powerful features of compilation allows a designer to make changes right up to the end. In the case of the 882000, Motorola called three weeks before the day Silicon Compiler Systems was to deliver masks of the chip and asked the design team to add one more bit in the memory array. "We were able to add the bit and its associated logic, recompile the entire layout, and not miss a day in the delivery schedule," says Hal Alles, vice president of engineering at Silicon Compiler.

Another example of a compiler's ability to accommodate change easily was in the design of a content addressable memory on the 882000. Silicon Compiler did not know exactly how much space it would have left over on the chip after everything else had been designed, but however much it was, the designers wanted to fill it with as big a content-addressable memory buffer as possible.

"Once the design was complete," says Alles, "we measured the space on the final chip that could accommodate the cell. It could accommodate 56 words, so we compiled a cell with this many words and inserted it into the available space." *–Jonah McLeod* all the caches and keeps its own cache coherent—the current correct values are retained; invalid ones are flushed out.

The complete chip set is designed for concurrent operations—Motorola claims 11 operations can occur at once. Typically, the cache subsystem will perform cache-coherency control, check for cache hits and misses, and do address translation. At the same time, the data unit and the instruction unit on the processor chip will store data in the register file, and the integer unit will execute an instruction and the floating-point unit will perform two operations.

A high level of concurrency helps to provide two features that no other RISC implementation has, according to Motorola. Multiprocessing and fault tolerance are both inherent in the 88000 architecture. Motorola's Microcomputer Group in Tempe, Ariz., is taking these multiprocessor and fault-tolerant features and mounting the chips in packages smaller than the standard pin-grid arrays to produce what it calls the Hypermodule in several combinations of processor and cache chips (see panel, below).

The chips from the microprocessor products group in Austin, Texas, are mounted in 180-pin pin-grid-array ceramic packages measuring 1.7 in. on a side. By contrast, the chips for the Hypermodule are in pad-grid arrays measuring 1.1 in. on a side.

Motorola is ramping up production of the first 20-MHz 88000 chips for volume deliveries by year end. Customers will be producing systems by the first quarter of 1989. The development group is going to 25-MHz versions by the end of the year—it is starting up its 25-MHz alpha site production now. Prices for the 20-MHz parts will be $495 for the 88100 processor chip and $795 for the 88200 cache/MMU. The company also has started development of an emitter-coupled-logic version in cooperation with Data General Corp. and says it is looking at gallium arsenide for the longer term. □

For more information, circle 480 on the reader service card.

FINE-PITCH PAD GRID ARRAYS ARE KEY TO MOTOROLA'S HYPERMODULE

Cramming up to four reduced-instruction-set processors, each with both floating-point and integer units, and eight cache/memory-management-unit chips, plus three 100-pin miniature connectors, onto a module 8.5 by 3.4 by 0.441 inches, produces a very dense, very high-powered processing module for system building. The microcomputer division of Motorola Inc., in Tempe, Ariz., decided that the 88000 chip set from its sister Microprocessor Group needed this compact packaging for many applications. So the Tempe team developed a family called Hypermodules containing different numbers and configurations of 88100 processors and 88200 cache/MMUs.

This development required both an infusion of new packaging technology and a full-fledged multidivision effort by Motorola. Ordinarily, the processor and the cache/MMU were both housed in pin grid arrays that were 1.7 in. on a side with pins on 100-mil centers. This package was much too large for the planned module and a completely new chip package had to be created.

Under the overall guidance of Motorola Computer Devices, Motorola's cellular telephone group designed a novel ceramic pad grid array (a multilayered structure whose input/outputs are brought out to a grid of pads on the bottom of its square package) with an overall footprint of 1.1 by 1.1 in. and with 288 pads on 60-mil centers.

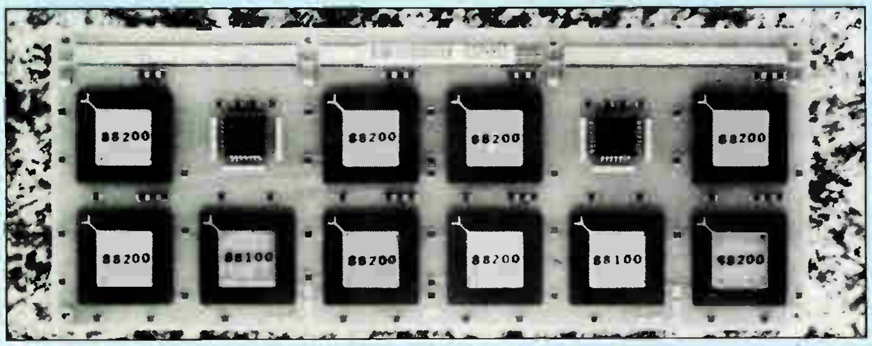
Pads for signal, power, and ground take up 186 of them. The remaining 102 are for interfacing to thermal vias on a mother board. Pad grid arrays had first been suggested by Honeywell Inc. for chips in the Department of Defense's Very High Speed Integrated Circuit program; Motorola appears to be the first commercial user.

The pad grid arrays required a special substrate. This resulted in a 10-layer board whose power and ground planes consisted of copper-invar-copper cores. These composite cores served the dual purpose of matching the modules' temperature coefficient of expansion to that of the ceramic packages, to prevent cracking of solder joints and to provide heat sinking for the module's complement of chips. Thermal vias bearing against the thermal pads of the pad grid arrays allow each chip to share the built-in heat-sinking evenly.

The module is normally mounted to a motherboard by six screws. Electrical connection between module, motherboard, and other systems is through the three miniature connectors.

Motorola is drawing on many divisions for the manufacturing of the Hypermodules. Motorola's semiconductor group will bond chips into the new carriers and its pager division will assemble the full module. The Microcomputer Device division will oversee all testing and integration of the completed modules.

By this summer, Motorola plans to have a simple version of the Hypermodule with one processor and two cache/MMUs in standard pin-grid arrays mounted to an identically sized printed-circuit board available for evaluation. Called the model HM88K-1P32, it will be priced at $1,400 in 100-piece lots. By the third quarter, prototypes of the pad grid array module will be available. By the fourth quarter, full-fledged Hypermodules will be at beta sites. Full-scale production of will start in the first quarter of 1989. *–Jerry Lyman*



In one version, Motorola's new packaging scheme, the Hypermodule, holds two 88100 RISC processors and eight 88200 cache/memory-management unit chips.

V70: 32-BIT CMOS MICROPROCESSOR

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The V70 features 32 general purpose registers (each 32 bits wide) and a modern orthogonal instruction set optimized for high-level languages and operating systems. V70 instructions are fully compatible with the V60. A high-speed emulation mode gives compatibility with V20 and V30 software.

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NUMBER 139

NEW AUTOMATED INTELSAT EARTH STATION

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Our Computerized Supervisory and Control System (CSCS) allows the operator to centrally control, monitor, and report on the operating status of equipment and circuits with utmost efficiency.

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Moreover, the Bukit Timah earth station is equipped with our Time Division Multiple Access/Digital Speech Interpolation (TDMA/DSI) equipment for maximum utilization of satellite circuits.

For coverage of the Pacific Ocean region, the Bukit Timah No. 2 earth station is also under construction by Singapore Telecom and NEC is supplying similar advanced systems.

FIRST CCD CAMERA DESIGNED FOR FIELD PRODUCTION

Following up the success of the SP-3A for news gathering, NEC introduces the EP-3, the first CCD color camera (NTSC system) expressly designed for field production.

Incorporating exclusive high density CCD sensors, the 2nd-generation solid-state camera goes head-to-head with any tube-based portable in picture quality. It offers 700-line horizontal resolution, 62dB S/N ratio and F5.6/2,000 lux sensitivity.

The threshold illumination level is 15 lux (+18dB gain).

The new field production camera features virtually no smear and a 7-speed electronic shutter (1/60 – 1/1,500 sec) thanks to NEC's anti-smear, interline frame transfer CCD technology.

The EP-3 camera has a host of sophisticated control functions to support the creativity of videographers. Its automatic functions include White Balance with two memories, Auto Black Balance and Auto Iris/Auto Black Level.

The EP-3 also provides complete flexibility in operation. It is remotely controlled via multicore, triax or wireless systems. For recording, either Beta or MII-format VTR is attached.

NEW OEICs TRANSMIT 52KM AT 1.2 GBPS

Optoelectronic ICs developed at the NEC Optoelectronics Research Laboratory were successfully tested in a recent experiment using a 1.3μm optical single-mode fiber. The new OEICs set a world record for high-speed, long-distance transmission without repeaters – 52.5km at data rates of 1.2Gbps.

The transmitter OEIC delivers over 10mW in output power with a low 13mA threshold current. Modulation up to 2.4Gbps is possible in the NRZ mode. The 350 x 900μm chip integrates a buried type InGaAsP laser diode and high-speed driver (3 GaAs MES FETs) on the same InP substrate.

The receiver OEIC features –26dBm sensitivity. It packs an InGaAs PIN photo-diode and low-noise amp (4 GaAs MES FETs, 5 GaAs Schottky diodes and one resistor) on a 1 x 1mm InP chip.

The new high-performance OEICs are expected to play key roles in terminal equipment for the emerging optical broadband ISDN and optical networks between cities or within intelligent buildings.

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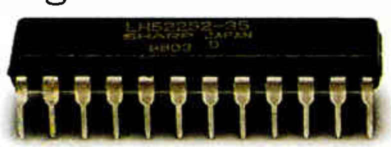

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LH52259	32k x 9	35 ns/45 ns/55 ns	3Q 1988
LH52251	256k x 1	35 ns/45 ns/55 ns	3Q 1988
LH52256	32k x 8	70 ns/90 ns/120 ns	Immediate
LH5261	64k x 1	25 ns/35 ns	1Q 1989
LH5262	16k x 4	25 ns/35 ns	4Q 1988

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CHOOSING A RISC CHIP: WHAT DRIVES CUSTOMERS?

RISC-chip users want performance, performance, performance; the first customers for Motorola's 88000 cite especially its multiprocessing performance growth path, but Unix software and vendor stability also enter into their decisions

by Jonah McLeod

The reason for RISC all along has been the performance advantage the design philosophy offers. All other things being equal, a system house shopping for reduced-instruction-set computer chips will pick the ones that give him the highest system speed, and the promise for more speed in the future.

But all other things are not equal, and customers also find themselves looking at the vendor itself, wondering how good its customer-support record is, how much system software it is making available, how likely it is to survive bad times in the electronics market, and how massive a bandwagon effect it can get going to encourage independent software publishers to support the hardware architecture.

Motorola scores well in all these areas, say the companies that plan to develop products around its new 88000 RISC processor. Tektronix, Data General, Convergent Technologies, Encore Computer, and Stratus Computer are among the system manufacturers that have revealed plans for products based on the 88100 central processing unit and companion 88200 cache memory-management unit. Others are keeping their commitments private so as to avoid alerting their competition.

Those that are talking talk most about the 88000's performance. Compute-intensive applications like graphics work stations and communications servers demand market-leading performance, which the chip set promises. Multiprocessing is another performance-related issue, especially for bigger systems—superminicomputers and larger. The 88000 was designed with parallel systems in mind (see p. 75), and Encore, Stratus, and Data General cite this virtue as the deciding factor for their 88000 selection. Multiprocessing, they agree, is the road to take in the 1990s.

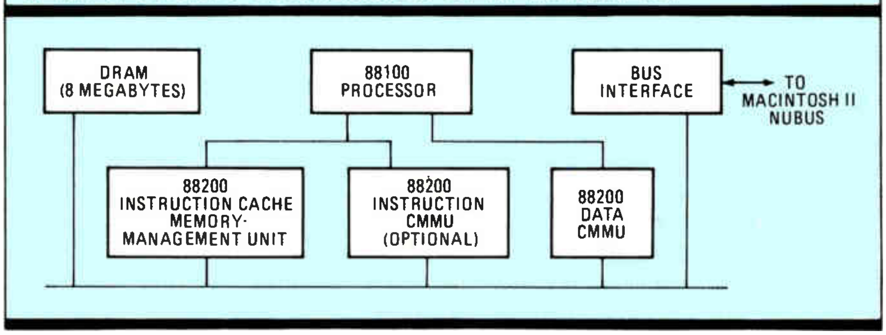
Motorola is in good shape to satisfy the types of customer concern that do not relate directly to performance. In terms of customer service and vendor stability, for example, Motorola is a standout. The only RISC competitor that is its peer in those areas is Intel Corp., another latecomer to the RISC party [*Electronics*, April 14, 1988, p. 97].

Furthermore, Motorola is making a hard charge in the software-support area, devoting internal resources to preparing 88000 compilers and signing on Unisoft Corp. to help get a Unix port ready, for example. It has finalized its agreement with AT&T Co. for the development of an application binary interface standard for the 88000 [*Electronics*, March 17, 1988, p. 32]. And Motorola has already got a big, noisy bandwagon rolling for the 88000 that should help convince software vendors to port programs to 88000-based systems. Many committed customers are talking, and in early April, Motorola enthusiastically supported the formation of the 88open consortium, a group of some 30 hardware and software companies that have joined forces to promote and define standards for the 88000 [*Electronics*, April 14, 1988, p. 31].

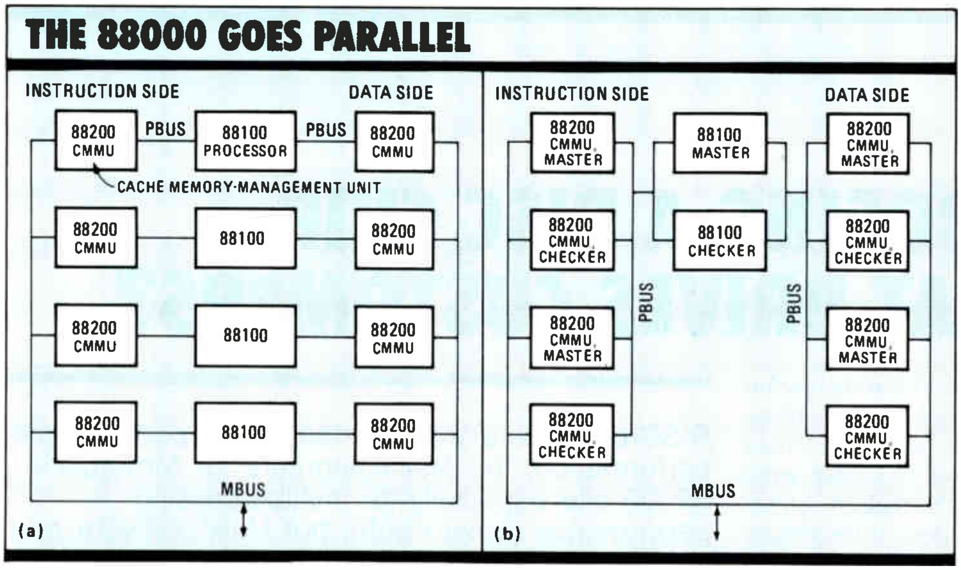
Tektronix Inc. was one of the first to jump on the Motorola bandwagon. One of the first products to use the 88000 is a system-development board built by the Tektronix Technologies Group (see fig. 1). The board fits into a Macintosh II personal computer, which becomes the development system. Tek's board comes with the minimum of one 88100 chip and two CMMU chips, or can carry a third CMMU so that the instruction cache can be doubled in size to improve performance.

Tektronix's board is a development tool available only to members of the 88open Consortium. The Bea-

TEK'S BOARD FOR 88000 DEVELOPMENT



1. An add-in card from Tektronix that fits into the Apple Macintosh II personal computer can be used to develop software for systems based on Motorola's 88000 while they are still in design.



2. Multiprocessing systems are primary design targets for the 88000, as in a four-processor, eight-CMMU setup (a), and a fault-tolerant system that checks up on itself (b).

verton, Ore.-based company also announced it would use the 88000 to increase the computing capability of its 4300-series color-graphics work stations, which are currently built around Motorola's 68000 family. The current generation already has a dual-processor architecture with separate compute and graphics engines. The new RISC chip will first be used to extend the work stations' compute capability, and may be used later to upgrade the graphics engine. "Although the 68000 and 88000 are not compatible, the new chips do lend themselves to moving applications over from the 68000 environment [better] than if the chips were made by two different vendors," says Robert Anudson, Tektronix's engineering work-station manager.

Data General Corp., Westboro, Mass., is working with Motorola to develop an emitter-coupled-logic version of the 88000 (see p. 32). It sees its choice of the 88000 for future systems as a part of its major push into the Unix marketplace. Users want industry-standard systems, says Ward MacKenzie, vice president for corporate marketing, and the Unix market is growing fast. "With industry-standard systems, the software is well-defined and transportable, and RISC is an especially good platform for Unix," he maintains. "Optimized compilers are highly efficient in transporting Unix and the RISC architecture couples well with compiler technology. We chose the 88000 after evaluating all the other RISC microprocessors because we think it offers the best current performance and the most extensible RISC environment for future growth."

"We had our own internal program to develop a RISC processor," says Donald Lewine, senior technical consultant with Data General's systems development division. "When we saw the 88000, we decided it was counterproductive to develop our own." The company plans to develop a separate line of products that are not software compatible with the MV series of computers currently being offered. But "we are not abandoning our current product line," Lewine emphasizes.

Convergent Technologies Inc. of Santa Clara, Calif., is exploring the use of the chip set as a back-end processor in the company's S series of computers. Thomas Mace, group product marketing manager for the company, says there are 20,000 applications now for the S series and the chore of moving them over to a new CPU is too formidable. The company plans instead to use the Motorola 68030 and 68040 as future compute engines. "The RISC chips could be used as data-base servers and as communications servers to our existing computers," says Mace.

Features of the 88000 that suit it to use as a server include its register-scoreboarding capability, which makes it possible for the system to switch from one task to another (called a context switch) in one clock cycle. To do this, the 88100 chip has duplicate sets of CPU registers used by different tasks running concurrently in the system. Switching from one task to another requires only a change in register sets.

"In addition, the 88000 offers the system manufacturer an architecture that more easily lends itself to multiprocessing than any of the other commercially available RISC chips," says Mace. There can be multiple processors, each with its own data and instruction caches (see fig. 2). Inside the device are the features that ensure cache coherency—they make sure that the cache always contains current data.

"Motorola had a clear strategy of a chip set that supports a symmetric multiprocessing architecture," says Frank Pinto, vice president of marketing at Encore Computer Corp., another 88000 supporter. "The chip set easily maps into the Encore architecture." The Encore Multimax 320 system has two processors per card and 10 cards in a system.

Pinto says the Marlborough, Mass.-based company plans to put more than two 88000s on each processor card in a future version of the system. While the current system performs 40 million instructions/s, future versions will have even more performance on a single card. "With the 88000, by 1990 we could have a 400-mips computer system," Pinto says.

Another thing the 88000 has going for it is completeness. "With other RISC chips, the memory-management unit and floating-point coprocessor have to be added separately," says Pinto.

Something that falls out of the 88000 multiprocessor architecture is the ease with which fault-tolerant systems can be configured. This fact has not been lost on Stratus Computer Inc., a manufacturer of fault-tolerant on-line transaction-processing systems. The company plans a future generation of 88000-based systems that will be software-compatible with its current family of XA2000 continuous-processing systems. Products are due in the early 1990s. □

AMD PUTS CACHE MEMORY ON ONE PROGRAMMABLE CHIP

The device combines controller logic and static RAM to form a component of the 29000 RISC processor

Cache-controller logic has usually been implemented with discrete circuits and cache-memory array in high-speed static random-access memory. The move to higher levels of cache integration with cache controllers was started by chip makers such as Intel Corp. and NEC Corp. Now Advanced Micro Devices Inc. is going to the next logical step: integrating an entire 8-Kbyte cache memory—controller logic and SRAM array—onto a single chip.

Scheduled for sampling in the fourth quarter of 1988, the Am29062 Integrated Cache Unit is a cache-memory component for the Austin, Texas, company's Am29000 reduced-instruction-set microprocessor [*Electronics*, March 19, 1987, p. 61]. Like the other members of the Am29000 RISC family (see p. 159), it is implemented in high-density CMOS technology. The Am29062 employs sophisticated mainframe-style caching mechanisms; several features match it to high-performance applications. The ICU includes user-programmable caching parameters, extensive multiprocessor support, compatibility with very high clock speeds, and complete support for the Am29000's pipelined, burst-mode bus (see fig. 1).

The Am29062 can be designed into systems as an instruction cache, a data cache, or a combined instruction and data cache. Many RISC systems based on the 29000 main processor will employ two of the chips—one for data and one for instructions. The Am29000 central processing unit has separate instruction and data buses, so a two-cache system can be built with no multiplexing or demultiplexing logic. In addition, if cache arrays larger than 8 Kbytes are required, multiple ICUs can be cascaded together (see fig. 2).

The new ICU's 8-Kbyte cache is organized in a two-way, set-associative fashion, instead of the simpler direct-mapped organization used in other controllers. The AMD device has a 16-byte block (also called line) size, instead of the conventional 4-byte block. This reduces transfers back and forth between the processor and the 29062, and increases the number of hits, or correct matches of data.

The cache works by comparing the address sent to it by the processor with a set of addresses or tags stored in an internal tag buffer. Associated with each tag is a collection of data bytes. If the address matches one of the tags (a cache hit), the cache either supplies the processor with the data bytes associated with the tag (reads), or modifies the data (writes). If no match is found (a cache miss), the cache initiates an access to main memory at the appropriate address. The data at that address is loaded into the cache and either supplied to the processor or modified.

The block size refers to the number of consecutive bytes that are associated with a tag. When a cache miss occurs, a new block is brought in from main memory. The more bytes that are fetched, the fewer main memory accesses have to be made if programs have reasonable locality. In general, increasing the block size improves the effective memory access time. The Am29062 contains 512 blocks of 16 bytes and therefore 512 tags; each tag consists of a 16-byte block.

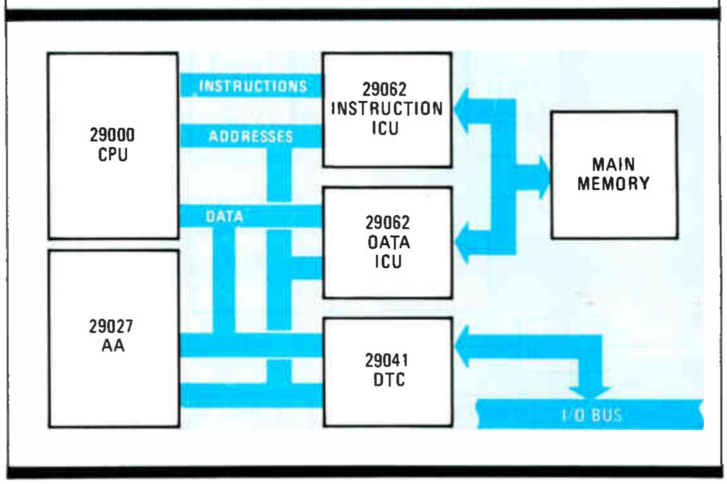
The cache's set associativity determines its flexibility in choosing what data to overwrite when a cache miss occurs. New data must then be brought into the cache from main memory. The more associativity, the more flexible the cache and the less likely that useful data will be overwritten. In a direct-mapped cache, each main memory location can be written into only one cache location, so new data must overwrite the existing data. In a two-way set-associative cache, each location in memory is mapped into two locations in the cache; if one cache slot is in use, the other one can be used instead of overwriting the first.

The cache's efficiency depends on both line size and set associativity—not just the size of the cache. In a cache system based on two Am29062s, a 16-Kbyte cache size, along with 16-byte block size and two-way set associativity, will yield a hit rate in excess of 95% for most applications.

The Am29062 was designed for maximum flexibility by implementing cache mechanisms, but the system programmer can specify the policies. One example is the cache-write strategy. For write accesses to a cache, a strategy must be chosen for updating main memory even when a cache hit occurs. (On reads, of course, main memory is unaffected when a hit occurs). There are two main cache-hit write strategies: write-through or copy-back. The Am29062 permits either protocol to be used on cache writes.

The simplest write strategy is write through. Here,

A COMPLETE RISC PROCESSOR



1. AMD's ICU, containing a user-programmable 8-Kbyte cache for the Am29000's RISC central processing unit, supports multiprocessor operations.

main memory is updated every time the cache is altered. Since the cache and main memory are changed simultaneously, they always contain the same data and main memory is always up to date. However, little or no benefit is derived from the cache for writes and the cache is only about half as effective as possible.

Under the copy-back strategy, memory is updated only when a line that has been modified in the cache needs to be overwritten by another line. At that point, the old modified line is "copied back" to memory before it is overwritten. Copy back minimizes memory accesses providing the highest performance, but requires more hardware support. Hardware-support mechanisms are built into the cache controller, so that a user can employ copy-back mode whenever high performance is required. Copy back can be selected for all writes, or specified on an access-by-access basis.

Another programmable policy is the number of bytes loaded from memory on a cache miss. There are several parameters that may be specified: the subblock size; which nonvalid words in the block to replace; and whether burst-mode memory accesses are enabled.

A subblock is a special Am29062 concept that provides much of the same effect as a variable block size. Data is fetched from memory to fill subblocks, not blocks, and the subblock size can vary from 1 word (4 bytes) to 4 words (16 bytes).

The cache loads data when a miss occurs but the exact number of words loaded is programmable. Options that can be specified are: all nonvalid words in the current subblock, all nonvalid words from the address of the missed access to the end of the subblock, or all nonvalid words from the address of missed address to the end of the next subblock. So the cache can fetch anywhere from 4 bytes to 32 bytes, depending on the subblock size and this parameter.

When performing a load from memory, the Am29062 may employ a special optional technique called burst mode to transfer all bytes in the load in a single memory access. Since only one access is made, only one address is transferred to memory. The next few clock cycles transfer the data words. Burst mode transfers of an entire block are often twice as fast as multiple conventional one-word transfers.

The choice of block replacement algorithm is also programmable. The Am29062 provides three independent block replacement algorithms—Least Recently Used, Random, and External—and lets the programmer select one of these. Other programmable parameters include enabling or disabling the prefetch mechanism, the write buffer, and the write-allocate facility. These parameters determine whether the cache prefetches data in burst mode; whether writes to memory are buffered (thus allowing the processor to proceed without waiting); and whether a new block is loaded when a write access misses (or memory is simply modified).

The main problem with multiprocessor systems is the cache's data consistency problem. This occurs when the caches for two processors contain copies of the data at the same memory location. The Am29062 provides several mechanisms to overcome this problem, such as the bus-watch facility, ownership-support mechanisms, and the interlock facility.

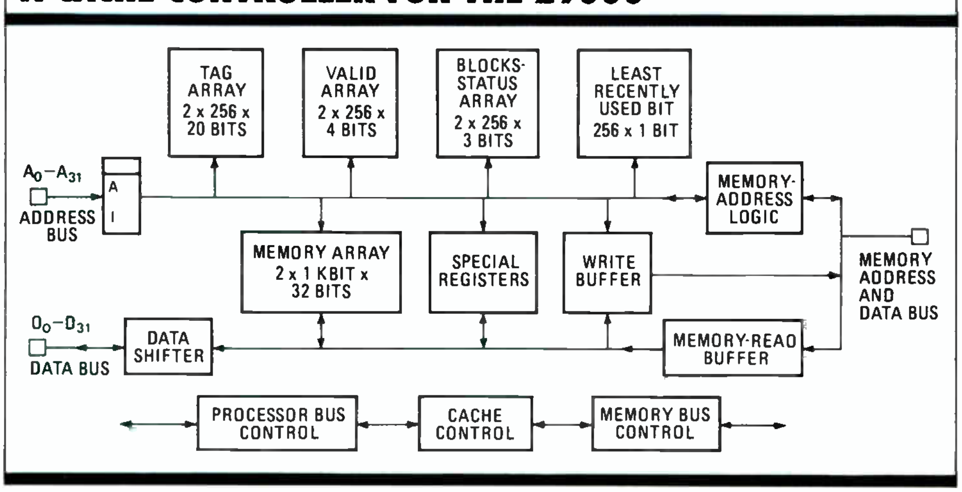
When bus watching is enabled in a cache, the cache hardware continuously monitors the memory bus for any access that matches one of its tags. If such an access is detected (a match), the cache may take any of a number of actions, depending on the type of access and which control bits are set. For example, it can invalidate its own matching block (write operation on bus); update its own matching block (write operation on bus); intervene on the memory bus, supplying the data in its own block to the accessing device (read operation on bus); or update memory (read operation on bus).

The action taken by the cache depends on the global ownership policy established by the system's programmer. Each block can be in one of five states (exclusive write-through, exclusive copy-back, shared unmodified, shared modified, not valid). The cache's ownership mechanisms perform the appropriate action on each block, depending on its state of global policy. The basic principle underlying all ownership policies is that a variable (the data in a block) is owned by only one cache or is unowned. This cache contains the most up-to-date copy and is responsible for maintaining its consistency.

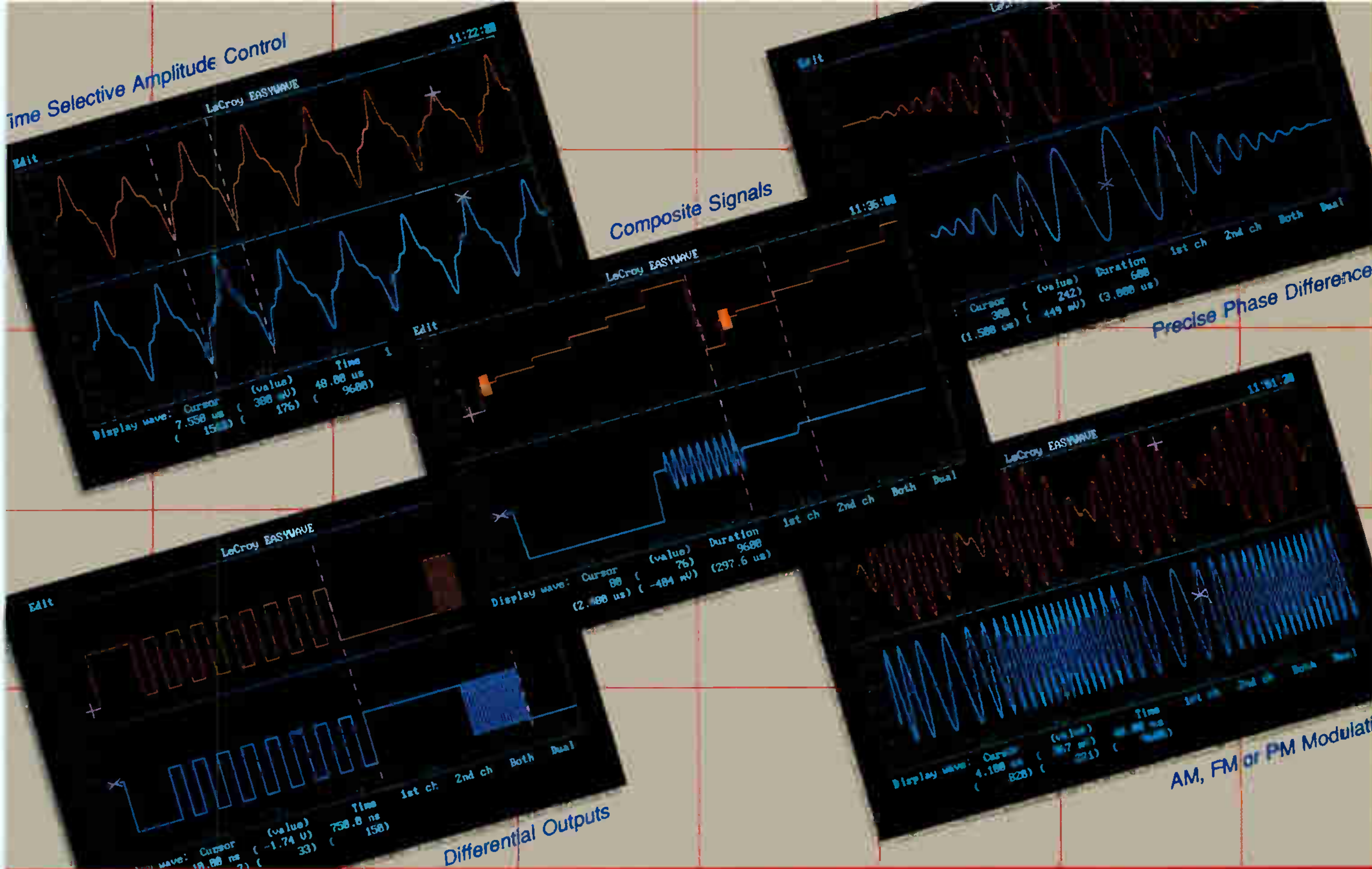
The Am29062 is compatible with the Am29000 CPU chip's bus interface and can be connected directly to it. Also, the Am29062 is designed to work with future CPU versions, up to a clock rate of 40-to-50 MHz. The CPU has three 32-bit buses—address, data, and instructions. The Am29062 connects to all three buses, and supports all of the Am29000 bus access protocols (single access, pipelined access, and burst-mode access). – *Bernard C. Cole*

For more information, circle 481 on the reader service card.

A CACHE CONTROLLER FOR THE 29000



2. The Am29062 can act as an instruction or data cache controller for the 29000 CPU; the ICU is compatible with the bus interface of the CPU, providing direct connections to each controller.



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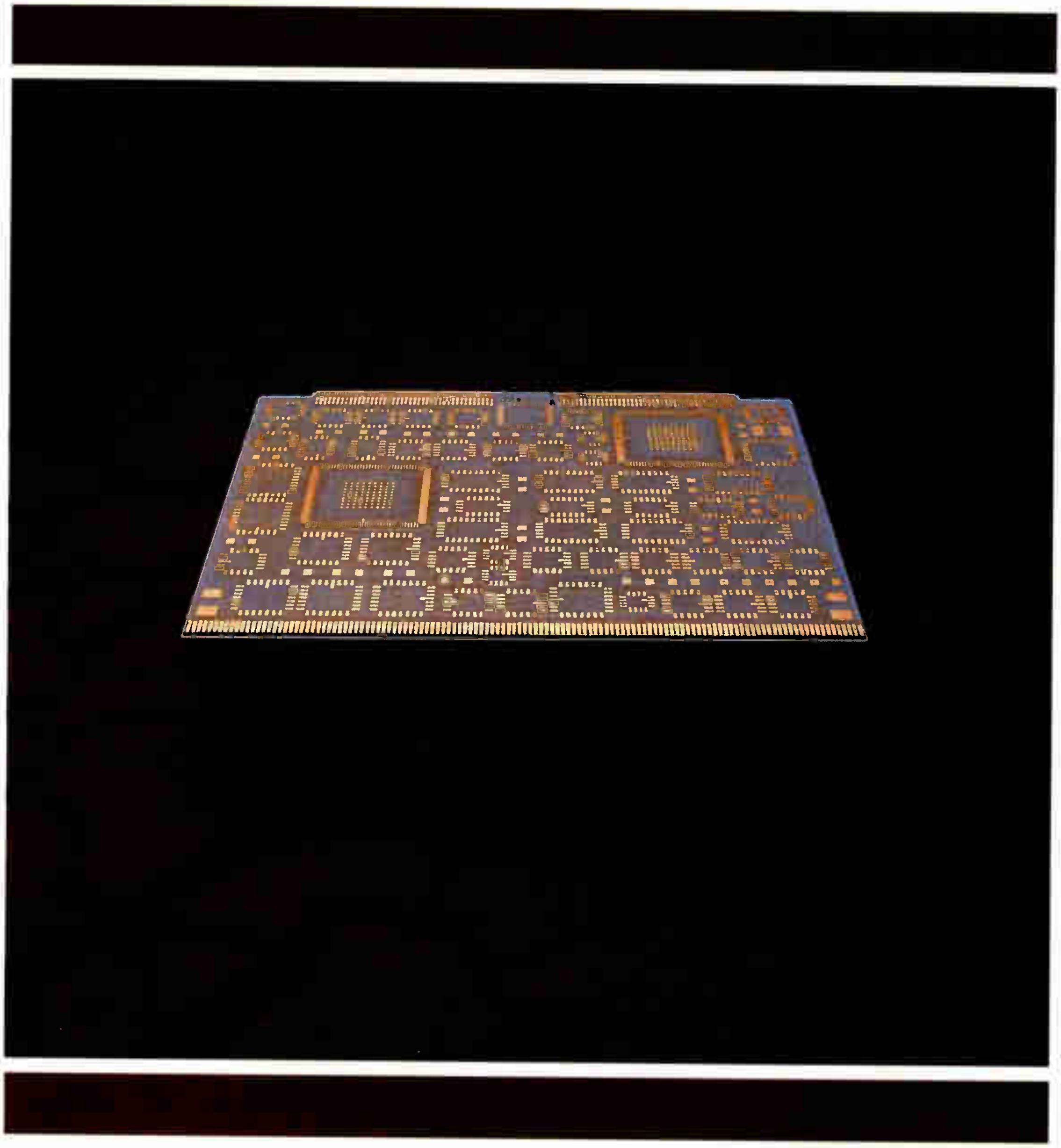

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CHIP SET CUTS POWER-SUPPLY DESIGN TIME UP TO 60%

International Rectifier's solution lets engineers use system, rather than circuit-design, approach

A set of power-system chips that will simplify the design of advanced off-line switched-mode power supplies and motor controls is on the horizon. The packaged components of the new chip set from International Rectifier Corp. will reduce both system design time and board space. The El Segundo, Calif., company's new devices transform design of switching power supplies and motor controls into a system design consisting mainly of interfacing circuit blocks rather than the rigorous circuit design required with discrete components. This will let engineers concentrate more on overall system issues instead of the problems of discrete power designs, thereby cutting design time by 50% to 60%.

The chip set comprises two power integrated circuits—the brand-new IR2110 half-bridge driver and the IR2100 buck converter bias supply, plus power and current-sensing MOS FETs, diodes, and rectifiers. The IR2110 is a dual-channel, monolithic, high-speed driver with floating high-side outputs up to 500 V and ground-referenced 10- to 20-V low-side outputs (see fig. 1). Designed to interface with low-level logic control signals, it can drive a pair of n-channel, high-voltage power MOS FETs or isolated-gate bipolar transistors in half-bridge or dual-forward converter topologies.

Compatible with CMOS logic levels, the high- and low-side inputs use Schmitt triggers to provide high noise immunity and accept inputs with slow rise times (see fig. 2). The two output drivers are independent and use identical low cross-conduction totem-pole output stages, each capable of sinking 2-A and 1-A sourcing. Interface to the floating high-side output stage is accomplished by a high-voltage level-shifting circuit operated in the latching, pulsed-current mode for low quiescent power dissipation and high dV/dt immunity.

The special level shifter is needed since the upper power device of a half wave bridge has a gate potential that can vary from ground to the value of the input dc voltage supply. The level shifter provides a floating voltage referenced to the source terminal of the upper power switch for driving its gate.

The other power IC in the combination is the IR2100 buck converter bias supply designed to be operated off-line. The chip accepts dc inputs between 100 and 500 V, operates at 150 kHz, and provides a fixed 15-V regulated output with a load current up to 500 mA. The IR2100 will be available in either TO-220 or TO-3 packages and the IR2110 will be available in a 14-pin plastic dual in-line package, small outline packages, or a sidebrazed ceramic DIP. The IR2100 will cost $9.10 each and the IR2110 $7.00 each in 1,000-piece quantities. Both parts will become available in the last quarter of this year. The remaining chips in the set are the IR current-sensing HEXSense power MOS FETs, and HEX FET power MOS FETs.

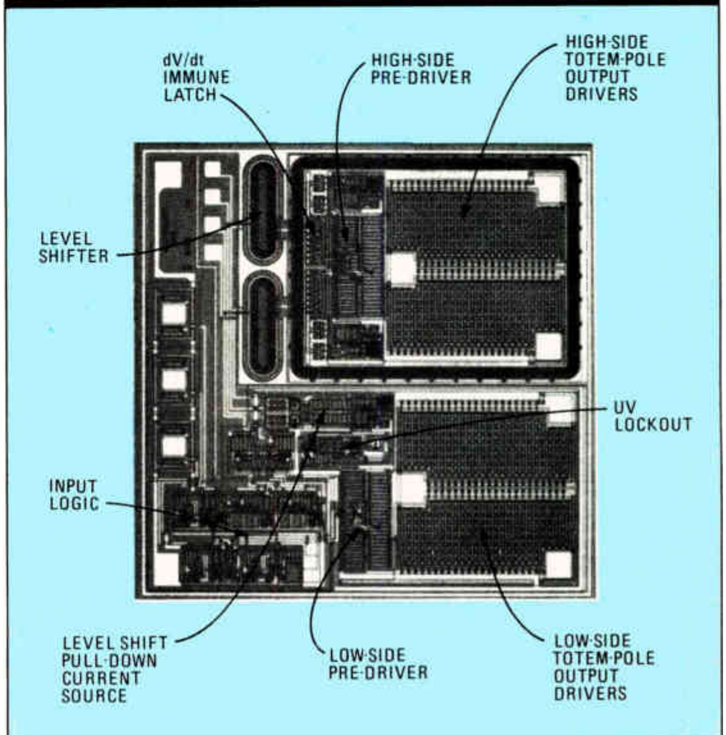
The basis of the chip set's two power ICs is International Rectifier's high-voltage integrated-circuit (HVIC) technology, which combines low-voltage bipolar and CMOS devices with high-voltage DMOS output devices. The high-voltage junction isolation process is based on a modular biMOS process flow that includes integration options for a wide variety of small-signal and power output devices.

The process is capable of a variety of lateral power outputs. The same diffusions forming the source and channel regions of the lateral DMOS can also form the emitter and base of a lateral npn transistor. Also available is a high voltage lateral pMOS device useful for high side switching or high voltage CMOS stages. The vertical pnp formed by the surface p+ diffusion and the substrate can be used for low-side switching.

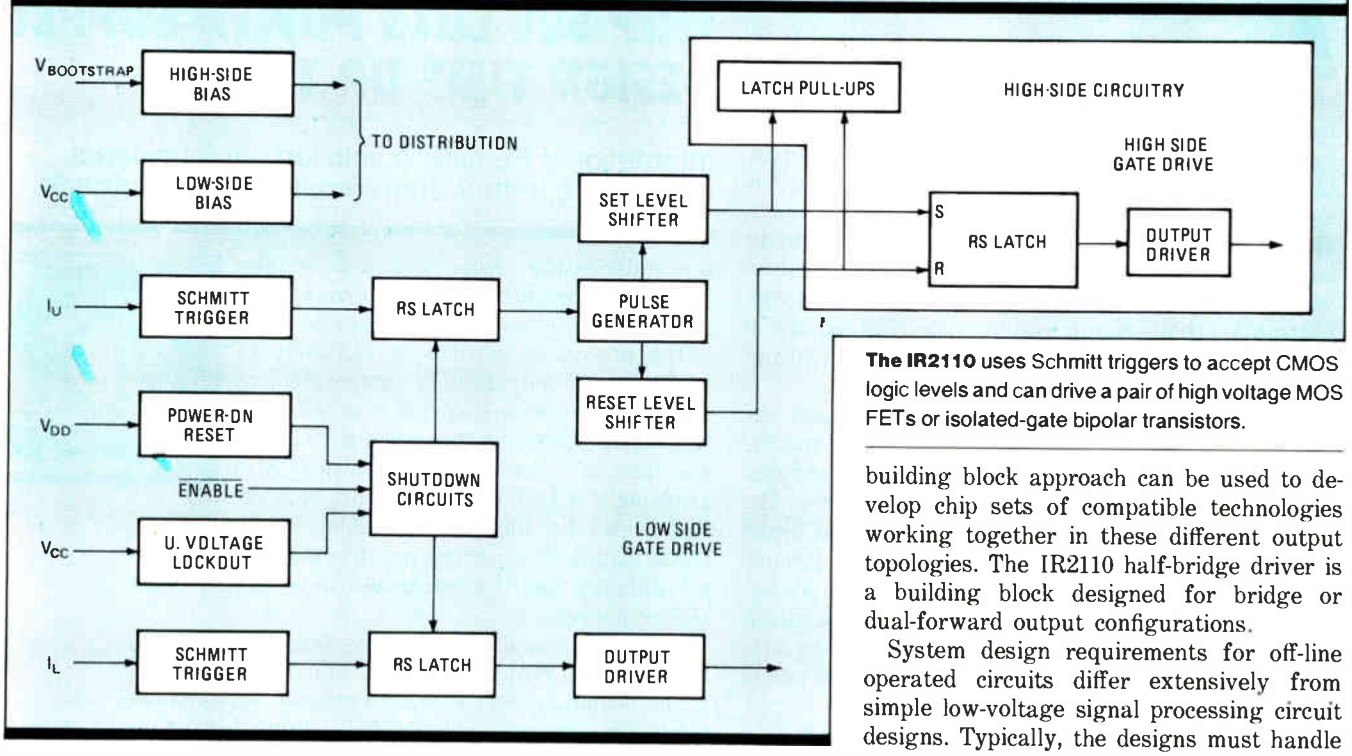
In HVIC technology, the high-voltage level shifting functions and output drives are integrated. Previously, high-voltage level shifting required additional external circuitry, with only the low-voltage driver functions available as commercial single-chip devices.

The new International Rectifier half-bridge driver and the bias supply power ICs use two-dimensional charge control techniques to fabricate high-voltage n-channel and p-channel DMOS and insulated-gate bipolar transistor devices on the same chip. In this pro-

INSIDE A DUAL-CHANNEL DRIVER



CHIP SET SUITS POWER SUPPLY OR MOTOR DRIVE



The IR2110 uses Schmitt triggers to accept CMOS logic levels and can drive a pair of high voltage MOS FETs or isolated-gate bipolar transistors.

cess, lateral DMOS devices with high breakdown voltages are fabricated in standard thin epitaxial junction isolated structures. Furthermore, this device structure allows for high-side operation of the output device. Also, the charge in the drift region of the lateral-diffused LDMOS device is finely tailored to achieve punch-through voltage greater than the high voltage rail from the surface p-type diffusions to the grounded p-type substrate. This feature allows drain and source to swing to the potential of the high-voltage rail. The high-voltage sections are isolated from the low-voltage sections, and from each other, by conventional diffused-junction isolation techniques used in linear bipolar and biCMOS technologies.

Within the International Rectifier HVIC technology, low-voltage CMOS analog and digital circuits can be designed for supply rails up to 30 V. In the new process, bipolar devices are available as precision linear circuits such as bandgap and Zener references, and high-voltage devices operate with typical breakdown voltages above 600 V, the limit of the high-voltage junction.

The two new power ICs and their companions in the chip set are used mainly as building blocks for power converters. Power-converter circuit systems are particularly suited for partitioning into functional building blocks; every power-converter system needs the same functions: system controller, interface, output drivers, output switching devices, LC filter stage, isolated feedback element, and system bias supply.

All basic functions can be designed as standard building blocks for use at specific voltage and current outputs for each topology, except the system controller whose circuitry varies with each application. This building block approach can be used to develop chip sets of compatible technologies working together in these different output topologies. The IR2110 half-bridge driver is a building block designed for bridge or dual-forward output configurations.

System design requirements for off-line operated circuits differ extensively from simple low-voltage signal processing circuit designs. Typically, the designs must handle up to 400 V for U. S. systems, and up to 800 V for European systems. Furthermore, with miniaturization driving every design, form factor and space utilization have become critical design parameters. Shrinking size requirements for efficient use of power and two-way communications with information-processing circuits make off-line power designs very demanding as complete electronic systems.

Switched-mode power conversion output topologies common to off-line designs are basically one, two, or four quadrant types. These circuits convert one level—or form—of voltage and current to another level such as dc-to-dc, dc-to-ac, ac-to-ac, or ac-to-dc.

Extremely efficient full and half-bridge off-line power converters can be designed using the IR2110 half-bridge driver and IR2100 bias supply power ICs, and IR HEXFET and HEXSense current-sensing power MOS FETs. These components are completely compatible, making design very simple. For example, a typical full-bridge power supply uses two IR2110s to drive two half-bridge output stages connected in parallel. The individual half-bridge consists of a high-voltage HEX FET on the high side, and a HEXSense on the low side. Current-sense signals from the two HEXSense devices are fed to the application-specific primary-side controller for pulse-by-pulse current-mode control or current-limit shutdown. The primary-side bias supply is provided by the IR2100 operating from the high-voltage dc input rail. In another example, typical brushless-dc or ac-motor drives use a three-phase bridge design made up of an IR2100 bias supply, three IR2110 half-bridge drivers, three HEX FETs, and three HEXSense current-sensing power MOS FETs in parallel half-bridge output stages. *–Jerry Lyman*

For more information, circle 482 on the reader service card.

BETTING THE COMPANY ON A HIGH-PRICED PLANT

No matter how they rate International Rectifier Corp.'s chances of becoming a major player in the worldwide power-chip game, even its sharpest critics and competitors concede that the small firm possesses vision and daring. Even in the power MOS FET world, which has been notable since the late 1970s for bickering over technology and fierce competition for market share, the El Segundo, Calif., company's stance is controversial.

During the past five years, the family-run company has focused industry attention on itself by attempting to become the recognized world leader in the efficient manufacture of power MOS FETs. Its vehicle is a new plant unlike others in the power field—it is designed and built entirely for production of the company's HEX FET version of the MOS FET. The 285,000 sq. ft. plant seeks efficiency through a design described as the only one to combine wafer fabrication and assembly in a continuous in-line manufacturing process. Production cycles as short as four days will allow a two-week turnaround for volume deliveries; a wait of up to ten weeks is the current norm for power chips.

At International Rectifier's Hexfet America, relatively few people operate one of the most highly automated wafer fabrication plants in the U. S.

But it is the scale of the plant, called Hexfet America, that raises industry eyebrows, mainly because of its relation to the size of the company as a whole. International Rectifier spent some $90 million on the plant, located in Rancho, Calif., about 90 miles southeast of corporate headquarters—a lot of money for a company with 1987 annual sales of $150 million. And the major expenditures were made during the 1985-86 chip recession when demand fell at the same time that competition sent unit prices plummeting. This caused the firm to go deeply into the red, losing nearly $25 million over the 10-quarter span ending Dec. 31, 1987.

The company ran out of funding before the plant went fully onstream last year. It borrowed $60 million last October from a financial subsidiary of Chrysler Corp., believing that the plant would still be a worthy investment. "It's a big strategic bet; in fact, they've bet the total assets of the company, " says John W. Johnson, research director of Cable Howse & Ragen, Inc., a Seattle brokerage firm. Johnson, who has followed the company during the building period, is among the small but growing cadre of Wall Street supporters who believe the investment can pay off.

Not surprisingly, company management also looks to brighter vistas, despite the strains of financing expansion and production problems caused from meeting now-heavy chip demand in a startup plant. Not only do they predict profitability for the quarter ending June 30, but they also say that a smooth ramp-up at Hexfet America promises even better performance. "We can see being dominant in power MOS FETs by the early 1990s," says Alexander Lidow, senior executive vice president for technology and manufacturing and the manager most closely identified with the plant.

The MOS FET plan is simple in outline, though not easy to carry out, especially with competition from major chip firms worldwide. It rests on the economies of scale to be gained when Hexfet America volumes go above the magic 30% capacity level at which it turns profitable, now slated to happen shortly. Above 30%, the company says it can grab ever-bigger market chunks from competitors and write increasingly profitable business because its unit costs will keep dropping. A big part of the future is leveraging off the MOS FET market position into the smart-power business. These devices, which integrate control logic and power switching on the same chip, are expected to start a meteoric growth in the next year or so and attain major chip status in the 1990s.

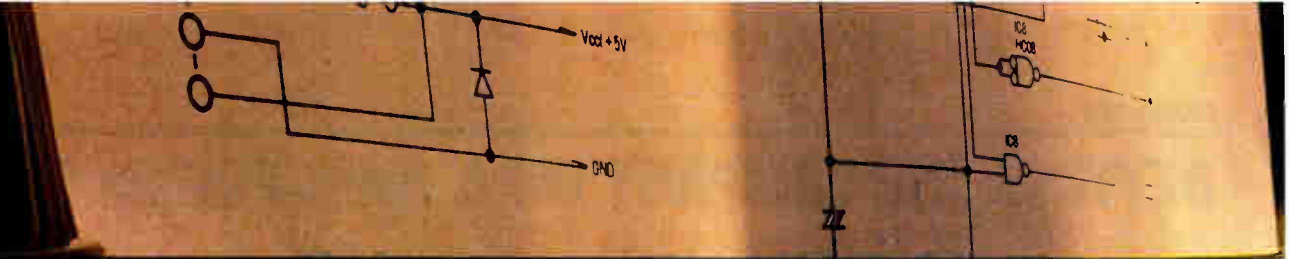
As events have unfolded since Hexfet America production started last year, however, breaking even keeps getting tougher. Large buyers such as automobile firms and scrappy power MOS FET sellers have combined to cause a drop in prices—from an average selling price of $1.42 each in December 1986 to well under $1 by January of this year, says Johnson.

Officials at competing firms point to this continuing slide as undercutting International Rectifier's move to sustained profitability, and thus any claim to product leadership. "Because of the magnitude of IR's debt, their profits can only be marginal in good years, and the bad years will be disastrous," says one, who declines to be identified. Others think that production from Far Eastern sources will keep the pressure on.

For now, a top company goal is keeping a healthy share of the world MOS FET market, which is between $240 million and $250 million this year, up from 1987's $170 million. "At present, we hold over 50% of the U. S.'s nearly $100 million," says Eric Lidow, company chairman and president. The company's share of the $70 million-to-$80 million European region is put at 30%, its share of the $70 million Japanese market at 10%. Its MOS FET sales are now more than $75 million a year.

But chief competitor Motorola Inc. challenges International Rectifier's figures, saying they are too high. "Their shares are really much lower than that," says one Motorola official.

Still, Alex Lidow sounds confident. "We're on a fast track, with at least a two-year lead, and others can't move fast enough," he says. *–Larry Waller*



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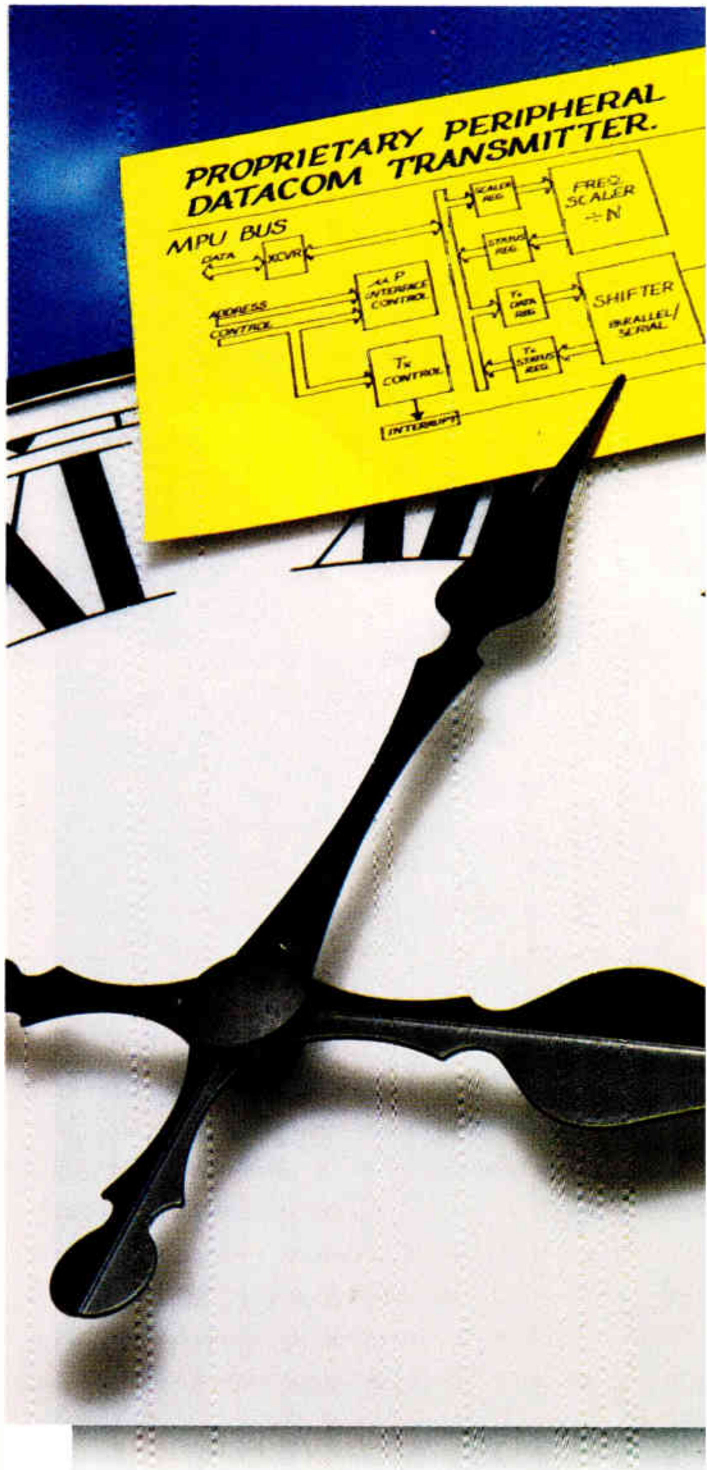

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OPTICAL DISK DRIVES FINALLY GET A CONTROLLER CHIP SET

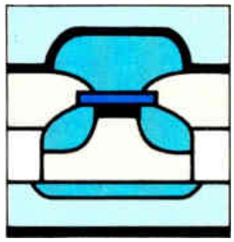
Western Digital's encoder/decoder completes a five-chip set that meets proposed ANSI standards

Since the advent of optical storage technology nearly a decade ago, one of the biggest barriers to building commercial disk drives has been the lack of both a standard controller format and the silicon to make it work. But now optical drive makers can buy a controller that meets proposed standards from Western Digital Corp., a seasoned controller supplier. The company's key accomplishment is an encoder/decoder chip, the WD60C31 Endec, due out in April in sample quantities, that fills the last socket of an optical-controller architecture the Irvine, Calif., firm has designed over the past several years. Western Digital now has in hand the five proprietary devices necessary for an integrated-controller chip set, including its WD60C80 error-detection-and-correction chip, which was unveiled late in 1987.

"All of [the devices] are here; it's a new architecture for high-performance optical controllers," says Raj Doshi, Western Digital's engineering manager for storage products, who has directed development of the project since it started two years ago. "We are the only company with a complete set of chips for the next wave of storage, which is optical." Doshi is also a representative on the American National Standards Institute committee charged with setting international standards for the optical storage physical format, including error-correction codes. These ANSI standards for a continuous-composite format are written for WORM, or write-once, read-many-times 5.25-in. optical drives. Because of Doshi's and Western Digital's involvement with standards activities, the new controllers fully satisfy requirements of the ANSI format, he says, and "by having a standard design, they help the optical industry move a key step toward interchangeability." Prospective users have approved the standards, Doshi says, and they will be sent later this year to be acted upon by the International Standards Organization.

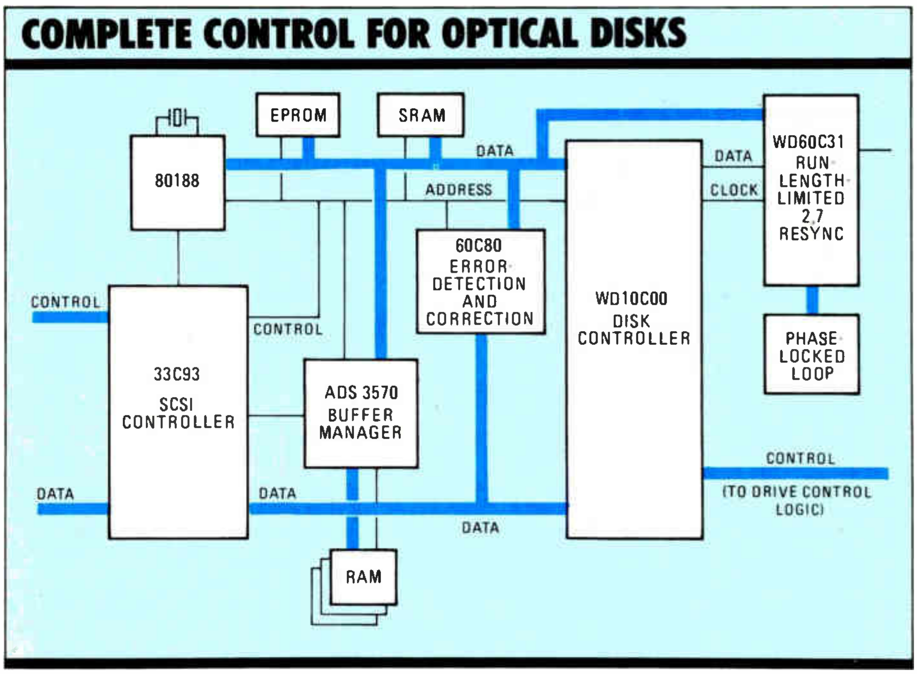
Some storage-equipment vendors already have a head start in designing the new chips into their optical drives, which are slated to debut in May at Comdex. At least four firms, which Western Digital declines to name, worked closely with the company during a six-month development period, using emulation boards provided by the company to take the place of the two error-correction chips. One measure of the new Endec's complexity: the emulation board requires 245 integrated circuits in place of the single chip.

With the integrated chip set in hand, Western Digital can sell the devices either as a unit or with an additional license for the source coding and formating. But buyers are likely to go for the new WD1008-OPT board, which contains the error-detection-and-correction devices and the three other chips: the WD33C93 Small Computer Systems Interface controller, the ADS3570 buffer manager, and the WD10C00 disk controller. The board bundles a number of features into an optical-memory prototyping tool for developing and debugging firmware and hardware (see fig. 1). It supports up to four drives, and has sustained 1:1 sector interleave and built-in diagnostics, along with either dynamic random-access memory or static RAM track buffer and limited defect mapping. The WD1008-OPT has a 5.25-in. footprint and runs from a single 5-V dc supply.



Both the board and the chip set support the SCSI protocol and the modified Extended Small Disk Interface. SCSI features include ANSI X3.131 performance, arbitration, disconnect/reconnect, and a common command set for optical applications. Asynchronous data transfer is at 1.8 Mbytes/s, and synchronous transfer at 4 Mbytes/s. Modified ESDI transfer speed is up to 15 Mbits/s, with optical commands and programmable format plus interleave.

"At the heart of the optical format is the encoder/decoder chip, which performs the critical detection of error conditions," Doshi says. Western Digital started design-



1. Optical-disk-drive manufacturers not only have a complete controller chip set or board to work with, but also one that performs the crucial error detection and correction.

ing the WD60C31 last June as soon as the ANSI optical-format standards reached final form. Besides using a triple-redundant scheme of media-sector ID fields for detecting errors in the optical media (magnetic disks need only a single field), the chip is tailored for another fundamental task: bridging Winchester technology and optical formatting. The chip encodes nonreturn-to-zero-inverted data from the disk controller to optical run-length-limited 2:7 data for the drive, and decodes the information in a reverse operation. It is a 44-pin 5-V CMOS device built at AT&T Co. fabrication facilities using a 1.25-μm process.

The chip operates by generating on-the-fly error-correction bytes, sometimes called "check bytes" or "redundancies". It reads the data field or generates corrections by reading potentially erroneous data and redundancies, with the external processor performing the actual data correction. Single-byte errors are corrected in 200 μs when the processor is an 8-MHz 80188. The error-correction software algorithm was developed by Western Digital and is licensed by the company.

In organization, the WD60C31 signals are functionally divided into three interface groups: disc controller, 10 pins; phase-locked loop, 12 pins; and microprocessor bus, 17 pins. General support of the chip requires 4 pins.

The Endec also generates and detects optical sync marks and supports resync generation and detection, which uses 16 code bits, along with extended recovery techniques. It also detects run-length violations and missing resyncs. Rotational-speed tolerance is ± 0.4%. Data rates of up to 15 MHz can be attained. Because the Endec is programmable, it will accommodate the changes in data formats.

The chip shares responsibility with its four Western Digital mates for defining the type and quantity of information to be written on the media. (An optical drive's data field has four types: the variable-frequency oscillator field; the data-address mark; encoded user data; and resync marks.) The major part of defining the information falls to the WD10C00 disk controller, working with the Endec. In the variable-frequency oscillator fields, for example, the disk controller specifies the field size and the Endec creates the specific high-frequency pattern. This happens after the controller initiates the writing function and sends an nonreturn-to-zero-inverted data pattern to the WD60C31, which then writes a fixed run-length-limited pattern on the disk. The controller ends the variable-frequency oscillator field with a signal during the last byte that also triggers writing of the previously programmed data address mark. The Endec completes this phase by encoding incoming nonreturn-to-zero-inverted data and injecting the data resync mark, which also is a preprogrammed pattern, into the encoded write data path. This entire operation continues as required.

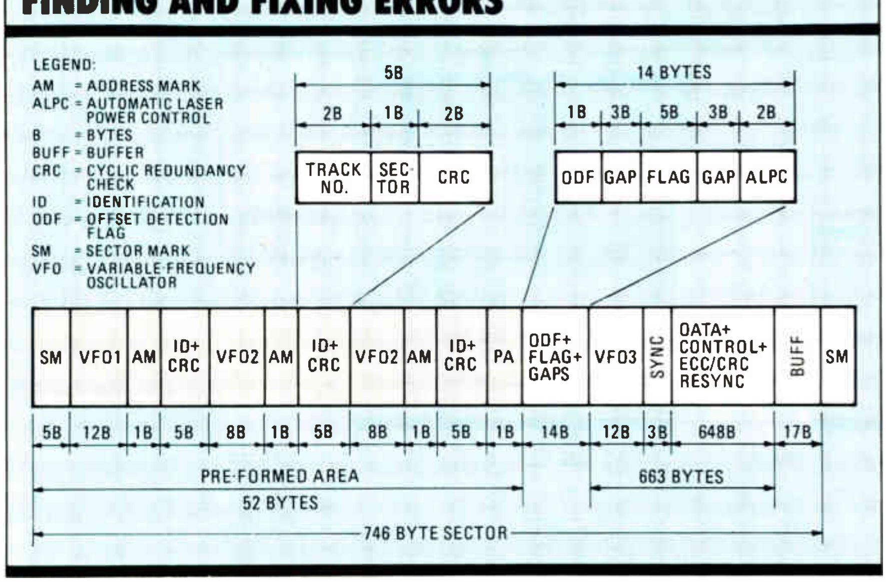
The layout of the 512-byte sector format shows the Endec's role in allowing the computer to read the optical media. Doshi notes that employing the triple-redundant ID fields for optical error detection and correction leads to the need for 746 bytes to write 512 bytes (see fig. 2). In a 1,024-byte sector format, 1,360 bytes are needed. "Regard that as overhead in the optical format," Western Digital engineers advise.

An example of how the Endec functions with respect to the ANSI standard for 5.25-in. optical drives is found in the format for the continuous servo in using the three redundant sector ID fields. Each field is identical in content except for the cyclic redundancy check and two bits for identification within the sector byte. For sector marking, the five-byte mark can be detected without using the phase-locked loop, instead employing alternating long marks of three- and five-bit times. These marks are prerecorded and have a read signal of greater than 0.5 V in amplitude. Of the three variable-frequency oscillator areas, it is necessary that VFO2 differ in both pattern and length. That is, it must be four bytes shorter. Because three concatenated ID fields and run-length-limited 2:7 modulation coding is employed, the conditions leading into each variable-frequency-oscillator 2 area will vary, depending on the last byte recorded in the preceeding ID field. The reason is that a different variable-frequency-oscillator pattern is needed prior to the second and third ID sectors, to allow the last byte of CRC to achieve correct decoding.

Effort and resources put into the Endec chip, along with the earlier WD60C80 error-detecting-and-correcting chip, "are the culmination of a significant investment in new technology for Western Digital," says Doshi. He estimates that altogether the chips required more than 90 man-months of development time, with the error-detection device taking up about 75% of the effort. –*Larry Waller*

For more information, circle 483 on the reader service card.

FINDING AND FIXING ERRORS



2. Triple-redundant identification fields, which are necessary to ensure that errors are detected and corrected, also mean extra bytes are needed to write—746 to write 512 bytes.

THIS LAPTOP HAS THE POWER OF AN 80386-BASED PC

The Turbosport 386 from Zenith Data Systems can run for up to 2 hours without system degradation

Zenith Data Systems's new portable computer is the first battery-operated laptop to offer the power of an 80386-based desktop personal computer. In addition, the Glenview, Ill., company says its Turbosport 386 is the only portable that can operate for up to 2 hours on battery power with no degradation in system performance.

To provide this high performance in a battery-operated system, the Turbosport features extensive power management capability, especially to cut power consumption in the liquid-crystal display and disk drive—the highest power consuming components of a laptop.

Innovations in the Winchester disk drive contribute the most to conserving battery power. It has four power modes: standby, idle, seek, and read/write. The first consumes a mere 0.5 W; the second, 2.0 W; the third, 2.8 W; and the last, 4.2 W. Power-management controls on the disk drive let the user increase battery life beyond two hours by reducing the system's performance.

Such technical prowess has made Zenith the leading supplier—but by no means the dominant one—of laptop portables with 25% of the U. S. market, says Peter Teige, senior analyst at Dataquest Inc., San Jose, Calif. This puts Zenith just ahead of Toshiba America Inc., of Tustin, Calif., which has 24%; Grid Systems Inc., the Mountain View, Calif., subsidiary of Tandy Corp., with 11%; and NEC Home Electronics Inc., of Wood Dale, Ill., with 8%. If Zenith can maintain its market share through 1991, when Teige expects the laptop market to reach $3.6 billion, the company could be shipping nearly $1 billion in laptops.

As it rolls out this newest line of portable computers, comprising a 286-based line called Supersport and a top-of-the-line 386-based product called Turbosport, Zenith is in a good position to capitalize on this expanding market. The new line, which has just begun reaching dealers, consists of the Supersport 286 model 20, Supersport 286 model 40, and Turbosport 386. At the top of the line, the Turbosport 386—which sells for $7999—does not require ac power to operate its high-resolution LCD, 40-Mbyte Winchester disk drive, and 12-MHz 80386 microprocessor (see fig. 1).

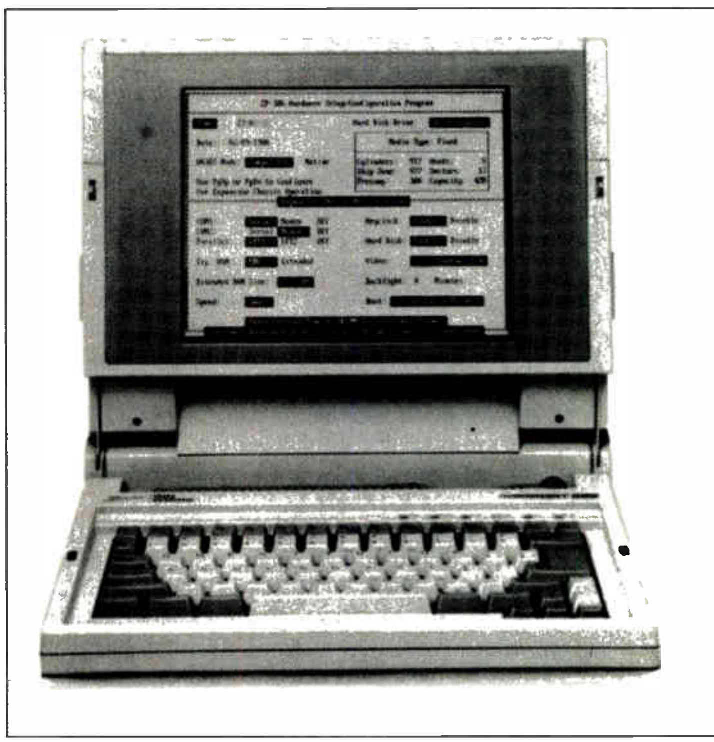
"Operating at 12 MHz with no wait states on battery power, the Turbosport 386 outperforms 16-MHz 80386-based desktop computers that require one wait state," says Howard Fullmer, program manager at Zenith. The relationship between the two is that the Zenith chip operates at both 12 and 6 MHz. At the faster 12-MHz speed, it outperforms a 16-MHz chip. The user can switch the microprocessor from 12 MHz to 6 MHz to accommodate software written for the slower clock speed and to extend battery life beyond two hours.

The system comes with 2 Mbytes of random-access memory, which can be expanded to 3 Mbytes. All RAM above 1 Mbyte adheres to the expanded-memory specification developed by Intel, Lotus, and Microsoft. The system comes with MS-DOS 3.21 software, but users can operate with OS/2, Xenix, or Windows 386.

The computer comes with a capability called intelligent power management (IPM) which provides the user with two power control modes—session and dynamic. In the former, the user calls on a set-up menu before beginning a computing session to tell the laptop which subsystems to power up during the session. For example, the system has an optional internal modem which the user can choose not to power so as to conserve battery life. IPM switches power to the user-chosen components.

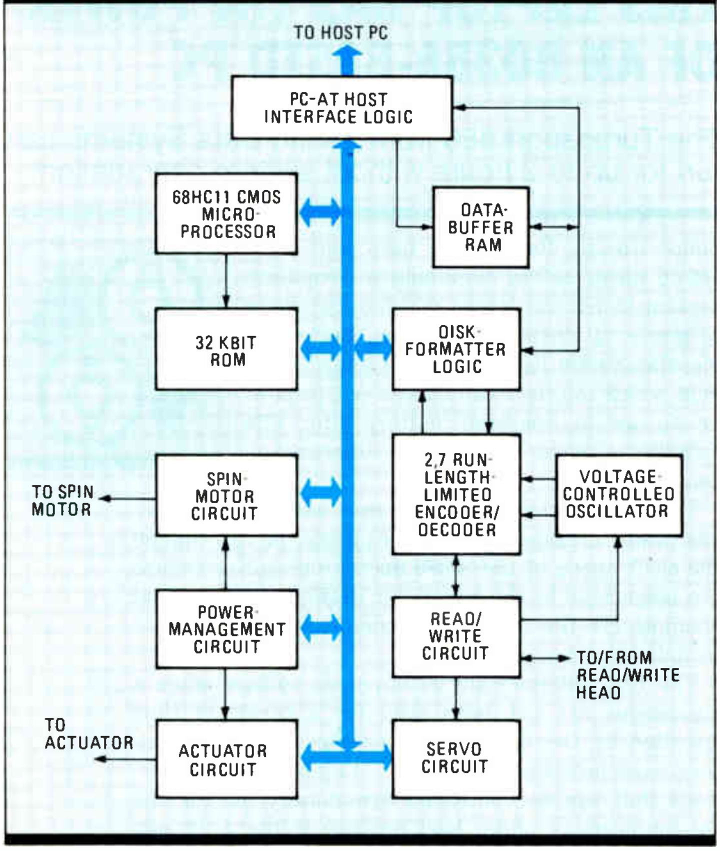
Under dynamic control, the user can change previous power arrangements. For example, he can change the clock speed of the 80386 microprocessor or reduce the brightness of the backlight. Besides these manual changes, the IPM can also automatically control power to individual components.

The IPM automatically removes dc voltage when a component has not been used for a period of time specified by the user. This conserves the Nicad battery pack powering the system. Components or functions that can be controlled dynamically include the communications ports, backlighting of the LCD, modem, disk drives, and processor speed. "Controlling the LCD and the hard-disk drive achieves the lion's share of the power savings," says Fullmer. He says



1. Zenith's new 386-based laptop holds its own with any desktop machine, yet it runs on batteries. Its LCD display offers high image quality.

MANAGING LAPTOP POWER



2. The Turbosport's 40-Mbyte drive has a power-management circuit to interact with the host CPU's power-management system.

80386-based laptops from competitors come with more power-hungry plasma displays and disk drives and must operate with ac power.

The Turbosport's leading-edge LCD contributes to its ability to operate on battery power alone for over two hours. The new display saves 20 to 30 minutes of battery life over a plasma display. "Our enhanced page-white display not only draws half the power of a plasma display," says Fullmer, "it is as easy to read as a plasma." The display has a 20-to-1 contrast ratio, comparable to cathode-ray tube displays and higher than the 18-to-1 ratio of a plasma display. "Its image quality stems from fluorescent backlighting, 400-line resolution, and descending characters formed with an 8-by-16-pixel raster for better clarity. In addition, the 80-character-by-25-line display screen is one-third larger than other portable screens, so its aspect ratio is comparable to a CRT screen," he says.

Desktop performance also comes from the fast-access-time Winchester disk drive, a specially designed 40-Mbyte unit codeveloped by Zenith and Conner Peripherals Inc., of San Jose, Calif. Called the PowerMiser, the drive offers a 27-ms average access time and a fast 8-Mbit/s data transfer rate. In other drives, a 5-Mbit/s transfer rate is more typical.

To achieve this fast-average access time, a rotary voice coil actuator positions the read/write head over the tracks and an embedded servo system ensures accuracy of positions. The faster transfer rate results from using run-length-limited encoding to compress more bits per inch onto the disk surface. Compressed data comes off the disk at a faster rate than uncompressed data. "There are several power-hungry elements on a disk drive," says John Squires, vice president of engineering and a founder of Conner Peripherals. "These include the read/write circuits, drive electronics, and spindle motor." To conserve power while maintaining performance, the drive has its own power management circuit which interacts with the computer's power management system (see fig. 2) controlled by the host central processing unit.

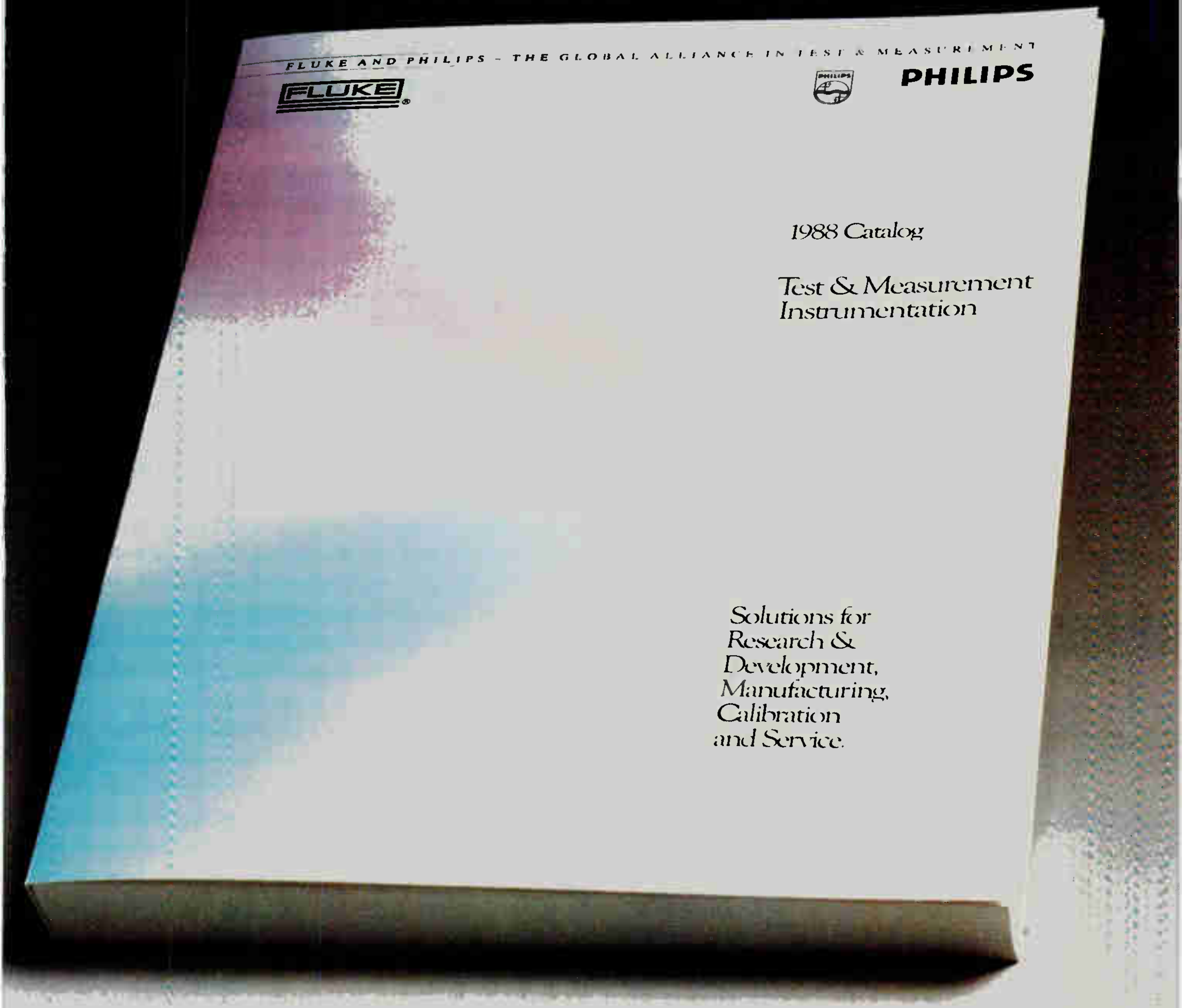
The drive's 68HC11 CMOS microprocessor controls the power-management circuit. The processor receives commands from the PC's host CPU directing the drive to operate in one of the two power saving modes: session or dynamic. In the dynamic mode, the drive offers the host CPU two additional commands not available on other disk drives: spin-up-and-set-time and spin-down timers. With the former, the host directs the drive to apply power to the spin motor and shut the power off if there is no activity from the host in some user prescribed amount of time. With the latter, the host directs the drive to turn the spin motor off. "In addition, the drive itself has four modes that provide different levels of performance and power savings," says Squires. "In order of increasing power consumption, these are standby, idle, seek, and read/write."

At the lowest level of power consumption, the standby mode, the spin motor is shut down and the drive consumes a mere 0.5 W of power. When this mode is operational, system performance is affected by the additional time needed to spin the drive up to fill a disk request, but battery life is extended beyond the two hours of normal operation. When the system operates at full performance, the drive is normally in idle mode, in which it consumes 2 W of power. In this mode, the drive's power-management circuit applies power to the spin motor and actuator, but not the read/write heads.

In the seek mode—when the host requests the drive to reposition the read/write head—the power-management circuit applies additional power to the actuator motor. The drive's power consumption rises to 2.8 W as power is applied to move the head, still low compared with most other drives. Finally, once the drive has found the correct track and the host CPU has requested data from a sector inside the track, the drive goes into the read/write mode. With the read/write circuits on, the drive consumes 4.2 W of power. Even with the drive operating in idle, seek, and read/write modes, the disk drive extends battery life 30 to 45 minutes longer than other low-power 3½-in. Winchester drives.

"CMOS is used throughout the control electronics of the drive to reduce power consumption," says Squires. "However, because the read/write circuit must operate at an 8-Mbit/s data rate internally, it is implemented with high-speed logic which draws over a watt of power. Controlling when those power-hungry circuits are on goes a long way toward conserving battery life and allows the computer to reach performance levels comparable to a desktop portable." *–Jonah McLeod*

For more information, circle 484 on the reader service card.



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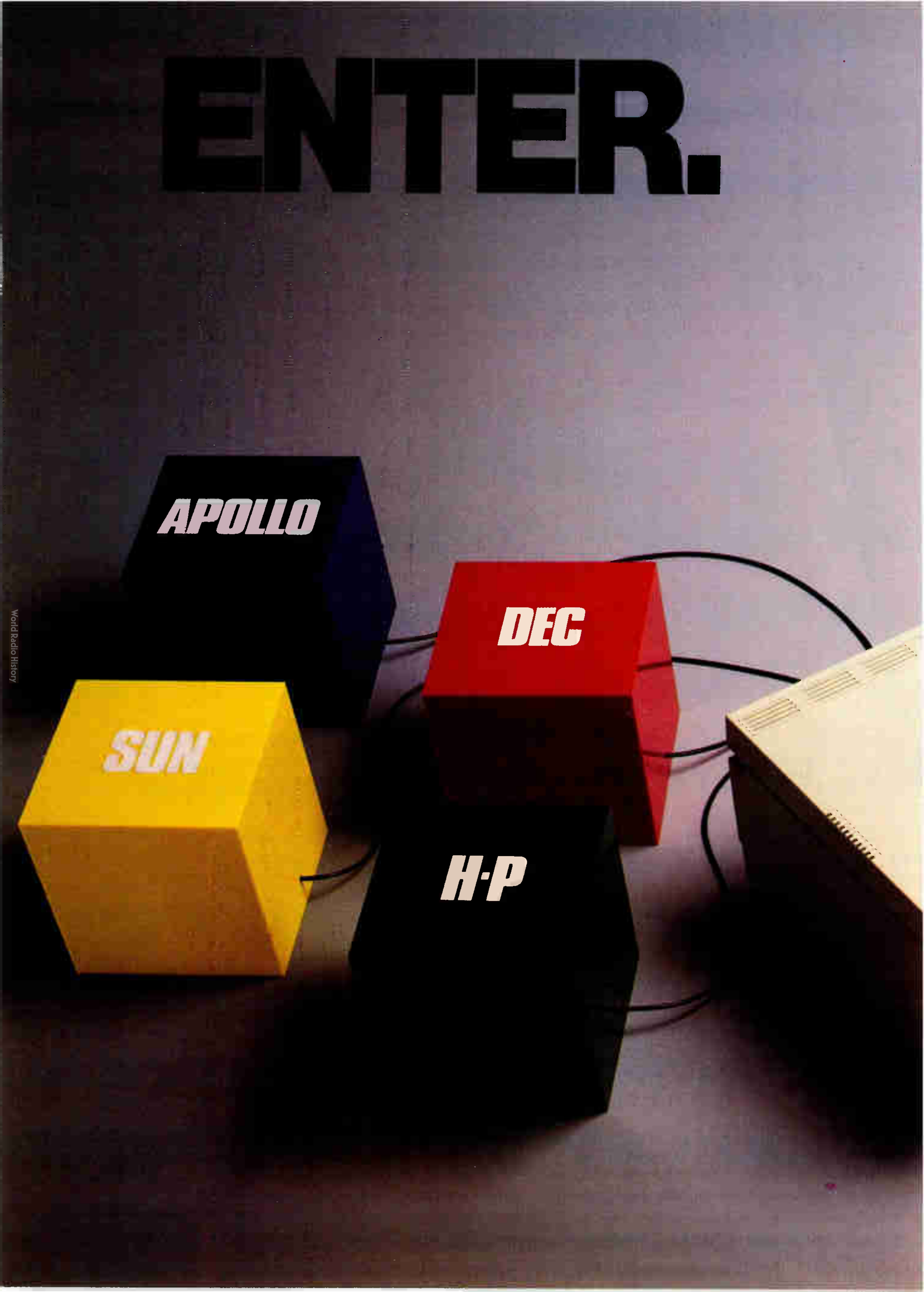
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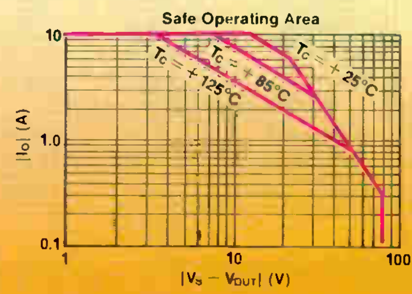

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ANALOG & POWER

Switching power supplies put system-level features onboard for the safety and convenience of users; monolithic instrumentation amplifiers begin to rival operating amplifiers; and smart power promises sweeping changes in the realm of power control

by Lucinda Mattera

Three of the brightest spots on the horizon of the analog and power markets are switching power supplies, instrumentation amplifiers, and smart power. They all are making measurable headway against long-established traditional choices. Switching power supplies are displacing linear ones faster than ever, monolithic instrumentation amps are beginning to take on op amps, and smart power is starting to fuel a revolution in the world of power control.

It was inevitable that switching power supplies would ultimately dominate linear modes because of their smaller size and vastly superior efficiency. But the full consequences of the market changeover from linears to switchers have become apparent only recently, as the special report on p. 113 points out.

One consequence is the arrival of an arsenal of protection features as standards rather than options. Virtually all of today's commercial switchers come with built-in protection against overvoltages, overcurrents, and thermal overloads. Even valuable system-level features are now becoming available at reasonable cost. Often nowadays, commercial switchers allow the user to parallel supplies for sharing load current, stack outputs to add voltage levels, turn the supply on and off remotely, and monitor input and output power to warn of impending problems.

The change in instrumentation amplifiers, simply because they are now available in monolithic form, is even more startling. Offering much more than their traditional characteristics of dc precision with high common-mode rejection, monolithic instrumentation amps are beginning to challenge the ubiquitous op amp as a universal gain block.

Today's broad variety of choice includes different types of instrumentation amps and therefore a selection of performance. Beyond the classic three-op-amp configuration, there is now the simple and economical difference amp, with its ability to handle high common-mode voltages at gain settings of up to 10, and even a broadband instrumentation amp—the transconductance device—that holds bandwidth constant even as gain increases. The technical article (p. 125)—contributed by Burr-Brown, a top analog manufacturer, and written by Jerald Graeme, one of the industry's foremost analog designers and author of the Burr-Brown/McGraw-Hill series of technical books on amplifiers—examines these important changes.

Like the instrumentation amp, power control is undergoing fundamental change. The fledgling technology known as smart power is bringing a number of substantial and startling differences because it combines control and power circuitry on the same chip of silicon. Beyond the obvious savings of space because of one device rather than two or more, smart power means the convenience of digital techniques to control power. It means the elimination of long antenna-like wire runs between the controller and the load. It means the advent of fast and effective protection. It means the ability to control multiple loads with a single device. And it means the ease of adding extra features to the system at virtually no cost penalty.

The technical article (p. 135) written by Art Fury deals with these and the other important issues concerning smart power. One of the leading experts on smart power, Fury is now one of the principals of a new smart-power startup company, Power Integrations Inc. Perhaps best known for his long association with Siliconix Inc., Fury has been one of the pioneering forces in the industry, first for power MOS and now for smart power.

SPECIAL REPORT: SWITCHING SUPPLIES
Winning handily over linear supplies because of their efficiency and small size, switchers of 150 W and more are also enhancing user conveniences with a full array of standard protection circuits and a host of system-level features like load sharing. Page 113.

INSTRUMENTATION AMPS GAIN ON OP AMPS
Hard to beat for dc precision and common-mode rejection, the instrumentation amplifier has now gone monolithic, and it is starting to give the operating amplifier a run for its money, offering a full selection of choices for the savvy designer. Page 125.

SMART POWER: READY, WILLING, AND ABLE
Because it puts control and power side by side on one chip, the impact of smart power goes beyond the expected savings in space and cost, proving performance enhancements such as better protection and extra features as a free bonus. Page 135.

SPECIAL REPORT: LESS IS MORE WITH THE LATEST SWITCHING SUPPLIES

Off-line switching power supplies of 150 W and up are cramming more performance into smaller sizes, especially protection and monitoring features for the supply and the system it powers

by Gene Heftman, *Contributing Editor*

In an era of ever tougher design decisions, there's one job that's getting easier: specifying power supplies. Designers are discovering that the newest off-line switching supplies of 150 W and up pack more power and more features into smaller packages. The newest switchers offer a variety of voltage and current combinations, so designers often can specify a ready-made supply for even highly complex systems. And new supplies that are using advances in component and packaging technology to incorporate such new system-level features as automatic current sharing, remote on/off control, and alarm circuitry to monitor input and output power are beginning to appear. Also, protection against excessive voltage, current, and temperature has pretty much become standard fare, even in low-cost supplies.

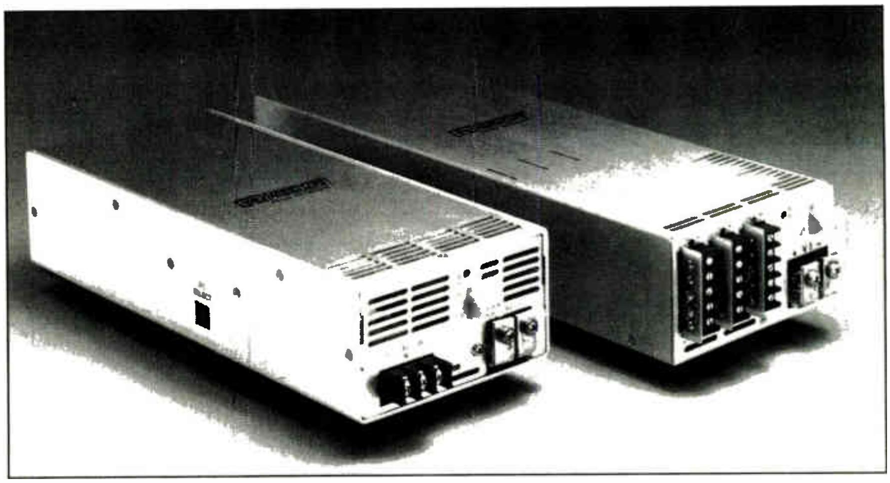
Moreover, switcher reliability and quality have improved dramatically. These days, impressive figures for mean time between failure are likely to be backed up by the burn-in of every supply before shipment and by warranties that cover materials and workmanship for up to five years.

Besides providing a wide range of features, today's switchers offer a variety of voltage and current combinations in a choice of both open and closed frames (see table, p. 114). Open-frame switchers use convection cooling (low-velocity air flow) for managing heat, while closed-frame ones employ a fan inside their housings to do so. Supplies rated from 150 W to 500 W can be either open- or closed-frame units. System supplies—switchers with ratings between 500 W and 1,500 W—are usually closed-frame units (see fig. 1). Even with the 65% to 75% efficiency typical of switchers nowadays, a system supply can generate hundreds of watts worth of heat that must be removed by forced air to prevent damage to both the supply and the system it powers.

To provide the voltage levels needed by today's systems, many switchers offer multiple outputs, typically four different voltage and current combinations—and sometimes up to seven or nine outputs. Since numerous applications employ 5-V logic, a 5-V output is virtually standard. That output can deliver from tens of amperes in medium-power switchers (150 W to 350 W) to hundreds of amperes in high-power (800 W to 1,500 W) units. Other common voltages are 12, 15, 18, 24, and 28 V for powering linear devices, electromechanical components, floppy disks, lamps, and other system elements. Generally, the higher the voltage level, the lower the current capability.

Another way to obtain various voltage levels is to join different single-output supplies into a power assembly. Original-equipment makers take this route because it can be difficult to find a cost-effective multiple-output supply that provides the right combination of voltage levels to serve a full range of systems.

That's why, for Kepco's RBX family of 600-W switchers, the company offers a standard package that will hold any combination of single-output units. For each supply, a module that contains the entire power section simply slips into the switcher case (see fig. 2). Current flows out on two busbars that not only can carry up to 120 A but also serve as structural supports for the module. To improve output filtering, the company can stack as many as 39 capacitors on a



1. For a compact system supply, Computer Products uses low-profile packaging in its medium-power (250 to 600 W) closed-frame switchers.

circuit board that sits in the center of the module.

As in the past, system designers face the familiar decision whether to buy a supply or build their own. Large OEMs tend to build their own supplies because they can justify the cost by the high production volume and the need to meet specific system requirements. But small manufacturers usually find buying to be more cost-effective than building. They either choose a standard switcher right off the shelf, or they ask for a simple modification to a standard product.

Cost, which is pivotal in buy/build decisions, can mount if an OEM must stock many custom supplies to suit a range of load requirements. To get around such problems, Lambda Electronics designed its LFQ series (see fig. 3) of WattBox multiple-output switchers in three power ranges to cover most medium-power applications: 325, 475, and 635 W. These units provide four output voltages (5 V, two 12-to-15-V outputs, and either 24 or 28 V). Those outputs are isolated from each other and from the chassis. The current on each output can be used up to its maximum value, provided the overall load does not exceed the total power capability of the supply.

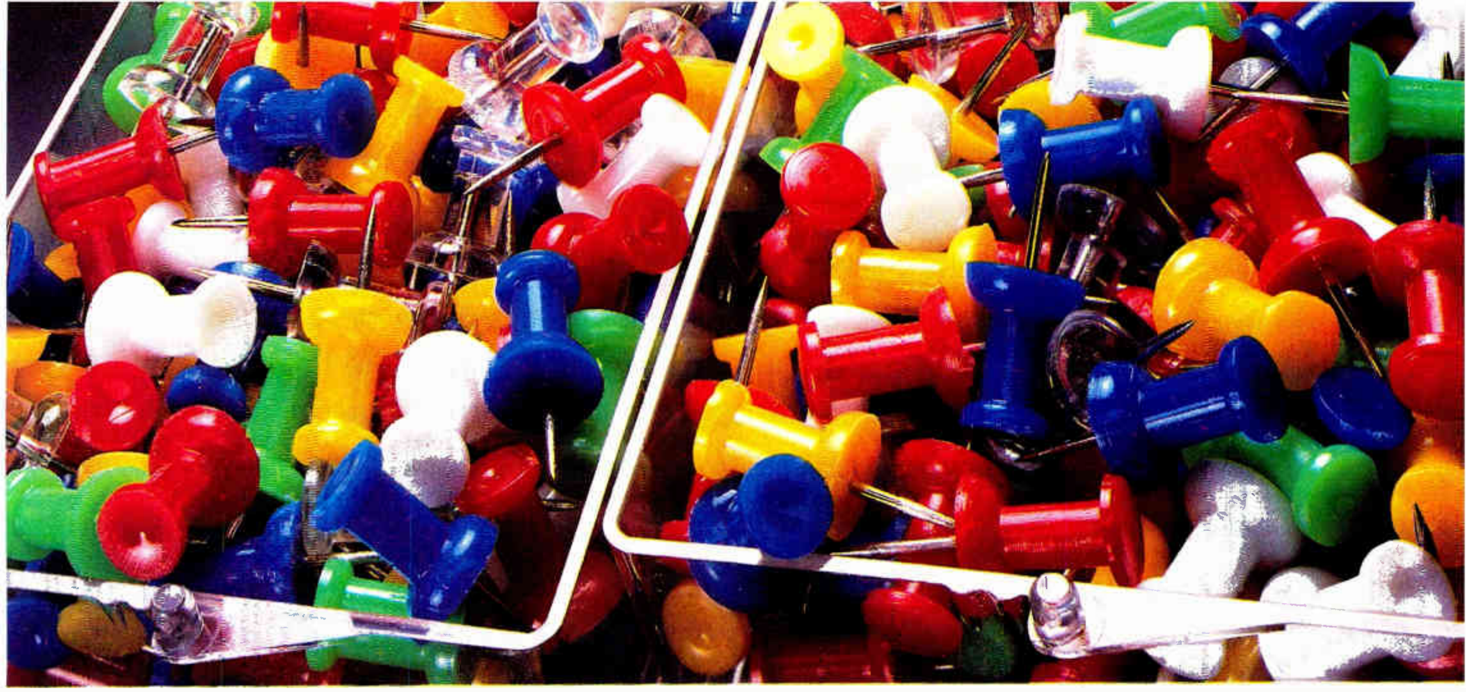
In the high-pressure world of international competition, buy/build decisions for power supplies are not as easy as they once were. One reason is the increasing scrutiny to which supplies are subjected. To sell in worldwide markets, power supplies must comply with stringent safety and electromagnetic- and radio-frequency-interference standards; and obtaining the necessary certifications for supplies built in-house can be costly and time-consuming. Purchased switchers, on the other hand, come in a range of multiple- and single-output units that meet worldwide standards for safety and emi/rfi.

Another reason users may opt to buy is that they can choose a proven switcher design having a high MTBF, thereby reducing the probability that a power-supply failure will compromise system reliability. Although a long-used design does not guarantee the MTBF for an individual supply, its proven track record does offer more assurance than designs recently off the drawing board.

In general, switching power supplies are less a technology-driven market than a cost-driven market in which reliability is key. As a result, switchers do not use advanced components, whether active or passive, as soon as they become available. For example, in the near future, commercial switchers are not likely to tap smart-power technology, which has been widely publicized but is still largely developmental. Similarly, such advanced design techniques as resonant topologies, which are already making possible megahertz operation for low-power dc-dc converters, are not on the immediate horizon for medium- and high-power commercial switchers. That's because high power and high switching frequency just do not mix. For the most

REPRESENTATIVE SWITCHING POWER SUPPLIES

Company	150–300 W	300–600 W	600–1,000 W	>1,000 W	Outputs	Circle No.
	(CF = closed frame OF = open frame)					
Abbott Transistor Labs Power Supply Div. Los Angeles, Calif. (213) 936-8185	CF only	–	CF only	–	single and multiple	370
ACDC Electronics Oceanside, Calif. (619) 757-1880	OF and CF	OF and CF	CF only	CF only	single and multiple	371
Acopian Easton, Pa. (215) 258-5441	–	CF only	CF only	–	single only	372
Computer Products Inc. Power Products Div. Pompano Beach, Fla. (305) 974-5500	OF and CF	OF and CF	CF only	CF only	single and multiple	373
Condor Inc. Oxnard, Calif. (805) 486-4565	OF only	–	–	–	single and multiple	374
Deltron Inc. North Wales, Pa. (215) 699-9261	OF and CF	OF and CF	CF only	CF only	single and multiple	375
Kepco Inc. Flushing, N.Y. (718) 461-7000	OF and CF	OF and CF	CF only	CF only	single only	376
Lambda Electronics Melville, N.Y. (516) 694-4200	OF and CF	OF and CF	CF only	CF only	single and multiple	377
LH Research Inc. Tustin, Calif. (800) 547-2537	OF and CF	OF and CF	CF only	CF only	single and multiple	378
NJE Power Supplies Dayton, N.J. (201) 329-4611	–	–	CF only	CF only	multiple only	379
Pioneer Magnetics Santa Monica, Calif. (800) 233-6216	CF only	CF only	CF only	CF only	single and multiple	380
Power Components Co. Gardena, Calif. (213) 323-8120	OF only	OF only	CF only	CF only	single and multiple	381
Power General Canton, Mass. (617) 828-6216	OF only	–	–	–	multiple only	382
Power One Camarillo, Calif. (805) 987-8741	OF and CF	OF and CF	–	CF only	single and multiple	383
Powertec Inc. Chatsworth, Calif. (818) 882-0004	OF and CF	OF and CF	CF only	CF only	single and multiple	384
RTE Power/Mate San Diego, Calif. (619) 299-3800	OF only	–	–	–	multiple only	385
RO Associates Sunnyvale, Calif. (408) 744-1450	CF only	CF only	CF only	CF only	single and multiple	386
Todd Products Corp. Brentwood, N.Y. (800) 223-8033	OF only	OF only	–	–	single only	387
Shindengen America Inc. Westlake Village, Calif. (805) 373-1130	OF only	CF only	CF only	CF only	single and multiple	388



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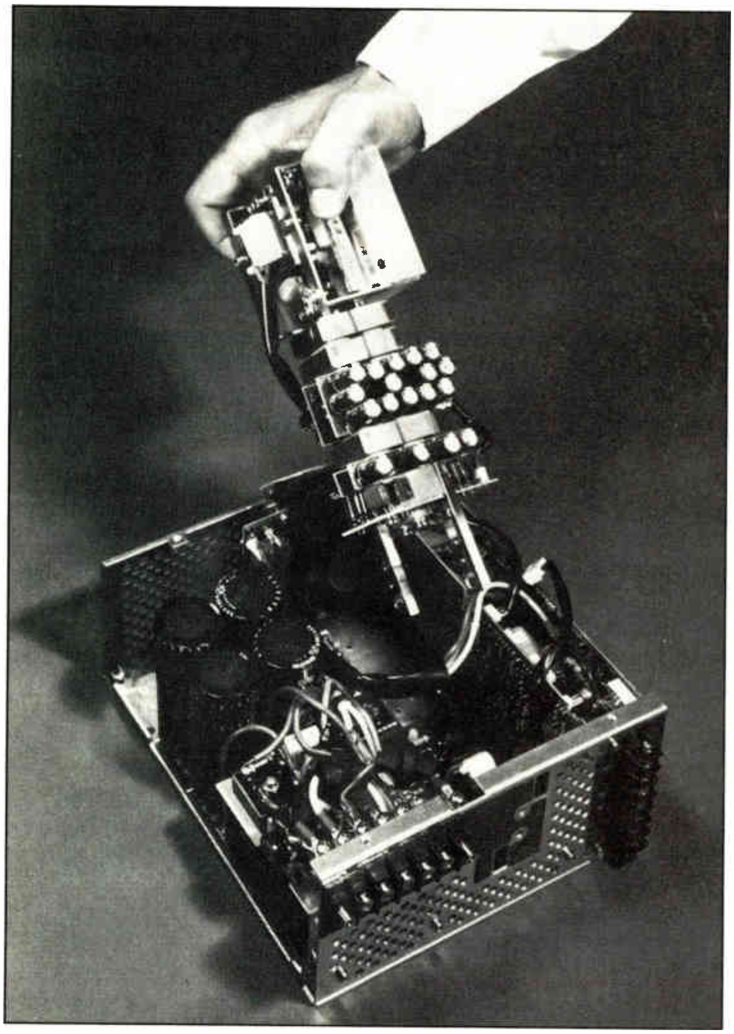
part, commercial supplies will continue to employ the pulse-width-modulated topologies that have proven to be efficient and reliable.

However, there are established technology advances that switchers are using to advantage. Most notably, power MOS FETs have all but displaced bipolar output transistors, allowing the switching frequencies of medium- and high-power supplies to rise as high as 100 to 150 kHz. Since MOS FETs do not store charge, they switch faster than bipolar transistors. Moreover, MOS FETs require simpler drive circuitry than bipolars, and the absence of secondary breakdown eliminates the need for snubber circuitry. As a result, supply manufacturers have additional board space for implementing new features.

To reduce overall package size, switchers are also taking advantage of surface-mount technology for both active and passive devices. Because of surface mounting, Todd Products has been able to raise the power of its MAX-500 single-output switchers by 25%, without increasing package size (see fig. 4 top). The upgraded open-frame version packs 500 W in 144 in^3., a volume that formerly housed 400 W. Likewise, Power General employs surface-mount technology to build its 4200 series of 200-W open-frame switchers on a single circuit board measuring 4 by 10 by 2.2 in. (see fig. 4 bottom). Furthermore, each unit in the 4200 series offers four output voltages.



2. In Kepco's family of RBX switchers, which features a modular approach, a removable 600-W power module occupying only 260 in.^{3} fits snugly in the case.

For space saving inside switchers, manufacturers are going to integrated-circuit and hybrid technologies that consolidate control functions once spread out over a entire board. In particular, pwm controller chips are at the core of most medium-power switchers based on the forward-converter topology. LH Research's MM and SM series of multiple-output supplies, for instance, contain a proprietary LSI control chip that eliminates some 50 discrete components and augments both performance and reliability, to boot. Similarly, Power One uses a thick-film hybrid control circuit in its International series of 200- to 500-W switchers to replace over 165 discrete components.

In addition to saving space and boosting performance, ICs and hybrids bring cost savings. One hybrid circuit with 20 chips interconnected on a ceramic substrate might be usable across an entire family of similarly specified switchers. When the supply manufacturer does not have to redesign and relayout the same circuitry for different switchers, the resulting cost savings can be passed on to the user.

Like chips and hybrids, passive components are also playing an important role in improving switchers, principally through the reduced size and increased capability of advanced passives. Electrolytic capacitors, once bulky space hogs, have trimmed down considerably in recent years. Not only do the new breed of electrolytics pack more capacitance in a smaller volume, but also their series inductance is lower and their operating frequency higher.

Even magnetic components are improving, albeit more slowly. These parts now allow switching frequencies in the range of 150 kHz. However, at higher frequencies, parasitic losses in transformers become significant due to skin effects in copper. So the hoped-for reduction in the size of magnetic components at higher frequencies is still around the corner.

SYSTEM-LEVEL FEATURES

Switching power supplies are parlaying these advances at the component level into new features—usually available as options—that are especially useful at the system level. Today, switchers can be connected in parallel for powering a common load and even can be turned on or off from a remote location. What's more, they now allow adjustment of output voltage level, monitoring of dc output voltage and ac line voltage, and power-factor correction for reduced input current.

The ability to parallel switching supplies so that they automatically share load current is an important new capability. Usually, it is difficult for two supplies to share a common load because their output voltages will never be exactly equal. Even small differences in potential between the supplies result in large differences in output current—the unit with the higher voltage will supply the full-load current. At present, current sharing is available only for high-power, closed-frame system supplies. Switchers that can be connected in parallel are essential for such equipment as

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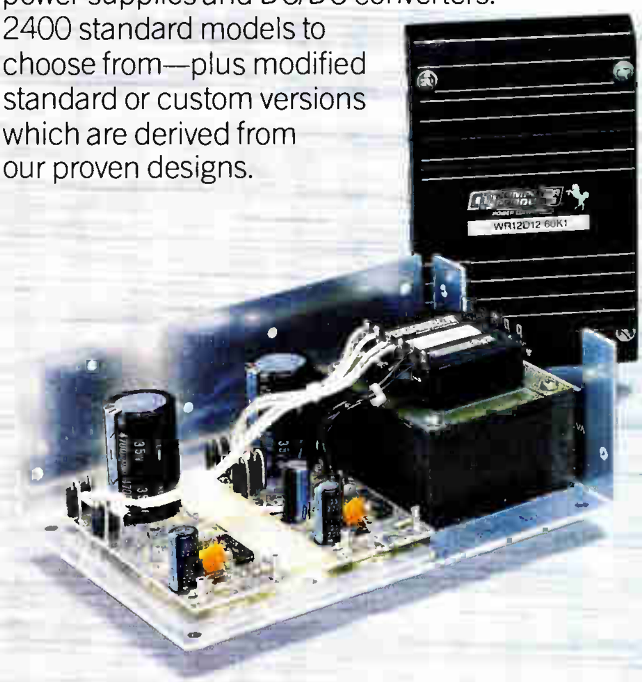

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fail-safe computer systems that require redundancy to prevent a complete system crash should a power supply fail. Such fault-tolerant systems employ N+1 supplies, each having the same output power. The number of supplies needed (N) is the system's total power requirements divided by the supply output power. Then one extra supply is added to ensure that the system has full power should one unit fail. One of the advantages of such an N+1 scheme is that a battery can replace a supply, creating an uninterruptible power system.

Switcher manufacturers are already addressing the rising demand for current sharing. ACDC Electronics offers direct paralleling via a single wire between its closed-frame JF and JFM series of switchers. Any number of units from the two different families can share current precisely. The single-output JF units deliver from 750 W to 1,500 W, while the multiple-output JFM units provide from three to five output voltages at 1,600 W total.

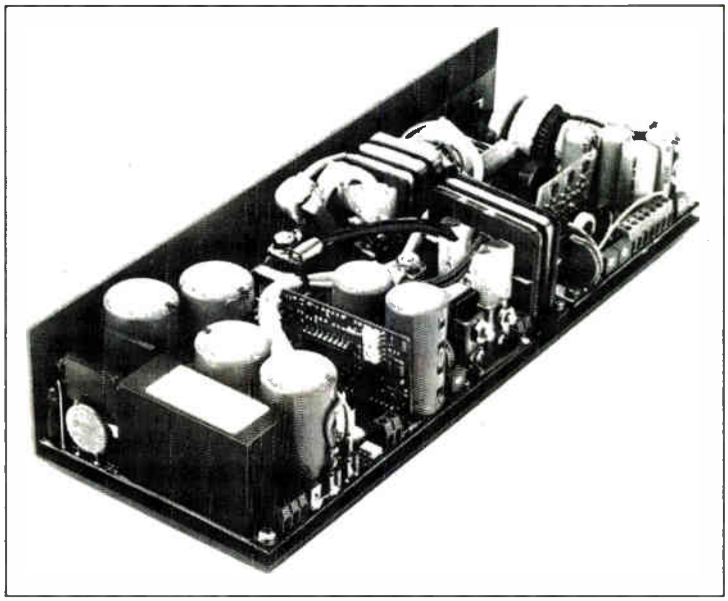
Likewise, two or more of Powertec's multiple-output, 200-to-300-W ValuSwitcher II units can automatically share current directly proportional to their current ratings. The supply having the greater output capability provides a proportionately greater share of the total load current. Built-in isolation diodes reduce the possibility of a failed unit pulling the entire system down. When a unit fails, its diode becomes reverse-biased, in effect, creating an open circuit between its output and the load. The company's Multi-Mod high-power switchers (600 W to 1,500 W) also allow direct paralleling on their main or auxiliary outputs with automatic load sharing.

Remote control to eliminate manual on/off switching is an important requirement, especially for computer and test equipment. Accommodating that need, a number of switchers include control terminals that allow TTL-compatible signals to turn the supply on or off. Among the switcher units providing remote on-/off are the 250-W PPM series and 400-W PFS series of closed-frame multiple-output switchers from Computer Products.

Another feature becoming popular is margining, which allows the user to vary the output voltage of a supply by around ±5%. With margining, the user can ensure his circuitry will function properly even if the nominal supply voltage were to rise or fall. In general, margining is available only on the main output of a multiple-output supply, and that is is usually the 5-V output used for logic circuitry. Typically, a toggle switch on the supply enables the margining feature.

Along with remote on/off control and margining, some switchers provide features for monitoring output voltage and the ac line. With the "power-good" feature, internal circuitry monitors one or more of the supply's output voltages to determine whether the actual level is above or below the set value by a certain percentage—usually ±4% or ±5%. If the supply voltage goes out of tolerance, that circuitry issues a TTL-compatible signal to the host system.

Complementing this feature is monitoring of the ac line voltage to indicate when the loss of that line is imminent. To flag the host system, the supply sends out a logic-level signal 5 ms before regulation fails.



3. Lambda's LFQ series of WattBox multiple-output switchers come in power ratings of 325, 475, and 635 W.

Power-factor correction, a new feature in switchers, converts the high current pulses that switchers draw from the ac line into a sinusoidal waveform that is in phase with the line voltage. When the current waveform exactly matches the voltage waveform, the power factor nears unity (0.99, to be exact).

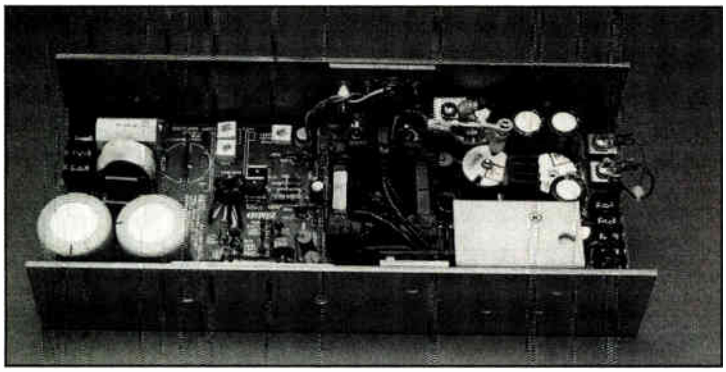
One benefit of power-factor correction is a reduction of the input current needed to power a supply. Pioneer Magnetics reports that a typical 115-V, 15-A ac circuit can support a 700-W uncorrected switcher or a 1,000-W switcher with power-factor correction. Other benefits include: reduced harmonics between 10 and 150 kHz so as to optimize effective input power from the ac line, longer hold-up time for a supply's output voltage to remain within specification after the loss of ac input power, and the elimination of sensitivity to frequency variations in the ac line up to 440 Hz. The power-factor correction option is available on Pioneer Magnetics' PM2900 and PM2501B switching supplies, which are closed-frame single-output units ranging in power from 250 to 1,500 W.

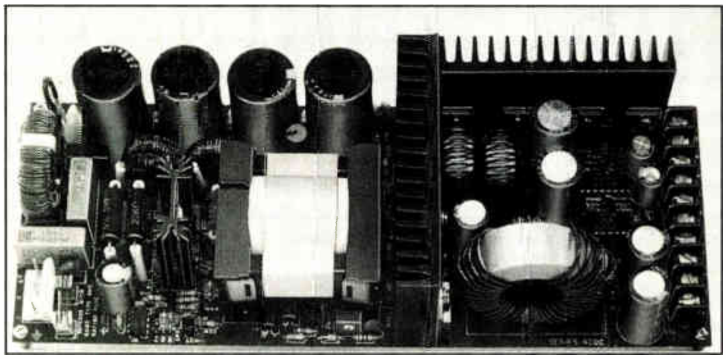
PROTECTION IS A GIVEN

Aside from the new features being added for more system-level flexibility and control, switchers are beefing up their protection for preventing harm to the circuitry they power. To do so, virtually all of them provide protection against overvoltage, excessive load current, and thermal overload. That protection comes from an array of circuits that monitor voltage, current, and temperature and then take the necessary action to save both the switcher and the system it powers should any parameter exceed its preset limits.

In addition to protection, remote sensing has also become a common feature on many switchers. With this capability, the supply compensates its output for voltage drops in the power lines running to its load.

Overvoltage protection limits the voltage across a





4. To reduce supply size by 25% to 35%, Todd Products' MAX 500 (top) and Power General's 4200 series (bottom) switchers use surface-mounted components.

load to a preset level. When an overvoltage occurs, most overvoltage protection circuitry first reduces the output voltage to a low value and then restores the output to its preset level only after the user has recycled the ac input power. The most common type of overvoltage protection is the well-known crowbar circuit, which responds quickly to act as a low-impedance shunt across the supply output. Overvoltage protection is a standard feature on at least the main 5-V output of commercial switchers.

Output current limiting, which protects against current overloads and short circuits, safeguards the supply from damage by automatically holding the load current to a predetermined value. After removal of the overload condition, the supply automatically reverts to normal operation.

The third arm in the protection arsenal prevents damage to a supply from internal heat. Thermal protection circuitry shuts down a supply's output power when its internal temperature exceeds a safe operating value. The user can restore the supply to normal operation by recycling the ac line voltage. Or the thermal protection circuitry may automatically reset the supply when the temperature returns to a safe level.

The closed-frame 300- and 500-W switching supplies made by Acopian offer all three types of protection. The overvoltage protection latches the supply off, and a red lamp signals the condition. Foldback current-limiting protects against excessive load currents, with automatic recovery when the overload is removed. A thermostat, which resets itself, senses overtemperature conditions. The units are also equipped for remote sensing, which compensates for up to a 0.5-V drop per output line.

Similar protection features are found in RO Associates' series 700 industrial switchers, which range in power capability from 500 to 840 W. All outputs are equipped with current limiting, and the main 5-V output has self-recovering overvoltage protection that allows the supply's logic to operate even through a fault condition. A thermostat provides thermal protection by disconnecting the input from the ac line when the case temperature rises above 80°C. Interestingly, the company uses magnetic elements to obtain pwm control, believing them to be more reliable than semiconductors. Those magnetics allow separate windings to control overvoltage and overcurrent protection, and they provide 5.5 kV of isolation between input and output.

The multiple-output high-power switchers from NJE Power Supplies pack the full complement of protection features. The MK series units contain overvoltage protection that is factory-set at 10% to 20%, or 1 to 2 V (whichever is greater) above the nominal output voltage. Foldback current limiting protects against overloads and shorts. The supplies shut down automatically when internal heatsink temperature exceeds a safe limit. Restarting is automatic when internal temperature returns to normal.

Today, protection circuitry has become standard fare even on so-called economy switchers, although they are not likely to incorporate any of the fancier new features, like current sharing and remote on/off control. These switchers find favor among designers who need basic medium-power sources to keep costs low.

RTE Power/Mate, for example, makes a line of economical open-frame, multiple-output switchers called the EVD series to fit such applications. The 150-, 165-, and 180-W versions offer four standard output voltages (5, 12, 15, and 24 V). Load regulation on the main 5-V output is ±1% for load changes from 20% to 100%, while it is ±3% on the auxiliary outputs. The main output has remote sensing and overvoltage protection, which reacts before the 5-V output drops 5% at 100% load conditions.

Condor is another manufacturer that provides the standard range of output voltages—5, 12, 15, 18, 24, and 28 V—in its 140- and 200-W SDM series of open-frame switchers. Certain models come with quasi-regulated secondary outputs for circuits that experience high peak currents. Other models offer tightly regulated (1%) secondary voltages for sensitive linear applications. To increase flexibility, the 12-V outputs can be combined to produce higher voltages and currents.

By harnessing advanced components and perhaps even new topologies, tomorrow's commercial switchers are likely to operate at much higher frequencies to reap the benefits of further size reductions while maintaining present power levels and operating efficiencies. The ultimate goal remains to control power from the ac line at megahertz frequencies. On the more practical side, new system-level monitoring features will become standard fare, on even the so-called economy units. □

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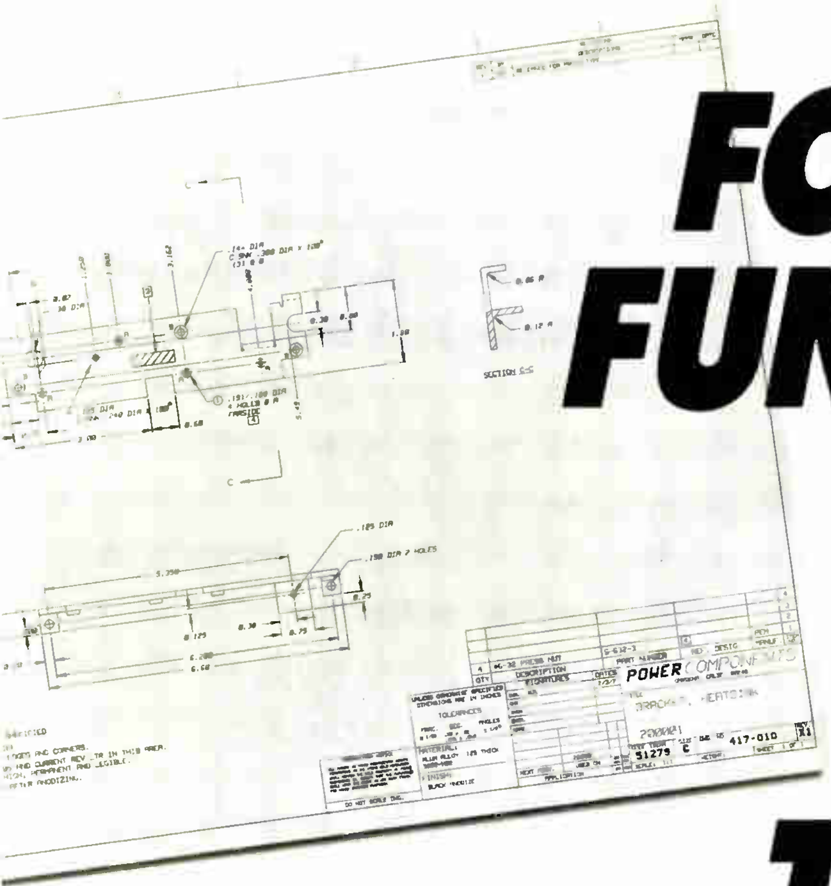

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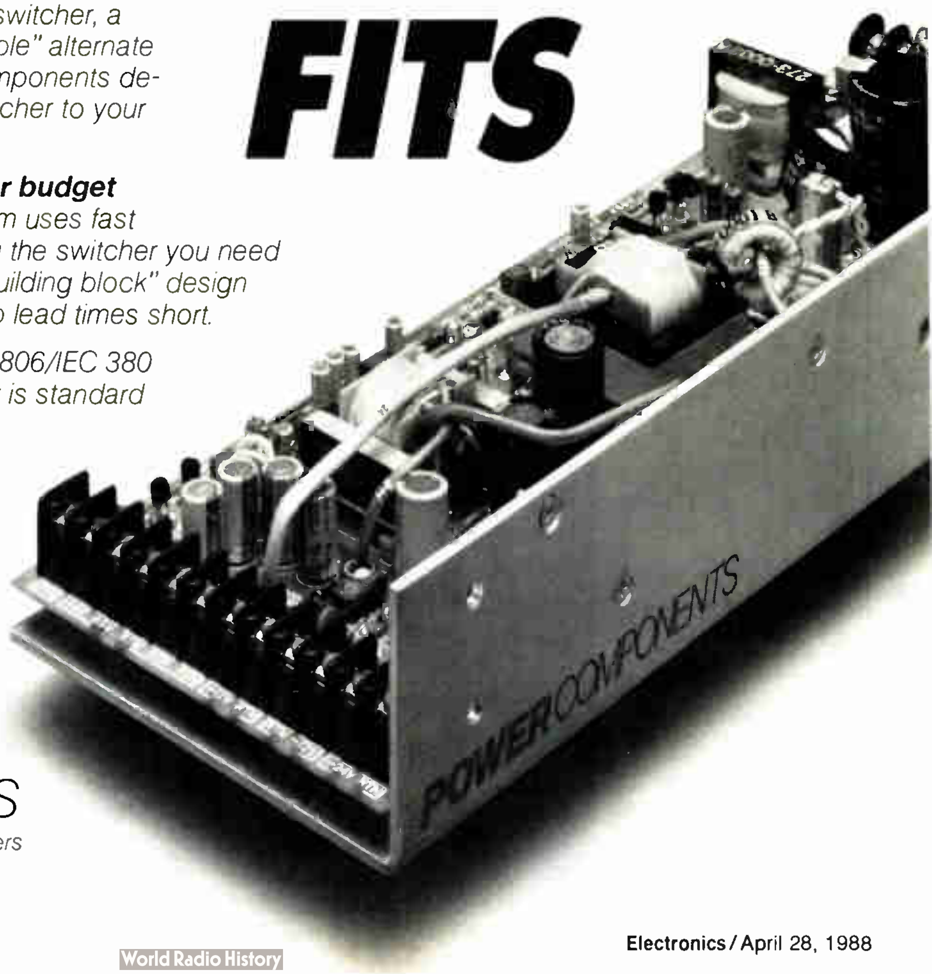

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INSTRUMENTATION AMPS BEGIN TO CHALLENGE OP AMPS

Besides displacing hybrid versions, monolithic instrumentation amplifiers are taking on precision op amplifiers, as they begin to appear in the same sort of variety but retain their inherent advantage of being able to reject common-mode voltages

by Jerald Graeme, *Burr-Brown Corp.*

Like much of the analog world, instrumentation amplifiers are going monolithic, and in the process they're taking on new roles. Besides providing the usual savings in cost and space that come with the replacement of hybrid implementations, integrated-circuit instrumentation amps are beginning to supplant operational amplifiers. Instrument-amp ICs are taking over especially in applications that require precise gain, such as test and measurement systems, and in applications such as bridge monitoring that need dc precision together with a high gain-bandwidth product. In short, the monolithic instrumentation amp promises to become the next universal gain block.

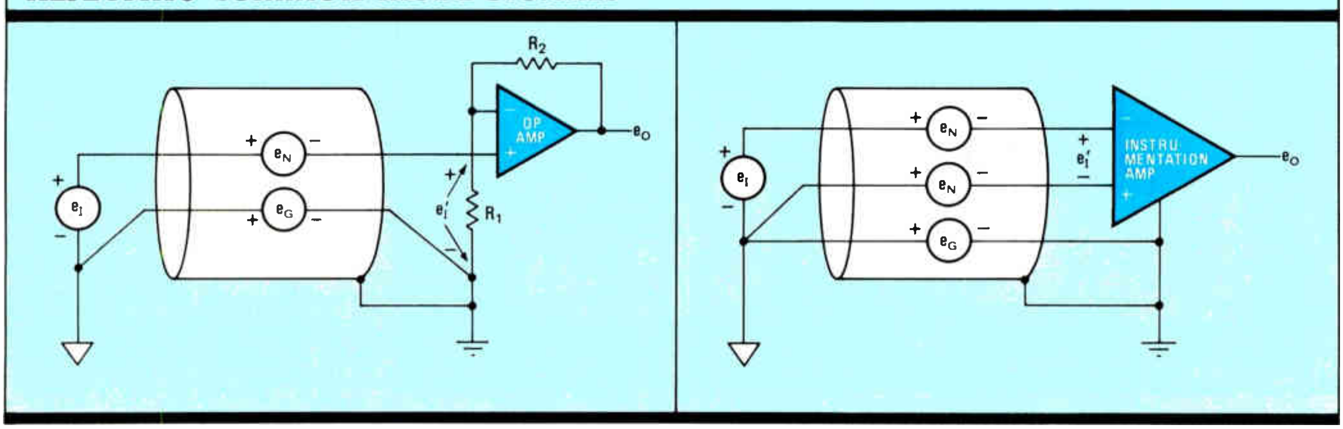
Because of monolithic technology, instrumentation amps are showing up in the same sort of variety generally associated only with op amps. Now there's a choice between bipolar and FET processes. Different performance enhancements, like high speed, high voltage, and low power are available; and low-cost options are starting to appear.

Furthermore, monolithic technology has brought new structures and new capabilities. The classic three-op-amp circuit is no longer the standard configuration for every instrumentation amp. Nowadays, instrumentation-amp chips come in three different configurations, each having its own specific merits. They are: the difference amp, the three-op-amp configuration, and the transconductance instrumentation amp.

Not that long ago, deciding between an op amp and an instrumentation amp was a clearer choice. That decision was pretty much based on the fundamental difference between the two. Basically, an instrumentation amp is a differential-input device with feedback committing it to voltage gain. In contrast, most op-amp configurations sacrifice their differential inputs to accommodate feedback. No doubt about it, those op amps do lose their ability to reject common-mode errors—and that ability is the primary feature of the instrumentation amp.

For many applications, the benefit of common-mode rejection can be considerable. In remote monitoring, for example, the op amp and the instrumentation amp respond differently to the presence of line error signals. Long connecting lines develop these ac signals from several sources, with noise pickup (e_N) common to all lines. For the ground return, there are the additional effects of ground line currents and ground loops that can add many volts of error. These effects create an ac net-ground-error signal (e_G), which is partly countered by the common presence of (e_N) in all the signal lines. In fact, even with the short signal lines, today's typical system mixture of digital and analog circuitry subjects sensitive analog inputs to

REJECTING COMMON-MODE SIGNALS



1. An op amp (a) amplifies line noise along with the signal; an instrumentation amp (b) uses common-mode rejection to attenuate noise.

radiated digital noise. With the op amp (see fig. 1a), the difference in the error signals (e_G–e_N) adds directly to the intended input signal (e_I), creating a combined input (e'_I):

$$e'_I = e_I + e_G - e_N.$$

That combination, which includes the error signals, is then amplified to produce an output voltage (e_O):

$$e_O = A(e_I + e_G - e_N),$$

where A is the op-amp's closed-loop gain.

To attenuate the error voltages, the instrumentation amp (see fig. 1b) adds a second input for remote sensing of the signal common. As a result, pickup errors (e_N) are common to the two inputs, and e_G merely shifts both input lines by the same amount, so that:

$$e'_I = e_I.$$

Both error sources produce voltages that are common-mode signals to the instrumentation amp. Such signals are attenuated by the amplifier's common-mode rejection ratio prior to amplification:

$$e_O = A[e_I + (e_G - e_N)/CMRR].$$

Typically, the amplifier's CMRR reduces the effect of line error voltages by 80 to 120 dB.

Of the three types of instrumentation amps, the difference amp offers the lowest cost and the highest common-mode voltage. It is the optimum choice in applications characterized by low voltage gain (up to 10) and small source impedances. Its structure (see fig. 2a) is simple, consisting of just an op amp and four resistors, but with demanding constraints on those resistors to achieve accepted levels of common-mode rejection.

The demands on the resistors used in this configuration also apply to the other two types of instrumentation amps. A good way to understand those requirements is the case where $R_1 = R_2$. With the e_2 input grounded, e_1 sees the op amp as a unity-gain inverter for a gain of –1. Alternately, with the e_1 input grounded, e_2 first faces a voltage divider that halves its amplitude (for a gain of ½). That diminished signal then sees a noninverting amp having a gain of +2. Therefore, the net gain for e_2 is +1. In the combined result, the two input signals receive equal but opposite gains for a net output that is proportional to the difference between them:

$$e_O = (R_2/R_1)(e_2 - e_1).$$

Any signal common to the two inputs is merely subtracted out, provided the resistance ratio of R_1 and R_2 is set precisely. For instance, Burr-Brown's INA105 monolithic difference amp provides 100 dB of common mode rejection by matching its internal resistor ratio to within at least 0.002%, or 20 parts per million. To realize such tight matching with components external to the op amp involves either the ultimate in resistor networks or labor-intensive trimming of low-drift discrete resistors. Although the diffused resistors of monolithic processes would be far from adequate, the addition of compatible thin film on the chip makes available the same resistor material used for the most precise resistor networks.

Circuit simplicity makes the difference amp the obvious winner in cost, yet it is not necessarily low man on the totem pole in performance. When appropriately configured, it can accommodate common-mode voltages more than an order of magnitude higher than the other two types of instrumentation amps, but it costs only about half as much.

The high common-mode capability of the difference amp comes from its voltage-divider action, which limits the voltage reaching the op-amp inputs. As a result, inputs to the difference amp can exceed the power-supply levels with the two R_1 resistors absorbing the excess. In the case of unity gain when $R_2 = R_1$, e_1 and e_2 can reach twice the power-supply level without damaging the circuit. For even greater voltage tolerance, the divider could be adjusted to make R_2 less than R_1, but then circuit gain would drop to less than unity.

With a modified feedback network, the difference amp can retain unity gain while accepting common-mode voltages on the order of 100 V, a level usually expected of only isolation amps. The modified configuration offers a low-cost alternative—typically by a factor of six—to isolation amps for demanding applications like sensing a motor's current from its line-powered winding.

The modification adds resistor R_3 and switches the value of the principal op-amp feedback resistance from R_2 to R_1 (see fig. 2b). Because of that value change, the e_1 signal sees a unity-gain inverter that is not affected by the presence of R_3. Since the resistor divider at the noninverting input does not change, the same attenuation and feedback actions protect the op-amp inputs. Making R_2 small compared to R_1 limits the voltage reaching those inputs to a small fraction of any common-mode input signal.

To restore unity gain to the

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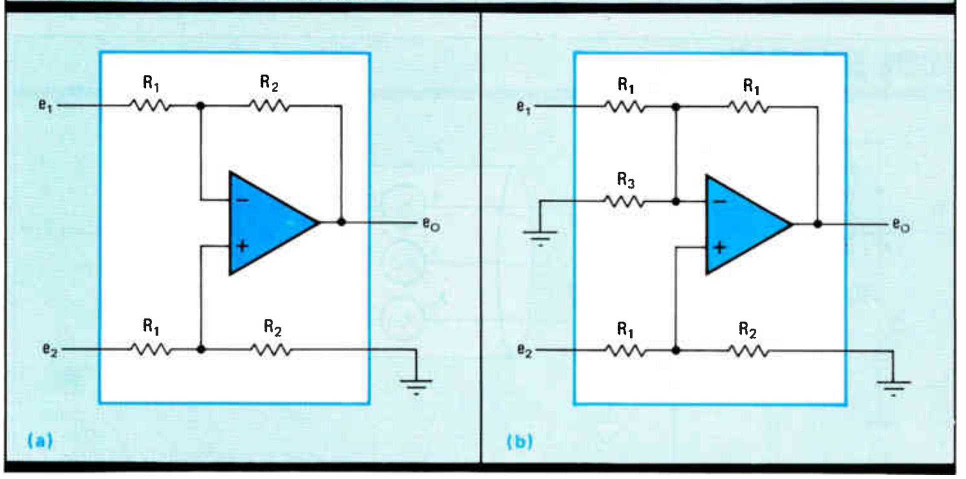

2. The simplest type of instrumentation amp (a) is the difference amp. Modifying its feedback configuration (b) lets it handle 200-V common-mode inputs.

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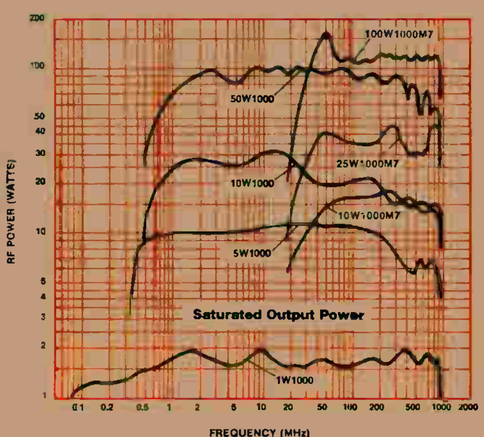

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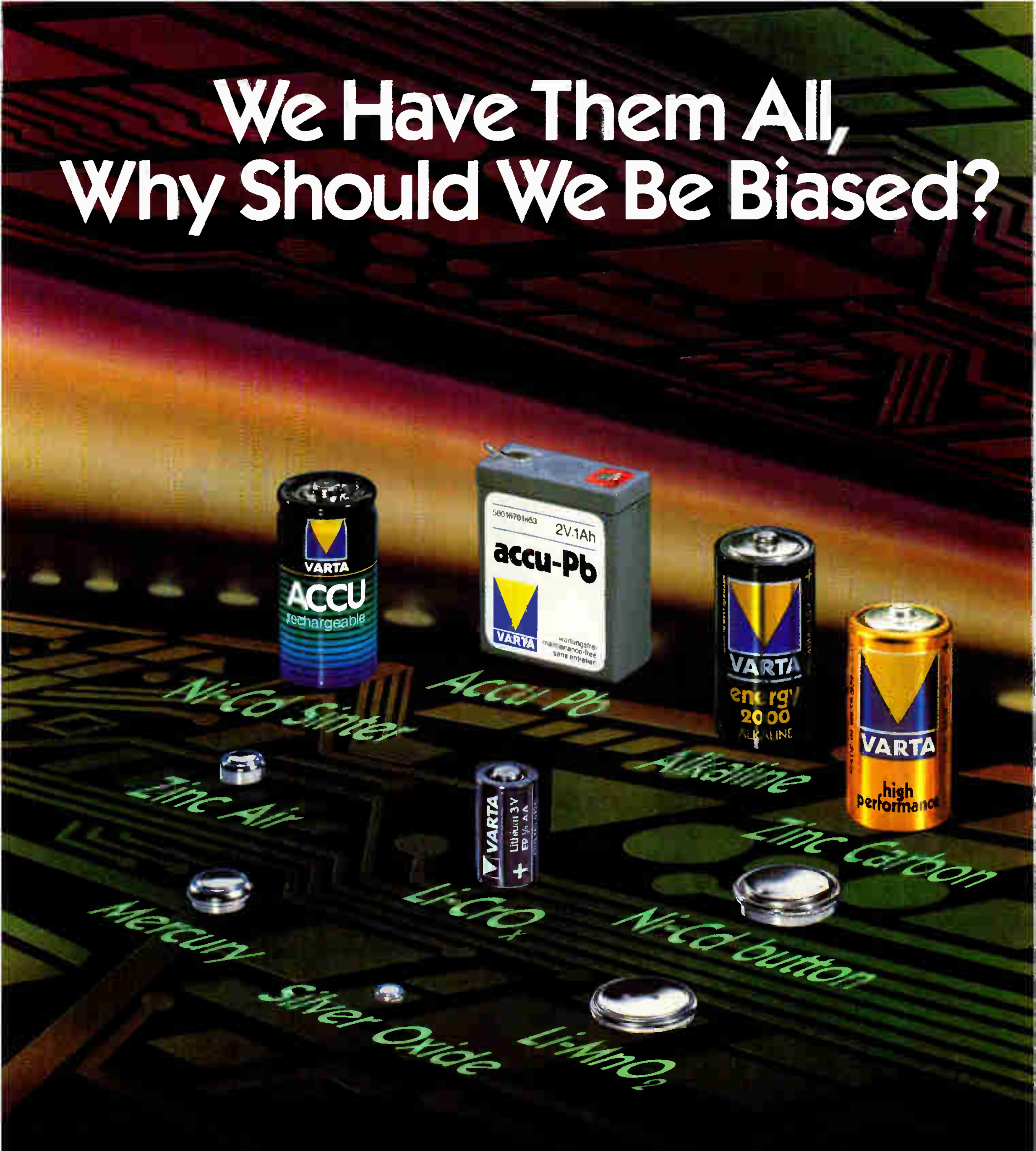

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e_2 signal after it has been attenuated by the R_1-R_2 voltage divider, R_3 raises the gain that e_2 sees at the noninverting op-amp input. For common-mode rejection, the gain magnitudes must be equal for the two inputs. When the parallel combination of R_1 and R_3 is the same as the value of R_2, the gain magnitudes are identical for e_1 and e_2, so that:

$$e_O = e_2 - e_1.$$

Using those resistor values, the recently introduced Burr-Brown INA117 monolithic modified difference amp accepts common-mode inputs of up to ±200 V even though it is powered from only ±15 V.

Naturally, whether it is modified or not, the difference amp does have certain limitations. Its gain, which is typically 10 or less, must remain fixed; and its input impedance compromises gain. For instance, the INA105 chip restricts gain to unity, while the unmodified INA106 monolithic difference amp extends gain to 10. Since gain is determined by the same resistors that are so carefully matched for high common-mode rejection, gain must stay fixed to preserve the benefit of the matching.

To realize higher gain values and variable gain settings requires the multiple stages that the other two types of instrumentation amps employ. Those additional stages buffer input impedance from low-gain-set resistance and eliminate the impact of gain on common-mode rejection.

The classic instrumentation amp, for instance, uses its three op-amp stages to improve other characteristics in addition to gain. One chip, the INA101, typifies the performance of this configuration. It offers an input impedance of 10 GΩ, selectable gain from 1 to 1,000, and 80 to 110 dB of common-mode rejection. Its 25-μV offset voltage and 0.25-μV/°C offset drift rival that of even precision industry-standard op amps like the OPA27. Those amps also lack the INA101's 100 dB of common-mode noise rejection and its internal resistance matching to within 0.1%.

The classic three op-amp configuration (see fig. 3) consists of two noninverting op amps, which control the circuit's gain, and a difference amp, which supplies the common-mode rejection. Input impedances are those of the op amps (A_1 and A_2), and feedback—rather than the signal source—supplies current for the gain-setting resistors.

Input amps A_1 and A_2 depart from the conventional noninverting op-amp connection—the normally grounded feedback resistor, R_G, is instead common to the two. This departure creates the differential input character of the composite structure. The feedback control of A_1 and A_2 transfers signals e_1 and e_2 to the two ends of R_G, making the voltage across R_G the difference between the two input signals. That difference voltage establishes a common feedback current for A_1 and A_2, allowing an amplified differential voltage to be developed between their outputs. The resistance values of R_1 and R_G control the gain applied to the differential signal:

$$e_O = (1 + 2R_1/R_G)(e_2 - e_1).$$

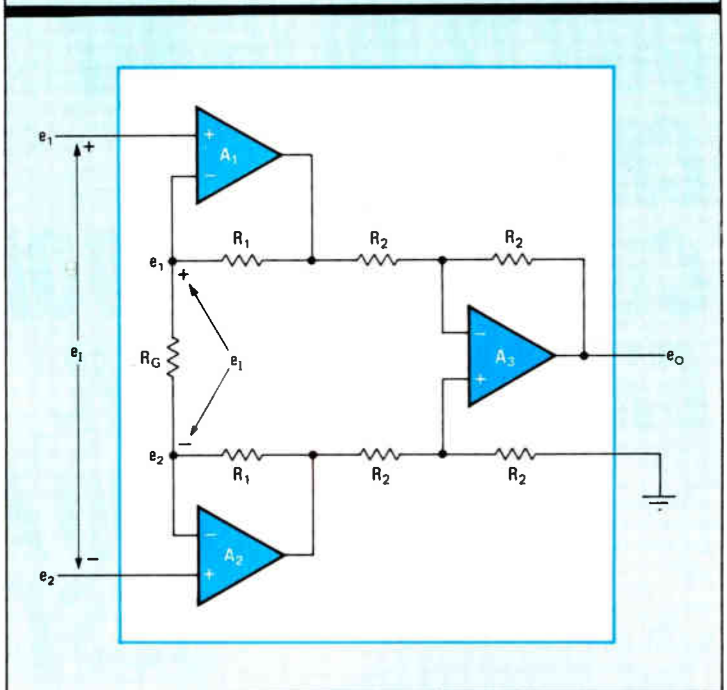
Signals common to the e_1 and e_2 terminals create no voltage across R_G and therefore no feedback current to benefit from circuit gain. Such common signals are, however, still transferred directly to the outputs of A_1 and A_2, producing a common-mode voltage for the difference amp (A_3). As before, the difference amp rejects this common-mode voltage but without conflicting demands for high input impedance and variable gain. And as before, common-mode rejection remains critically dependent on the ratio matching of equivalent resistors, but the effect of any mismatch occurs only after A_1 and A_2 have boosted the differential signal. High gain settings, therefore, bring greater overall common-mode rejection.

For most amplifiers, including the difference amp and the classic instrumentation amp, increasing gain causes a proportional decrease in bandwidth. But the transconductance type of instrumentation amp is an exception to this rule. Besides delivering high gain, it dramatically reduces bandwidth shrinkage as gain goes up. Moreover, at those higher gains, its bandwidth is 20 times broader than that of the classic configuration, although its cost is about the same.

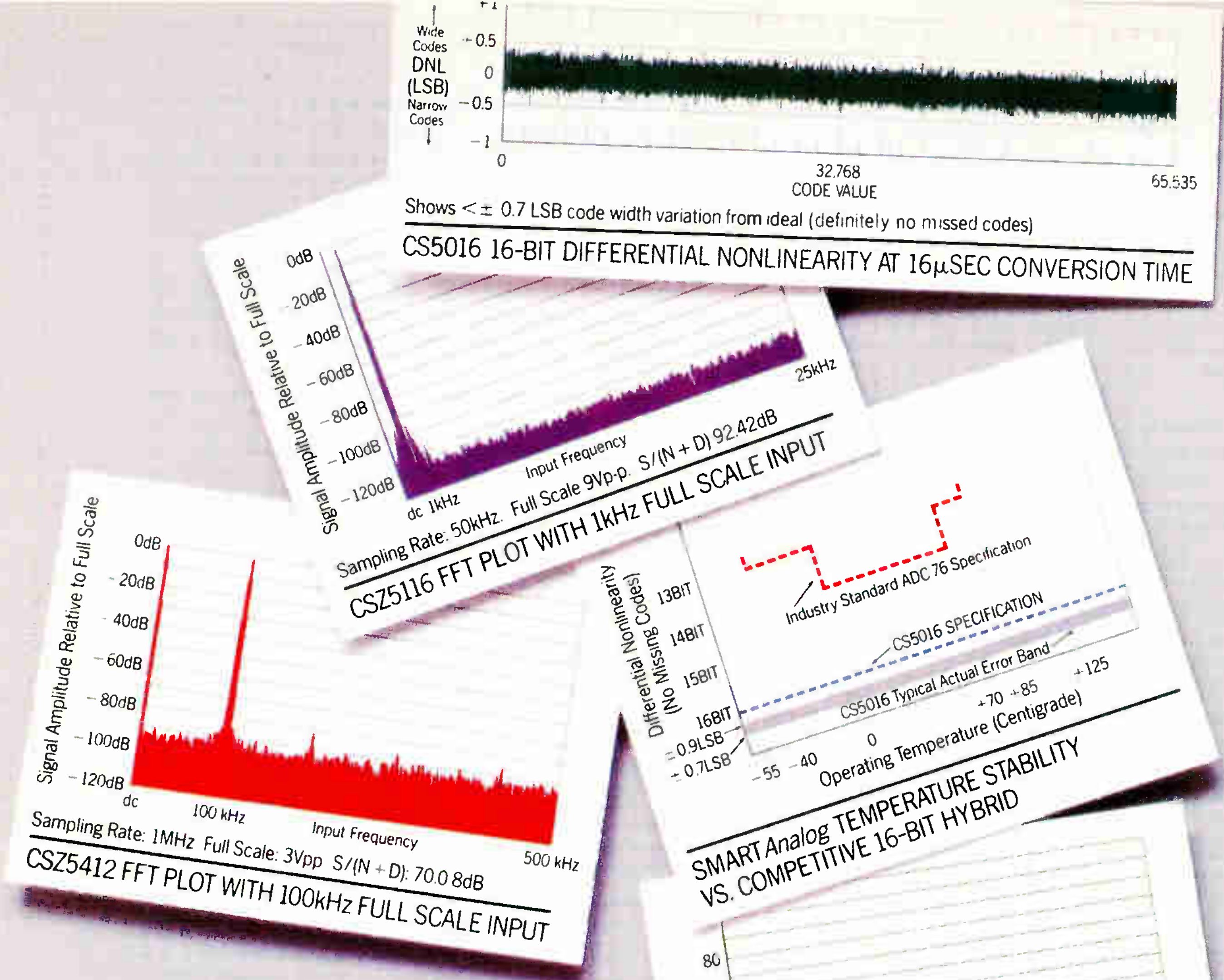
In fact, the transconductance instrumentation amp provides a gain-bandwidth product and dc accuracy that is unequaled even by broadband op amps. The monolithic INA110, for example, sustains a gain of 500 up to 100 kHz for a gain-bandwidth product of 50 MHz. While a few op amps have similar speed, they sacrifice dc accuracy for that speed. They cannot match the INA110's 100-μV input offset voltage and associated 2-μV/°C drift.

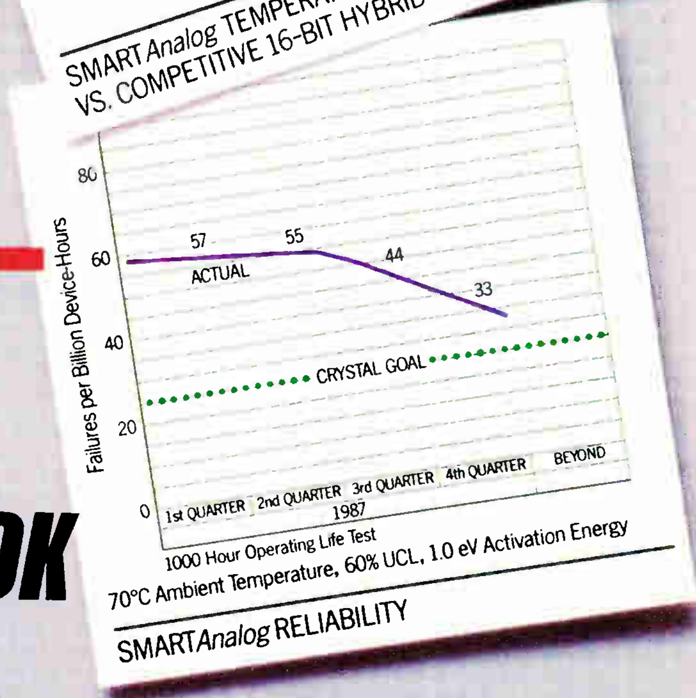
Nor do op amps offer the 0.1% pretrimmed gain accuracy of the INA110. Although the industry-standard OPA156 monolithic op amp offers excellent gain-bandwidth product and dc accuracy, its bandwidth is a fifth that of the INA110 and its offset voltage drift is

HIGH REJECTION WITH HIGH GAIN



3. Two amps (A_1, A_2) plus a difference amp (A_3) equals a three-op-amp instrumentation amp, with gain and common-mode rejection functions.





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No Missing Codes (Bits)	16	14	12	8	12	16	16	14	12
Dynamic Specifications									
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S/(N+D) (dB)					70	84	92	83	73
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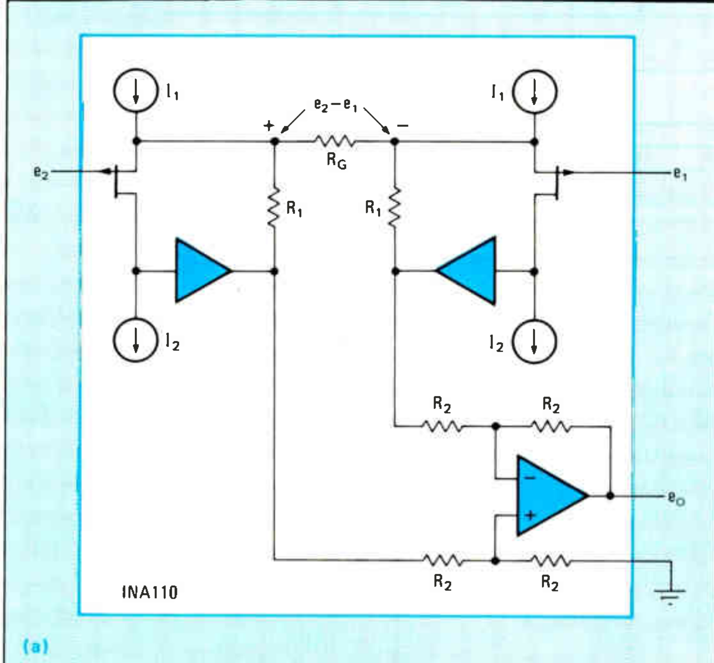

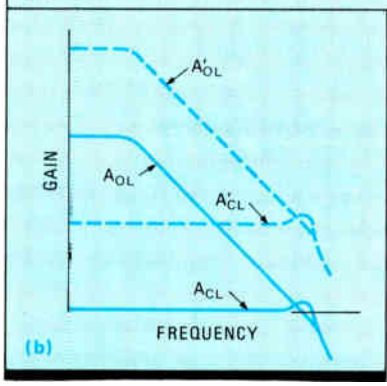

4. Gain-bandwidth product of the transconductance amp (a) is constant; when gain changes, closed- and open-loop responses (b) shift in tandem.

2.5 times greater in high-gain applications. Additionally because of its FET inputs, the INA110 holds input bias currents to just 20 pA, allowing this part to accept the resistance of input filters or high-impedance transducers without developing significant dc error.

The feedback arrangement of the transconductance amp (see fig. 4a) closely resembles that of the classic configuration. The principal difference comes in the input stage, which uses a pair of FETs, connected as source-followers, instead of the op amps. As in the classic configuration, the differential input signal is transferred to gain-setting resistor R_G, and the difference voltage across R_G defines the signal current in the two R_1 resistors, aided by feedback gain in the input stage. And as previously, a difference amp handles the signal from there.

In spite of these similarities, the transconductance amp operates differently than the classic device. Because R_G is connected between the sources of the input FETs, it degenerates the gain of the input stage and therefore affects the gain of the overall amplifier. Setting the value of R_G adjusts both closed-loop gain and attendant open-loop gain for optimal bandwidth.

The response curves (see fig. 4b) illustrate the effect of R_G on open-loop gain (A_{OL}), closed-loop gain (A_{CL}), and the amplifier's frequency stability. With R_G set at its highest value for unity gain, the solid curves show the circuit's open-loop and closed-loop responses. Open-loop gain supports the closed-loop response up to the bandwidth limit. Since the A_{OL} curve has only one pole prior to its intercept with the A_{CL} curve, the circuit provides frequency stability.

Substituting lower values of R_G moves A_{OL} and A_{CL} in tandemto the dashed curves of fig 4b. With a conventional op amp, increasing closed-loop gain would move only the closed-loop curve upward, and bandwidth would be interrupted at the intersection of A'_{CL} and A_{OL}. Alternately, starting with the dashed curves, a decrease in closed-loop gain that shifted only A'_{CL} downward and left A'_{OL} fixed would compromise frequency stability.

High-gain applications requiring good input dc accuracy, like bridge monitoring, are the best candidates for the transconductance amp as they are less affected by the device's increased output offset and drift. These output errors, which are higher for the transconductance device than the other instrumentation amps, are not amplified by circuit gain, and they become less significant when the effects of input offset error are highly amplified. Output offset is larger for the transconductance device because of the relatively high level of currents that the input circuitry must match.

With the transconductance amp, if the I_1 current sources exactly match the I_2 sources, there is no residual dc current delivered to the R_1 resistors. In practice, some mismatch will result in these 100-μA currents and that mismatch will drift with temperature. Part of the resulting voltage on the R_1 resistors is a common-mode signal to the difference amp, and thus it is rejected. The remainder of that voltage creates an output offset that is 1 mV for the INA110 transconductance amp compared with 0.2 mV for the INA101 classic configuration.

In the future, monolithic instrumentation amps will reap the benefits of higher common-mode voltage, lower noise, faster settling time, and broader bandwidth, as the three basic classes mix further with different and more exotic monolithic processes. Innovations in circuit structures and lower cost through improved yields will also transfer more complex instrumentation amps from hybrid to monolithic form. With other advances in monolithic technology, tomorrow's instrumentation amp chip is likely to offer gain settings that can be programmed electronically and selectable filter functions, like low-pass filtering, integrated right on the chip. □

JERALD GRAEME, design manager for instrumentation components at Burr-Brown Corp., is a leading analog designer. In his 22 years at Burr-Brown, he has worked with discrete, hybrid, and monolithic technologies to develop a broad cross-section of parts, including operational and instrumentation amplifiers, voltage-to-frequency converters, and analog signal-processing circuits. He is also the author of the Burr-Brown/McGraw-Hill series of books on amplifiers, published throughout the 1970s.

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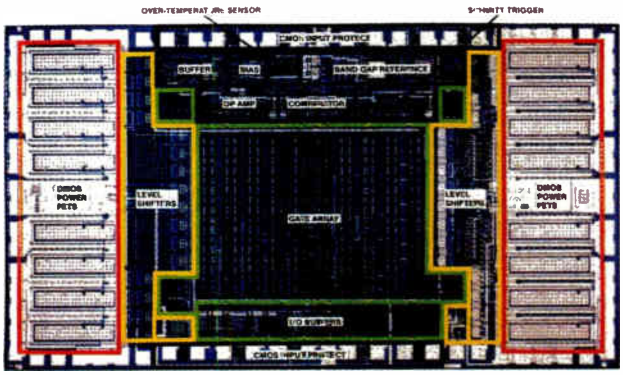

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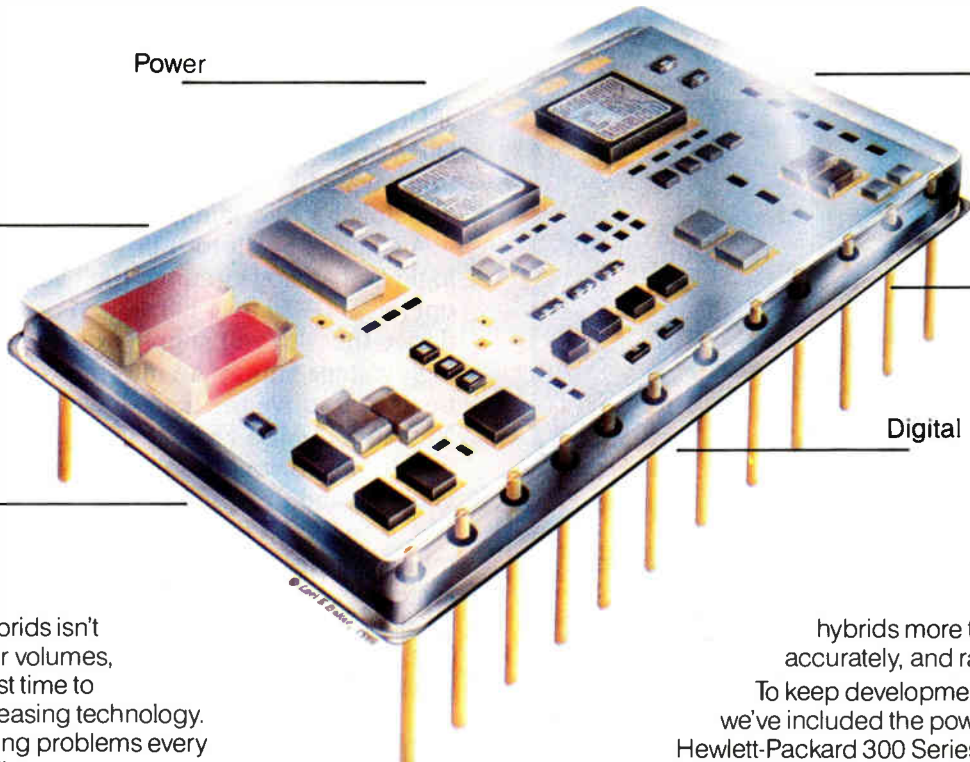
Finally, the hybrid system for testing hybrids.



Developing hybrids isn't easy. You have lower volumes, higher unit costs, fast time to market, rapidly increasing technology. And all kinds of testing problems every step of the way. Until now.

Introducing the SZ-M3600, the first test system designed specifically for testing hybrid circuits and modules.

The SZ-M3600 is a hybrid itself, combining the best features of the ATE world. Linear, digital, and power test capabilities. Rapid test development tools like those in expensive high-volume device testers. The modularity of rack and stack. The ease of operation of incoming inspection. And the latest technology to achieve a whole new price/performance level.

The SZ-M3600 reflects a decade of providing test solutions for standard and hybrid devices. Experience that includes the SZ-M3000, the largest selling compact device test system in Europe.

With the SZ-M3600, you get a modular architecture. Comprehensive instrumentation set. A choice of switching matrices. Pin drivers. Power supplies. IEEE interface. Everything you need to test and characterize hybrids more thoroughly, accurately, and rapidly.

To keep development time down, we've included the powerful 32-bit Hewlett-Packard 300 Series workstation. Plus a comprehensive high-level test development language, utilities, and template library routines.

Fully networkable, the SZ-M3600 is compatible with the entire SZ-M3000 family. And it's equally at home in engineering, production, incoming inspection and repair.

A short list of its features includes high-speed time measurement with 50 PSec resolution. Up to 4 x 48 switching matrices. Up to 64 pin driver/sensors. And multiple power sources, up to 2000 volts and 5 amps continuous.

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SMART POWER: CHANGING THE FACE OF POWER CONTROL

With its ability to combine control and power circuitry on the same chip, smart power has a host of advantages: higher speed and enhanced digital control and, at the system level, space and cost savings, plus better protection and diagnostics

by Art Fury, *Power Integrations Inc.*

Smart power is an emerging technology that may well exert a fundamental influence on the entire field of power control. Besides offering the traditional solid-state benefit of space savings, it also opens new markets, permitting electronics to encroach on what has been the sole domain of electromechanical devices. It brings significant performance enhancements because of its speed and digital control techniques. And it provides associated benefits for protection and diagnostics at the system level.

Yet the thrust into smart-power technology has brought confusion in its wake. Just what is a smart-power device? Everyone agrees that it is one that combines small-signal control with power circuitry—but there the consensus stops. Can a smart-power device be either a monolithic chip or a multichip hybrid? Is smart power strictly a MOS-based technology? What voltage and current capabilities should it have? Because of differences in definition, the market estimates for smart power show wide disparity: projections range anywhere from $25 to $275 million for 1987, growing to $2 or $3 billion by 1995.

Recently, the muddle was clarified by a definition devised by several major market researchers, including Dataquest Inc. in San Jose, Calif. A smart-power device, they agreed, should be an integrated circuit containing both control circuitry and the power-handling capability of supplying at least 1 A to the load or withstanding at least 100 V. Under this definition, smart power includes not only a number of significant older products, like three-terminal regulators and audio amplifiers, but also some major new developments. Among them are automotive circuits, motor controllers, flat-panel display drivers, and high-voltage multiplexers.

The most notable exclusion from this definition is multichip hybrid implementations. The omission is based on the argument that hybrid technology is simply an assembly technique that is an alternative to modules and printed-circuit boards.

Also, the definition does not specify a particular semiconductor process. There are many processes already in use to make smart-power ICs, with more on the way. It is not clear which of them, if any, will prevail and for what market segments.

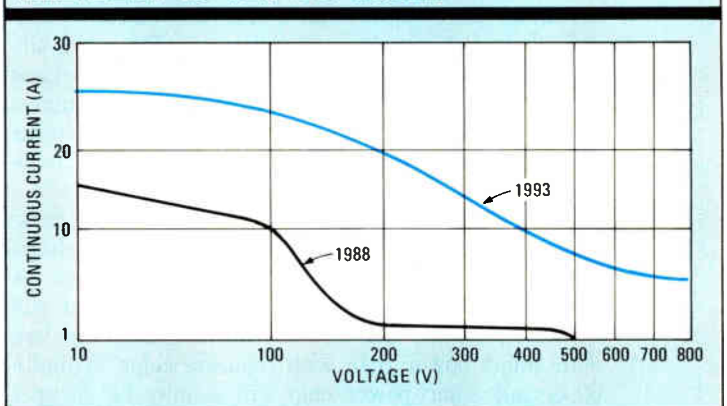
Finally, the class of ICs called "smart discretes" is also excluded. These small-scale chips add protection circuitry such as thermal shutdown or current limiting to a discrete bipolar or MOS transistor. However, because they do not integrate control circuitry, they are not considered to be smart power.

The first and most obvious benefit of smart power is space savings. When the end product can benefit, consolidation can be significant—for example, a motor controller can be mounted inside the motor itself. In fact, the advent of smart power requires a change in and system-design thinking (see panel, p. 145).

But there are more subtle advantages as well. With smart power, the close-by location of the protection circuitry makes it easy to measure current, voltage, temperature, and signal timing, thereby promoting safe operation. In contrast, remote sensing requires long wire runs, with their associated costs, and those wire runs can introduce errors.

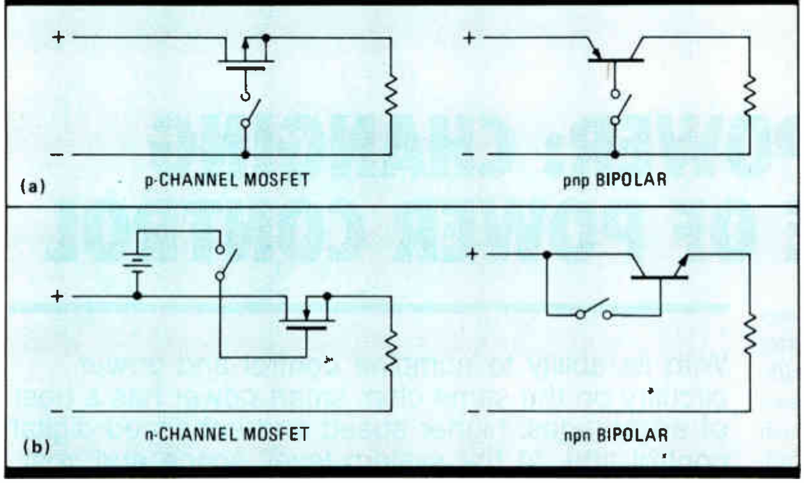
Long wires act as antennas, both radiating energy in the power section and receiving energy in the control section. The presence of fast-rising high-energy pulses, as in pulse-width-modulation circuits, can cause serious errors for low-level control signals, such as position sensors on a motor, or high-impedance drive circuits, such as the gate of a MOS power tran-

THE BEST IS YET TO COME



1. Smart-power voltage and current ratings will improve sharply, over the next five years, at least doubling across the entire range.

CONNECTING LOADS IN COMMON



2. P-type transistors (a) are best for driving loads connected to a common negative point; the gate voltage of n-channel MOS FETs (b) must be higher than the supply.

sistor. Combining power and control circuitry on one chip dramatically lowers these errors.

Smart power also addresses timing problems. MOS transistors switch in tens to hundreds of nanoseconds, so long wires act as delay lines in the feedback loop. These delays reduce protection for the device driving the load when it becomes overloaded, or they allow high voltage and high current to be present simultaneously.

Many benefits of smart power come from its high-voltage capability. For example, high-voltage displays, which require nearly 200 V, will not tolerate either the large space required by discretes or the reliability problems created by having a large number of components. Smart power enhances reliability in three ways: it reduces the number of separate components per circuit so as to decrease the probability of failure; it minimizes the number of interconnections; and its high-voltage ratings increase the margin above normal operating voltages. In some cases, the high-voltage capability of smart power allows logic to operate at the same voltage as the load, thereby eliminating a power supply and increasing noise immunity.

Generally speaking, combining control with power consumes more silicon than would be used for a separate control chip and a power discrete. The extra silicon provides isolation between the different sections of the smart-power chip. Moreover, at high voltages, the penalties in die size go up because good bipolar transistors or vertical MOS transistors require additional silicon.

Often offsetting the penalty in die size is high package cost. If the die sizes are small, as for high-voltage transistor arrays, or if the package costs are high, as for high-power housings, then the package cost will dominate. So the net cost to the user becomes less with smart power than with separate chips. A multiple-output smart-power chip will usually be cheaper than an equivalent control IC plus power discretes, but a single-output smart-power device may not be an obvious cost-effective choice, depending on its price and interconnection costs. By far, the greater cost impact comes from factors other than the smart-power chip itself. Besides the advantages of less parts to mount and fewer parts for greater reliability, smart-power chips also simplify interconnection. Typically, the power portion of a system must be mounted so as to dissipate heat, thereby requiring more than just traces on a board. A single package not only consolidates two assemblies into one, but it also minimizes the number of interconnection lines.

Furthermore, since the power section often dominates the die size and since package cost dominates at high power levels, the addition of extra control and protection circuitry has little or no impact on cost. As a result, a smart-power IC may often contain extra control features for the same cost. In fact, a custom or semicustom smart-power device can bring significant end-product advantages at no cost penalty.

The maximum current rating for smart power is a matter of economics, not technology. The higher the current, the bigger the die and the higher the cost—and the cost goes up exponentially. At some point, it is less expensive to use separate control and power chips. Once again, factors such as package cost enter, but as a good rule of thumb, smart power seems to be economically viable up to about 10 A total at low voltage and up to around 5 A above 200 V. However, technological advances are likely to improve these figures significantly (see fig. 1).

Likewise, the higher the voltage, the larger the die size, so low-voltage smart-power ICs tend to be more economical than high-voltage ones. At 100 V and below, there are several viable technologies, both bipolar and MOS, for obtaining voltage isolation between input and output, including self-isolation and junction isolation. These technologies can be stretched to 200 V—but with compromises. Above 200 V, it is difficult to get isolation between input and output. Also, at that level, it is hard to build good bipolar transistors and vertical MOS devices, so most high-voltage ICs use lateral MOS outputs, which are large but perform well. One other technique is dielectric isolation, but since it requires mechanical backlapping of the wafers, cost is significantly higher. Today, with dielectric isolation, voltages of 400 to 600 V are practical.

When MOS transistors, rather than bipolar devices, make up the smart-power output, users must understand the different impact of speed and current ratings. MOS transistors are generally much faster than bipolar devices. Although that speed is a great advantage, it can be a mixed blessing, causing such problems as loss of protection. Moreover, the question of how much current a MOS output can handle does not have as clear an answer as in the case of a bipolar output. A bipolar device can burn up when its maximum current rating is exceeded. With a MOS FET, however, the critical parameter is on-resistance, not current rating.

Every MOS FET has a parasitic bipolar diode con-

LD SERIES Linear Power Supplies

SINGLE OUTPUT. WIDE RANGE.

	MAX CURRENT AT OPERATING TEMPERATURE OF (A)[1] 40°C	50°C	60°C	DIMENSIONS[2] (inches)	PRICE	MODEL
0-7V ADJ.	3.4(3.4)	2.9(2.85)	2.4(1.8)	5 5/8 × 4 7/8 × 2 5/8	$247	**LDS-Y-01**
	4.8(4.1)	4.0(3.4)	3.1(2.6)	7 × 4 7/8 × 2 7/8	307	**LDS-X-01**
	6.6(5.6)	5.7(4.8)	4.5(3.8)	9 × 5 × 2 7/8	372	**LDS-W-01**
	9.5(9.0)	8.5(8.0)	7.5(7.1)	11 × 4 7/8 × 4 13/32	466	**LDS-P-01**
0-18V ADJ.	1.8(1.8)	1.6(1.6)	1.4(0.9)	5 5/8 × 4 7/8 × 2 5/8	247	**LDS-Y-02**
	2.3(1.95)	1.9(1.6)	1.5(1.3)	7 × 4 7/8 × 2 7/8	307	**LDS-X-02**
	3.2(2.7)	2.8(2.4)	2.2(1.9)	9 × 5 × 2 7/8	372	**LDS-W-02**
	4.5(4.3)	4.0(3.8)	3.3(3.1)	11 × 4 7/8 × 4 13/32	466	**LDS-P-02**
0-32V ADJ.	1.1(1.1)	1.0(0.95)	0.8(0.6)	5 5/8 × 4 7/8 × 2 5/8	247	**LDS-Y-03**
	1.5(1.25)	1.3(1.1)	1.1(0.95)	7 × 4 7/8 × 2 7/8	307	**LDS-X-03**
	2.1(1.8)	1.9(1.5)	1.4(1.2)	9 × 5 × 2 7/8	372	**LDS-W-03**
	2.7(2.5)	2.5(2.4)	2.3(2.2)	11 × 4 7/8 × 4 13/32	466	**LDS-P-03**

SINGLE OUTPUT. FIXED VOLTAGE.

	MAX CURRENT AT OPERATING TEMPERATURE OF (A)[1] 40°C	50°C	60°C	DIMENSIONS[2] (inches)	PRICE	MODEL
5V ±5% ADJ.	5.4(5.0)	4.4(4.0)	3.3(3.0)	5 5/8 × 4 7/8 × 2 5/8	$247	**LDS-Y-5-OV**
	10.0(8.5)	8.6(7.3)	7.0(6.0)	7 × 4 7/8 × 2 7/8	307	**LDS-X-5-OV**
	14.0(11.9)	11.7(9.9)	9.1(7.7)	9 × 5 × 2 7/8	372	**LDS-W-5-OV**
	22.0(20.9)	18.8(18.0)	15.6(14.8)	11 × 4 7/8 × 4 13/32	466	**LDS-P-S-OV**
12V ±5% ADJ.	3.7(3.4)	2.9(2.55)	2.0(1.75)	5 5/8 × 4 7/8 × 2 5/8	237	**LDS-Y-12**
	6.5(5.5)	5.5(4.7)	4.5(3.8)	7 × 4 7/8 × 2 7/8	294	**LDS-X-12**
	8.5(7.2)	7.0(6.0)	5.3(4.5)	9 × 5 × 2 7/8	359	**LDS-W-12**
	14.0(13.3)	12.4(11.8)	10.0(9.5)	11 × 4 7/8 × 4 13/32	454	**LDS-P-12**
15C ±5% ADJ.	3.25(3.0)	2.5(2.25)	1.7(1.55)	5 5/8 × 4 7/8 × 2 5/8	237	**LDS-Y-15**
	5.5(4.7)	4.6(3.9)	3.6(3.1)	7 × 4 7/8 × 2 7/8	294	**LDS-X-15**
	7.7(6.55)	6.2(5.3)	4.7(4.0)	9 × 5 × 2 7/8	359	**LDS-W-1S**
	12.0(11.4)	10.6(10.0)	8.5(8.1)	11 × 4 7/8 × 4 13/32	454	**LDS-P-1S**
20V ±5% ADJ.	2.5(2.25)	2.0(1.8)	1.5(1.35)	5 5/8 × 4 7/8 × 2 5/8	237	**LDS-Y-20**
	4.4(3.7)	3.6(3.1)	2.6(2.2)	7 × 4 7/8 × 2 7/8	294	**LDS-X-20**
	6.1(5.2)	5.0(4.3)	3.8(3.2)	9 × 5 × 2 7/8	359	**LDS-W-20**
	10.0(9.5)	8.9(8.5)	7.0(6.6)	11 × 4 7/8 × 4 13/32	454	**LDS-P-20**
24V ±5% ADJ.	2.1(1.9)	1.7(1.55)	1.3(1.15)	5 5/8 × 4 7/8 × 2 5/8	237	**LDS-Y-24**
	3.8(3.2)	3.2(2.7)	2.4(2.0)	7 × 4 7/8 × 2 7/8	294	**LDS-X-24**
	5.4(4.6)	4.4(3.7)	3.3(2.8)	9 × 5 × 2 7/8	359	**LDS-W-24**
	9.0(8.5)	8.0(7.6)	6.0(5.7)	11 × 4 7/8 × 4 13/32	454	**LDS-P-24**
28V ±5% ADJ.	1.9(1.65)	1.5(1.35)	1.1(1.0)	5 5/8 × 4 7/8 × 2 5/8	237	**LDS-Y-28**
	3.4(2.9)	2.9(2.5)	2.2(1.9)	7 × 4 7/8 × 2 7/8	294	**LDS-X-28**
	4.7(4.0)	4.0(3.4)	3.1(2.6)	9 × 5 × 2 7/8	359	**LDS-W-28**
	8.0(7.6)	7.1(6.7)	5.2(4.9)	11 × 4 7/8 × 4 13/32	454	**LDS-P-28**
48V ±5% ADJ.	1.36(1.2)	1.05(0.95)	0.75(0.70)	5 5/8 × 4 7/8 × 2 5/8	247	**LDS-Y-48**
	2.1(1.9)	1.8(1.6)	1.4(1.2)	7 × 4 7/8 × 2 7/8	307	**LDS-X-48**
	3.0(2.6)	2.6(2.2)	2.0(1.7)	9 × 5 × 2 7/8	372	**LDS-W-48**
	4.5(4.28)	4.0(3.8)	3.4(3.2)	11 × 4 7/8 × 4 13/32	466	**LDS-P-48**
100V ±5% ADJ.	0.55(0.55)	0.45(0.45)	0.35(0.35)	5 5/8 × 4 7/8 × 2 5/8	264	**LDS-Y-100**
	1.6(1.6)	1.4(1.4)	1.2(1.2)	11 × 4 7/8 × 4 13/32	483	**LDS-P-100**
120V ±5% ADJ.	0.45(0.45)	0.35(0.35)	0.25(0.25)	5 5/8 × 4 7/8 × 2 5/8	264	**LDS-Y-120**
	1.4(1.4)	1.2(1.2)	1.0(1.0)	11 × 4 7/8 × 4 13/32	483	**LDS-P-120**
150V ±5% ADJ.	0.35(0.25)	0.25(0.25)	0.15(0.15)	5 5/8 × 4 7/8 × 2 5/8	264	**LDS-Y-150**
	1.1(1.1)	0.9(0.9)	0.8(0.8)	11 × 4 7/8 × 4 13/32	483	**LDS-P-150**

NOTE: 1. Ratings in parenthesis when cover is used.
2. Dimensions include cover.

LR SERIES
Specifications

DC OUTPUT
Voltage range shown in tables.

REGULATED VOLTAGE

regulation, line .... 0.1% from 95 to 132VAC. 95 to 132VAC or 187 to 265VAC on LRS-57, 58 and "M" option models. 187 to 265VAC on LRS-59 and "V" option models.
regulation, load .... 0.1% from no load to full load.
ripple and noise .... 10mV RMS, 35mV pk-pk for 5V and 6V models. (25mV pk-pk for 2V models.)
15mV RMS, 100mV pk-pk for 12V through 28V models.
35mV RMS, 150mV pk-pk for 48V models.
temperature coefficient .... 0.03%/°C.
remote programming resistance .... 1000Ω/volt.
remote programming voltage .... volt per volt.

AC INPUT

line .... 95 to 132VAC, 47-440Hz.
95 to 132VAC or 187 to 265VAC (user selectable), 47-440Hz on LRS-57, 58 and "M" option models. 187 to 265VAC, 47-440Hz on LRS-59 only.
power .... LRS-52: 137 watts maximum.
LRS-53: 225 watts maximum.
LRS-54: 380 watts maximum.
LRS-55: 515 watts maximum.
LRS-56: 819 watts maximum.
LRS-57: 1100 watts maximum.
LRS-58: 1350 watts maximum.
LRS-59: 1900 watts maximum.

DC INPUT
145VDC ± 10%. (260 to 370VDC for LRS-57, 58, 59, and "M" and "V" option models.)

EFFICIENCY
55% min for 2V models. 67% min for 5V and 6V models of LRS-52. 70% min for 5V through 15V models of LRS-53, 54. 75% min for 5V and 6V models of LRS-55, 56; 5V through 15V models of LRS-57, 58, 59; 12V through 20V models of LRS-52; 20V through 48V models of LRS-53, 54. 77% min for 12V through 20V models of LRS-55, 56. 78% min for 24V through 48V models of LRS-52. 80% min for 20V through 48V models of LRS-57, 58, 59; 24V through 48V models of LRS-55, 56.

OVERSHOOT
No overshoot at turn-on, turn-off or power failure.

OPERATING TEMPERATURE RANGE
Continuous duty −10°C to +71°C with suitable derating above 40°C. Guaranteed turn-on at −20°C.

STORAGE TEMPERATURE RANGE
−55°C to +85°C.

OVERLOAD PROTECTION
ELECTRICAL
External overload protection, automatic electronic current limiting circuit limits the output current to a preset value, thereby providing protection for the load as well as the power supply.

THERMAL
Self-resetting thermostat.

FUSING
Line fuse removes the power supply from the line if a short occurs in the input circuitry.

OVERVOLTAGE PROTECTION
Overvoltage protection is standard on all models. If output voltage increases above a preset level, inverter drive is removed.

COOLING
All units are convection cooled. No fans or blowers are needed.

IN-RUSH LIMITING
The turn-on in-rush current will not exceed 40 amps peak from a cold start. (50 amps on LRS-57, 58, 59.)

DC OUTPUT CONTROLS
Simple screwdriver adjustment over the entire voltage range.

INPUT AND OUTPUT CONNECTIONS
All input, output, sensing, and remote on/off connections for LRS-52 and LRS-53 are made through barrier strip terminals. All input, sensing and remote on/off connections for LRS-54, LRS-55, LRS-56, LRS-57, LRS-58 and LRS-59 are made through barrier strip terminals. DC output connection is made through heavy duty threaded bus bars.

MOUNTING
Two mounting surfaces and two mounting positions on LRS-52, 53, 54. One mounting surface and one mounting position on LRS-55, 56, 57, 58, 59.

POWER FAILURE
2V, 5V and 6V models will remain within regulation limits for at least 16.7 msec. after loss of AC power when operating at full load, V_O max, and 105VAC input at 60Hz. (105 or 210VAC for LRS-57, 58 and "M" option models. 210VAC at 60Hz for LRS-59.)

REMOTE SENSING
Provision is made for remote sensing to eliminate the effects of power output lead resistance on DC regulation.

REMOTE TURN-ON/TURN-OFF
Provision is made for digitally controlled remote turn-on, turn-off (TTL Compatible).

FUNGUS PROOFING
All units are inherently fungi inert.

MILITARY SPECIFICATIONS
The LR series has passed the following tests in accordance with MIL-STD-810C.
1) Low Pressure — Method 500.1, Procedure I.
2) High Temperature — Method 501.1, Procedures I and II.
3) Low Temperature — Method 502.1, Procedure I.
4) Temperature Shock — Method 503.1, Procedure I.
5) Temperature-Altitude — Method 504.1, Procedure I. Class 2 (−10°C Operating).
6) Humidity — Method 507.1, Procedure I.
7) Fungus — Method 508.1, Procedure I.
8) Vibration — Method 514.2, Procedures X and XI.
9) Shock — Method 516.2, Procedures I and III.

EMI
Conducted EMI conforms to FCC Docket 20780 Class A, and MIL-STD-461A Notice 4 CEO4 for power leads. LRS-57, LRS-58, LRS-59, and "M" and "V" option models also conform to VDE 0871 Class A.

PHYSICAL DATA

Package Model	Lbs. Net	Lbs. Ship	Size Inches
LRS-52	2¼	3¼	2 × 4⅞ × 6¼
LRS-53	3¼	4¼	2⅜ × 4⅞ × 8½
LRS-54	6½	7½	3 × 4⅞ × 11
LRS-55	7	8½	3¾ × 4⅞ × 10½
LRS-56	8½	10	4 7/16 × 4⅞ × 11½
LRS-57	10½	12	5 × 4⅞ × 12
LRS-58	12½	14	5½ × 4⅞ × 13⅛
LRS-59	16½	19	6⅝ × 4⅞ × 13 25/32

OPTIONS

AC Input

Add Suffix[1]	For Operation at:	Price
−V (LRS-55, 56 only)	185 to 265VAC 47-440Hz	12%
−M (LRS-52, 53, 54 only)	95 to 132VAC or 187 to 265VAC, 47-440Hz (customer selectable)	12%

[1] Add Suffix after package number, i.e.: LRS-55V-5, LRS-52M-5.

ACCESSORIES
Rack Adapters (LRA-14, LRA-15, LRA-17) and cable system available.

FINISH
Grey, Fed. Std. 595, No. 26081.

GUARANTEED FOR 5 YEARS
Five year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of 5 years.

UL /CSA
UL Recognized. CSA Certified. LRS-57, 58, 59 under evaluation.

TUV LICENSED
110/220 and 220 input versions.

LN AND LD SERIES

Specifications

DC OUTPUT
Voltage range shown in tables.

REGULATED VOLTAGE
regulation, line .... LN Series: 0.1%. (0.15% for LN-Z)
LD Series: 0.005% + 0.5mV for line variations from 105 to 127VAC.

regulation, load .... LN Series: 0.1% (0.15% for LN-Z).
LD Series: 0.005% + 0.5mV for load variations from 0 to full load.

ripple and noise .... LN Series: 1.5mV RMS, 5mV pk-pk (5mV RMS, 15mV pk-pk for LNS-P-48) with either positive or negative terminal grounded.
LD Series: 1mv pk-pk, 150µV RMS (250µV for 100V, 120V, 150V units).

temperature coefficient .... LN Series: 0.03%/°C.
LD Series: ±(0.005% + 10µV)/°C on wide range models with external programming resistors. ±(0.01% + 10µV)/°C on wide models with internal programming resistors, and then from 1 volt to final desired value.

remote programming resistance .... LN Series: 200Ω/volt nominal (LNS models only).
LD Series: 1000Ω/volt nominal. Downward programming to voltages less than 1 volt must be accomplished in two steps; first, from original voltage value to 1 volt, and then from 1 volt to final desired value.

remote programming voltage .... volt per volt (LNS and LD models only).

AC INPUT
line .... 105 to 127VAC, 210 to 254VAC (by transformer tap change) 47-440Hz. Consult factory for operation at frequencies other than 57-63Hz.

OVERSHOOT
No overshoot on turn-on, turn-off or power failure.

OPERATING TEMPERATURE RANGE
Continuous duty from 0° to +71°C on LN Series with corresponding load current ratings for all modes of operation. Continuous duty from 0° to 60°C on LD Series with suitable deratings above 40°C.

STORAGE TEMPERATURE RANGE
−55°C to +85°C.

OVERLOAD PROTECTION
ELECTRICAL
External overload protection, automatic electronic current limiting circuit limits the output current to a preset value, thereby providing protection for the load as well as the power supply.

THERMAL
Thermostat — automatically reset when overtemperature condition is eliminated.

OVERVOLTAGE PROTECTION
Overvoltage protection module crowbars output when trip level is exceeded — standard on all 5V models and both outputs of model LND-X-MPU.

COOLING
All units are convection cooled. No external heat sinking or forced air is required.

DC OUTPUT CONTROLS
Simple screwdriver adjustment over the entire voltage range of LN Series and fixed voltage LD models. On wide range LD models, an adjustable range of 1%-Vo max to Vo max is provided by the internal programming potentiometer; programming over the full 0 to Vo max range can be accomplished by remote sensing.

INPUT AND OUTPUT CONNECTIONS
Heavy-duty screw terminals on printed circuit board. Solder turrets provide for remote programming operation on LD Series.

TRACKING ACCURACY (DUAL TRACKING MODELS ONLY)
3% absolute voltage difference, 0.2% change for all conditions of line, load and temperature.

MOUNTING
Three mounting surfaces, three mounting positions. One mounting position for LN-P models. LN Series: LDS-Y, X, W: Three mounting surfaces, two mounting positions. Two mounting surfaces on wide range and 48V models when used with optional adjustable LHOV. One mounting surface one mounting position on LDS-P.

REMOTE SENSING
Provision is made for remote sensing to eliminate the effect of power output lead resistance on DC regulation.

TRANSFORMER
MIL-T-27C, Grade 6; Electrostatic shield; 4000VAC input/output isolation.

ISOLATION RATING
Minimum, 10 Megohm isolation from DC to ground at 750VDC.

FUNGUS PROOFING
No fungi nutrient material used.

MILITARY SPECIFICATIONS
The LN and LD Series has passed the following tests in accordance with MIL-STD-810C.
1) Low Pressure—Method 500.1, Procedure I.
2) High Temperature—Method 501.1, Procedures I & II.
3) Low Temperature—Method 502.1, Procedure I.
4) Temperature Shock—Method 503.1, Procedure I.
5) Temperature-Altitude—Method 504.1, Procedure I. Class 2 (0°C operating)
6) Humidity—Method 507.1, Procedures I & II.
7) Fungus—Method 508.1, Procedure I.
8) Vibration—Method 514.2, Procedures X & XI.
9) Shock—Method 516.2, Procedures I & III.
MIL-I-6181D—Conducted and radiated EMI with one output terminal grounded.

PHYSICAL DATA

Package Model	Lbs. Net	Lbs. Ship	Size Inches
LN-Z	3	3¼	4⅞ × 4 × 1¾ (w/cover)
			4⅞ × 4 × 1⅝ (w/o cover)
LN-Y/LD-Y	5	5½	5⅝ × 4⅞ × 2⅝ (w/cover)
			5⅝ × 4⅞ × 2½ (w/o cover)
LN-X/LD-X	7¾	8¼	7 × 4⅞ × 2⅞ (w/cover)
			7 × 4⅞ × 2¾ (w/o cover)
LN-W/LD-W	9	9½	9 × 4⅞ × 2⅞ (w/cover)
			9 × 4⅞ × 2¾ (w/o cover)
LNS-P/LD-P	14	15½	11 × 4⅞ × 4 13/32 (w & w/o cover)
LND-P	15½	17	11 × 4⅞ × 4 13/32 (w & w/o cover)

ACCESSORIES
Overvoltage protectors (standard on 5V models and on LND-X-MPU).

Power Supply Series	OV Series
LNS-Z	L-6-OV (Fixed)
LNS-Y/LDS-Y	L-6-OV (Fixed)
LNS-X/LDS-X	L-12-OV (Fixed)
LNS-W/LDS-W	L-20-OV (Fixed)
LNS-P/LDS-P	L-35-OV (Fixed) for 5 & 6V Models
	L-20-OV (Fixed) for others
LND (All Series)	L-12-OV (Fixed)
All 01, 02, 03 and 48V Models	LH OV (Adjustable)

FINISH
Grey, Fed. Std. 595, No. 26081.

GUARANTEED FOR 5 YEARS
5-year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of 5 years.

UL /CSA
UL Recognized. CSA Certified. (100V, 120V and 150V models of LD Series presently under test.

THE LAMBDA LR SERIES

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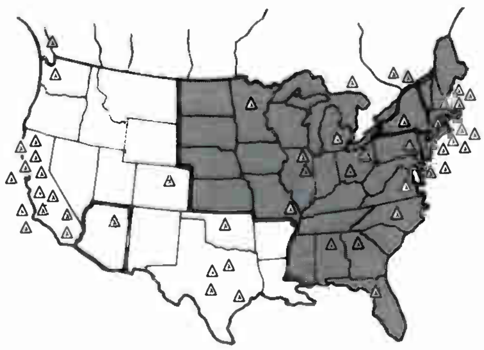

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3/88

LN SERIES Linear Power Supplies

DUAL OUTPUT

	VOLT VDC	MAX CURRENT AT OPERATING TEMPERATURE OF (A)[1] 40°C	50°C	60°C	71°C	DIMENSIONS[2] (inches)	PRICE	MODEL
5V ±5% ADJ. 9V-12V ADJ.	5±5%	7.0(6.0)	6.0(5.1)	4.7(4.0)	3.2(2.7)	7 × 4$\frac{7}{8}$ × 2$\frac{7}{8}$	$268	**LND-X-MPU**[3]
	9-12	1.2(1.0)	1.1(1.0)	1.0(0.8)	0.8(0.7)			

DUAL TRACKING

	VOLT VDC	40°C	50°C	60°C	71°C	DIMENSIONS (inches)	PRICE	MODEL
±15V to ±12V ADJ.	±15 to	0.6(0.5)	0.55(0.5)	0.45(0.4)	0.3(0.3)	4$\frac{7}{8}$ × 4 × 1$\frac{3}{4}$	$127	**LND-Z-152**
	±12	0.6(0.5)	0.55(0.5)	0.45(0.4)	0.3(0.3)			
	±15 to	1.4(1.2)	1.2(1.0)	0.9(0.8)	0.6(0.5)	5$\frac{5}{8}$ × 4$\frac{7}{8}$ × 2$\frac{5}{8}$	179	**LND-Y-152**
	±12	1.2(1.0)	1.1(0.9)	0.8(0.7)	0.5(0.4)			
	±15 to	2.5(2.1)	2.1(1.8)	1.6(1.4)	1.1(0.9)	7 × 4$\frac{7}{8}$ × 2$\frac{7}{8}$	235	**LND-X-152**
	±12	2.3(2.0)	1.9(1.6)	1.4(1.2)	0.9(0.8)			
	±15 to	3.3(3.0)	3.1(2.8)	2.6(2.3)	2.0(1.8)	9 × 5 × 2$\frac{7}{8}$	266	**LND-W-152**
	±12	3.1(2.8)	2.8(2.5)	2.3(2.1)	1.6(1.4)			
	±15 to	5.3(5.0)	4.7(4.5)	3.9(3.7)	2.9(2.7)	11 × 4$\frac{7}{8}$ × 4$\frac{13}{32}$	357	**LND-P-152**
	±12	4.6(4.4)	4.0(3.8)	3.3(3.1)	2.5(2.4)			

SINGLE OUTPUT

	MAX CURRENT AT OPERATING TEMPERATURE OF (A)[1] 40°C	50°C	60°C	71°C	DIMENSIONS[2] (inches)	PRICE	MODEL
5V ±5% ADJ.	3.0(2.7)	2.7(2.4)	2.3(2.1)	1.7(1.5)	4$\frac{7}{8}$ × 4 × 1$\frac{3}{4}$	$118	**LNS-Z-5-OV**
	6.0(5.4)	5.1(4.6)	4.2(3.8)	3.1(2.8)	5$\frac{5}{8}$ × 4$\frac{7}{8}$ × 2$\frac{5}{8}$	172	**LNS-Y-5-OV**
	10.0(8.5)	8.9(7.6)	7.3(6.2)	5.3(4.5)	7 × 4$\frac{7}{8}$ × 2$\frac{7}{8}$	220	**LNS-X-5-OV**
	14.0(11.9)	12.2(10.4)	10.0(8.5)	7.5(6.4)	9 × 5 × 2$\frac{7}{8}$	261	**LNS-W-5-OV**
	22.0(20.9)	19.5(18.5)	16.5(15.7)	13.0(12.4)	11 × 4$\frac{7}{8}$ × 4$\frac{13}{32}$	326	**LNS-P-5-OV**
6V ±5% ADJ.	2.5(2.25)	2.2(2.0)	1.9(1.7)	1.4(1.3)	4$\frac{7}{8}$ × 4 × 1$\frac{3}{4}$	112	**LNS-Z-6**
	20.5(19.48)	18.1(17 2)	15.3(14.54)	12.0(11.4)	11 × 4$\frac{7}{8}$ × 4$\frac{13}{32}$	298	**LNS-P-6**
12V ±5% ADJ.	1.7(1.55)	1.6(1.45)	1.5(1.4)	1.3(1.2)	4$\frac{7}{8}$ × 4 × 1$\frac{3}{4}$	112	**LNS-Z-12**
	4.0(3.6)	3.5(3.15)	2.9(2.6)	2.2(2.0)	5$\frac{5}{8}$ × 4$\frac{7}{8}$ × 2$\frac{5}{8}$	163	**LNS-Y-12**
	6.5(5.5)	5.5(4.7)	4.5(3.8)	3.3(2.8)	7 × 4$\frac{7}{8}$ × 2$\frac{7}{8}$	203	**LNS-X-12**
	8.5(7.2)	7.2(6.1)	5.9(5.0)	4.2(3.6)	9 × 5 × 2$\frac{7}{8}$	245	**LNS-W-12**
	14.0(13.3)	12.4(11.8)	10.0(9.5)	7.3(6.94)	11 × 4$\frac{7}{8}$ × 4$\frac{13}{32}$	298	**LNS-P-12**
15V ±5% ADJ.	1.4(1.3)	1.3(1.2)	1.2(1.1)	1.0(0.9)	4$\frac{7}{8}$ × 4 × 1$\frac{3}{4}$	112	**LNS-Z-15**
	3.4(3.1)	3.1(2.8)	2.6(2.35)	2.0(1.8)	5$\frac{5}{8}$ × 4$\frac{7}{8}$ × 2$\frac{5}{8}$	163	**LNS-Y-15**
	5.5(4.7)	4.8(4.1)	3.9(3.35)	2.8(2.4)	7 × 4$\frac{7}{8}$ × 2$\frac{7}{8}$	203	**LNS-X-15**
	7.7(6.55)	6.7(5.7)	5.5(4.7)	3.8(3.15)	9 × 5 × 2$\frac{7}{8}$	245	**LNS-W-15**
	12.0(11.4)	10.6(10.1)	8.5(8.1)	6.3(6.0)	11 × 4$\frac{7}{8}$ × 4$\frac{13}{32}$	298	**LNS-P-15**
20V ±5% ADJ.	1.0(0.69)	0.85(0.77)	0.65(0.59)	0.45(0.41)	4$\frac{7}{8}$ × 4 × 1$\frac{3}{4}$	112	**LNS-Z-20**
	4.4(3.75)	3.6(3.1)	2.6(2.2)	1.6(1.4)	7 × 4$\frac{7}{8}$ × 2$\frac{7}{8}$	203	**LNS-X-20**
24V ±5% ADJ.	0.9(0.81)	0.75(0.68)	0.6(0.55)	0.4(0.36)	4$\frac{7}{8}$ × 4 × 1$\frac{3}{4}$	112	**LNS-Z-24**
	2.3(2.1)	2.1(1.9)	1.7(1.5)	1.1(1.0)	5$\frac{5}{8}$ × 4$\frac{7}{8}$ × 2$\frac{5}{8}$	163	**LNS-Y-24**
	3.8(3.2)	3.2(2.7)	2.4(2.0)	1.4(1.2)	7 × 4$\frac{7}{8}$ × 2$\frac{7}{8}$	203	**LNS-X-24**
	5.4(4.6)	4.6(3.9)	3.7(3.1)	2.5(2.1)	9 × 5 × 2$\frac{7}{8}$	245	**LNS-W-24**
	9.0(8.6)	8.0(7.6)	6.7(6.4)	5.0(4.8)	11 × 4$\frac{7}{8}$ × 4$\frac{13}{32}$	298	**LNS-P-24**
28V ±5% ADJ.	0.8(0.75)	0.65(0.6)	0.5(0.45)	0.35(0.32)	4$\frac{7}{8}$ × 4 × 1$\frac{3}{4}$	112	**LNS-Z-28**
	2.0(1.8)	1.8(1.65)	1.5(1.35)	1.0(0.9)	5$\frac{5}{8}$ × 4$\frac{7}{8}$ × 2$\frac{5}{8}$	163	**LNS-Y-28**
	3.4(2.9)	2.9(2.5)	2.2(1.5)	1.2(1.0)	7 × 4$\frac{7}{8}$ × 2$\frac{7}{8}$	203	**LNS-X-28**
	4.7(4.0)	4.0(3.4)	3.2(2.75)	2.2(1.9)	9 × 5 × 2$\frac{7}{8}$	245	**LNS-W-28**
	8.0(7.6)	7.1(6.75)	6.0(5.7)	4.5(4.3)	11 × 4$\frac{7}{8}$ × 4$\frac{13}{32}$	298	**LNS-P-28**
48V ± 5% ADJ.	4.5(4.28)	4.0(3.8)	3.4(3.2)	2.5(2.38)	11 × 4$\frac{7}{8}$ × 4$\frac{13}{32}$	363	**LNS-P-48**

NOTE: 1. Rating in Parenthesis for LN Series when cover is used.
2. Dimensions include cover.
3. Includes OV protection on both outputs (5V OV trip point is 6.6 ± 2V fixed; 9—12V OV trip points is 13.7 ± 4V fixed).

LR SERIES Switching Power Supplies

SINGLE OUTPUT

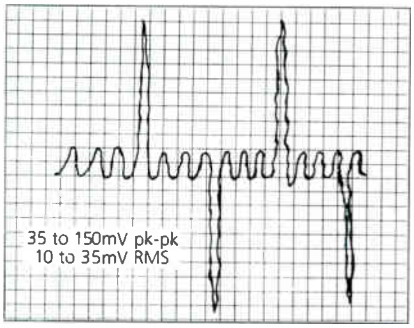
Output	MAX CURRENT AT OPERATING TEMPERATURE OF (A) 40°C	50°C	60°C	71°C	DIMENSIONS (inches)	PRICE	MODEL
2V ±5% ADJ.	15.0	13.7	11.1	5.9	2 × 4 7/8 × 6 1/4	$308	**LRS-52-2**
	25.0	21.5	17.5	10.0	2 3/8 × 4 7/8 × 8 1/2	420	**LRS-53-2**
	40.0	34.0	27.5	19.5	3 × 4 7/8 × 11	515	**LRS-54-2**
	60.0	51.0	41.0	30.0	3 3/4 × 4 7/8 × 10 1/2	655	**LRS-55-2**
	90.0	77.0	61.0	45.0	4 7/16 × 4 7/8 × 11 1/2	812	**LRS-56-2**
	130.0	110.0	90.0	68.0	5 × 4 7/8 × 12	1064	**LRS-57-2**
	180.0	147.0	120.0	83.0	5 1/2 × 4 7/8 × 13 1/8	1288	**LRS-58-2**
	250.0	200.0	165.0	125.0	6 5/8 × 4 7/8 × 13 25/32	1568	**LRS-59-2**
5V ±5% ADJ.	15.0	13.7	11.1	5.9	2 × 4 7/8 × 6 1/4	275	**LRS-52-5**
	25.0	21.5	17.5	10.0	2 3/8 × 4 7/8 × 8 1/2	375	**LRS-53-5**
	40.0	34.0	27.5	19.5	3 × 4 7/8 × 11	460	**LRS-54-5**
	60.0	51.0	41.0	30.0	3 3/4 × 4 7/8 × 10 1/2	585	**LRS-55-5**
	90.0	77.0	61.0	45.0	4 7/16 × 4 7/8 × 11 1/2	725	**LRS-56-5**
	130.0	110.0	90.0	68.0	5 × 4 7/8 × 12	950	**LRS-57-5**
	180.0	147.0	120.0	83.0	5 1/2 × 4 7/8 × 13 1/8	1150	**LRS-58-5**
	250.0	200.0	165.0	125.0	6 5/8 × 4 7/8 × 13 25/32	1400	**LRS-59-5**
6V ±5% ADJ.	13.5	12.2	9.9	5.2	2 × 4 7/8 × 6 1/4	275	**LRS-52-6**
	21.0	18.5	16.0	8.3	2 3/8 × 4 7/8 × 8 1/2	375	**LRS-53-6**
	35.0	31.0	24.0	17.0	3 × 4 7/8 × 11	460	**LRS-54-6**
	52.0	44.0	36.0	26.0	3 3/4 × 4 7/8 × 10 1/2	585	**LRS-55-6**
	80.0	69.0	54.0	39.0	4 7/16 × 4 7/8 × 11 1/2	725	**LRS-56-6**
	110.0	93.0	76.0	58.0	5 × 4 7/8 × 12	950	**LRS-57-6**
	150.0	123.0	100.0	70.0	5 1/2 × 4 7/8 × 13 1/8	1150	**LRS-58-6**
	210.0	170.0	140.0	105.0	6 5/8 × 4 7/8 × 13 25/32	1400	**LRS-59-6**
12V ±5% ADJ.	7.8	6.8	4.9	2.3	2 × 4 7/8 × 6 1/4	275	**LRS-52-12**
	12.5	11.2	9.6	7.2	2 3/8 × 4 7/8 × 8 1/2	375	**LRS-53-12**
	22.0	18.5	15.0	10.0	3 × 4 7/8 × 11	460	**LRS-54-12**
	30.0	26.0	22.0	16.0	3 3/4 × 4 7/8 × 10 1/2	585	**LRS-55-12**
	47.0	41.0	34.0	21.9	4 7/16 × 4 7/8 × 11 1/2	725	**LRS-56-12**
	65.0	58.0	48.0	34.0	5 × 4 7/8 × 12	950	**LRS-57-12**
	84.0	69.0	56.0	40.0	5 1/2 × 4 7/8 × 13 1/8	1150	**LRS-58-12**
	110.0	92.0	74.0	53.0	6 5/8 × 4 7/8 × 13 25/32	1400	**LRS-59-12**
15V ±5% ADJ.	6.4	5.6	4.0	1.9	2 × 4 7/8 × 6 1/4	275	**LRS-52-15**
	10.0	9.0	7.7	5.8	2 3/8 × 4 7/8 × 8 1/2	375	**LRS-53-15**
	18.0	15.0	12.0	8.0	3 × 4 7/8 × 11	460	**LRS-54-15**
	25.0	22.0	19.0	13.0	3 3/4 × 4 7/8 × 10 1/2	585	**LRS-55-15**
	38.0	33.0	28.0	17.9	4 7/16 × 4 7/8 × 11 1/2	725	**LRS-56-15**
	52.0	46.0	38.0	27.0	5 × 4 7/8 × 12	950	**LRS-57-15**
	68.0	56.0	45.5	32.0	5 1/2 × 4 7/8 × 13 1/8	1150	**LRS-58-15**
	90.0	75.0	60.0	43.0	6 5/8 × 4 7/8 × 13 25/32	1400	**LRS-59-15**
20V ±5% ADJ.	4.9	4.3	3.0	1.5	2 × 4 7/8 × 6 1/4	275	**LRS-52-20**
	7.7	6.9	5.9	4.5	2 3/8 × 4 7/8 × 8 1/2	375	**LRS-53-20**
	13.5	11.5	8.5	5.5	3 × 4 7/8 × 11	460	**LRS-54-20**
	19.0	16.5	14.0	10.0	3 3/4 × 4 7/8 × 10 1/2	585	**LRS-55-20**
	29.5	27.0	22.0	13.8	4 7/16 × 4 7/8 × 11 1/2	725	**LRS-56-20**
	40.0	36.0	30.0	21.0	5 × 4 7/8 × 12	950	**LRS-57-20**
	52.0	43.0	35.0	24.5	5 1/2 × 4 7/8 × 13 1/8	1150	**LRS-58-20**
	70.0	58.0	46.0	33.0	6 5/8 × 4 7/8 × 13 25/32	1400	**LRS-59-20**
24V ±5% ADJ.	4.1	3.6	2.6	1.2	2 × 4 7/8 × 6 1/4	275	**LRS-52-24**
	6.5	5.8	5.0	3.8	2 3/8 × 4 7/8 × 8 1/2	375	**LRS-53-24**
	11.5	9.5	7.5	4.5	3 × 4 7/8 × 11	460	**LRS-54-24**
	16.0	14.0	12.0	8.0	3 3/4 × 4 7/8 × 10 1/2	585	**LRS-55-24**
	25.0	22.5	18.5	11.6	4 7/16 × 4 7/8 × 11 1/2	725	**LRS-56-24**
	33.5	29.0	24.0	17.0	5 × 4 7/8 × 12	950	**LRS-57-24**
	44.0	36.0	29.5	20.5	5 1/2 × 4 7/8 × 13 1/8	1150	**LRS-58-24**
	60.0	50.0	40.0	28.0	6 5/8 × 4 7/8 × 13 25/32	1400	**LRS-59-24**
28V ±5% ADJ.	3.5	3.1	2.2	1.1	2 × 4 7/8 × 6 1/4	275	**LRS-52-28**
	5.7	5.1	4.4	3.3	2 3/8 × 4 7/8 × 8 1/2	375	**LRS-53-28**
	9.5	8.5	6.5	4.0	3 × 4 7/8 × 11	460	**LRS-54-28**
	14.0	12.0	10.0	7.0	3 3/4 × 4 7/8 × 10 1/2	585	**LRS-55-28**
	22.0	20.0	16.0	10.0	4 7/16 × 4 7/8 × 11 1/2	725	**LRS-56-28**
	29.0	25.5	21.0	15.0	5 × 4 7/8 × 12	950	**LRS-57-28**
	38.0	31.0	25.5	17.5	5 1/2 × 4 7/8 × 13 1/8	1150	**LRS-58-28**
	52.0	43.0	34.0	24.0	6 5/8 × 4 7/8 × 13 25/32	1400	**LRS-59-28**
48V ±5% ADJ.	2.0	1.7	1.2	0.6	2 × 4 7/8 × 6 1/4	275	**LRS-52-48**
	3.3	2.8	2.4	1.8	2 3/8 × 4 7/8 × 8 1/2	375	**LRS-53-48**
	5.8	5.1	3.6	2.3	3 × 4 7/8 × 11	460	**LRS-54-48**
	8.2	7.2	6.2	4.2	3 3/4 × 4 7/8 × 10 1/2	585	**LRS-55-48**
	13.0	12.0	9.5	6.0	4 7/16 × 4 7/8 × 11 1/2	725	**LRS-56-48**
	17.5	15.5	12.5	9.0	5 × 4 7/8 × 12	950	**LRS-57-48**
	22.5	18.5	15.0	10.5	5 1/2 × 4 7/8 × 13 1/8	1150	**LRS-58-48**
	31.0	26.0	21.0	15.0	6 5/8 × 4 7/8 × 13 25/32	1400	**LRS-59-48**

NEW MRS FILTERS:

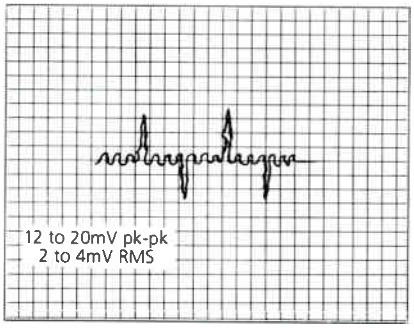
LAMBDA'S UNIQUE SWITCHING SOLUTION FOR ULTRA-LOW NOISE APPLICATIONS PROVIDES OVER 65% REDUCTION IN OUTPUT RIPPLE AND NOISE

Lambda's new line of MRS Filters mount directly to an LR Series Switching Power Supply. Together they provide an option for low noise applications which challenge linear power supply specifications, while maintaining the size, efficiency and weight advantages of state-of-the-art switchers.

On its own, Lambda's LR Series Switching Power Supplies have become the industry standard for enduring performance in MIL-STD-810C and other rugged applications. Designed using a unique technology developed by Lambda, the LR Series provides a significant reduction in output ripple and noise over other switching power supplies. Now, simply by adding an MRS Output Filter, the LR Series joins Lambda's established lines of LD and LN Series Linear Power Supplies in powering noise-sensitive circuits. Just compare the specifications in Figure 1.



Maximum Specified For LRS Switching Power Supplies
(Typical performance is less than half the maximum specified amplitude.)



MRS Filters Ensure Ripple and Noise Less Than 2 to 4mV RMS Using LRS Series Switching Power Supplies

POWER SUPPLY SERIES	RIPPLE AND NOISE SPECIFICATION
LD	0.15mV RMS 1mV pk-pk
LN	1.5mV RMS 5mV pk-pk
LR (with MRS Filter)	2 to 4mV RMS 12 to 20mV pk-pk

Figure 1

SPECIFICATIONS

FILTER INPUT
2 to 28VDC designed for direct connection to LR Series power supply terminals.

ATTENUATION
Ripple and noise measurements vary according to the particular circumstances of each application. Based on balanced probe measurement at 20kHz bandwidth (to minimize pickup of externally radiated spikes), MRS Filters will reduce ripple and noise of the LR Power Supply Series to 2mV RMS, 12mV pk-pk on 2, 5, and 6V models; 4mV RMS, 20mV pk-pk on 12 through 28V models.

REGULATED VOLTAGE
LR Series Power Supply regulation and stability margins are not affected by the addition of MRS Output Filters.

OUTPUT CONNECTIONS
MRS-53 via two position terminal block. MRS-54, 55 via heavy duty bus bars. Sense leads for connection from the power supply to filter output terminals, and all mounting hardware are supplied with the unit.

MOUNTING
Designed for direct mounting to LR Series Power Supplies. Contact factory for remote mounting accessories.

FINISH
Grey, Fed. Std. 595, No. 26081.

WARRANTY
Five year warranty includes labor as well as parts. Guarantee applies to operation at full published specifications at the end of five years.

MRS SERIES

MODEL	COMPATIBLE POWER SUPPLIES	APPLICABLE* OUTPUT VOLTAGES	DIMENSIONS (Inches)	WEIGHT (Lbs.)	PRICE
MRS-53	LRS-52, 52M, LRS-53, 53M	2V - 28V	1 15/16 × 1 13/16 × 1 5/8	.6	$60
MRS-54	LRS-54, 54M	2V - 28V	3 1/8 × 15/16 × 1 7/16	1	65
MRS-55	LRS-55, 55V	2V - 28V	3 1/8 × 15/16 × 1 7/16	1	70

*Contact factory for 48V special filters.

nected in reverse across its source and drain. Although that diode is fast, it is not as fast as the MOS transistor. Often used like a freewheeling diode for transient suppression or energy recovery, the parasitic device may be too slow to protect the transistor. In addition, to drive their output toward either the supply voltage or ground, many circuits connect two transistors in series across the supply, as in totem-pole, push-pull, complementary-pair, and half-bridge outputs. However, when both transistors turn on at the same time, they create a short circuit—and usually smoke. The speed with which MOS devices switch on poses the danger that the control circuit will not be fast enough to keep both transistors from turning on simultaneously. Also, MOS speed requires a control circuit that is fast enough to protect itself, say, by means of a very fast feedback loop.

For a MOS power transistor, the current that causes destruction is often more than an order of magnitude greater than the device's practical maximum current limit. That limit is determined by either the maximum voltage drop (current times on-resistance) that the application will tolerate, or the maximum steady-state power the MOS device dissipates. As a result, the current a MOS FET can carry increases significantly if the voltage drop can be large or if the current is pulsed. Smart-power users who understand the principle of on-resistance can realize dramatic cost savings just by specifying that parameter properly.

Like speed and current rating, isolation is also a critical issue for smart power. Isolation has three possible meanings—maximum voltage differential, safety, and signal coupling. The process technique used to obtain isolation for the smart-power device dictates the maximum voltage differential that the chip can withstand between its output circuitry at a high voltage and its control circuitry at a low voltage. Although this voltage differential can be much higher than the chip's output breakdown voltage, a good rule of thumb is to assume they are the same, unless specifically indicated otherwise in the device's data sheet.

Safety is usually specified as a leakage current at a high voltage, so that touching a conductor would not be hazardous. For example, the Underwriters Laboratory requires maximum leakage to be 5 mA at 1.5 kΩ for a 120-V ac line. Another aspect of safety is the creepage distances between package terminals. The use of potting or conformal coating largely takes care of creepage. However, with high voltages applied to chips that typically have 0.1-in. spacing between terminals, smart-power packages should have leads removed or disconnected for good safety practice anyway.

With smart-power MOS transistors switching amperes of current in nanoseconds, some coupling of these rapid high-current signal transitions into the small-signal circuitry of the chip must be expected. Depending on the application, the likely results of unwanted signal coupling include charge transfer, crosstalk, and glitches. Before the user commits to a certain design approach, he should examine the probable consequence of signal coupling.

Because there is still no clear best way to make a smart-power device, a number of semiconductor processes can be used. The choice is more than just all-bipolar or all-MOS processes: In all likelihood, mixed processing of one sort or another will be the mainstream technology for smart power over next three years.

Bipolar technology is hard to beat at less than 100 V. Beyond the usual npn output structures, bipolar processing allows a large number of different configurations, including complementary pairs, silicon controlled rectifiers, and even multiple outputs. It can also easily implement high-performance linear circuitry such as stable references or high-speed amplifiers for feedback.

Most of the disadvantages of this process lie with the bipolar output. Smart-power circuits largely use high-speed switching to control their output. When the

HOW SMART POWER CAN MAKE A DIFFERENCE

For the designer, the main thing to keep in mind when working with smart power is that more of the system resides on one chip. Therefore, it is critical to view the project as a whole and consider what changes in the system make sense.

One advantage to using smart power is that new features which could make a big difference in the end product can be added with little or no impact on cost. For example, the ability to diagnose a problem easily could add significant value to a variety of products. With smart power, it is simple to add test points or a light-emitting diode for the convenience of service technicians.

Also important is the shift from linear to digital control techniques. This brings many additional advantages. The combination of high voltage and speed that smart-power chips make possible allows the use of such digital techniques as pulse-width modulation for controlling power from the ac line. The switching power supply, for example, provides efficiencies as high as 80% to 90%, compared with 30% to 60% for linear supplies. There are, in addition, reductions in size and weight by up to of 80%.

Another advantage of smart-power circuitry is the chance to eliminate a low-voltage power supply. All too often, an application requires a low voltage just to operate the necessary semiconductor controls. For example, many good stepper-motor controllers operate at 40 V, with a power supply physically much larger than the controller itself and the motor. If the controller were a smart-power chip that could run from a rectified ac line, overall size, weight, and cost would be significantly reduced.

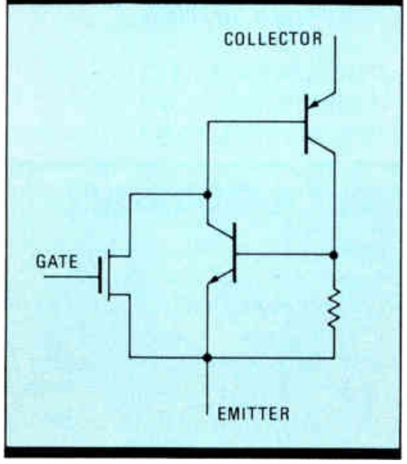
Unfortunately, electromagnetic interference is the evil that comes with high speed and power. Although combining power and control on one chip gets rid of the antennas between them, the power lines to the chip and to the load can radiate.

Solving the problem calls for utilizing basic rf techniques, such as shielding, bypassing, and ground planes, for whatever boards, equipment, or systems contain a smart-power device. Some years ago, switching power supplies encountered the very same EMI problems—and solved them. This lesson provides a good model of standards and techniques for smart power. *–A. F.*

load is reactive, as in a motor or a flat-panel display, such fast switching causes safe-operating failures. Bipolar outputs are also slower than MOS outputs, limiting operating frequency generally to around 500 kHz. In addition, the lower power gain of bipolar transistors not only increases a chip's power dissipation, but it also often requires an extra driver stage. Moreover, overall power consumption is higher because of the greater power drain of the control circuitry.

For smart power, MOS offers three advantages: the lower power consumption of CMOS control circuitry, the fast switching speed of MOS outputs, and immunity from secondary breakdown for assured safe operating area. The major limitation to MOS smart power stems from its transistor structures. Vertical MOS structures limit the smart-power device to a single output, whereas lateral devices begin to become uneconomic at on-resistances below 50 Ω and are definitely too costly below 10 Ω. On the horizon, however, are several new technologies based on Resurf (for reducing surface fields) techniques that promise economical multiple p- and n-channel outputs. Still in development, Resurf schemes permit controlling the field distribution of voltage on the surface of the chip to obtain high breakdown voltage with small chip size.

MIXING STRUCTURES



3. For higher current density, smart-power chips can employ output structures that use MOS transistors to gate a bipolar transistor.

Another factor that influences output structures, be they bipolar or MOS, is the application itself, especially when multiple loads must be connected to a common negative point. In such a situation, the ideal solution is to use either a pnp bipolar transistor or a p-channel MOS FET (see fig. 2, p. 136). Unfortunately, high-voltage pnp and p-channel transistors are expensive and hard to build on-chip. For the same ratings, pnp bipolars are substantially larger than npn devices, and p-channel MOS FETs occupy about three times the silicon of n-channel ones.

Rather than taking on the difficulty and expense of p-type transistors, chip makers often use various schemes to drive n-type transistors. To turn on an n-channel MOS FET fully, its gate must be driven above the power-supply voltage level. In the case of high-voltage n-channel MOS FETs, that drive voltage must be 10 to 15 V above the supply. In smart-power parts, an on-chip "charge pump" provides the necessary drive; with discretes, another power supply or IC is needed. Although npn bipolars do not require drive voltages above the supply, they do turn off very slowly.

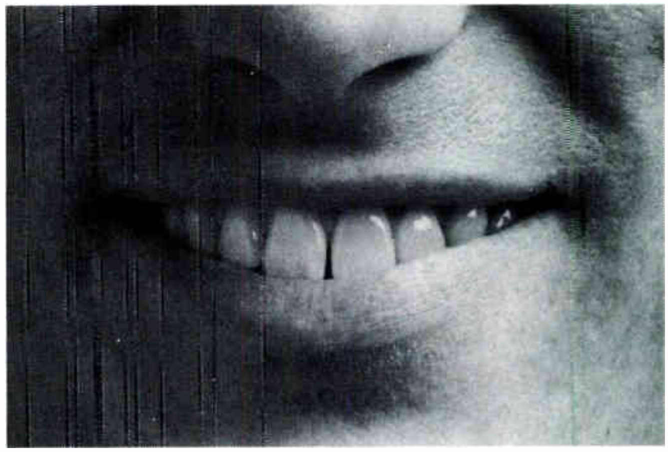
And then there are the so-called mixed processes. The alphabet soup of technologies that are intermingled on the same chip for input and output circuitry—biMOS, CMOS/DMOS, biMOS/DMOS, and so on—represents attempts to maximize the benefits of each individual process. For instance, with biMOS, the small-signal circuitry may be CMOS and the output bipolar, or CMOS logic may be combined with bipolar linear circuitry and either MOS or bipolar devices in the output, depending on what method is best for the application under consideration.

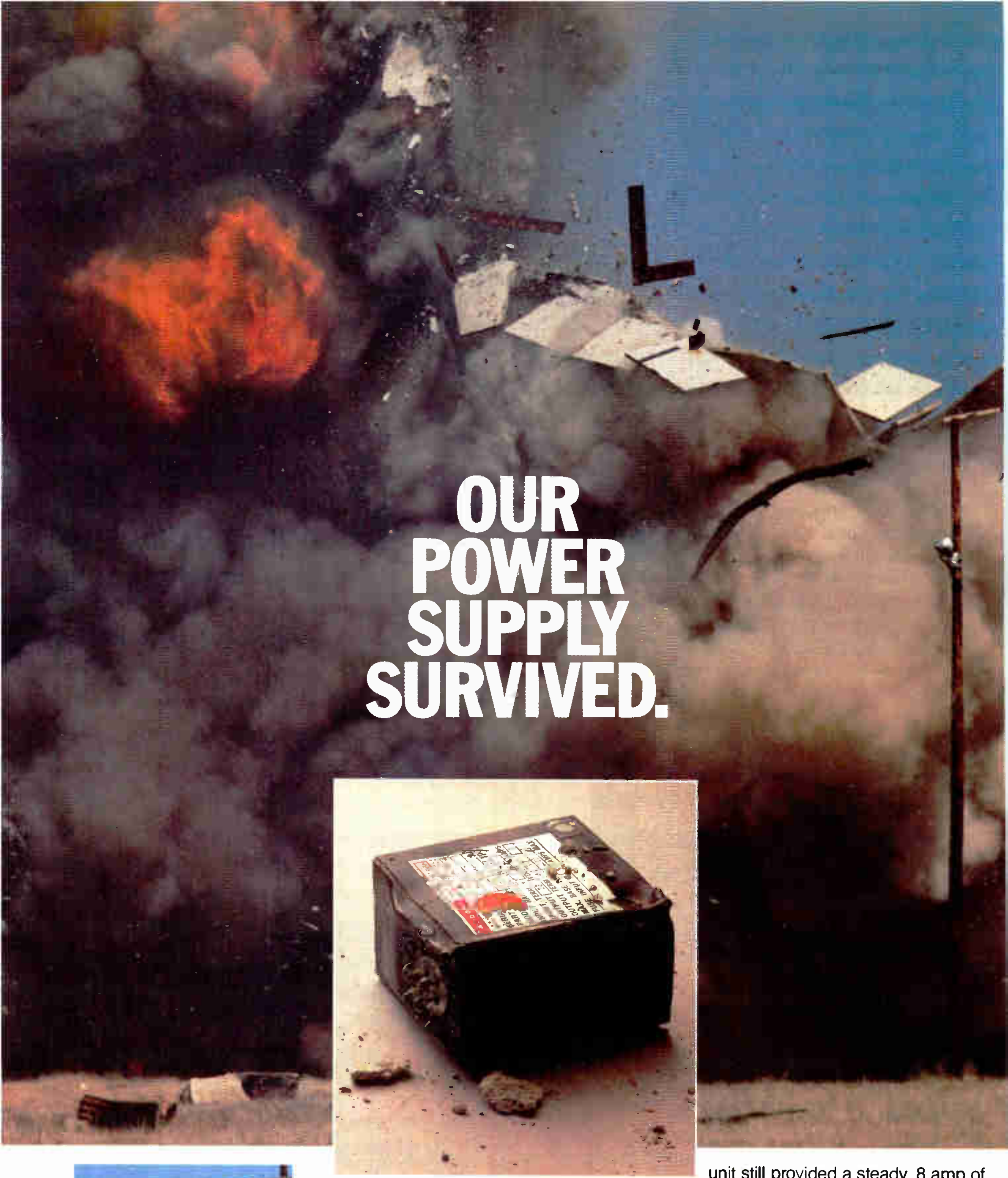
Besides mixing processes for control and power circuitry, smart power may even combine bipolar and MOS devices to create special output structures. For example, combining a MOS driver with a bipolar output leads to a MOS-gated bipolar transistor (see fig. 3), which uses a MOS FET to gate a bipolar transistor. Known variously as a COM-FET, for conductivity modulated FET, or an IGBT, for insulated-gate bipolar transistor, such a structure offers the advantage of high current density compared with a bipolar transistor or MOS FET alone. However, the MOS-gated device has the drawback of being slower and of latching above a specific current threshold. Other advantages are cost and low drive power.

Whatever the process, the three common ways to obtain voltage isolation between sections of the smart-power chip are junction isolation, self-isolation, and dielectric isolation. The most widely used technique today, junction isolation employs a reversed-biased pn junction to achieve isolation at moderate voltages. Its greatest disadvantage is cost, because of the need for an epitaxial layer. Self-isolation reverse-biases the junctions of the components on the chip. This approach eliminates the cost of the epitaxial layer, but the amount of current it can handle is limited. Then too, in both junction isolation and self-isolation there is the possibility of problems when polarities are inadvertently reversed on the chip. In contrast, dielectric isolation, which places each section in a separate dielectric tub, offers the best performance, allowing high voltage, polarity reversal, and mixed technology. But it's expensive.

Smart power is still evolving, so its performance will keep improving as costs fall. Voltages through 400 V are practical, higher voltages are available, and 600-V capability is coming within the next year. At lower voltages (60 to 80 V), currents can reach 10 A, and even higher-current devices are possible. And in the near future, smart power will be capable of handling nearly 400 V with current ratings up to 10 A and reasonable pricing and availability. □

ART FURY is vice president of Power Integrations Inc., a smart-power startup in Sunnyvale, Calif. A 21-year semiconductor-industry marketing veteran, he introduced the first power MOS devices while at Siliconix Inc. He also introduced that company's first smart-power ICs. Before that, he worked at National Semiconductor Corp., where he was responsible for the 324 quad op amps, and the industry-standard 339 quad comparator. Earlier, at Signetics Corp., he helped develop the phase-locked loop.





In a Navy test, a Tomahawk cruise missile exploded into a concrete building. When the dust settled, little remained but gravel and fragments of casing.

And the Abbott model C28D0.8 you see here.

Its aluminum baseplate and an adjustment cap were ripped off in the blast. But reconnected on a workbench, the unit still provided a steady .8 amp of DC current — just as it was designed to.

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MILITARY/AEROSPACE NEWSLETTER

THE AIR FORCE IS OVERHAULING ITS EMBEDDED-PROCESSING STANDARD . . .

The standard architecture for embedded processing on Air Force aircraft—Mil Std 1750A—is being overhauled, but today's 1750A implementations probably won't require extensive updates. The new Mil Std 1750B, which was written by the Processors Committee of the Society of Automotive Engineers' Avionics Division, will most likely be implemented as a set of optional enhancements to the 16-bit 1750A standard—if it is implemented at all. The changes are essentially additions to requirements for 1750A, says Randal Moore, engineering chief for avionics processors at General Dynamics Corp. in Ft. Worth, Texas, and the former chairman of the SAE Processors Committee. These include additional page registers, a memory mapper, and new instructions for such things as unsigned integer arithmetic, which is useful for writing Ada compilers. The SAE committee will probably approve the standard in July, but it could be a year before changes are invoked. □

. . . BUT WITH A 32-BIT STANDARD ON THE WAY, THE EFFORT MAY BE FOR NAUGHT

Not everyone thinks the Air Force really needs a new version of its 1750A, and there's a push on instead to replace the old 16-bit standard with a new 32-bit architecture. Backers of the 32-bit concept say revamping the 1750A is a waste of time. "In the originally agreed-upon guidelines [to upgrade 1750A], there was to be strict upward compatibility. We did that," says Jim James, chairman of the Processors Committee, the unit of the Society of Automotive Engineers that has been revising 1750A. "But is there enough of a change to warrant a revision of the standard? Probably not enough of one to cause everyone to go back and do more silicon." James, who is manager of avionics computer architecture at Control Data Corp., suggests instead that the SAE simply "drop it and put the effort into the 32-bit standard." That work has already begun, and task groups are now studying three approaches: using an existing 32-bit instruction-set architecture; designing a new architecture from scratch; or building on current Pentagon efforts to develop high-speed reduced-instruction-set-computer chips. □

CAN NEURAL NETWORKS HELP THE ARMY'S BATTLEFIELD PERFORMANCE?

Hecht-Nielsen Neurocomputers Inc. has begun work on a $50,000 research contract to show the Army how neural-network computers might improve battlefield performance. The small San Diego, Calif., company is part of the Army's Neural Network Computer Architecture Project. Its goal is to identify Army battlefield problems and develop a battlefield neurocomputer that can solve them. Hecht-Nielson believes that neural networking, which attempts to simulate the human brain's analog parallel-processing nature, is especially adaptable to military problems, which defy solutions with conventional computers because they often involve contradictory or imprecise data. □

THIS SOFTWARE PROGRAM BRINGS CONTRACT MANAGEMENT TO THE PC LEVEL

Managing large military contracts—and all the associated data maintenance requirements—is traditionally a heavy mainframe task that can add significantly to a program's cost. That's why Micro-Frame Technologies Inc. of Ontario, Calif., developed M*PM LAN, a program-management software program that can support a newtwork of up to 100 IBM Corp. Personal Computer ATs or compatibles. The key to the program, which s now in beta test at Computer Sciences Corp. and Motorola Inc., is what the company calls its Work Breakdown Structure, a tree-like data organization hierarchy that can handle scheduling, proposal pricing, and cost reporting more efficiently than the critical-path techniques usually used for program management. □

MILITARY/AEROSPACE NEWSLETTER

LOSING THIS CONTRACT COULD FORCE MARCONI OUT OF THE RADAR BUSINESS . . .

Ferranti International plc and Marconi Defence Systems Ltd. are squaring off in a battle that could drive one of the UK's top two military electronics suppliers out of the airborne military radar business. The two defense equipment makers are on opposing teams that are competing for the contract to develop radar systems for the European Fighter Aircraft project; and, in an unusual twist, they are teamed with largely the same partners. So while Ferranti and Marconi face off in what amounts to a winner-take-all contest, West Germany's AEG AG, which is leading the Marconi team, Italy's FIAR SpA, and Inisel of Spain have nothing to lose—they're members of both teams, so they win regardless. Marconi, though, stands to lose plenty: the company is billing the contest as its fight for survival in the radar business. UK analysts agree. They point to Marconi's recent troubles with radar, such as the failure of its Nimrod airborne early-warning radar system and problems with its Fox Hunter radar for the Tornado Interceptor aircraft, as signs that anything less than a victory could make it tough for Marconi, a subsidiary of General Electric Co. plc, to bid on radar programs in the future. □

. . . IF EUROPEAN LEADERS CHOOSE NEW TECHNOLOGY OVER A PROVEN SYSTEM

Marconi Defence Systems Ltd. is pinning its last hopes of staying in the airborne military radar market on Hughes Aircraft Co. and its APG-65, a radar system that's now flying in some West German F-4s and Spanish F-18s. Marconi, AEG AG of West Germany, and others are offering an upgraded version of the APG-65, dubbed the DMS-2000, for installation in the coming European Fighter Aircraft. The EFA is a joint European effort to develop a next-generation fighter similar to the U. S. Advanced Tactical Fighter and Advanced Tactical Aircraft programs. The Marconi-AEG combo, however, is far from a shoe-in for the prize—800 radars worth roughly $1 billion. Driving hard in competition is Ferranti International plc, which is bidding an all-new system, the ECR-90. Marconi argues that its system is a proven design, and is compatible with equipment to be installed in other fighters soon to enter service in Europe. The company also argues that relying on all-new technology may make the Ferranti bid too risky. But Ferranti counters by pointing to its recent success with Blue Vixen, an airborne early-warning radar now in development, which uses software written exclusively in the ADA programming language. Ferranti officials claim that to develop the DMS-2000, Marconi and friends will first have to cross-compile software from the Hughes assembly language used for the APG-65—a time-consuming task that may not be too easy to complete. □

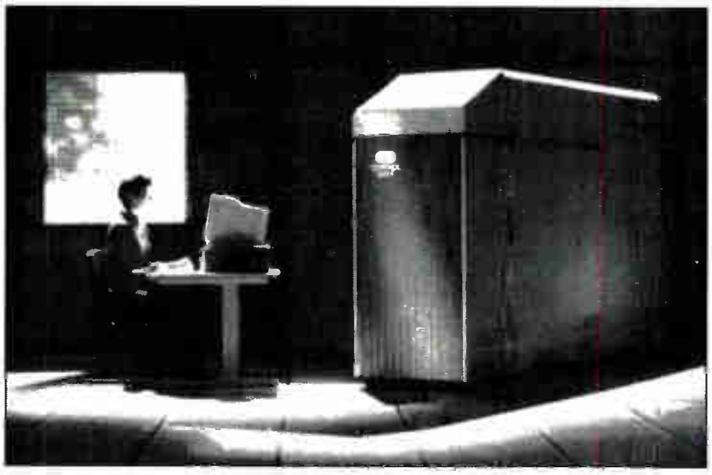
IR SENSORS HELP PILOTS FIRE MISSILES FOUR TIMES FASTER

The infrared eye of an air-to-ground Maverick missile helps a new Air Force system from Hughes Aircraft Co. to automatically select targets and aim up to six missiles. Called Rapid Fire, the system is intended to substantially increase a pilot's battle performance by attacking multiple targets in a single pass. It does: in the same time it now takes a pilot to manually aim and fire a single Maverick, a pilot using Rapid Fire can launch four missiles, say officials at Hughes' Missile Systems Group in Canoga Park, Calif. The system searches an area viewed by the infrared seeker, determines likely targets—usually vehicles, such as tanks—and aims the missiles. The pilot views the data on a cockpit-mounted display and has final control over firing decisions. Hughes has already developed the target-identification algorithms under the first phase of a $2.6 million development deal, and will demonstrate the system later this year. Full-scale tests and launchings from an F-16 are still a ways off, however. □

NEW PRODUCTS

CDC's 960 MIDRANGE MAINFRAMES BOOST THROUGHPUT, CUT COST OF OWNERSHIP

Eight dual-processor systems in a cluster deliver up to 200 mips



Cyber 960's 30-in.-wide-by-76 in.-high cabinet delivers a four-to-one reduction in size compared with Control Data's previous midrange computers.

Control Data Corp.'s Cyber 960 family of midrange mainframe computers offers up to 50% better throughput than the company's current midrange line at 70% of the price. That's a price/performance ratio that delivers up to a 23% better cost-of-ownership figure over five years than competitors such as IBM Corp., Digital Equipment Corp., and others, says the Minneapolis company.

The new Control Data mainframes come in either single- or dual-processor configurations. Up to eight of the single- or dual-processor Cyber 960 systems can be clustered, providing a performance range from 8.9 million instructions/s to more than 200 mips, based upon the DEC approach to calculating mips, says Tapan Bhattacharya, director of tactical marketing for Control Data's Computer Systems Division.

NUMBER CRUNCHER. Like other Control Data mainframes, the Cyber 960 is designed with an eye toward scientific/engineering and other numerically intensive computing tasks. The family is positioned to compete against systems such as DEC's VAX 8820 and VAX 8840, as well as machines in IBM's 4300 and 3090 series.

"Our studies indicate that we are the lowest in five-year cost of ownership," Bhattacharya says. He pegs the 60-month cost for a Cyber 962-11 including hardware, software (operating system, Fortran and Cobol languages, and database management), disk storage, communications, tape drive, printer, and maintenance at $2.36 million. That compares with $2.54 million for a comparably equipped VAX 8820 and $3.05 million for an IBM 4381-23, Bhattacharya says. Likewise, the five-year, $3.94 million cost of a Cyber 962-32 matches up against $4.65 million for an IBM 3090-150E, he adds.

The Cyber 960 machines feature the first volume use of the FGE6300 line of bipolar gate arrays from National Semiconductor Corp. The arrays, built in a 1.5-μm emitter-coupled-logic process, were developed jointly by Control Data with Fairchild Semiconductor Corp. (which has since been acquired by National Semiconductor Corp.). Boasting 6,300 gates, they are among the industry's densest commercially available ECL arrays, both firms say. Each chip replaces an entire board of logic in the older midrange Cyber 180, models 850, 860, and 870, which the Cyber 960 replaces. Control Data is taking first production deliveries on the National chips now, and plans to roll out all six air-cooled Cyber 960 models for availability in this year's third quarter.

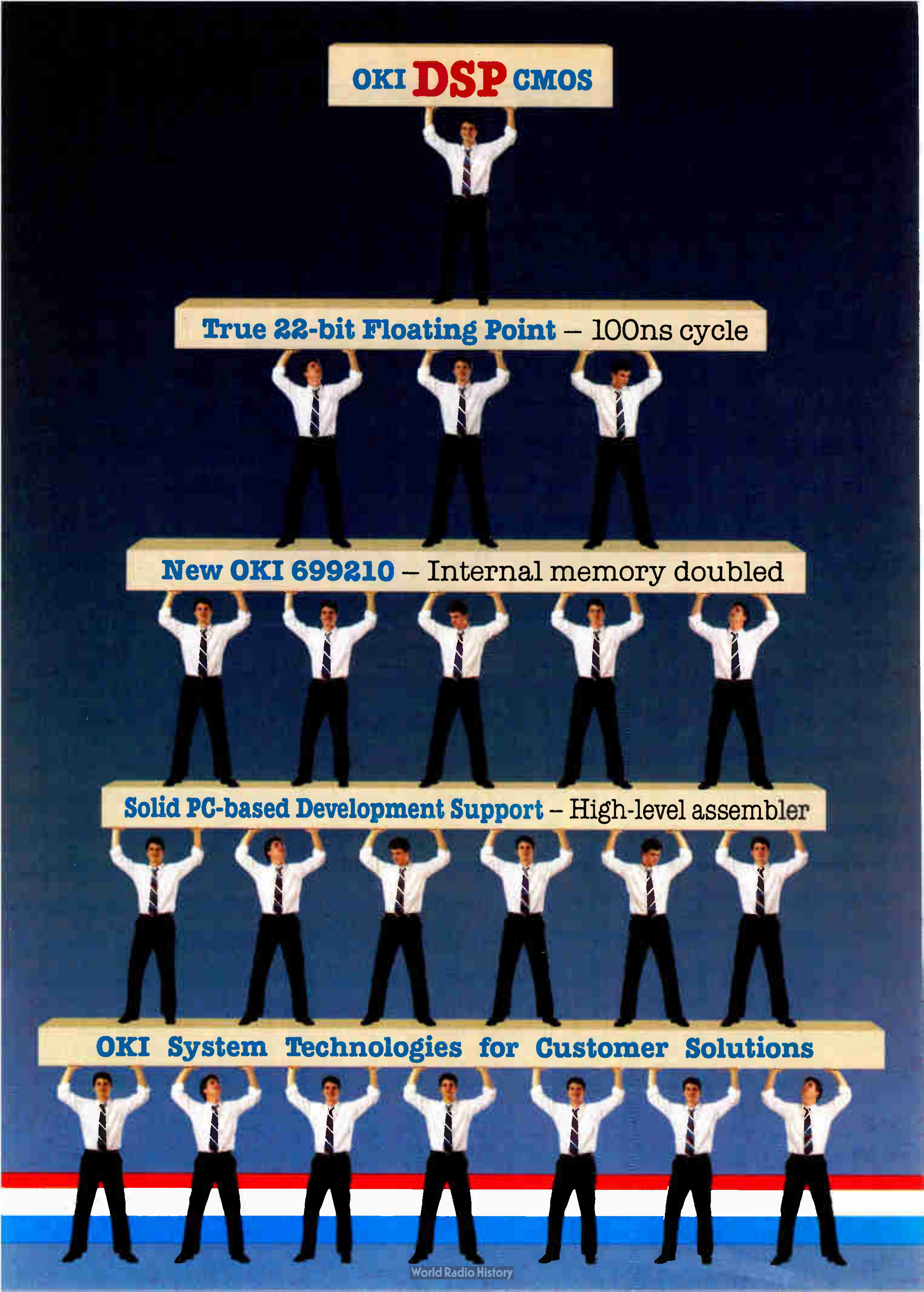
With an eye toward a smooth migration path for current Control Data users, the Cyber 960 is offered in two versions. The single-processor Cyber 960-11 and 960-31, and the dual-processor 960-32, run under NOS/VE (for network operating system/virtual environment), as well as under Control Data's older NOS. This provides compatibility with Control Data's low-end and top-end mainframe systems, the Cyber 930 and Cyber 990 lines, respectively, which use NOS/VE. It also provides a migration path from NOS-based Cyber 180 model 800 series machines. The Cyber 962-11, 962-31, and 962-32, by contrast, run only under NOS/VE. Control Data plans to offer a stand-alone Unix System V operating system for both 962 models as well in late 1989.

In clustered Cyber 960 systems, one or two 15-Mbyte/s channels are used to connect a maximum of eight or four processor cabinets, respectively. The Cyber 960's input/output facility uses 10 of the 15-Mbyte/s channels for communication with peripherals. Another 10 channels are optional. And still another 20 channels can be added with a stand-alone I/O unit. Cyber 960 systems can address up to 2 gigabytes of real memory and up to 8.8 gigabytes of virtual memory per task.

Cyber 960 pricing starts at $533,500 for a 962-11 with the minimum 32 Mbytes of main memory. A 960-11 equipped with a minimum 64 Mbytes goes for $705,000. At the high end, a dual-processor 962-32 is priced at $2.24 million with 256 Mbytes (the maximum for the whole family). A similarly equipped 960-32 sells for $2.35 million. Main memory is based on 1-Mbit dynamic RAM devices on all Cyber 960 machines, and is expandable in 64-Mbyte increments, priced at $3,500 per Mbyte. Clustering hardware and software is priced from $175,000 for linking two systems, to $300,000 for tying together eight machines. A 12-month maintenance warranty is included in the price.

GATE ARRAYS. Each Cyber 960 processor uses 204 of the National 6300-gate arrays. At a maximum of 24 chips per board using 51 different options of the array, each processor is housed on eleven 12-by-16 in. boards, with two additonal memory-control boards. Vias on the 18-layer boards are on 0.004-in. spacings. The system, which also employs 200-gate ECL arrays from National, uses space-saving surface-mount technology.

A full-blown dual-processor Cyber 960 thus requires 24 boards, since the central memory-control boards serve both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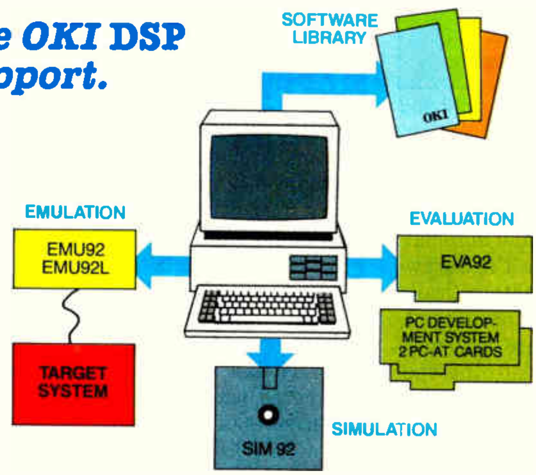
The OKI DSP chips.

Now joining our widely-applied 6992 DSP: the new *code-compatible* OKI 699**210**, setting new benchmarks in both price and performance. A 1.5 micron CMOS design, the new **210** significantly expands your DSP capabilities—at a significantly lower cost.

We built in twice as much internal memory: 512 × 22-bit words of data RAM; 2K × 32-bit words of instruction ROM. **210** instructions have been expanded to include a power-down mode, save and recover modes, as well as the ability to inhibit post-normalization. Plus programmable wait states for interfacing with slow memory.

Both single-chip DSPs, 6992 and 210, can be configured for floating point format, fixed data format or logical data format. Both offer 100ns instruction cycle times. And any code written for the 6992 can be run on the 210.

The OKI DSP support.



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650 N. Mary Avenue, Sunnyvale, CA 94086. **(408) 720-1900.**

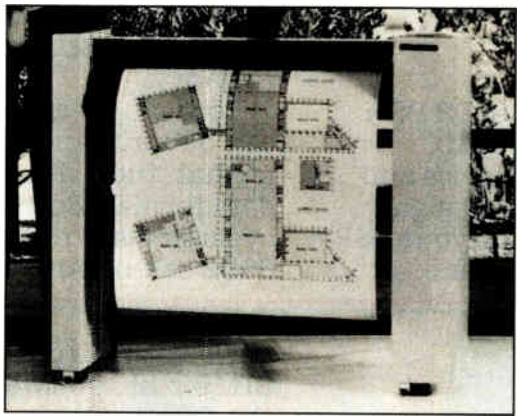
CPUs. By contrast, the Cyber 180 model 800 series required more than a hundred 10-by-4-in. boards housing water-cooled 168-gate ECL circuits.

The Cyber 960 design allows "a four-to-one reduction in the size of the cabinetry," compared with the old midrange line, says Bhattacharya. All cabinets in the new line are 30 in. wide and 76 in. high. A CPU and memory cabinet that handles either one or two processors measures 50 in. long. Other required units, a power cabinet and a standard I/O cabinet, are 30.3 in. and 42.6 in. in length, respectively. A complete, three-cabinet system thus fits into a 122.9-by-30-in. footprint. – *Wesley R. Iversen*

Control Data Corp., HQW10H, P.O. Box 0, Minneapolis, Minn. 55440.
Phone (800) 553-2215 Ext. 100 [Circle 340]

PLOTTER MEETS TEMPEST SPECS, HANDLES 48-IN.-WIDE PAPER

Integrators of systems based on personal computers and work stations that conform to the Defense Department's Tempest anti-electronics eavesdropping security regulations now have a high-speed, high-resolution plotter that handles paper sizes up to 48 in. wide—a format large enough for circuit diagrams and other engineering drawings.



HP's Tempest plotters sense the size of the paper and automatically adjust the scale of the CAD drawing to it.

Hewlett-Packard Co.'s HP 7595A-T and 7596A-T Draftmaster plotters deliver the same performance as HP's high-end commercial versions, the 7595A and 7596A. But until now, printers were not available that both met Tempest specifications and handled media as large as ANSI's E and ISO's A4 formats, says the Palo Alto, Calif., company.

SECURITY. Tempest computers and their peripheral devices must have the electromagnetic fields emanating from them sufficiently dampened or scrambled to frustrate highly sophisticated intelligence-gathering equipment that might be used in espionage.

HP's new Tempest Draftmaster plotters target computer-aided-design and computer-aided-engineering applications that demand high throughput, precise line quality, and multiple colors, says project manager Craig Fix. They boast a maximum pen speed of 60 cm/s, acceleration of up to 5.7 g, and support up to eight colors in a revolving ink-pen carousel. A total of 12 color ink pens are available from HP.

The same smooth-curve generator circuitry used in the commercial Draftmasters has been incorporated in the two Tempest versions. Addressable line resolution is 0.0025 mm and repeatability is 0.10 mm.

Fiber-tipped and roller-ball color pens are accepted by the writing carousel as are disposable and refillable liquid-ink pens. The plotters are capable of drawing on a variety of media, including vellum, polyester film, tracing bond, and plotter or glossy paper.

Several intelligent features have also been built in, including the ability to sense the size of the paper and automatically adjust the scale of the CAD drawing to it. Pens are capped automatically to eliminate ink clogging or drying out, and pen speed and force are automatically adjusted to accommodate the specific media in the plotter.

The plotters are compatible with industry-standard HP plotter products. Software written for the HP 7585B and 7566B will run on the Tempest Draftmaster. Both products offer RS-232-C and RS-422-A serial interfaces. Using the dual input/output ports allows the plotters to be controlled by either the host computer or a remote terminal.

Besides the U. S. government agencies, the plotters will find applications among prime defense contractors for the governments belonging to NATO. Canada, Australia, New Zealand, and other nations also have Tempest-compatible programs.

Both Draftmaster models are available now. The 7595A-T costs $14,900, and the 7596A-T, which handles paper rolls as well as paper sheets, costs $16,900. Delivery takes about eight weeks after order. – *Jack Shandle*

Hewlett-Packard Co., Customer Information Center, 19310 Pruneridge Ave., Cupertino, Calif. 95014. [Circle 341]

SOFTWARE RUNS CAD IN UNIX ENVIRONMENT

Software developers can combine a complete computer-aided software engineering tool kit with the multitasking Unix environment by using Interactive Development Environments Inc.'s Software through Pictures.

Fully compatible with Sun Microsystems Inc.'s Sun386i work stations, Software through Pictures offers an unlimited data dictionary, support for concurrent users, sophisticated diagram-editing methods, and optimization of available hardware. What's more, it also supports standard networking and connectivity methodologies.

Users can easily incorporate Software through Pictures with project-management, documentation, and user-developed tools to create a full-cycle software development environment.

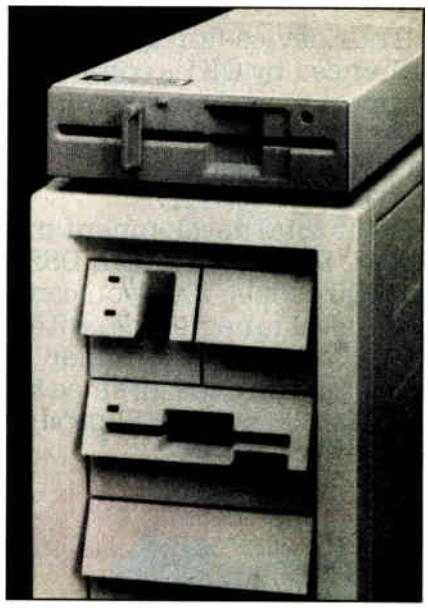
The tool kit will be available in the third quarter of 1988. Prices will start at $5,000 with discounts offered for volume purchases.

Interactive Development Environments Inc., 150 Fourth St., Suite 210, San Francisco, Calif. 94103.
Phone (415) 543-0900 [Circle 346]

FLOPPY DRIVE DELIVERS 3-MS ACCESS FOR PS/2

Procom Technology Inc.'s PXF1200 5¼-in. floppy-disk drive boasts 1.2-Mbyte capacity, fast data-access time, compatibility with all IBM Corp. Personal System/2 models, and a data-transfer rate of up to 500 Kbits/s.

Unlike other drives for the PS/2 that require up to three expansion slots, the PXF1200 can be installed in models 25, 30, and 50 without them. However, one expansion slot is required for use with the model 80. By means of an embedded



controller, the drive can handle the formats on both 360-Kbyte and 1.2-Mbyte diskettes.

The drive's 5¼-in. format allows users to easily convert data from the 5¼-in. format that is common to the PC series into the 3½-in. format standard with the PS/2 systems.

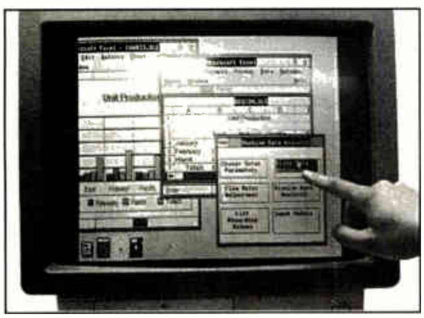
The PXF1200 is available now, priced at $450 each.

Procom Technology Inc., 3100 Airway Drive, Suite 128, Costa Mesa, Calif. 92626.
Phone (714) 549-9449 [Circle 345]

TOUCHSCREEN SOFTWARE INCORPORATES WINDOWS

Personal computers that use touch-screen technology can now take advantage of the versatility offered by Microsoft Corp.'s Windows environment by using MicroTouch Systems Inc.'s Touch WindowsDriver software for its MicroTouch Screen.

The driver runs on IBM Corp. Personal



Computers and compatibles as well as on Apple Computer Co.'s Macintosh. Present applications using Windows include spreadsheet and word-processing programs from Microsoft and computer-aided design and desktop publishing programs from third-party vendors.

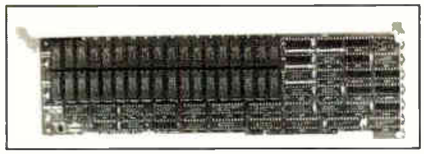
Touch WindowsDriver works with all versions of Windows through release 2.03. By the end of 1988, a version will be ready for Windows/386. The product is available now. A site license for the software costs $695 and the MicroTouch Screen costs $350 in volume purchase.

MicroTouch Systems Inc., 10 State St., Woburn, Mass. 01801.
Phone (617) 935-0080 [Circle 348]

MEMORY BOARD OFFERS OS/2, DOS EXTENSIONS

Boca Research Inc.'s Bocaram 50/60 memory board for IBM Corp. Personal System/2 models 50 and 60 lets users choose between OS/2 extended memory and LIM EMS extended memory for DOS systems so that software for both can be run.

The new board implements up to 4 Mbytes of memory in 1-Mbit dynamic random-access-memory chips—enough to take advantage of OS/2's multitasking features and DOS applications such



as spreadsheets and data bases.

The 1- and 2-Mbyte versions are easily expanded to 4 Mbytes by adding 1-Mbit 120-ns RAM chips. A menu drive installation program is included.

The 1-Mbyte Bocaram 50/60 board costs $645, the 2-Mbyte board costs $995 and the 4-Mbyte board, $1,695. A version without RAM chips costs $295. All are available now.

Boca Research Inc., 6401 Congress Ave., Boca Raton, Fla. 33487.
Phone (305) 997-6227 [Circle 347]

DISPLAY TUBE BOASTS 30% BETTER FOCUS

A 21-in. high-resolution flat and square color display tube from Toshiba America Inc. uses a new electron-gun design to deliver 30% better focus at the screen periphery than the company's present generation of color displays.

The E8170 tube uses the DAC-QFP electron gun, which has six electrodes so it can operate as a compensating four-pole lens for both horizontal and vertical projection. The tube itself incorporates a shadow mask made of Invar to prevent color degradation. Together, the electron gun and shadow mask improve screen brightness as much as 50%.

The display tube's screen offers a dot pitch of 0.31 mm and horizontal scanning frequency up to 90 KHz. It can display up to 1,280 lines with 1,600 pixels per line.

Samples of the E8170 are available now. Pricing has not been disclosed.

Toshiba America Inc., Electron Tubes and Devices Division, 1101-A Lake Cook Rd., Deerfield, Ill. 60015.
Phone (312) 945-1500 [Circle 349]

DISK CONTROLLER BRIDGES EDSI, UNIBUS INTERFACES

Emulex Corp.'s UD23 disk controller links disk drives using the industry-standard Enhanced Small Device Interface to Digital Equipment Corp.'s proprietary Unibus.

The controller supports up to four physical drives with clock rates up to 15 MHz and includes a 32-Kbyte buffer, data-transfer rates of 2 Mbytes/s, and block-mode direct memory access. Storage is limited by the size of the drive or drive system.

Unibus users with small, high-performance EDSI drives can use the UD23 as a bridge between their computer and DEC's Q-bus because the controller board also supports DEC's Mass Storage Control Protocol.

Available now, the UD23 is priced at $2,800.

Emulex Corp., 3545 Harbor Blvd., P. O. Box 6725, Costa Mesa, Calif. 92626.
Phone (714) 662-5600 [Circle 350]

68030-BASED COMPUTER RUNS AT 10 MIPS

By utilizing Motorola Inc.'s 68030 microprocessor, Force Computers Inc.'s System 32U computer achieves 10-million-instructions/s performance—a 200% performance advantage over the company's 68020-based systems.

System 32U runs under both the Unix operating system and Force Computer's VMEPROM real-time kernel operating systems. Its 12-slot backplane allocates seven slots for user customization.

The computer integrates either a 25- or 30-MHz 68030, a 20- or 25-MHz floating-point coprocessor, 1 Mbyte of local, zero-wait-state memory, and four erasable programmable read-only memory sockets capable of holding up to 4 Mbytes, as well as two serial communication ports.

Also included are 4 Mbytes of global memory, a Small Computer System Interface controller with a 128-Kbyte buffer, an eight-channel input/output board, a 170-Mbyte Winchester disk drive, and a 120-Mbyte cartridge tape drive. The system is available now. In standard configuration, it is priced at $19,900.

Force Computers Inc., 3165 Winchester Dr., Campbell, Calif. 95008.
Phone (408) 370-6300 [Circle 351]

PC-AT HARD DISK STORES 159 MBYTES

The SpeedStor AT160 hard disk from Storage Dimensions Inc. boosts the capacity of hard-disk storage for IBM Corp. Personal Computer ATs and compatibles to 159 Mbytes—20% more than the previous high.

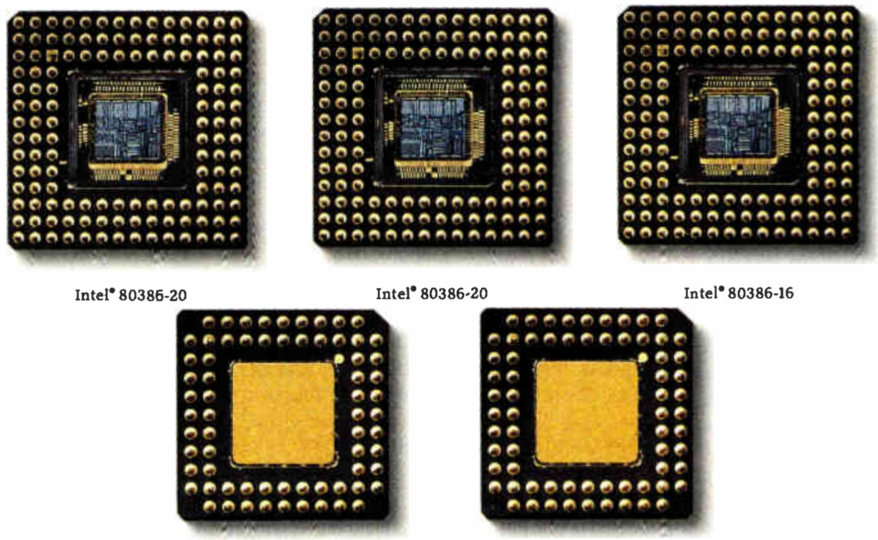
The AT160 is compatible with the industry-standard WD1003 series of disk controllers from Western Digital Corp., Irvine, Calif., as well as most controllers supplied with personal computers based on Intel Corp.'s 80286 and 80386 microprocessors.

It includes more efficient software drivers for increased performance between the DOS operating system and the hard disk, and supports DOS versions 2.1 through 3.3.

The AT160 is available now and is priced at $2,620. An upgrade kit called SpeedStor Verson 5.12 is available for the company's AT133 drives. It is priced at $50.

Storage Dimensions Inc., 981 University Ave., Los Gatos, Calif. 95030.
Phone (408) 395-2688 [Circle 352]

These give you high-performance personal computers.



Intel® 80386-20 Intel® 80386-20 Intel® 80386-16

Intel® 80286-12 Intel® 80286-12

COMPAQ personal computers offer far more than advanced, high-speed microprocessors. Each offers a combination of innovative features which work with the processor to maximize overall system performance. So there's nothing to slow you down.

Take system architecture, for example. The COMPAQ DESKPRO 386/20 and COMPAQ PORTABLE 386 are built around an advanced 32-bit concurrent bus architecture which exploits the speed of the computers' 20-MHz 80386 microprocessors. Two buses—one for memory and one for peripherals—eliminate information bottlenecks, allowing each component to run at its maximum speed. This ensures the highest system performance without sacrificing compatibility with industry-standard hardware and the world's largest library of business productivity software.

Similar performance enhancements are engineered into each subsystem of every COMPAQ personal computer. Each component is then optimized individually, yet designed to work as part of the total system.

For instance, COMPAQ Fixed Disk Drives deliver both high capacity and high performance. You can install up to a 300-megabyte fixed disk drive in the COMPAQ DESKPRO 386/20 and up to a 100-megabyte drive in the COMPAQ PORTABLE 386. More importantly, you can get to that data almost instantly thanks to some of the industry's fastest access times—averaging less than 30 milliseconds. When you combine this speed and capacity with disk caching, the result is the highest-performance storage subsystem in the industry. To take it one step further, Compaq helps you protect that data with internal high-

*Based on an independent study of major brands. COMPAQ®, COMPAQ DESKPRO 386® and COMPAQ DESKPRO 286® are registered trademarks of Compaq Computer Corporation. ®Registered U.S. Patent and Trademark Office. COMPAQ DESKPRO 386/20™, COMPAQ PORTABLE 386™ and COMPAQ PORTABLE III™ are trademarks of Compaq Computer Corporation. IBM® is a registered trademark and IBM PS/2™ is a trademark of International Business Machines Corporation. Intel® is a registered trademark of Intel Corporation.

These give you the highest-performance personal computers.

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Another graphic example of Compaq total system performance comes from the COMPAQ Video Graphics System. This system supplies VGA graphics with high-resolution COMPAQ Color and Monochrome Monitors along with speed enhancements from the COMPAQ Video Graphics Controller Board. When the board is used in a 16-bit slot, it makes screen updating 50% faster than the IBM® PS/2™ Video Graphics Array and other comparably equipped systems.

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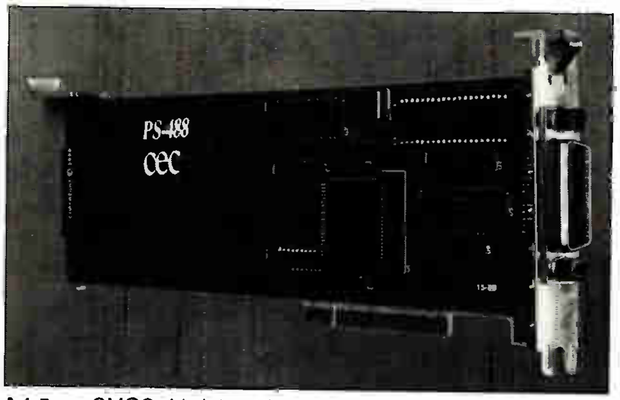
DESIGN PACKAGE MAKES BUILDING PS/2 BOARDS SIMPLE

Capital Equipment's One Chip Plus gets Micro Channel boards to market fast and handles memory, data-acquisition I/O, and multifunction boards

More than a year after IBM Corp. introduced the Personal System/2 and its Micro Channel architecture, the market for add-in boards to mate with the PS/2 has been slow to develop. Capital Equipment Corp., Burlington, Mass., intends to change that with One Chip Plus—one CMOS chip accompanied by a design system—which aims at getting fully compliant PS/2 Micro Channel boards to market in about half the design time and half the cost now required.



A 1.5-μm CMOS chip integrates extended and expanded memory functions, multiple I/O ports, and read-only memory.

One Chip Plus includes all the decoding and logic needed for users to design any kind of Micro Channel add-in board, including memory, data-acquisition input/output, and multifunction boards. What's more, it consists of a CMOS chip that incorporates the Micro Channel interface, plus a comprehensive hardware/software and documentation package that reduces the time and cost necessary for the design of Micro Channel boards.

BIG MARKET. The market potential for PS/2 Micro Channel add-in boards is huge but essentially untapped, says Kerry Newcom, president of Capital Equipment, because IBM's advanced-technology design has created barriers to easy entry for add-in hopefuls. Specifically, IBM's boards are only 45% of the size of the earlier IBM PC cards, dictating the use of costly multilayer boards and surface-mounted devices to pack all the functions onto smaller boards.

The 1.5-μm silicon-gate CMOS device designed by Capital Equipment and fabricated by VLSI Technology Inc., San Jose, Calif., includes programmable decoding for extended memory, expanded memory, multiple I/O ports, and read-only memory. It supports the Micro Channel direct-memory access arbitration and burst-mode DMA. It also has programmable memory and I/O timing to match slow or fast devices, and can address and connect directly to single in-line or dual in-line memory modules.

The design system includes schematics for memory; I/O and multifunction board designs; a technical reference manual that includes chip specifications and Micro Channel timing; recommended PC-board layout; utility software for developing add-in boards; an extended and expanded memory manager that meets Lotus-Intel-Microsoft 4.0 specifications; plus a real-time software interface—called the Acquisition Engine—for all I/O board functions.

With the Acquisition Engine's real-time control language, users can write test scripts for the engine with a word-processing program or use the engine's interactive control panel to help them develop the acquisition or control script.

One Chip Plus offers designers a more comprehensive solution than competing products. A chip-set and design package from Edsun Laboratories Inc., Waltham, Mass., [*Electronics*, March 17, 1988, p. 152] for example, implements the Micro Channel interface—but for expansion memory only. Newcom says that although a few other companies offer products similar to One Chip Plus, they are for PS/2 clones rather than for the IBM computer itself.

Newcom estimates that first-year sales of the PS/2 models 50, 60, and 80—those that use the Micro Channel—translate into more than two million add-in slots "waiting to be filled by third-party manufacturers." He claims that One Chip Plus can save those vendors at least $100,000 in development costs, and perhaps $20/board in manufacturing costs by eliminating the need for multilayer boards and SMT devices in many cases.

Newcom's estimates assume about 20 man-months would be required to design an add-in board without One Chip Plus, a figure he says the product will reduce by half.

The design system sells for $995. The interface chip is priced at $27.50 each in quantities of 100. Both are available now. – *Lawrence Curran*

Capital Equipment Corp., 99 S. Bedford St., Burlington, Mass. 01803.
Phone (617) 273-1818 [Circle 360]

AMD CONFIGURES AN ALU FOR PARALLEL-PROCESSING SYSTEMS

A new CMOS 32-bit arithmetic logic unit from Advanced Micro Devices Inc. contains three separate bit-paths for data, address, and control lines. That configuration eliminates bus contention and makes the ALU chip suited for high-speed parallel-processing systems. The Am29C332 combinatorial ALU circuit also reduces board-space requirements by integrating many common functions, such as funnel shifter, barrel shifter, priority encoders, and mask generators.

The debut of the 169-pin chip completes AMD's introduction of core functions in its 29C300 series of 32-bit microprogrammable CMOS building blocks. The company's San Antonio-based Micro Instruction Programmable Products directorate is already shipping two other core members: the 29C331 interruptible microprogram sequencer, and the 29C334 32-bit dual-access, four-port register file. The 29C300 family, which uses a three-bus architecture, is targeted at building parallel-processing systems that can execute hundreds of millions of instructions per second.

The new ALU member of the family is hitting the market in April with higher speeds than predicted last summer, when AMD simulated the design. AMD had expected to see standard products with 110-ns microcycle times, and some selected parts with 80-ns speeds. But the silicon parts are faster, says Eric Taborek, product marketing manager for micro instruction programmable products. The standard 29C332 has 80-ns cycle times; selected parts will be offered with 75-ns speeds, he says.

AMD is considering the release of a second-generation speed-grade product "because it appears we can beat our initial expectations easily," he says. The integrated ALU chip offers single-cycle execution on all of its 128 instructions. In pipelined mode, the 29C332 will achieve 12 mips. The 1.2-μm CMOS part has maximum power dissipation of 825 mW running at 10-MHz, which is about 80% less than AMD's bipolar version of the function, the Am29332.

The 29C332 contains several integrated functions commonly used in graphics control and floating-point processing applications. For example, priority encoders can be used in graphics software application to fill in polygons. The encoders also are used to detect high-bit (ones) in denormalization routines in floating-point math, says Taborek. The mask generator on the chip can be used to select bits in a field of data for single-cycle operations, which "comes in handy in pixel processing," adds Taborek. The chip's funnel shifter block takes 64-bit words in and outputs 32-bit words. It is capable of shifting n-bits up or down. It also can be used as a 32-bit barrel shifter or to extract a 32-bit field from data.

"Surveys of customers have told us that these are functions many customers are using. So we put them on one chip in the ALU," he says. The 29C332 has a flow-through architecture, featuring two 32-bit input ports and one 32-bit output port. The ALU chip is aimed at a range of applications, such as graphics, superminicomputers, telecommunications, simulators, switching equipment, laser printers, artificial intelligence systems, and military gear.

In 100-piece quantities, the 169-lead pin-grid array part sells for $175 each. The complete core of the 29C300 family (the 29C332 ALU with 29C331 sequencer and 29C334 register file) sells for $355 each. *– J. Robert Lineback*

Advanced Micro Devices Inc., 901 Thompson Place, P.O. Box 3453, Sunnyvale, Calif. 94088.
Phone (512) 647-6364 [Circle 361]

BIT'S CHIP SET RUNS AT 60 MEGAFLOPS

Bipolar Integrated Technology Inc.'s latest bipolar floating-point chip set delivers performance of 60 million floating-point operations/s.

The chip handles double-precison, 64-bit multiply operations in 50 ns and does add/subtract operations in 25 ns. They target applications primarily in minisupercomputers and work stations.

Consisting of a multiplier and an arithmetic logic unit, the chip set comes in versions compatible with either 10K ECL or TTL technology. The B3110A050 mulitplier and B3120A-25 ALU are 10K compatible; and, the B2110A-50 and B2120A-25 are TTL compatible.

A flowthrough architecture—instead of the conventional pipelined techniques—is the primary reason for the chip set's higher performance. With the flowthrough architecture, each operation is completed in a single clock cycle.

Both IEEE STD 754 and Digital Equipment Corp. F and G floating-point standards are supported. Worst-case mulitply times for a single-precision mulitply are 40 ns—and 50 ns for double-precision. Worst-case division times are 180 ns and 300 ns for single- and double-precision, respectively.

Available now packaged in 169-pin PGAs, the 10K-compatible set costs $565 each and the TTL-compatible set, $490 each. Prices are for 100-unit purchases.

Bipolar Integrated Technology Inc., 1050 N.W. Compton Dr., Beaverton, Ore. 97006.
Phone (503) 529-5490 [Circle 365]

NATIONAL ADDS 1 MBIT EEPROM LIBRARY CELL

A 256-by-8-bit electrically erasable programmable read-only memory megacell integrated into National Semiconductor Corp.'s application-specific integrated circuit library features 5-V operations, a fully synchronous read time of 100 ns, a maximum cycle time of 10 ms, and a minimum of 10,000 erase/write cycles.

A built-in voltage generator for programming eliminates the need for a second power source, and unlike competing EEPROM cells, redundancy and error detection/correction logic is on board and operates transparently to the user.

National's ASIC library can be used on Daisy, Mentor, and FutureNet work stations. The EEPROM megacell is available now.

National Semiconductor Corp, 2800 Semiconductor Dr., P.O. Box 58090, Santa Clara, Calif. 95052.
Phone (408) 721-5884 [Circle 366]

MODULES HAVE EEPROMS, DECODERS, AND BUFFERS

A family of 1.25-μm CMOS electrically erasable programmable read-only memory modules from Dense-Pac Microsystems Inc. targets avionics and other applications where space is at a premium.

The DPE45128 module integrates 16 32-K-by-8 bit EEPROMs, two decoders, three buffers and a data receiver all on one 48-pin dual in-line package. The DPE51288 puts four 32-K-by-8-bit EEPROMs and a decoder on a 32-pin ceramic substrate. Both modules are available now.

Dense-Pac Microsystems Inc., 7321 Lincoln Way, Garden Grove, Calif. 92641.
Phone (714) 898-0007 [Circle 368]

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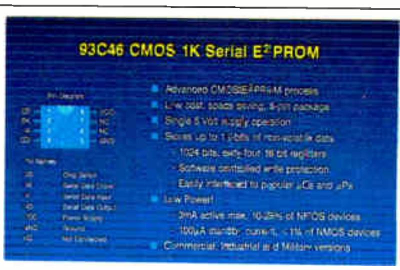
WINTEK CORP. — CIRCLE 250



1024-BIT SERIAL CMOS EEPROM

The 93C46 is a CMOS EEPROM configured as a 1K bit serial access, 64x16, 5 volt only. The device draws only 3 milliamps max. active and 100 microamps in standby. For applications requiring up to 10,000 erase/wire cycles per register. The 93C46 is in stock at all Marshall Industries locations. Pricing is $1.66 each for 100 pieces. International CMOS Technology, Inc., 2125 Lundy Av., San Jose, CA 408/434-0678.

INTERNATIONAL CMOS TECH. — CIRCLE 217

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ELECTRONICS WEEK

SUN AND XEROX TIGHTEN THE KNOT

Sun Microsystems Inc. of Mountain View, Calif., and Xerox Corp. of Stamford, Conn., have solidified the technology alliance they began last fall. Xerox has pledged to buy or manufacture at least $200 million in Sun systems and components over the next five years. Xerox agreed in October to support Sun's Sparc chip, a reduced-instruction-set-computer architecture, in future work-station products. The systems and components Xerox buys from Sun will be Sparc-based. In another move, the two companies also announced a cross-licensing agreement for the Open Look graphical user interface that AT&T Co. is backing for use with its Unix System V operating system.

MATRA-HARRIS JOINS CYPRESS ECL VENTURE

Cypress Semiconductor Corp. has enlisted the help of French chip maker Matra-Harris Semiconducteurs—already a Cypress partner in other endeavors—in its quest to develop ultra-high-speed emitter-coupled-logic bipolar integrated circuits. Cypress started up Aspen Semiconductor Corp. this summer to handle that task, but has now decided to share the development burden with its French partner. As for Matra-Harris, it will provide design and manufacturing assistance, and the company hopes eventually to be able to export the resulting ECL process to its European fab.

HUGHES ACQUIRES SIMULATION FIRM

Hughes Aircraft Co., a subsidiary of GM/Hughes Electronics Corp., Los Angeles, is adding a new weapon to its arsenal of aviation businesses: Rediffusion Simulation of Crawley, UK. Hughes is buying Rediffusion, one of the world's largest suppliers of flight simulators for civil and military aviation, from BET Ltd., an international services company based in London. Hughes says the $283 million acquisition gives it a strong entry in the growing training and simulation market.

LOTUS WILL DEVELOP 1-2-3 FOR UNIX

No introduction date has been set, but Lotus Development Corp. is working on a version of the 1-2-3 spreadsheet to run under the Unix System V operating system. Lotus, Cambridge, Mass., is developing the Unix version concurrently with 1-2-3 release 3.0 for DOS and OS/2 environments. The company says it will support Posix, the proposed IEEE Portable Operating System standard, and comply with standards set by the X/Open consortium of Unix users and vendors.

ARE THE RBOCs' PLANS INADEQUATE?

The Computer and Business Equipment Manufacturers Association strongly criticized the open network architecture plans of the regional Bell Operating Companies for being self-serving, confusing, and unresponsive to customer needs in a report filed with the Federal Communications Commission on April 13. CBEMA says the RBOCs are bundling service elements in such a way that customers will likely have to pay for services they neither want nor need, and charges that the RBOCs have not adequately provided for the future. "There are no provisions for crucial services, such as Integrated Services Digital Network," Washington-based CBEMA says.

NEW AI LANGUAGE BOWS AT SYMBOLICS

Symbolics Inc. is looking to a new language called Joshua to knock down the walls that are barring wider use of expert systems. The Cambridge, Mass., company has been known so far as a vendor of artificial intelligence hardware engines. But Symbolics says Joshua is a programming language with full Lisp capabilities embedded in an artificial-intelligence development environment that goes beyond expert-system shells. Site licenses will cost $15,000 per computer, or $60,000 for a computer license, beginning in June.

CAN THE U. S. MAKE MONEY SELLING TVs?

The TV business has been rough on U. S. companies for over a decade—only Zenith Electronics Corp. remains as a TV maker that is owned and operated in the U. S. But the Commerce Department is bullish on the U. S. TV market—the advanced TV market, that is. Commerce projects that domestic advanced TV sales could top $20 billion early in the next century, providing upwards of 700,000 jobs. And now the American Electronics Association is picking up the message. The AEA has called a June 6 industry-wide meeting in Santa Clara, Calif., to discuss a unified U. S. strategy to capture that market—and this time hold onto it tightly.

STEREO TV SALES RISE BY 27%

While the market for advanced TV systems is still years away, the comparatively conventional stereo TV market is still causing something of a sensation and sales are booming. The Electronic Industries Association's Consumer Electronics Group says sales to dealers of color TVs with integral stereo were up 27.4% in February over the same month a year ago—even though total color TV sales were down 6.2%. TV makers shipped 312,428 stereo color TVs in February 1988, up from 249,119 in 1987. But total color TV sales dipped from 1.42 million in February 1987 to 1.34 million this year.

ICL COMMITS TO SUN'S SPARC

Sun Microsystems Inc.'s Sparc chip has been racking up support in the U. S., but now it's finally won its first overseas commitment: from International Computers Ltd., the UK's top computer maker. Sparc, for scaleable processor architecture, is Sun's bid to establish an industry standard reduced-instruction-set-computer architecture. So far Sun has lined up such U. S. supporters as AT&T, Unisys, and Xerox.

AMD SETS UP UNIT TO HANDLE RISC

Advanced Micro Devices Inc. is joining the reduced-instruction-set-computer fray with a new business unit dedicated to the RISC business. AMD's Streamlined Instruction Processors Directorate will support the company's fledgling 32-bit RISC chip, the AM29000, and its associated development tools. The AM29000, the first in what AMD says will be a series of RISC-based chips, is capable of running 17 million instructions/s. AMD's new unit will be based in Austin, Texas.

INTERGRAPH FINDS AN ALLY FOR CLIPPER

Intergraph Corp. has found an ally in its effort to attract designers to its Clipper 32-bit microprocessor—Hunter Systems Inc., a Mountain View, Calif., software house. The two are working on a Clipper version of Hunter Systems' ⋗△○✓ operating system, which lets MS-DOS software run in a Unix environment. The result, they hope, will be high-performance and compatibility—two key issues for Intergraph as it seeks to get its chip designed into future systems.

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Toshiba LED Module Achieves Delicate Display with 16-Gradient Control.

The forms and functions of information and its handling are diversifying with great speed. Toshiba, a world leader in the opto-electronics field, has developed a 16 × 16 LED dot matrix module that opens new possibilities in information display. By combining these modules, a display equivalent to that of a TV can be realized. By use of Toshiba's outstanding two-color LED together with its unique gate array for driving, 16-gradient control is achieved in this new product. Compact design makes the module lightweight and optimally thin. Unique heat radiation design greatly improves the dispersion of heat from the module, and connections are simple, ensuring freedom from maintenance. In applications ranging from simple messages to visual displays such as message boards, entertainment and projector use, Toshiba's LED module is a standout.

CHARACTERISTICS	DETAIL					
Type Name	TLMM501B2	TLGM501B2	TLSM501B2	TLMM502A1	TLGM502A1	TLSM502A1
Color Display*	Red, Green, Amber	Green	Red	Red, Green, Amber	Green	Red
Dot Size	∅5mm			∅3mm		
Dot Pitch	6mm			4mm		
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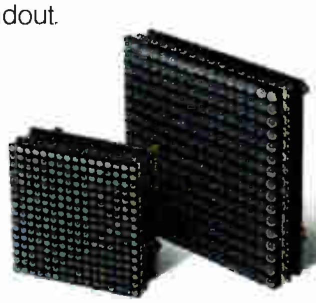
*Amber color is made by a mixture of red and green.



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